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Firmware development and testing for L1/L2 IBL upgrade

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Tesi di Laurea in
Fisica delle Particelle

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"Qui potis est? inquis, quod amantem inuria talis
Cogit amare magis, sed bene velle minus"

Abstract

Il lavoro di questa tesi riguarda principalmente l'upgrade, la simulazione e il test di schede VME chiamate **ReadOut Driver (ROD)**, che sono parte della catena di elaborazione ed acquisizione dati di **IBL** (Insertable B-Layer). IBL è il nuovo componente del Pixel Detector dell'esperimento ATLAS al Cern che è stato inserito nel detector durante lo shut down di LHC; fino al 2012 infatti il Pixel Detector era costituito da tre layer, chiamati (partendo dal più interno): Barrel Layer 0, Layer 1 e Layer 2. Tuttavia, l'aumento di luminosità di LHC, l'invecchiamento dei pixel e la richiesta di avere misure sempre più precise, portarono alla necessità di migliorare il rivelatore. Così, a partire dall'inizio del 2013, IBL (che fino a quel momento era stato un progetto sviluppato e finanziato separatamente dal Pixel Detector) è diventato parte del Pixel Detector di ATLAS ed è stato installato tra la beampipe e il layer B0. Questa tesi fornirà innanzitutto una panoramica generale dell'esperimento ATLAS al CERN, includendo aspetti sia fisici sia tecnici, poi tratterà in dettaglio le varie parti del rivelatore, con particolare attenzione su Insertable B-Layer. Su quest'ultimo punto la tesi si focalizzerà sui motivi che ne hanno portato alla costruzione, sugli aspetti di design, sulle tecnologie utilizzate (volte a rendere nel miglior modo possibile compatibili IBL e il resto del Pixel Detector) e sulle scelte di sviluppo e fabbricazione. La tesi tratterà poi la catena di read-out dei dati, descrivendo le tecniche di interfacciamento con i chip di front-end, ed in particolare si concentrerà sul lavoro svolto per l'upgrade e lo sviluppo delle schede ReadOut Drivers (ROD) introducendo le migliorie da me apportate, volte a eliminare eventuali difetti, migliorare le prestazioni ed a predisporre il sistema ad una analisi prestazionale del rivelatore. Allo stato attuale le schede sono state prodotte e montate e sono già parte del sistema di acquisizione dati del Pixel Detector di ATLAS, ma il firmware è in continuo aggiornamento. Il mio lavoro si è principalmente focalizzato sul debugging e il miglioramento delle schede ROD; in particolare ho aggiunto due *features*:

- **programmazione parallela delle FPGA** delle ROD via VME. IBL richiede l'utilizzo di 15 schede ROD e programmandole tutte insieme

(invece che una alla volta) porta ad un sensibile guadagno nei tempi di programmazione. Questo è utile soprattutto in fase di test;

- **reset del Phase-Locked Loop (PLL)** tramite VME. Il PLL è un chip presente nelle ROD che distribuisce il clock a tutte le componenti della scheda. Avere la possibilità di resettare questo chip da remoto permette di risolvere problemi di sincronizzazione.

Le ReadOut Driver saranno inoltre utilizzate da più layer del Pixel Detector. Infatti oltre ad IBL anche i dati provenienti dai layer 1 e 2 dei sensori a pixel dell'esperimento ATLAS verranno acquisiti sfruttando la catena hardware progettata, realizzata e testata a Bologna.

Contents

Introduction

This thesis work mainly concerns the upgrading and testing of VME boards called **ReadOut Drivers (ROD)** that are a component of the data acquisition and elaboration chain of IBL. **Insertable B-Layer IBL** is the new layer of the ATLAS experiment's Pixel Detector that has been added to the detector during the long shut-down of LHC. Until 2012 the Pixel Detector was composed by three layers called (starting from the inner one): Barrel Layer 0, Layer 1 and Layer 2. However, due to the LHC's luminosity increment, the aging of the pixels and the need to have more precise measurements, it was necessary to upgrade the detector. So, starting from the beginning of 2013, IBL (that was until that moment a project developed and funded separately from the Pixel Detector) became part of the Pixel Detector and was inserted between B0 and the beam-pipe. This thesis will provide a general description of the ATLAS experiment at CERN and of the detector components, focusing mainly on Insertable B-Layer. In particular this thesis will focus on the motivation that led to his realization and on constructive parameters (aimed at making IBL as compatible as possible with the rest of the Pixel Detector). This thesis will also discuss the data Readout chain, describing in particular the ReadOut Driver (ROD) boards and the improvements made by me (aimed to correct firmware bugs and to prepare the system to a performance analysis of the detector). Actually these boards have already been produced and installed at CERN, but the firmware needs to be continuously updated. My work mainly consisted in debugging and upgrading the ROD boards; in particular I added two *features*:

- **parallel programming of ROD FPGAs** via VME. The IBL readout chain requires 15 ROD boards; programming those boards at the same time (instead that serially) leads to a programming time gain (useful especially during test procedures);
- **Phase-Locked Loop (PLL) resetting** via VME. PLL is a chip (contained in the ROD) that distributes the clock signal to all the board components. When synchronization problems arise it is necessary to

reset the PLL.

In the next future those boards will be also used for Pixel Layer 1 and Layer 2 data ReadOut in order to make the system more versatile.

Chapter 1

The ATLAS Experiment at CERN

1.1 The Large Hadron Collider

The Large Hadron Collider (LHC) is the largest particle accelerator on Earth. It is located at CERN (Conseil Europeen pour la Recherche Nucleaire) at the boarder between France and Switzerland. CERN is a collaboration between the 20 European member states and non-member states from the rest of the world. The Large Hadron Collider is approximately 27 km in circumference and lies 100 m below the ground. There are four interaction points where protons or lead ions are collided at high energies. At the four interaction points, gigantic experiments (ALICE, ATLAS, CMS and LHCb) are recording every detail of the particle collisions.

As shown in Fig. 1.1, the acceleration chain consists of several steps. Protons begin their acceleration in the linear accelerator LINAC 2, where they are accelerated from rest to an energy of 50 MeV. They are then fed to the Booster to be accelerated to 1.4 GeV after which they are injected into the Proton Synchrotron to be accelerated to 25 GeV. The last acceleration before the Large Hadron Collider is provided by the Super Proton Synchrotron where they are accelerated to 450 GeV. In the LHC protons are accelerated from 450 GeV to 6.5 TeV by radio frequency (RF) cavities situated on the ring between ALICE and CMS.

1.1.1 Machine Parameters

The design collision energy for protons is 14 TeV, but the LHC is now running at a collision energy of 13 TeV, 6.5 TeV per proton beam. At this level of energy, protons move with a speed very close to the speed of light. The proton

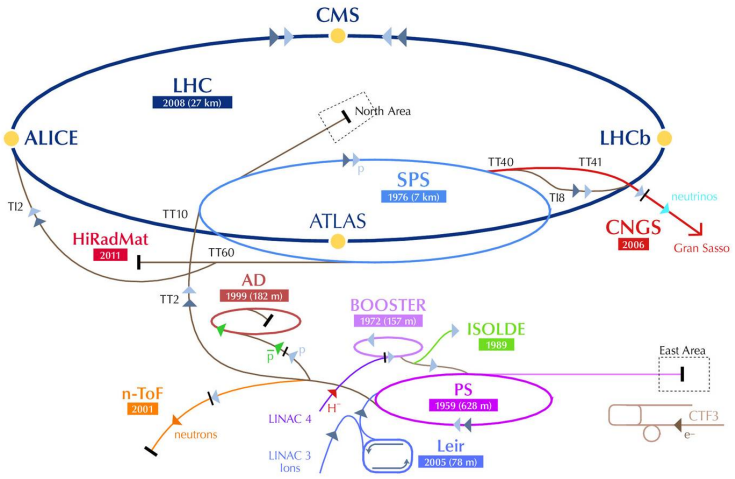


Figure 1.1: The accelerator complex at CERN.

beams consist of 2808 bunches of protons. Each bunch contains $1.2 \cdot 10^{11}$ protons so that many proton collisions can happen at each bunch crossing. This is known as *in time pile up*. The protons are held in the accelerator ring by 1232 superconducting dipole magnets with a maximum magnetic field of 8.33 T. The beams are focused and defocused by 392 quadropole magnets. The Large Hadron collider is built to have a peak instantaneous luminosity of $L = 10^{34} cm^{-2} s^{-1}$ at ATLAS and CMS and many factors of tens lower at LHCb and ALICE.

1.1.2 Main experiments at LHC

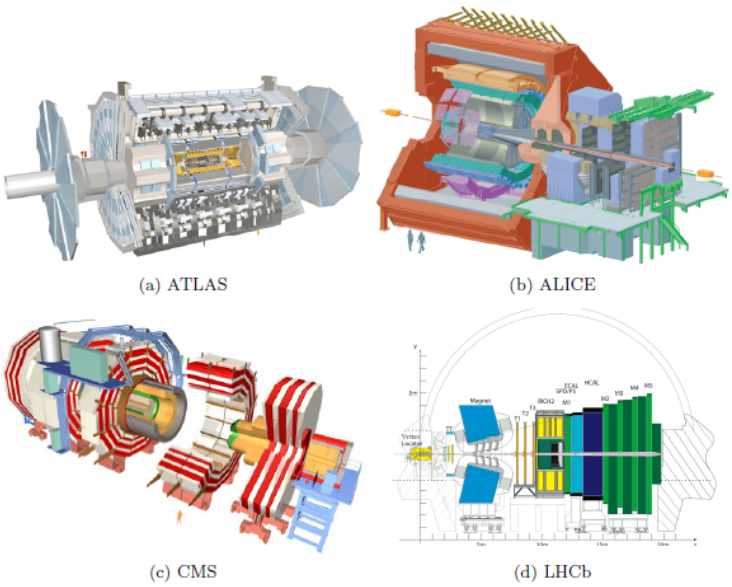
As already stated, at the four interaction points where protons or lead ions are collided there are four experiments (fig 1.2).

- **ATLAS, A Toroidal Lhc ApparatuS:** this experiment has been designed for the research of the Higgs Boson (not yet discovered when LHC was built), for searching concerning Beyond Standard Model Physics (Dark Matter, Supersymmetries) and for precision measurements of the Standard Model parameters;

- **CMS, Compact Muon Solenoid:** it has the same purpose of the ATLAS experiment but uses different technologies and methods;

- **ALICE, A Large Ion Collider Experiment:** this experiment studies heavy ions collisions in order to investigate proprieties of the state of matter called *Quark Gluon Plasma*;

- **LHCb:** it studies the quark b in order to investigate differences between matter and anti-matter.



(a) ATLAS (b) ALICE

(c) CMS (d) LHCb

Figure 1.2: Main experiments at LHC.

1.2 The ATLAS Experiment

The ATLAS experiment is a general-purpose particle detector installed at the LHC, which records collision events for various physics analyses. It is 46 m long, 25 m high, 25 m wide and weighs 7000 tons. It is operated by an international collaboration with thousands of scientists from all over the world: more than 3000 scientists from 174 institutes in 38 countries work on the ATLAS experiment.

1.2.1 The coordinate system of ATLAS

ATLAS describes collision events using right-handed spherical coordinates, with the origin defined as the nominal interaction point, the z-axis along the beam direction and the transverse x-y plane composed of the positive x-axis pointing at the center of the LHC ring and the positive y-axis pointing upwards. Therefore, a vector can be described using the azimuthal angle ϕ, the polar angle θ and the radius r, as shown in figure 1.3. Instead of using θ in the y-z plane, it is usual to take the *pseudorapidity* η defined

as $\eta = -ln\, tan\left(\frac{\theta}{2}\right)$; its absolute value varies from 0, corresponding to the vector being along the y-axis, to infinity, referring to the vector being along the z-axis. Using the pseudorapidity-azimuthal angle space, the distance ΔR between two objects can be defined using

$$\Delta R = \sqrt{\Delta\eta^2 + \Delta\phi^2}$$

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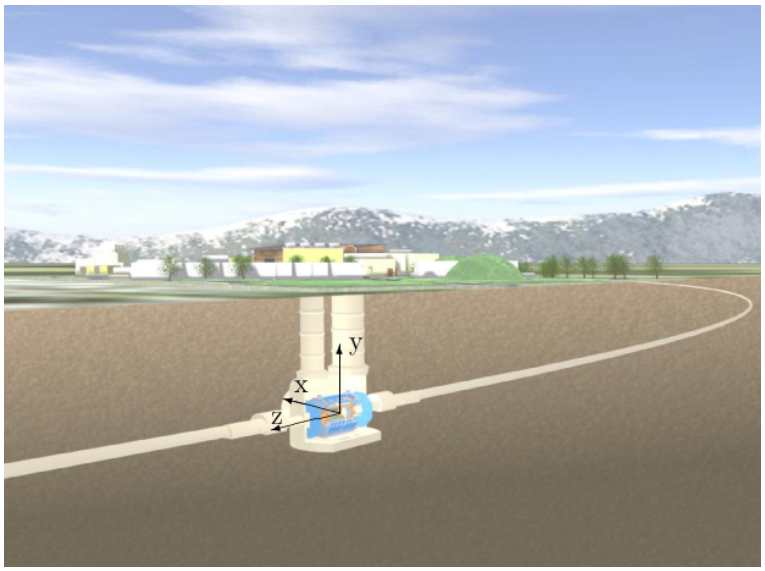


Figure 1.3: LHC's ATLAS well and its coordinate system.

The hadron collisions at the LHC are in fact parton collisions. The partons carry a fraction of the hadron's momentum which can not be evaluated on a collision-by-collision basis. Given that the initial momentum in the transverse x-y plane equals zero, the transverse missing energy E_T^{miss}, the transverse momentum p_T and the transverse energy E_T, which are often used in analyses, are defined in this plane.

1.3 The Layout of the ATLAS detector

The overall layout of the ATLAS detector is illustrated in a cut-away view in Figure 1.4. It is built with a cylindrical symmetry around the interaction point; it is geometrically divided into a barrel region (low η region), two end-cap regions (medium η region), and two forward regions (high η region). The ATLAS detector is a laterally symmetric detector centered on the interaction point.

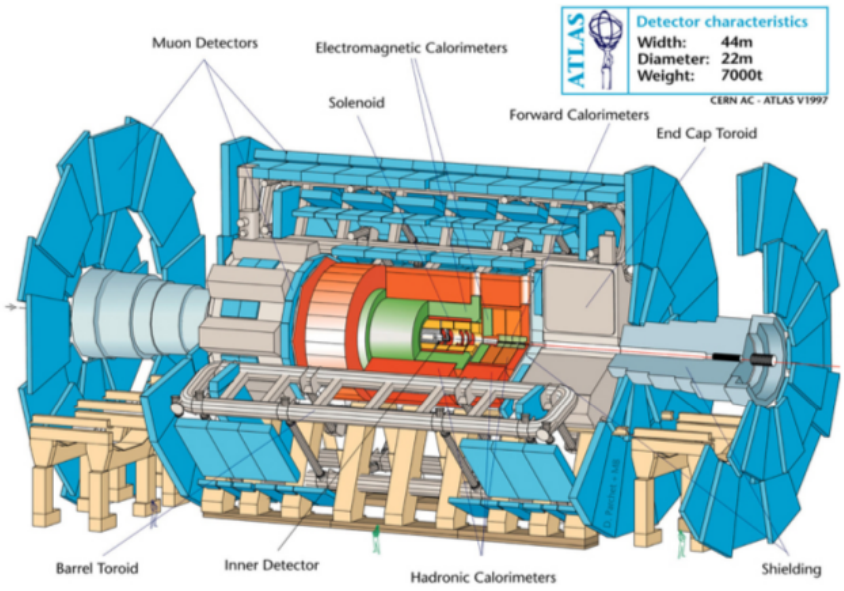


Figure 1.4: An overall layout of the ATLAS detector [1].

The full detector is made up of a chain of sub-detectors, that are designed to identify and record the particles coming out of the proton-proton collisions. From inwards to outwards, these sub-detectors form three systems: the inner detector (ID), the calorimeters and the muon spectrometer. Besides, a central solenoid surrounds the ID in order to provide a 2 T magnetic field, whilst toroids support magnetic fields of approximately 0.5 T and 1 T in the barrel and end-caps sections of the muon spectrometer. Particles produced from the proton-proton collisions firstly arrive in the inner detector which covers the region of $|\eta| < 2.5$. The charged particles will interact with different layers of the detector and form discrete hits which will be used to reconstruct their trajectory. The momenta and charge of these charged particles can be measured, as their trajectories are bent by the 2 T magnetic field provided by the central solenoid. As the innermost layer of ATLAS, the ID provides essential information, such as the recognition of first and second vertices. The ID is therefore designed to have a high granularity with intrinsic accuracy varying from $\sim O(10)$ micrometers to $\sim O(100)$ micrometers and a high momentum measurement resolution which is measured as $\sigma_{p_T}/p_T = (4.83 \pm 0.16) \cdot 10^{-4} GeV^{-1} \cdot p_T$ [2] . In order to meet the performance requirement, semiconductor detectors are used for precise measurement close to the beam (the pixel detector and the semiconductor tracker) and a noble gas detector is used in the outer layer (the transition-radiation tracker). Further away from the collision point are the calorimeters, composed of the

hadronic calorimeters and the electromagnetic calorimeters, which are designed to identify hadrons or electron/photon respectively and measure their energy and coordinates. The incident particles can interact with the instrumented material of the calorimeters via electromagnetic or strong processes, and produce a shower of secondary particles. The energy information will eventually be recorded by collecting the charge or the light produced by the shower. The position information is obtained by segmenting the calorimeters longitudinally and laterally. Sampling calorimeters are composed of an absorber made of dense material to develop the shower, and of an active medium to develop the signal.
The calorimeters will not stop muons as they interact very little with the calorimeter absorber. Muons will pass through the full detector and arrive in the outermost layer of the ATLAS detector, which is the muon spectrometer designed to record and identify the muons. The muon spectrometer contains four types of muon chambers: two types of precision tracking chambers providing position and momentum measurement, and two types of trigger chambers to provide fast and robust information for the hardware-based trigger decision making. Figure 1.5 illustrates the detector response to different particles, using a transverse section view of the ATLAS detector.

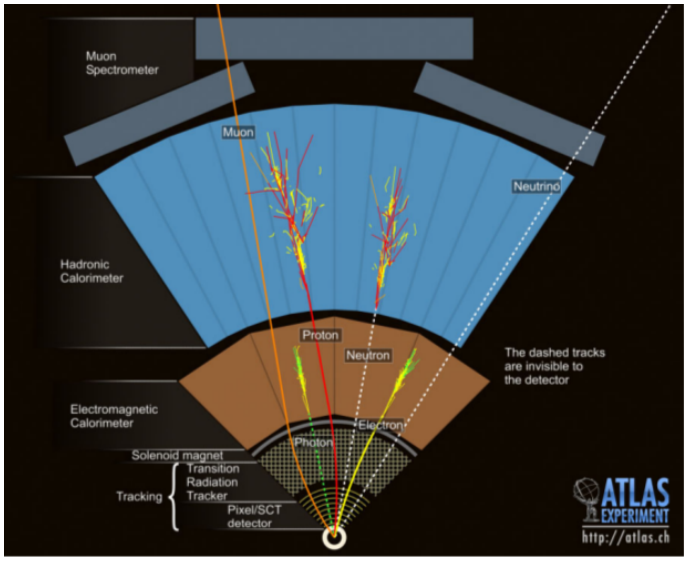


Figure 1.5: A sector view in the transverse plane of the ATLAS detector, which illustrates how the different particles interact with the detector [3].

1.3.1 Magnet System

The ATLAS superconducting magnet system can be seen in Figure 1.6 and 1.7(a). It is an arrangement of a Central Solenoid (CS) providing the Inner Detector with magnetic field, surrounded by a system of three large air-core toroids generating the magnetic field for the muon spectrometer. The overall dimensions of the magnet system are 26 m in length and 20 m in diameter. The two End-Cap Toroids (ECT Figure 1.7(a)) are inserted in the Barrel

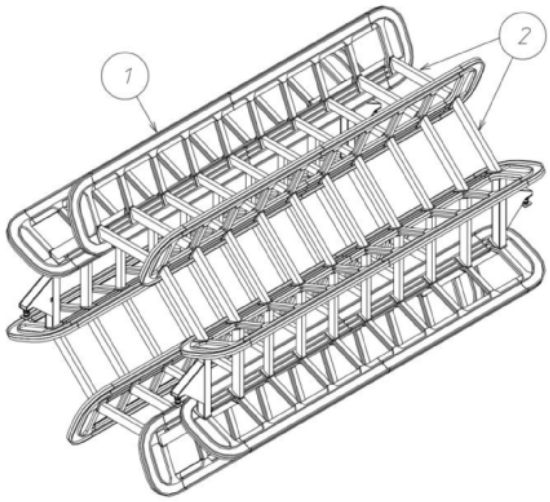
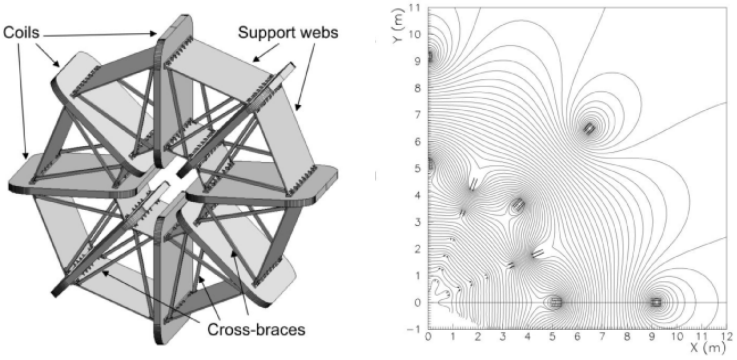


Figure 1.6: Magnets inside ATLAS detector.

Toroid (BT) at each end and line up with the CS. They have a length of 5 m, an outer diameter of 10.7 m and an inner bore of 1.65 m. The CS extends over a length of 5.3 m and has a bore of 2.4 m. The unusual configuration and large size make the magnet system a considerable challenge requiring careful engineering. The CS provides a central field of 2 T with a peak magnetic field of 2.6 T at the superconductor itself. The peak magnetic fields on the superconductors in the BT and ECT are 3.9 and 4.1 T respectively. The performance in terms of bending power is characterised by the field integral $\int Bdl$, where B is the azimuthal field component and the integral is taken on a straight line trajectory between the inner and outer radius of the toroids.

The bending power is lower in the transition regions where the two magnets overlap ($1.3 < |\eta| < 1.6$). The position of the CS in front of the EM calorimeter demands a careful minimisation of the material in order to achieve the desired calorimeter performance. As a consequence, the CS and the LAr calorimeter share one common vacuum vessel, thereby eliminating two vacuum walls.



(a) End Cap Toroids

(b) Magnetic field inside the detector

Figure 1.7: The magnetic field with the contribute of main magnets and ECT, as we see can, with some correction factor, be considered constant.

1.3.2 Inner Detector

The Inner Detector (ID) is placed closest to the beam line, therefore its design must allow excellent radiation hardness and long-term stability in addition to ensure adequate performance. The full ID is a cylinder of 6.2 m long and 2.1 m diameter with coverage of $|\eta| < 2.5$, and is segmented into cylindrical layers in the barrel region, and coaxial disks in the end-cap regions, as shown in Figure 1.8.

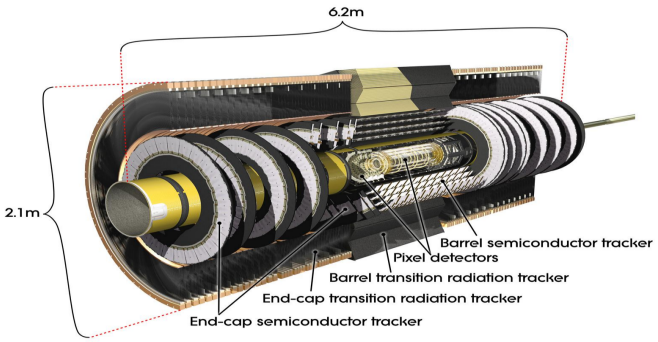


Figure 1.8: A cut-away view of the ATLAS inner detector [1].

The structural arrangement of the layers of the ID in the barrel region is shown in Figure 1.9, whilst one end-cap side of the ID is illustrated in Figure 1.10. The basic geometrical parameters of each layer are also given in these two figures. The main parameters of each sub-detector are summarized in

Table 1.1, including the η coverage, the number of layers/disks/tubes, the number of hits left per track, the dimension of the basic element and the hit resolution.

	Hits/track	Element size	Hit resolution [μm]
Pixel, $\|\eta\| < 2.5$			
4 barrel layers	3	$50 \cdot 400 \mu m^2$	10(R $-$ ϕ), 115 (z)
2 $\times$ 3 end-cap disks			10(R $-$ ϕ), 115 (R)
SCT, $\|\eta\| < 2.5$			
4 barrel layers	8	$50 \mu m$	17(R $-$ ϕ), 580 (z)
2 $\times$ 9 end-cap disks			17(R $-$ ϕ), 580 (R)
TRT, $\|\eta\| < 2.0$			
73 barrel tubes	~ 30	d=4 mm, l=144 cm	130/straw
160 end-cap tubes		d=4 mm, l=37 cm	

Table 1.1: Summary of the characteristics for each sub-detector of the inner detector.

Pixel Detector
In order to have good vertex performance, the pixel detector is designed to have the finest granularity, as shown in Table 1.1. The system consists of four barrels (Insertable B-Layer, B-Layer, Layer 1 and Layer 2) and three disks on each side. It will be described in detail in the next Chapter.

Semiconductor Tracker
In each SCT layer, it has two sets of SCT strips. In order to measure both lateral and longitudinal coordinates, the two sets of strips are glued back-to-back with an angle of 40 mrad in between, i.e. one set is either parallel, or perpendicular to the beam line.

Transition Radiation Tracker
The TRT detector is packaged in straw tubes made of polyamide, and uses a Xenon-based (70%) gas mixture with CO_2 (27%) and O_2 (3%). It measures only one coordinate with z$-$axis or radius information missing in barrel or end-caps due to their axial or radial placement. The TRT occupies the largest space of the ID and provides the majority of hits per track, and hence it contributes most to the momentum measurement. Although the TRT has lower precision compared to the silicon precision detectors, it offers longer measurements of tracks to retrieve the momentum information.

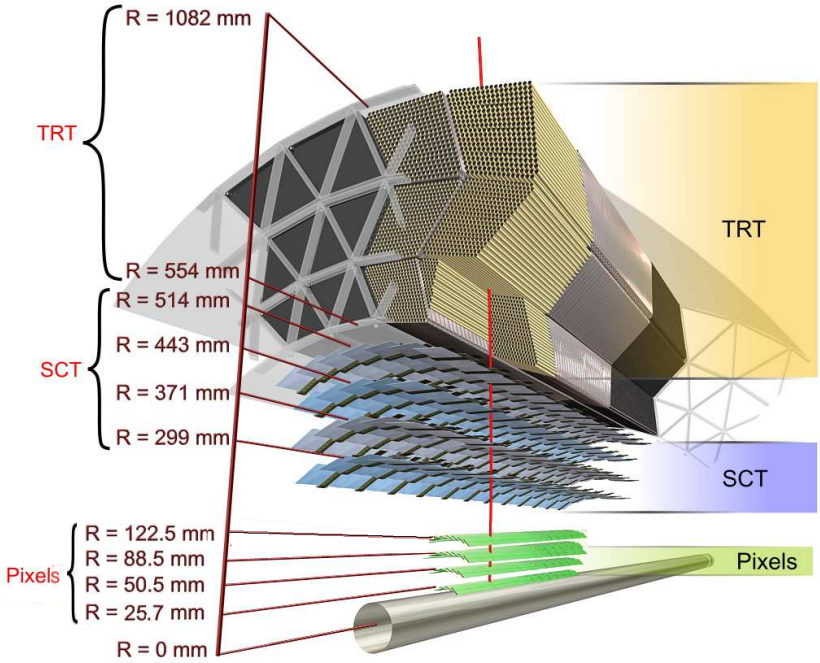


Figure 1.9: A three-dimensional drawing illustrating the structural arrangement of the ID layers in the barrel region, with their radii.

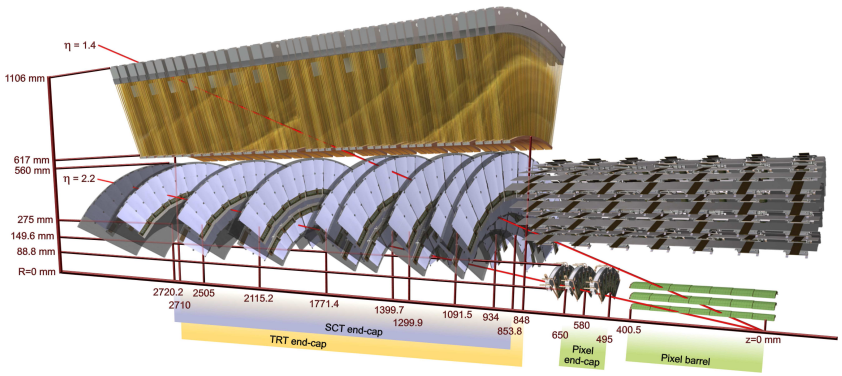


Figure 1.10: A three-dimensional drawing illustrating the structural arrangement of the ID layers in one end-cap region, with their radii and z-axial distance (using the detector center as origin).

The tracks left by the charged particle in the ID can be reconstructed using two main algorithms. One is the baseline inside-out algorithm designed for the reconstruction of primary tracks left by the charged particles originating from the p-p collisions. It starts from three point seeds from the silicon detectors (both Pixel and SCT), and adds the successive hits using a combinatorial Kalman-fitter [4]. The other algorithm is the outside-in algorithm which is designed for the reconstruction of the secondary tracks orginating from secondary particles in decays of primary or other secondary particles in the ID. The outside-in algorithm extends the reconstructed TRT segment [4] by adding the silicon hits with the combinatorial Kalman-fitter as the inside-out does. The TRT segments which do not have any extension in the silicon detectors will be reconstructed as the TRT standalone tracks. The reconstruction efficiency of a track can be measured in simulated events by taking the ratio of the tracks matched to charged particles to the number of generated charged particles; the efficiency varies as a function of p_T and η. For example, for primary tracks with $p_T = 10$ GeV, the efficiency is 92% when averaged over η [5].

1.3.3 Calorimeters

The calorimeters should contain the showers initiated by the incident particles and have good segmentation for space-point measurements. Besides, the calorimeters must have sufficient coverage for both η and ϕ to be able to measure well the total energy. The design of the ATLAS calorimeters thus includes an overall pseudorapidity up to $|\eta| = 4.9$, and a full ϕ coverage without cracks around the beam line. The overall layout of the calorimeters in ATLAS is shown in Figure 1.11. The inner part of the calorimeter system is composed of LAr electromagnetic calorimeters (EM Calo), in the barrel (EMB), the end-cap (EMEC) and the forward (FCal) regions. Hadrons not stopped by the EM Calo will reach the hadronic calorimeters, consisting of tile calorimeters in the barrel and extended barrel regions, the liquid argon (LAr) hadronic end-cap calorimeter (HEC) and the LAr forward calorimeters (FCal). The full calorimeter system must provide a good hermeticity to fully contain the electromagnetic and hadronic showers.
The ATLAS calorimeters are sampling calorimeters using different absorber (lead, copper or iron) and media (plastic scintillator or liquid argon), and the resolution of sampling calorimeters can be written as:

$$\frac{\sigma_E}{E} = \frac{a}{\sqrt{E}} + \frac{b}{E} + c$$

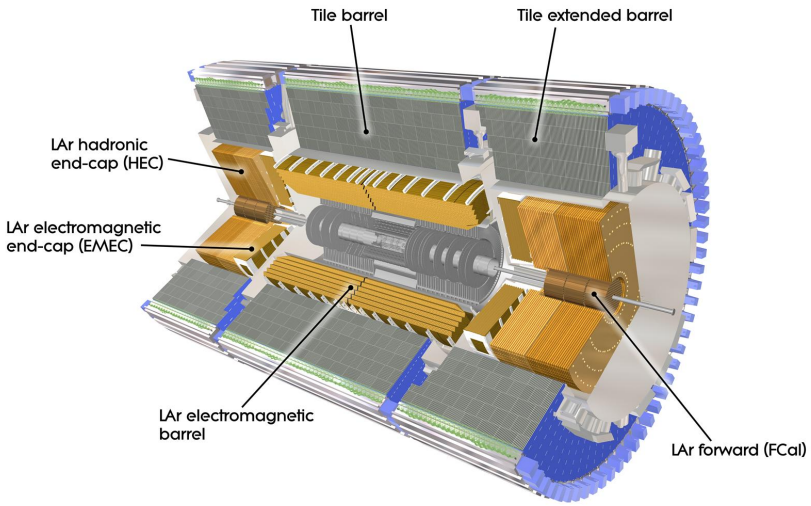


Figure 1.11: A cut-away view of the ATLAS calorimeter system.

The first term is called the stochastic (sampling) term, coming from the fact that the secondary particle shower has intrinsic fluctuations due to the interleaved layers of the absorber and the active medium. The second term is known as the noise term which mainly comes from the electronic noise of the readout channels. The last constant term depends mainly on the detector mechanics and readout system and, besides, it can be affected by the temperature gradients, detector aging and radiation damage. The electromagnetic calorimeter is measured to have a resolution of $\sigma_E/E = 10\%/E + (1.2 \pm 0.1^{+0.5}_{-0.6})\%$ [6] in the barrel region, while the resolution for the hadronic calorimeter in barrel and end-caps is measured varying from 0.13 to 0.06 when jet p_T increases; the FCal for electromagnetic measurements is measured to have $\sigma_E/E = 100\%/E + (2.5 \pm 0.4^{+1.0}_{-1.5})\%$.

1.3.4 Muon system

The muon system is the outermost layer of ATLAS. It is designed to measure the momentum of muons in $|\eta| < 2.7$. It contains a muon spectrometer and a toroid magnet system which consists of three large superconducting air-core toroid magnets. In addition to tracking the muons, the muon system contains trigger chambers with timing resolution of the order of 1.5-4 ns. The layout of the ATLAS muon system is shown in Figure 1.12. It is composed of various gas detectors: Monitored drift tubes (MDT's), Cathode strip chambers (CSC's), Resistive plate chambers (RPC's) and thin gap chambers (TGC's).

The four components can be classified by function into precision tracking chambers and trigger chambers. In the barrel region, the chambers form layers in cylinders that are placed at radii of approximately 5m, 7.5m and 10m, and in the transitions and end-caps they are disposed in wheels at a distance from the interaction point of approximately 7.4m, 10.8m, 14m and 21.5m.

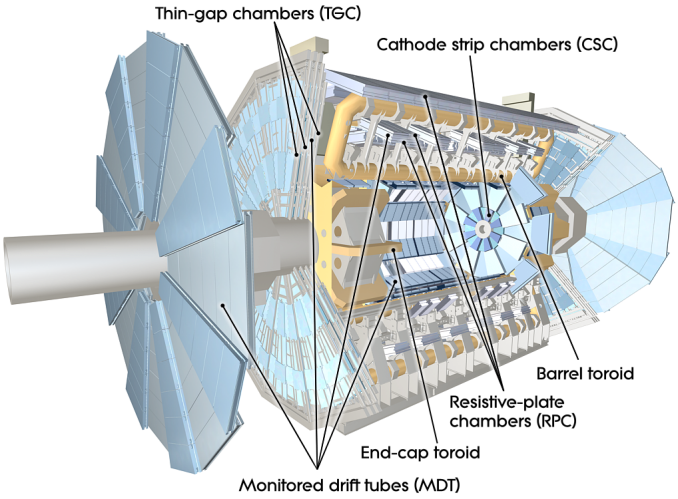


Figure 1.12: A cut-away view of the ATLAS muon system.

Precision tracking chambers

The precision tracking measurement carried out by the muon system combines the output of the MDT chambers and the CSC chambers. The MDT chambers are made up of aluminum tubes placed transverse to the beam axis, and filled with mixed Ar/CO_2 gas. They are designed to provide precision measurement of hit over $|\eta| < 2.0$ with resolution of approximately 80 μm in r $-$ ϕ . There are 1150 MDT chambers in total, and they are arranged in cylindrical layers in the barrel region and end-cap wheels. The CSC's are filled with mixed Ar/CO_2 gas and the basic element is a plane of perpendicular cathodes strips with multiple anode wires. They are placed in the region $2.0 < |\eta| < 2.7$, forming the two innermost wheels in the end-cap region, as shown in Figure 1.12. Each wheel contains four small and four large chambers which comprise four CSC's planes each, leading to four independent measurements on both coordinates (ϕ , η) per track. The CSC provide a resolution of ~ 60 μm in r $-$ ϕ per CSC plane.

Trigger chambers

The trigger chambers of the muon system are composed of RPC's in the bar-

rel region ($|\eta| < 1.05$) and TGC's in the end-caps ($1.05 < |\eta| < 2.7$). They are designed to provide fast muon information for Level 1 trigger determination, as well as timing information for bunch-crossing identification, within $|\eta| < 2.4$. In addition, the trigger chambers provide a second coordinate measurement complementary to the MDT's up to $|\eta| = 2.7$. The RPC is made of parallel electrode plates separated by a 2 mm gap filled with mixture of $C_2H_2F_4$, isobutane and SF_6 . The RPC's are constructed into three barrel layers: the two inner layers (RPC1 and RPC2) enable the trigger to select low-p_T tracks of 6–9 GeV, and the outer layer (RPC3) provides information for higher momentum tracks of 9–35 GeV for the trigger. All three layers are placed next to the MDT barrel layers in order to provide the second azimuthal coordinate to complement the MDT measurement, and it provides time measurement with a resolution of approximately 1.5 nanoseconds. The other trigger chamber, TGC, is a multi-wire proportional chamber, with a gas mixture of CO 2 and n-pentane. It also helps providing coordinate measurement complementary to the MDT. Besides, it provides time measurement with a resolution of 4 nanoseconds. To summarize, the whole muon system is designed to recognize muons within $|\eta| < 2.7$ with a threshold of $p_T >\sim 3$ GeV, as lower–p_T muons will mostly lose their energy before entering the muons chambers. The muon spectrometer is measured to be able to provide stand-alone muon p_T resolution of approximately 20% at 1 TeV. The magnetic field leads to a maximum accessible muon momenta determination of around 3 TeV. In addition to the momentum measurement, the muon system provides good position and charge measurements.

1.3.5 Trigger System

At the designed luminosity of $10^{34}\ cm^{-2}\ s^{-1}$, the rate of collisions is approximately 1 GHz. However, only $\sim 300Hz$ can be recorded due to limited resources. In order to effectively operate an online reduction of the data to be recorded, a multi-level trigger system is used, which is a chain of three levels of triggers: the Level-1 (L1), the Level-2 (L2) and the event-filter (EF) triggers. A schematic illustration of the trigger flow used in the ATLAS experiment is shown in Figure 1.13, with the event rate at each step. The L1 triggers are hardware-based only, and they must take a decision in less than 2.5 microseconds using the information directly from customized front-end electronics, provided by the muon system and calorimeters only, with a relatively coarse resolution.

The L1 triggers effectively reduce the data rate to 50 kHz. Before parsing events to next level trigger, Regions-of-Interest (RoI's) are defined containing the potential particle candidates found by the L1 triggers. The L2 and EF

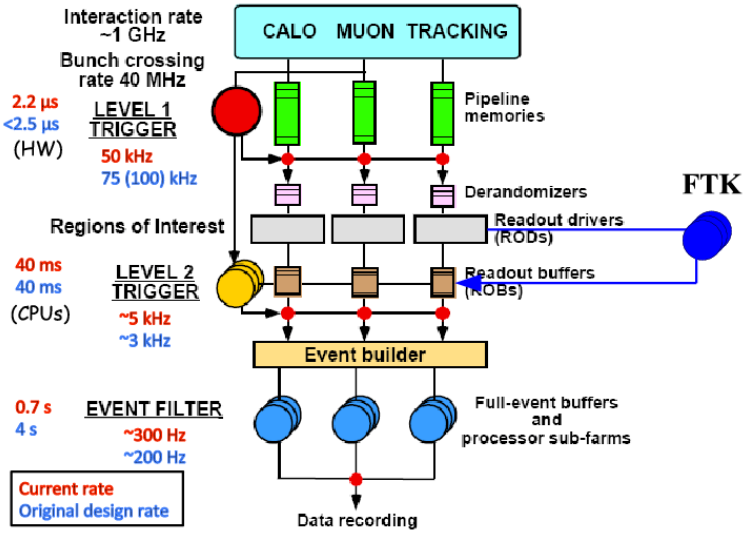


Figure 1.13: The trigger system [7].

triggers make up the High-Level Trigger (HLT), which lowers the data recording rate to the objective of 300 Hz. Unlike the L1 triggers, the HLT takes full-granularity measurement from all detectors using algorithms running on computers, and thus the HLT operates slower than the L1 triggers. The L2 triggers use CPU farms to process data from RoI's, and it takes the L2 triggers an average of 40 milliseconds to lower the rate from $\sim$ 50 kHz to $\sim$ 5 kHz. As the last element of this trigger chain, the EF uses algorithms close to the offline ones, and operates on the complete information from events to reach the final data rate within one second in average. The trigger menu contains a list of physics signatures (trigger chains), each of which specifies the thresholds and selection criteria on selected physics objects implemented throughout the trigger system. The trigger chain names follow a given convention defined in ATLAS indicating the trigger level and the criteria, for example, the *EF_g120_loose* trigger represents a HLT chain selecting events with at least one loose photon of $p_T > 120$ GeV.

Chapter 2

Insertable B-Layer

2.1 The Pixel Detector without IBL

Before the accelerator's shut-down in 2013, the Pixel Detector consisted of three layers; B-Layer (L0), Layer 1 (L1) and Layer 2 (L2). Their construction, in terms of radiation hardness and resolution, required the most advanced technology.

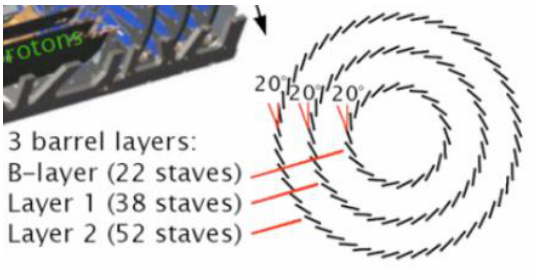
Layer Number	Mean Radius(mm)	Number of Staves	Number of Modules	Number of Channels	Active Area (m^2)
0(B)	50.5	22	286	13178880	0.28
1	88.5	38	494	22763520	0.49
2	122.5	52	676	31150080	0.67
Total		112	1456	67092480	1.45

Table 2.1: Summary of the characteristics for each sub-detector of the inner detector.

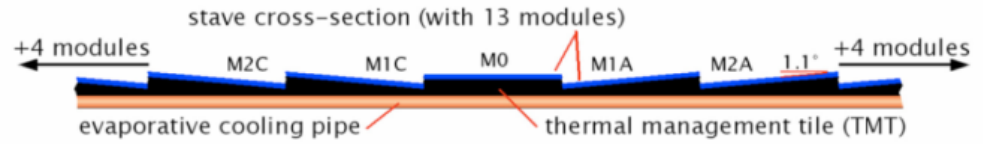
The pixel detectpr is composed of 112 long staves in total that are made of 13 modules tilted on z axis by 1.1 degrees toward the interaction point as shown in Figure 2.1(b); furthermore, to allow overlapping, the staves are tilted by 20 degrees on the x-y plane as shown in Figure 2.1(a).

2.1.1 Modules

Sensors, 16 Front End(FE-I3) chips, a flex-hybrid, a Module Controller Chip (MCC) and a pigtail together form what is called a module. FE-I3 is responsible for reading the charge signal from the pixel. Each 195 μm thick and 1.09 by 0.74 cm large FE-I3 counts 3.5 millions of transistors in 250



(a)



(b)

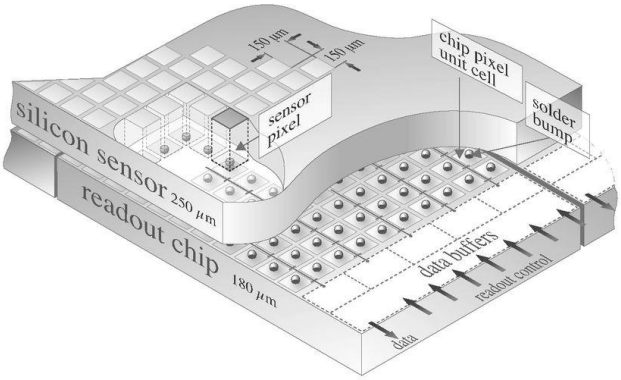
Figure 2.1: Staves disposition around the beam pipe(a), and modules layout inside each stave(b).

nm CMOS technology. They are bump bonded over the sensors (Figure 2.2) and each one has an analog amplifier able to discriminate signals of 5 000 e^- with a noise threshold of 200 e^- . Analog signals are then digitized and buffered inside the End Of Columns (EOC) electronic waiting for a trigger. EOC signals departs toward the MCC that has the following responsibilities:

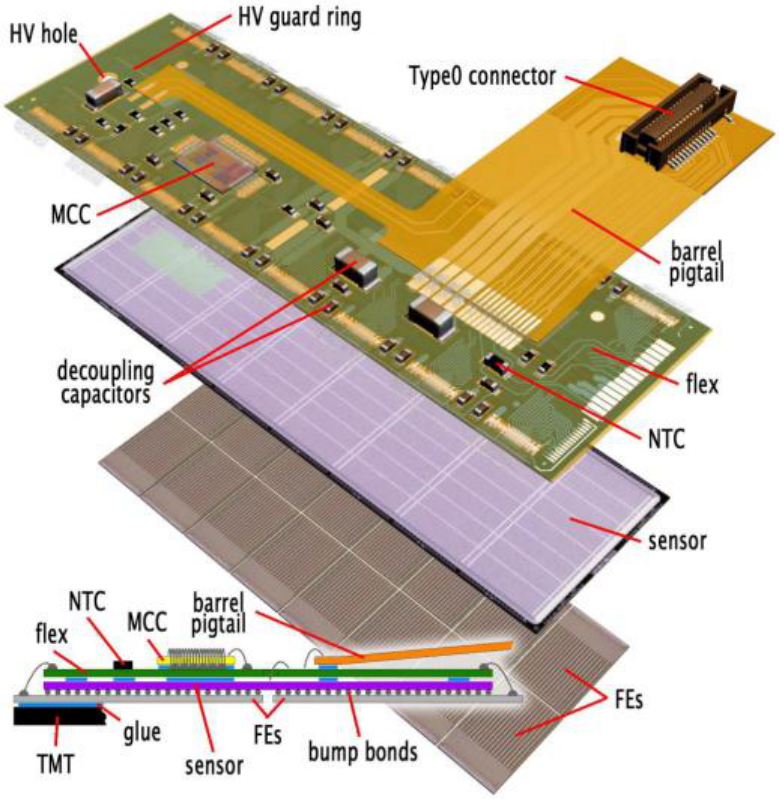
- distributing timing, trigger, reset and calibration signals;
- ordering the 16 FE-I3 EoC data and producing an event for the Read-Out Driver board (described in the next Chapter) .

Last but not least, the opto-board converts into optical signals the electric output from 6 MCC and send it out to the Back Of Crate board described later. Each opto-board is equipped with:

- PiN diode that converts optical to electrical;
- Digital Optical Receiver Integrated Circuit (DORIC) that adapt to LVDS standard the PiN signals;
- Vertical Cavity Surface Emitting Laser (VCSEL) that does a great efficiency electrical to optical conversion;
- VDC that interfaces MCC and VCSEL.



(a) Silicon sensor and read out chip (FE-I3) bump bonded.



(b) A figure representing all parts that forms a module.

Figure 2.2:

2.1.2 Sensors

A single pixel is composed of an n-doped crystalline semiconductor with a p-doped well, this "diode" is reverse polarized so the depletion region extends until a ionizing particle passes and frees some other electrons and holes. Before this charges can recombine the electric field separates and lead them on the metal contacts where a charge amplifier collect them as can be seen in Figure 2.3.

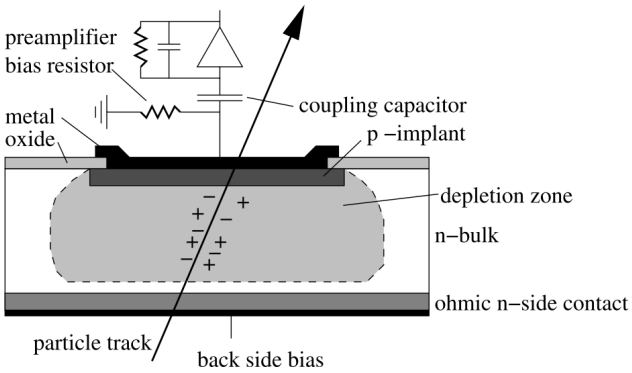


Figure 2.3: Single pixel layout with front end electronics connected.

Energy is proportional to the amount of charge collected by the contacts for that is the particle's track. Each module is made of a $256\mu m$ thick crystalline silicon layer and it is divided in 47232 pixels. 41984 pixels are 400 by $50\mu m$, and the others are slightly bigger ($600\times50\mu m$) and are located on the sides to minimize signal loss in the zone between two modules. The area of each pixel is bound to that of the read-out electronics, but the rate between length is not: the choice were made to have the maximum performance in x and y thus sacrificing z resolution.
Radiation affects pixels in two ways:

- increasing the leakage current, requiring a better cooling system;
- changing the n substrate type to p, thus moving the junction from the upper (Figure 2.3) to the lower face. The bias voltage need to be gradually increased from 150V to 600V until end of life as a result.

Two techniques were used to increase the radiation hardness and they were quite successful, leading to a doubled lifetime as resulting from tests:

- adding oxygen atoms into the crystalline structure;

- creating p-doped dividing zones among the n-doped wells with a technique called p-spray . In particular p-spray creates a decreasing distribution near the edges of n wells.

Another mean to reduce the damages is to keep silicon at -20 °C during all the data taking, in fact annealing consists of rising the amount of dopant absorbed by the substrates increasing its temperature.

2.2 IBL

The Insertable Barrel Layer (IBL) is a new pixel detector that has been inserted with a new shrunk beam-pipe inside the actual B-Layer. The main reasons for this upgrade are the following:

- the actual inner layer is suffering of a great mortality of pixels that will increase over time due to radiation exposure. This inefficiency causes a serious loss of b-tagging capability. IBL restores this capability even in the case of B-Layer complete failure;

- luminosity increase before the HL-LHC completion is too much for the cur- rent read-out system and the pile-up will lead to readout inefficiencies. The higher occupancy induced by luminosity will affect the present B-Layer more than other ones, leading to inefficiencies in the b-tagging. With IBL the b- tagging capability is restored and some redundancy added, also the high granularity leads to lower occupancy and higher precision;

- the tracking precision is strongly improved also with pixels closer to the interaction point. Improving the precision of impact parameter results in better sensitivity for signals in physics channels involving b jets.

Being this close to the beam pipe forces some constraints that are not needed in other layers: electronics has to be a lot more radiation hard and sensible area need to cover more than 70% of the surface, as is in B-Layer, to achieve those objective the FE-I4 was developed leading to an active area of 90%.

2.3 Sensors and Modules

IBL's modules and sensors are different from ATLAS ones because of the technology chosen for the pixels. There were 3 candidates:

- planar;
- 3D;
- diamond.

Diamond ones, due to economic reasons, were left out, and the FE-I3 chip was upgraded to FE-I4 that is described below.

2.3.1 Planar Sensors

Planar sensor were used within the B-Layer too, but the requests on IBL's one are much more strict, in fact the inactive border has to pass from 1mm of the old ones to $450\mu m$, and the acceptable effects on signal has to extend the actual NIEL dose of $2 \cdot 10^{15} n_{eq}/cm^2$ by at least 2 times. Various studies were done since B-Layer pixels were produced and now it is known that an irradiated sensor is capable of double the collected charge if it is less thick.

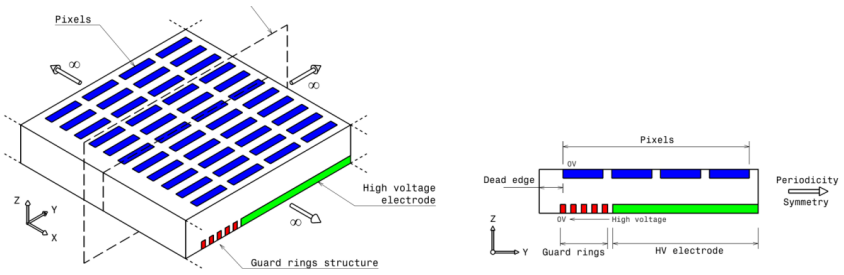


Figure 2.4: Planar Sensor graphic, configuration thin border.

Allowed configurations for planar sensors are 3:

- **Conservative:** layout of the sensors would not change if this type of con- figuration were chosen. Length would be reduced to 250 μm to shrink the inactive border, and guard rings would be reduced from 16 to 13. This choice would produce characteristics pretty much equal to the old pixel's while responding IBL's constraints;
- **Thin border:** an n-type bulk with a conservative like structure with guard rings on the p-doped side instead of the n one are the characteristics of this layout (Figure 2.4). A 100 μm inactive border and a non uniform electric field are the characteristics of this sensor, it seems that the non uniform field effect decrease with the irradiation;
- **Thin p-doped substrate:** these sensors are produced with a technology similar to the one of new ATLAS's strip detectors and a thinner wafer can be used.

2.3.2 3-D sensors

The geometry of 3-D sensors (Figure 2.5) is completely different from planar one and the need of reading from two electrodes at once is risen by the low level of charge collected by this pixels. Unfortunately noise rises along with the number of electrodes and is even affected by their diameter. The difference between full 3-D and double sided lies in etching, from one side or from each side of the wafer, during the productive process. Full 3-D sensors active area extends much closer to the surface reducing non sensible volume.

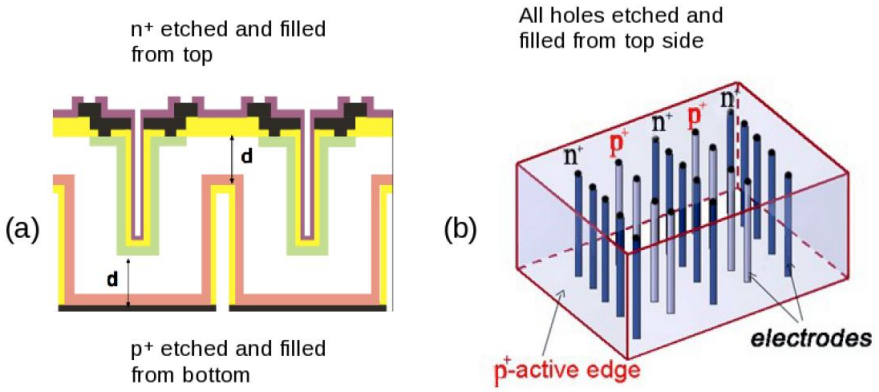


Figure 2.5: Two types of 3-D sensors, double sided(a) and full 3-D(b).

The faces of 3-D sensors, independently from the type, are much closer one another ant that allows a much lower bias voltage (150V versus 1000V of a planar sensor). This leads to a lower leakage current an thus less cooling. When a particle passes through the electrode area, efficiency results diminished by 3.3%. This effect affects only in perpendicular particles and thus will not affect IBL for its sensors are tilted by 20°.

2.4 FE-I4

FE-I4 (Figure 2.6) is the new ATLAS pixel chip developed to be used in upgraded luminosity environments, in the framework of the Insertable B-Layer (IBL) project but also for the outer pixel layers of Super-LHC.

FE-I4 is designed in a 130 nm CMOS process, in an 8 metal option with 2 thick aluminium top layers for enhanced power routing. Particular care has been taken to separate analog and digital power nets. With the thinning down of the gate oxide, the 130 nm CMOS process shows an increased radiation tolerance with respect to previous larger feature size processes.

The motivations for the redesign of the pixel Front-End FE-I3 came from several aspects, related to system issues and physics performances of the pixel detector. With a smaller innermost layer radius for the IBL project and an increased luminosity, the hit rate increases to levels which the FE-I3 architecture is not capable of handling.

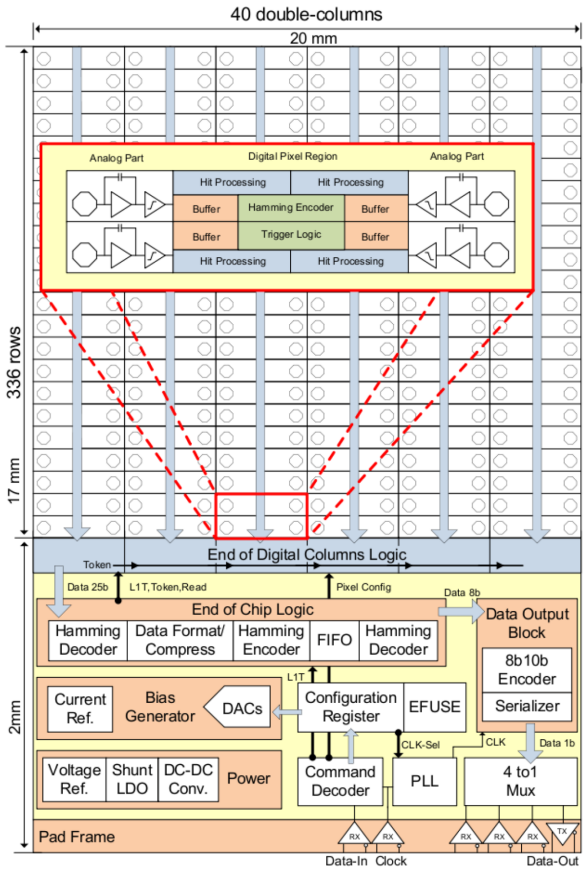


Figure 2.6: FE-I4 architecture layout.

In particular, it was shown that the current FE-I3 column-drain architecture [8] scales badly with high hit rates and increased FE area, leading to unacceptable inefficiencies for the IBL. FE-I4 stores hits locally to avoid a column-drain based transfer. The FE-I4 pixel size is also reduced, from 50×400 μm^2 to 50×250 μm^2 which reduces the pixel cross-section and enhances the single point resolution in z direction. FE-I4 is built up from an array of 80 by 336 pixels, each pixel being subdivided into analog and digital section. The total FE-I4 active size is 20 mm (z direction) by 16.8 mm (ϕ direction), with about 2 mm more foreseen for periphery, leading to an active area of close to 90% of the total. The FE is now a standalone unit avoiding

the extra steering of a Module Controller Chip for communication and data output. Communication and output blocks are included in the periphery of the FE. Going to a bigger FE size is beneficial with respect to active over total area ratio as well as for the building up of modules and staves. This leads to more integrated stave and barrel concepts, and as a consequence reduces the amount of material needed per detector layer. Such a reduction of material has a drastic effect on physics performance, e.g. on b-tagging efficiency vs. light quark rejection factor. One of the main advantages of having a big FE is also the cost reduction.

2.4.1 The Analog Pixel Section

The analog pixel section (Figure 2.7) fits $\sim 50 \times 150\ \mu m^2$, 60% of the total pixel size. It is implemented as a 2-stage architecture, optimized for low power, low noise and fast rise time, followed by a discriminator. The first stage is a regulated cascode pre-amplifier, with a triple-well NMOS input.

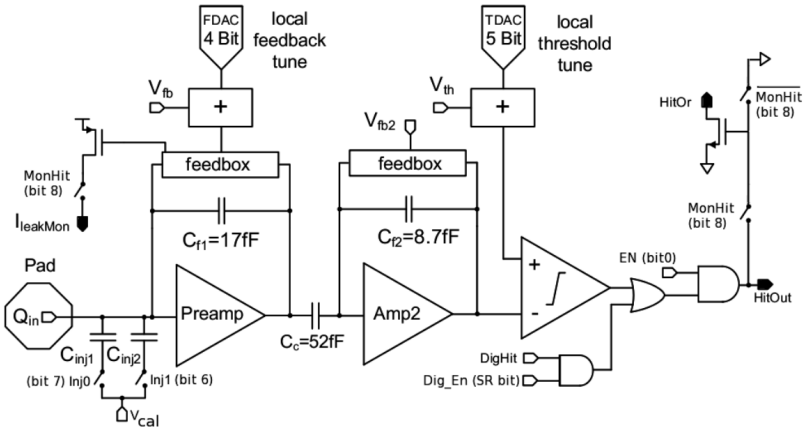


Figure 2.7: Front-end analog circuit.

It contains an active slow differential pair, tying the pre-amplifier input to its output, and used to compensate sensor radiation-related leakage current. The DC leakage current tolerance is above 100 nA. The second stage is AC coupled to the pre-amplifier, and is implemented as a PMOS input folded cascode. AC-coupling the second stage to the first brings mainly two benefits: This decouples the second stage from leakage current related DC potential shift, and gives an additional gain factor of about 6 (ratio of coupling capacitance to feedback capacitance of the second stage). As a consequence, the feedback capacitance of the first stage can be increased with positive

consequences on charge collection efficiency, signal rise time and power consumption, without degrading the signal pulse amplitude at the discriminator input.

2.4.2 The Digital Pixel Region and the Double-Column

To avoid sources of inefficiency related to a column-drain-based architecture, FE-I4 is based on a local storage of pixel hits in buffers located at pixel level, taking advantage of the small feature size of the CMOS 130 nm process. The choice of a 2 by 2 pixel region leads to an efficient hit recording with hit losses below 0.6% at hit rates corresponding to 3 times LHC full luminosity. As 4 pixels are tied together from the point of view of their digital logic, digital processing can be shared by the 4 pixels together, which leads to area reduction and power savings. Finally, as pixels recording a small number of electrons are most of the time located in the vicinity of pixels recording rather large signals (clustered nature of real physics hit in our experiment), small hits can be recovered without being time-stamped, which gives a handle on time-walk. The 4-pixel region is sketched in Figure 2.8.

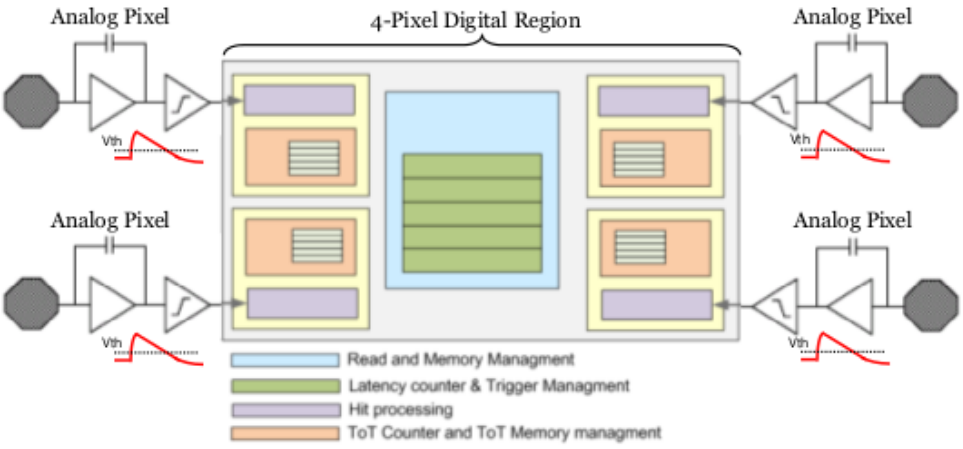


Figure 2.8: The 4-pixel regional digital logic.

The four pixels of the region form a 2 by 2 logic block inside a Double-Column which is fed by the 40MHz clock (LHC bunch-crossing). Latency counters and trigger management units, as well as read and memory management units are shared between four adjacent pixels. The 8-bit latency counters count down a programmable latency. The pixels still retain individual Time over Threshold (ToT) 4-bit counters, as well as individual hit

processing circuitry. Any discriminator that fires in the corresponding four analogue pixels starts the common latency counter, effectively time-stamping a particular event. It is to be noted that even if several pixels are hit in the same bunch-crossing, a single latency counter is allocated. This has the important consequences of reducing digital activity, reducing digital power and improving the efficiency of the architecture. Furthermore, it is possible to distinguish in the digital logic small hits from big hits, by the time the corresponding pixel comparators stay above threshold. The logic allows smaller hits to be associated with bigger hits in their immediate vicinity, either in the same region, or in adjacent regions (so-called "neighbour logic" mechanism). This provides a way to avoid recording small hits with time-walk.

The readout is based on a dual token passing scheme (Double-Column/ End of Column tokens), made triple redundant with majority voting for yield enhancement. A pixel configuration shift register runs in each Double-Column for tuning of each analogue pixel locally. For yield enhancement, it is made redundant as well. The End of Column logic is kept very simple and serves only as a dedicated interface between each of the 40 Double-Columns and the digital control block with its FIFO.

2.4.3 Periphery of the FE-I4 chip

The periphery schematic of the FE-I4 contains blocks that fulfill the following operations: communication and operational tuning of the IC; organization of the data read back and fast data output serialization. Finally some blocks are implemented to provide extra testing capabilities (e.g. redundant memories, low speed multi-purpose multiplexer), or as prototype blocks for the future production IC (e.g. powering section). Two LVDS inputs are required to communicate to the FE-I4: the clock (nominally 40 MHz) and the command input Data-In (40 Mb/s). In the FE-I4 command decoder, the command stream is decoded into local pixel configuration, global configuration and trigger commands. It is based on the architecture for the module control chip of the existing ATLAS pixel detector. No separate module control chip is needed for the IBL, further reducing the IBL mass. The decoded pixel configuration is sent to the pixels for storage in the 13 local register bits of the pixel. The 32 16-bit deep registers are used for global tuning of the operation of the chip. In the bias generator section, based on an internal current reference, DACs convert the stored configuration values to voltages and currents needed to tune the various sections of the IC. The decoded trigger is propagated to the pixels and to the "End of Chip Logic" block where the readout is initiated. When a trigger confirms a hit (the coincidence of a trigger with a latency counter reaching its latency value inside a 4-PDR), data stored

in the 4-PDR ToT buffers are sent to the periphery and associated to the bunch-crossing corresponding to the specific trigger. In the double-column, the 4-PDR address as well as the 4 ToTs are propagated to the "End of Chip Logic" (the transmitted signals are Hamming coded for yield enhancement). The data are then re-formatted (for band-width reduction and to facilitate the following data processing steps) and stored in a FIFO to be sent out. In addition to stored pixel data, read back information from pixel and global registers, as well as some diagnostic information (error messages), can be included. The data is then 8b10b-encoded in the "Data Output Block" and serialized at 160 Mb/s. Fast serialization is made possible by use of a high speed clock provided by a "Phase Lock Loop" clock generator.

Chapter 3

Off detector electronics for IBL

The IBL's readout requires an appropriate off-detector system that is schematically shown in Figure 3.1.

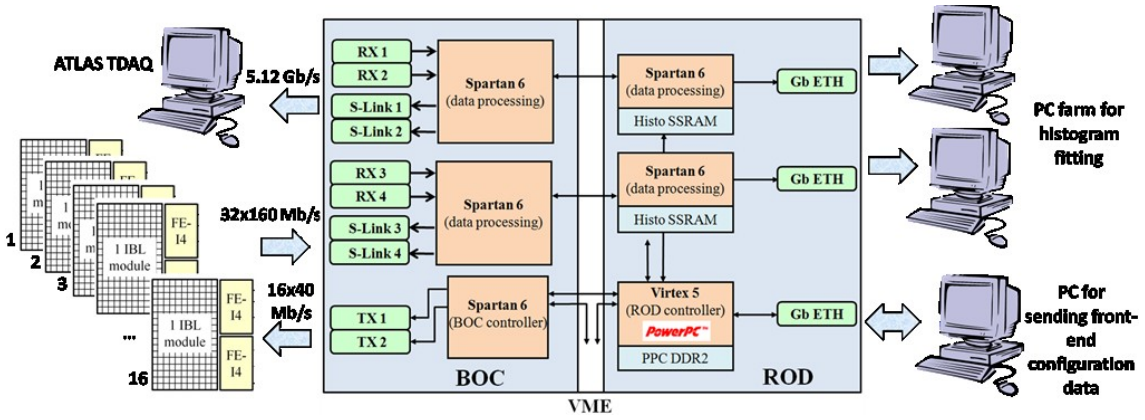


Figure 3.1: Block schematic of the IBL readout system.

The readout system is composed by several components:

- Back Of Crate (BOC) board;
- ReadOut Driver (ROD) board;
- VME Crate;
- TTC Interface Module (TIM);
- Single Board Computer (SBC);
- S-Link for sending data from BOC board to ATLAS TDAQ system;

- optical modules for communications between FE-I4 and BOC board;
- Gigabit Ethernet for sending front-end configuration data and histograms.

Each component's task will be described in detail in next sections.

FE-I4 data are received from the BOC board via the RX optical modules, then 8B/10B decoding is performed before passing data to the ROD that processes them. During physics runs events to be sent to the ATLAS TDAQ are sent back to the BOC, where 4 S-Link modules are implemented for a total output bandwidth of 5.12 Gb/s.

Each BOC-ROD pair is able to readout data coming from 16 IBL modules (32 FE-I4 front-end chips for a total input bandwidth of 32 x 160 Mb/s = 5.12 Gb/s) so the whole IBL readout requires 15 BOC-ROD pairs hosted in a single VME crate.

3.1 IBL BOC

The BOC board (Figure 3.2) is responsible for handling the control interface to the detector and the data interface from the detector. Also, one major

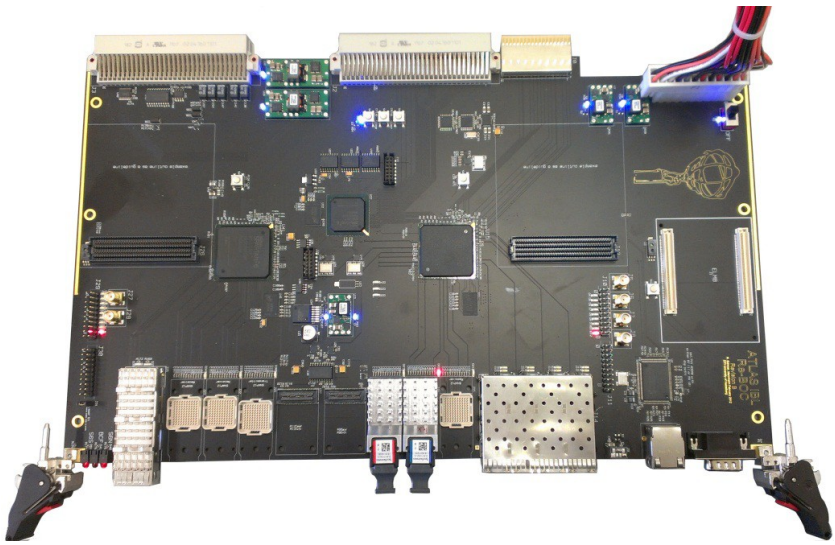


Figure 3.2: IBL BOC board.

task of the BOC is to provide the clock to the connected detector parts. Therefore the TIM clock is received by the BOC and can be delayed if needed. Furthermore, a PLL generates copies from this for the ROD and for the

detector. The detector clock is handled by the FPGAs and coded into the control streams for the individual detector modules.
The IBL BOC contains three Xilinx Spartan 6 FPGAs:

- one BOC Control FPGA (BCF);
- two BOC Main FPGAs (BMF).

3.1.1 BOC Control FPGA (BCF)

The BOC Control FPGA (BCF) is responsible for controlling the card. Central part of the firmware is a Wishbone interconnect [9] which builds the basis for accessing all peripherals on the card. Two master units are connected to this interconnect: a Setup-Bus connector and the Microblaze processor. The Microblaze processor is mainly used to provide Ethernet access to the card but there are also some self test functions for the card implemented in it. The Setup-Bus (Figure 3.3) is an asynchronous configuration interface between the ROD and BOC card. It provides 16 address, 8 data and 3 control lines.

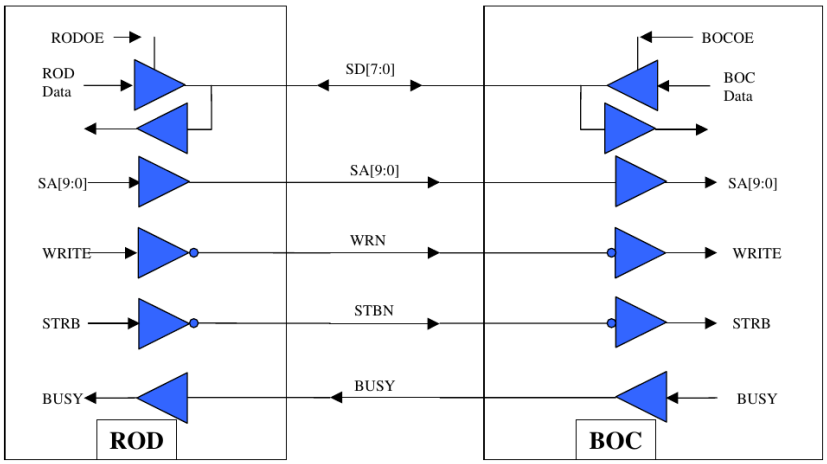


Figure 3.3: Setup Bus interface.

The BCF is also responsible for FPGAs configuration; indeed a two-step start-up sequence is used. Firstly, the BCF loads its configuration in “Master Serial Peripheral Interface” mode from a 64Mbit SPI FLASH. Subsequently the BCF firmware reads the configuration data for the two main FPGAs from a second SPI FLASH and downloads it via the Slave Serial configuration ports. Depending on the configuration the BCF will finally load software from a third SPI FLASH.

3.1.2 BOC Main FPGA (BMF)

The two BMF encode the configuration data coming from ROD into a 40 Mbit/s serial stream and then send it out to front-end. The TX path is used to send commands and triggers to the modules. In normal detector operation it is used to do the **Bi-Phase Mark (BPM)** encoding (Figure 3.4) of the incoming data from the ROD and to adjust the detector timing using coarse and fine delay blocks. The coarse delay is implemented using a variable-tap shift register clocked with 160 MHz.

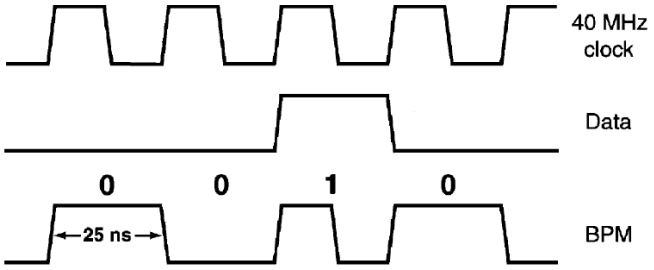


Figure 3.4: Bi-phase Mark encoding example.

The RX path in the firmware is responsible for the reception and decoding of incoming detector data. After decoding the data 4 channels are collected and multiplexed to the ROD.

3.1.3 BOC-ROD communication

The BOC-to-ROD interface carries all data which has been received from the detector. There are 96 lines with SSTL3 (Stub Series Terminated Logic [10]) I/O standard between the cards. The 96 lines are divided into 8 12-bit wide data busses. Each data bus transfers the data of 4 front-end chips at a rate of 80 MHz. Table 3.1 shows the assignment of the lines to the busses. Data lines carry the decoded 8b/10b data of the channels and the control line shows if the data is a 8b/10b-k-word (see Appendix A).

3.2 IBL ROD

IBL **ROD** board is a 14-layer 9U x 400 mm VME64x board meant to be the upgrade of the ATLAS Silicon Read Out Driver (**SiROD**), that is used in the ATLAS Off-Detector electronics sub-system in order to interface with Silicon Tracker (SCT) and Pixel B0, L1 and L2 Front End Detector modules.

Name	Function	
RXDATA< 7 : 0 >	Data	BMF south, channel 0...3
RXDATA< 9 : 8 >	Address	BMF south, channel 0...3
RXDATA< 10 >	Valid	BMF south, channel 0...3
RXDATA< 11 >	Control	BMF south, channel 0...3
RXDATA< 35 : 28 >	Data	BMF south, channel 4...7
RXDATA< 37 : 36 >	Address	BMF south, channel 4...7
RXDATA< 38 >	Valid	BMF south, channel 4...7
RXDATA< 39 >	Control	BMF south, channel 4...7
RXDATA< 19 : 12 >	Data	BMF south, channel 8...12
RXDATA< 41 : 40 >	Address	BMF south, channel 8...12
RXDATA< 43 >	Valid	BMF south, channel 8...12
RXDATA< 42 >	Control	BMF south, channel 8...12
RXDATA< 27 : 20 >	Data	BMF south, channel 13...16
RXDATA< 45 : 44 >	Address	BMF south, channel 13...16
RXDATA< 47 >	Valid	BMF south, channel 13...16
RXDATA< 46 >	Control	BMF south, channel 13...16
RXDATA< 55 : 48 >	Data	BMF north, channel 0...3
RXDATA< 57 : 56 >	Address	BMF north, channel 0...3
RXDATA< 58 >	Valid	BMF north, channel 0...3
RXDATA< 59 >	Control	BMF north, channel 0...3
RXDATA< 83 : 76 >	Data	BMF north, channel 4...7
RXDATA< 85 : 84 >	Address	BMF north, channel 4...7
RXDATA< 86 >	Valid	BMF north, channel 4...7
RXDATA< 87 >	Control	BMF north, channel 4...7
RXDATA< 67 : 60 >	Data	BMF north, channel 8...12
RXDATA< 89 : 88 >	Address	BMF north, channel 8...12
RXDATA< 91 >	Valid	BMF north, channel 8...12
RXDATA< 90 >	Control	BMF north, channel 8...12
RXDATA< 75 : 68 >	Data	BMF north, channel 13...16
RXDATA< 93 : 92 >	Address	BMF north, channel 13...16
RXDATA< 95 >	Valid	BMF north, channel 13...16
RXDATA< 94 >	Control	BMF north, channel 13...16

Table 3.1: Assignment of the lines to the busses.

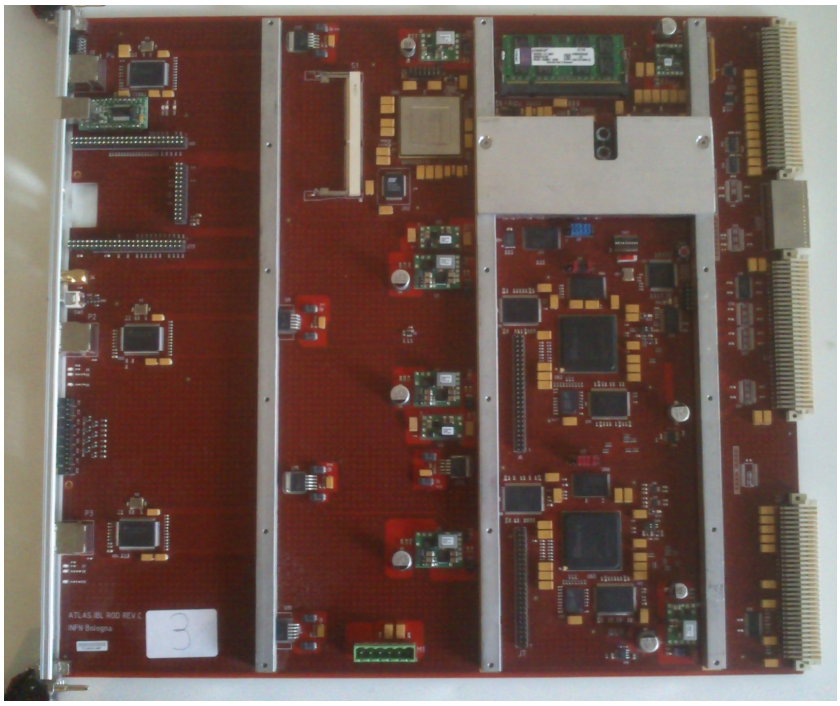


Figure 3.5: IBL ROD board.

This board was mainly developed in Bologna and this thesis work will focus in its firmware upgrading and testing. Its tasks are:

- data gathering and event fragment building during physics runs;
- histogramming during calibration runs;

IBL ROD contains:

- 1 Digital Signal Processor **MDSP** (Texas Instruments TMS320C6201-GJC200) currently not used;
- 1 Program Reset Manager (**PRM**) FPGA (Xilinx **Spartan6** XC6SLX45-FGG484);
- 1 ROD Controller (**master**) FPGA (Xilinx **Virtex5** XC5VFX70T-FF1136);
- 2 "**slave**" FPGAs (Xilinx **Spartan6** XC6SLX150-FGG900);
- 1 Phase-Locked Loop **PLL** (Lattice ispClock 5620);
- 32 MByte SDRAM DDR;

- 4 Mbit FLASH SST39VF040-70-4C-NH;
- 2 GByte DDR2 SODIMM;
- 64 Mbit FLASH Atmel AT45DB642D;
- 3 Gbit Ethernet interfaces with PHY DP83865.

3.2.1 PRM

One Xilinx Spartan6 FPGA acts as a Program Reset Manager (**PRM**). It interfaces with the VME bus, the ROD Controller FPGA, the slave FPGAs and the Phase-Locked Loop (PLL). Due to its interconnections with both VME bus (mastered by the Single Board Computer SBC) and the FPGAs, the PRM has a fundamental role in the VME FPGA's programming and resetting (as explained in Chapter 4).

3.2.2 ROD Controller

The Virtex5 FPGA is the Master of the Read Out Driver, which must interface with the front end chips, the triggers that comes from TTC Module and all the information that refers to the Trigger itself.
Embedded in this FPGA there is a Power PC **PPC**, a specific architecture of microprocessor. The modification of buses and peripherals of this component is possible with a Xilinx's program called EDK. The task of connecting PPC to the registers of all main FPGAs and routing each read and write command to the right register is accomplished by the **Address Decoder Busbridge**. In Figure 3.6 Rodmaster firmware logic blocks are shown.

Event ID and Trigger Processor Event ID and Trigger Processor can be driven either by PPC or by TIM signals. One of its duty is to process the trigger information (like Event ID, Trigger Type and Bunch Counter 50ID) and deliver it to the Spartan. The other one is to tell the Front End Command Processor to generate and send the necessary commands (like LV1) to the front end.

FE Command Processor This block generates the proper commands for the front end; it can generate fast and slow commands so it is involved in the configuration process too. When a trigger is issued by the TIM it immediately generates an LV1 command. This is a much faster process than issuing a command via PPC.

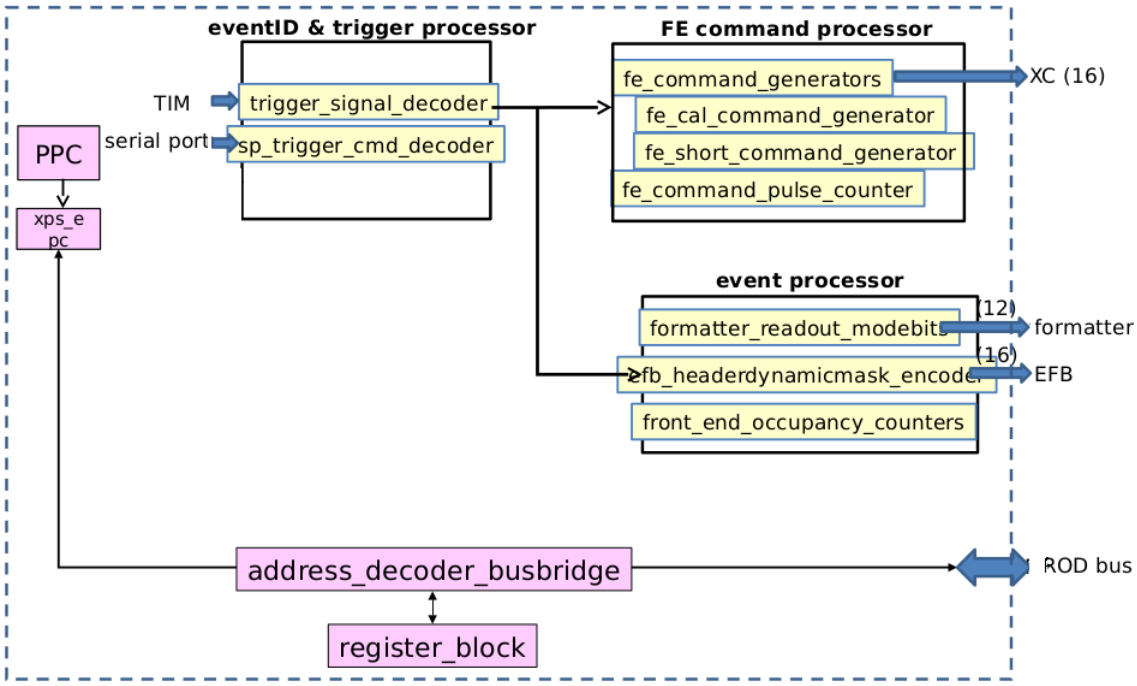


Figure 3.6: Rodmaster firmware logic blocks.

Event Processor It sends Event ID, Trigger Type and Bunch Crossing ID to Spartan's Event Fragment Builder. They will be written inside the header of each ROD event as identifiers.

3.2.3 Spartan 6 Slave FPGAs

Spartans FPGAs cope with all passing data during the data taking process, collect histogram data inside an SSRAM and sends them to an histogram server if required. To master all those tasks a MicroBlaze processor was implemented on each Spartan. It also manages the Ethernet connection and sends out the histograms through it.
In Figure 3.7 Spartan 6 Slave firmware logic blocks are shown.

Dual clock FIFO The dual clock FIFO works as a connection between two clock domains: the 80MHz of the bus and the 40MHz for the FPGA.

Event Fragment Builder (EBF) Data coming from all its input channels are connected to a EFB that adds header and trailer infos such as trigger type, event ID or bunch counter ID.

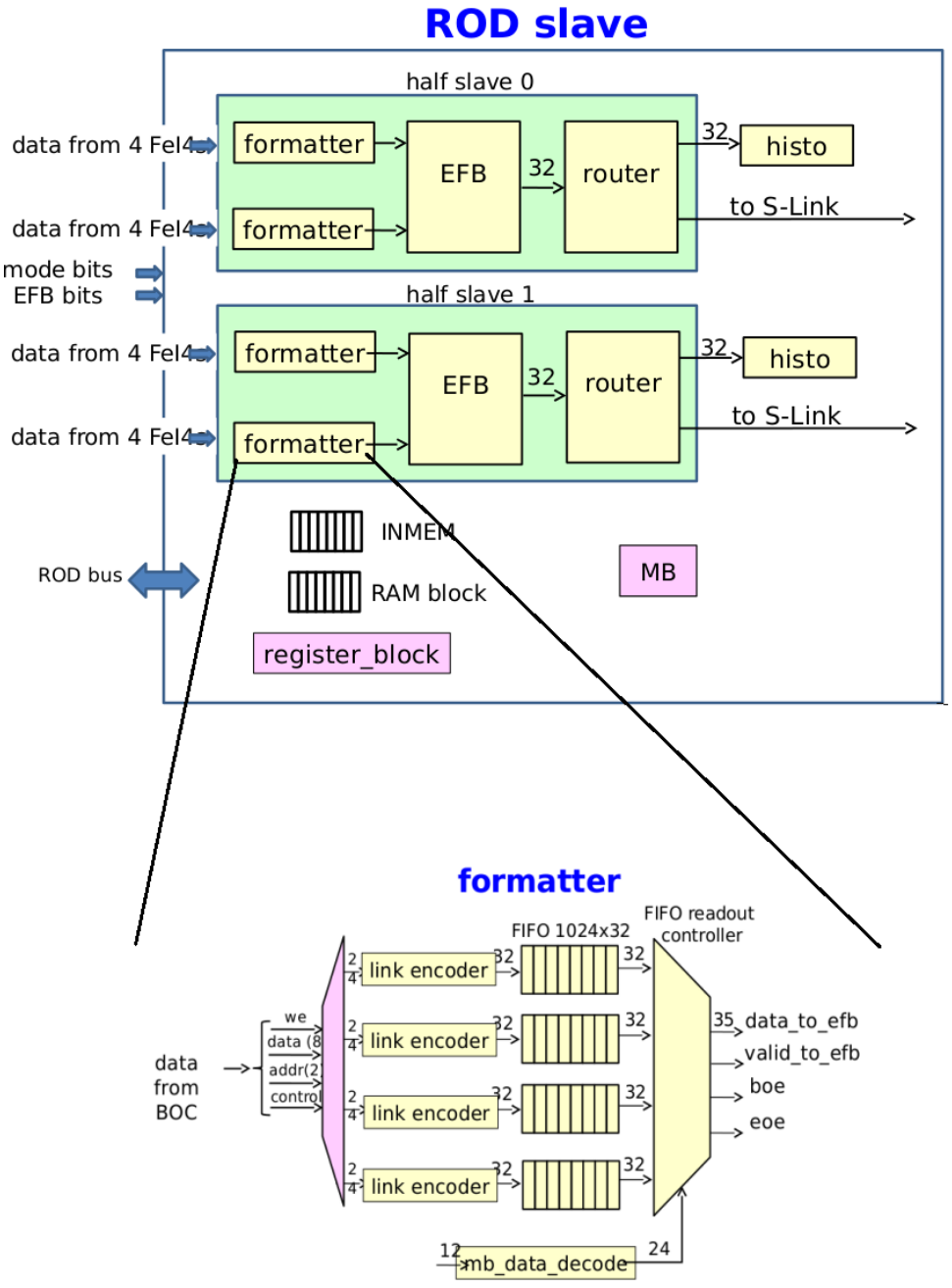


Figure 3.7: Spartan 6 Slave firmware logic blocks. **Formatter** is the component that contains the EFB and the dual clock FIFOs.

Inmem FIFO This is mainly a debug feature: this FIFO collects all inputs from the BOC-ROD buses and can be accessed by the PPC; data can then be verified even before entering the gatherer giving an insight of what should happen.

Histogrammer Histogrammer collects information about calibration runs. As inputs it has the TOT (Time over Threshold) and address coming directly from the FE-I4. It creates a map of pixels calibration responses inside a dedicated memory.

3.2.4 Lattice PLL

Lattice ispClock 5620 **Phase-Locked Loop** (PLL) is a control system that generates an output signal whose phase is related to the phase of an input signal. The function of the PLL is to compare the distributed clock to the incoming reference clock, and vary the phase and frequency of its output until the reference and feedback clocks are phase and frequency matched. In Figure 3.8 the functional block diagram is shown; we can distinguish four basic elements:

- Phase-Detector;
- Loop Filter;
- Voltage-Controlled Oscillator VCO;
- feedback path.

Phase Detector A phase detector (PD) generates a voltage which represents the phase difference between the reference input and the feedback from the VCO. The PD output voltage is used to control the VCO such that the phase difference between the two inputs is held constant, making it a negative feedback system. When there are no more phase differences a *LOCK* signal is produced.

Loop Filter The block called the PLL loop filter has two distinct functions.

The primary function is to determine loop dynamics, also called stability. This is how the loop responds to disturbances, such as changes in the reference frequency, changes of the feedback divider, or at startup. Common considerations are the range over which the loop can achieve lock (pull-in range,

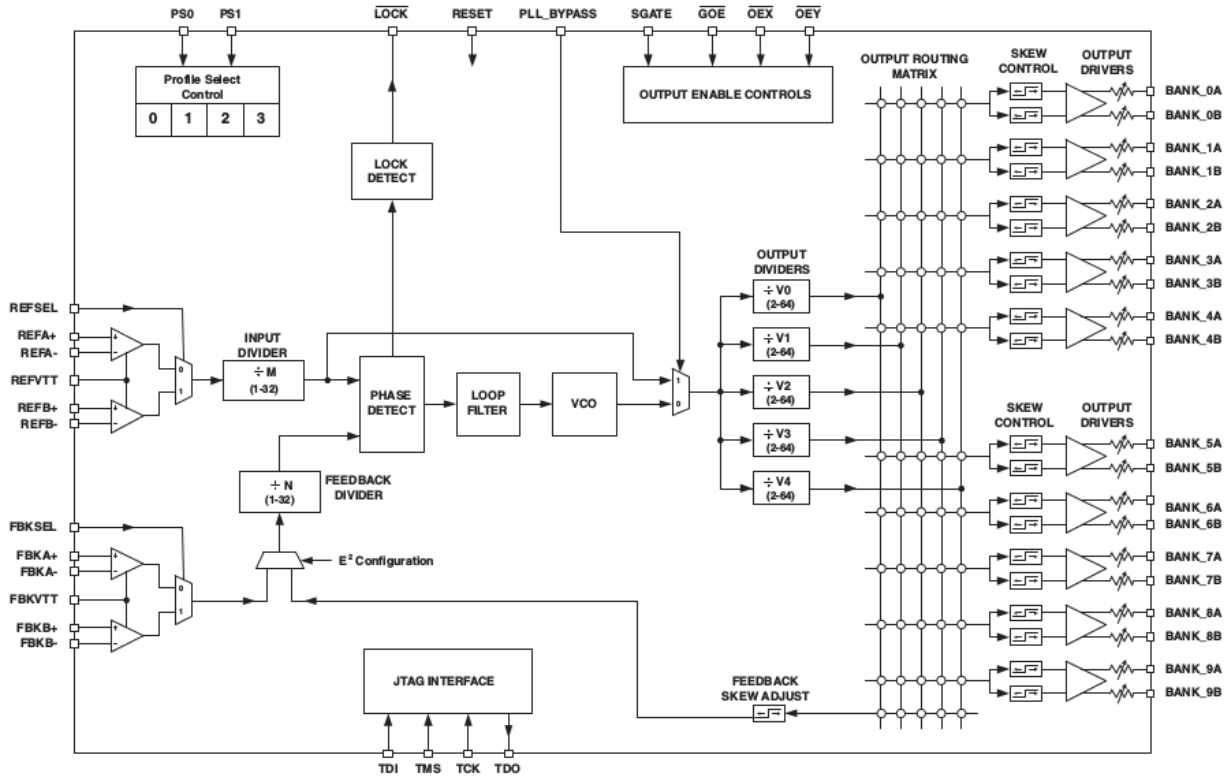


Figure 3.8: ispClock 5620 Functional Block Diagram.

lock range or capture range), how fast the loop achieves lock (lock time, lock-up time or settling time) and damping behavior. The second consideration is limiting the amount of reference frequency energy (ripple) appearing at the phase detector output that is then applied to the VCO control input. This frequency modulates the VCO and produces FM sidebands commonly called "reference spurs". The low pass characteristic of this block can be used to attenuate this energy, but at times a band reject "notch" may also be useful.

Voltage-Controlled Oscillator A Voltage-Controlled Oscillator (VCO) is a LC oscillator (Figure 3.9) made of an inductor and a capacitor, that have a resonance frequency:

$$f_0 = \frac{1}{2\pi\sqrt{LC}}$$

At the resonance the circuit behaves as a periodic oscillator. To obtain a variable oscillation frequency *inverse polarized diodes* (varactors) replace the capacitor.

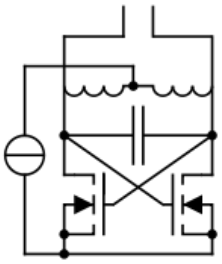


Figure 3.9: Example of a LC oscillator.

3.3 TIM

The TTC (Timing, Trigger and Control) Interface Module **TIM** (Figure 3.10) interfaces the ATLAS Level-1 Trigger system signals to the Pixel Read-Out Drivers using the LHC-standard TTC and Busy system [11, 12]. TIM tasks are basically the following:

- to propagate the TTC clock all over the experiment;
- to receive and propagate triggers;
- to keep updated with Bunch and Event Counters via Bunch Counter Reset(BCR) and Event Counter Reset(ECR) signals, with main TTC;

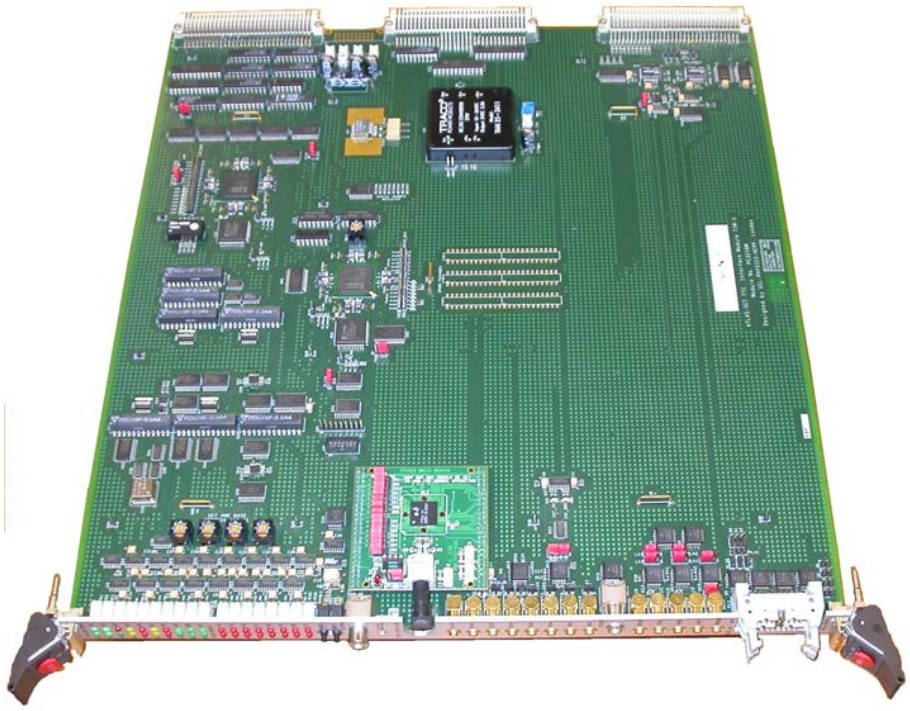


Figure 3.10: Photograph of a TIM.

- to propagate the previous informations to the ROD.

The production TIM design uses two FPGA's specifically to perform two different roles.
FPGA1 is the board manager supporting the more generic board functions: VME Interface, local bus control, board reset and provides status information on FPGA2.
FPGA2 hosts all the TIM specific functions and provides interfaces to front-panel and ROD backplane signals.

3.4 SBC

Single Board Computer, as the name suggests, is actually a computer mounted on a 6U board with a VME interface chip. It is used to control all the VME operations on the ROD, and it can actually program some of its components. It can also be used to monitor the temperature on a particular ROD's component.

3.5 S-Link

A Simple LINK (**S-Link)** is a link that can be thought of as a virtual ribbon cable, moving data or control words from one point to another.

The specification describes the interface between the Front-end Motherboard (FEMB) and the Link Source Card (LSC) and the interface between the Link Destination Card (LDC) and the Read-out Motherboard (ROMB). It does not describe the physical link itself. This concept is shown in Figure 3.11.

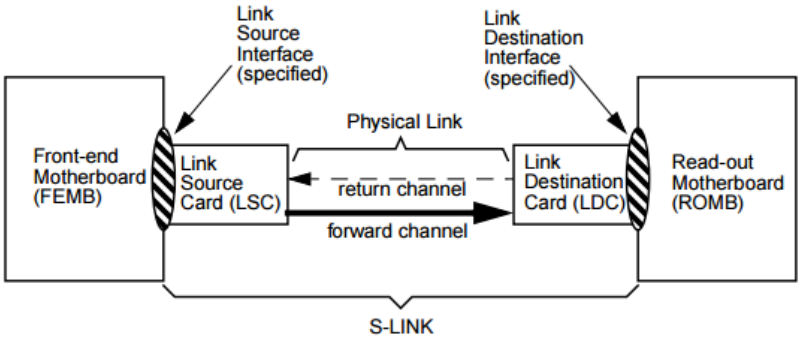


Figure 3.11: S-Link concept.

In addition to simple data movement, S-LINK includes the following features:

1. **Control/Data bit:** all words transmitted are accompanied by an additional bit which enables the user to mark any word and thus identify the word with a private meaning (e.g. block address, event header, end of block etc.);

2. **Error Reporting:** an S-LINK detects transmission errors and reports these using the LDERR line. In addition, the data error LED is illuminated and held until reset;

3. **Test Function:** the LSC and LDC can be switched to a test mode where the LSC transmits a fixed pattern which the LDC verifies. If any data errors are detected, the LDC illuminates the data error LED. The test pattern can be transferred to the ROMB by the LDC if desired;

4. **Reset Function:** a hard reset function is provided on both the LSC and the LDC.

Chapter 4

Firmware developing and upgrading

In this chapter my work on the IBL ROD board will be explained in detail. The boards had to be operative at the moment of the reactivation of LHC in May 2015, so they were already produced and tested when I started working on them. Also, the firmware was already existing but it contained some *bugs*. So my work mainly consisted in debugging the firmware, but I also added two features:

- FPGAs parallel programming via VME;
- PLL resetting via VME.

Those features will be described in detail in next sections, as well as the JTAG standard, used for programming and testing the FPGAs (the VME standard is described in Appendix B).

4.1 JTAG

The Joint Test Action Group (JTAG) is an electronics industry association formed in 1985 for developing a method of verifying designs and testing printed circuit boards after manufacture. In 1990 the Institute of Electrical and Electronics Engineers codified the results of the effort in IEEE Standard 1149.1-1990, entitled Standard Test Access Port and Boundary-Scan Architecture.

This standard defines test logic that can be included in an integrated circuit to provide standardized approaches to:

- testing the interconnections between integrated circuits once they have been assembled onto a printed circuit board or other substrate;

- testing the integrated circuit itself;
- observing or modifying circuit activity during the component's normal operation.

The objective of this standard is to define a boundary-scan architecture that can be adopted as a standard feature of integrated circuit designs, thus allowing the required test framework to be created on assembled printed circuit boards and other products. The test logic consists of a boundary-scan register and other building blocks and is accessed through a Test Access Port (TAP).

4.1.1 Boundary Scan

Boundary scan is a method for testing interconnects (wire lines) on printed circuit boards or sub-blocks inside an integrated circuit. The boundary-scan technique involves the inclusion of a shift-register stage (contained in a Boundary-Scan register Cell **BCS**) adjacent to each component pin so that signals at component boundaries can be controlled and observed using scan testing principles.

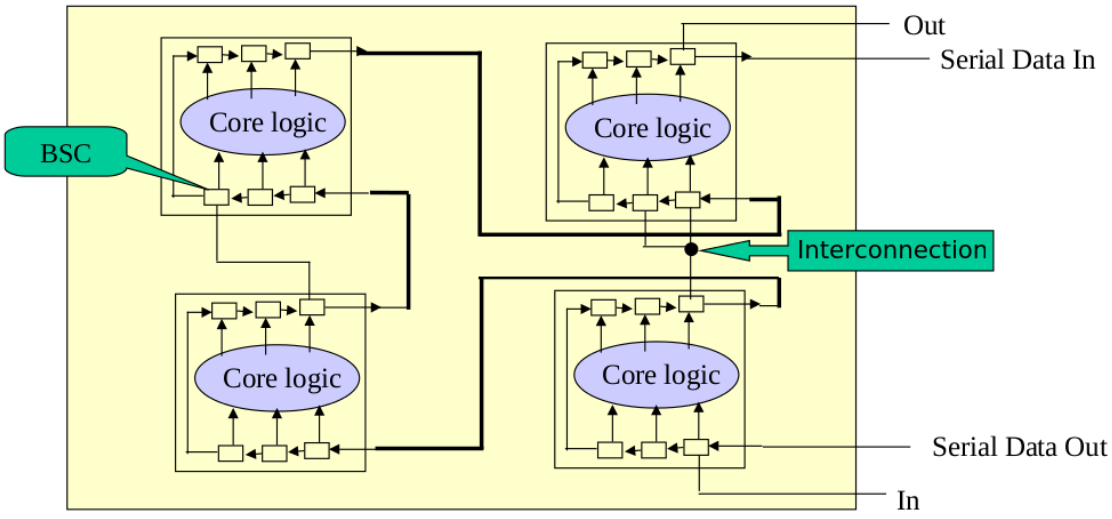


Figure 4.1: Board design with a single path that connects all the integrated circuits. Each IC pin has a Boundary Scan Cell (BCS).

The boundary-scan register cells for the pins of a component are interconnected to form a shift-register chain around the border of the design, and this

path is provided with serial input and output connections and appropriate clock and control signals.

The boundary-scan registers for the individual components of a product assembled from several integrated circuits could be connected in series to form a single path through the complete design (Figure 4.1) or, alternatively, a board design could contain several independent boundary-scan paths.

The resulting serial path through the complete design can be used in two ways:

- to allow the interconnections between the various components to be tested;
- to allow the components on the board to be tested.

4.1.2 BSC

Boundary Scan Cells (BSCs) are additional logic added to each pin of a device; these cells are then connected together to form a scan path to provide controllability and observability access via scan operations. In Figure 4.2 the scheme of a single BCS is shown.

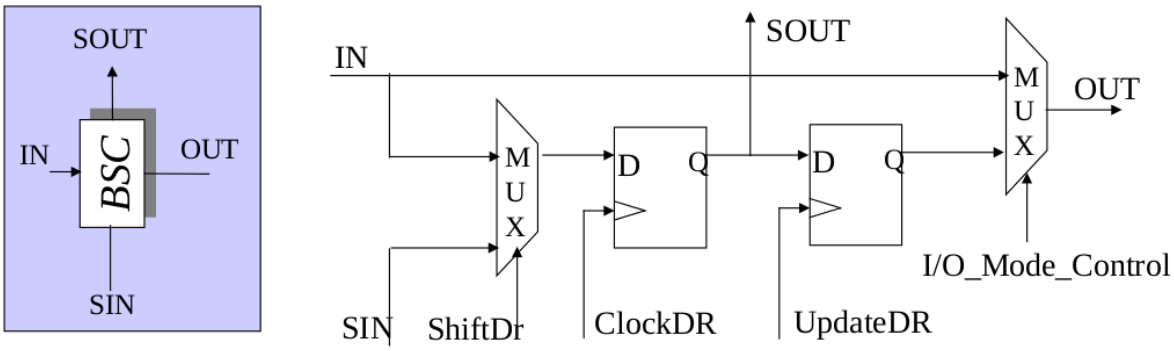


Figure 4.2: Boundary Scan Cell (Schematic).

BSC's signals are:

- **IN:** it is connected to a *primary* input of the chip (if the BSC is connected to an input pin) or to a *core* output of the chip (if the BSC is connected to an output pin);
- **SIN (Serial INput):** it is connected to SOUT of the previous BSC;
- **SOUT (Serial OUTput):** it is connected to SIN of the following BSC;

- **OUT:** it is connected to a *core* input of the chip (if the BSC is connected to an input pin) or to a *primary* output of the chip (if the BSC is connected to an output pin);
- **ClockDR (Clock Data Register):** clock for data shifting;
- **UpdateDR (Update Data Register):** clock for updating data to be sent to the chip logic core.

Depending on signals sent to the multiplexers, a Boundary Scan Cell can operate in four ways:

1. **Normal Mode:** data pass directly from IN port to OUT port (Mode Control = 0);
2. **Scan Mode:** all BSCs are cascade connected (ShiftDR = 1, clock applied to ClockDR);
3. **Capture Mode:** the value applied to the primary input of the chip is captured and memorized (ShiftDR = 0, clock applied to ClockDR);
4. **Update Mode:** test data that have to be sent to Core Logic (imposing Mode Control = 1) are updated (clock applied to UpdateDR).

4.1.3 Boundary Scan Architecture

Figure 4.3 shows the IEEE Std 1149.1 architecture. The architecture consists of an instruction register, a bypass register, a boundary-scan register, optional user data register(s), and a test interface referred to as the test access port (**TAP**). The instruction register and data registers are separate scan paths arranged between the primary test data input TDI pin (connected to the first BSC SIN pin) and primary test data output TDO pin (connected to the last BSC SOUT pin). This architecture allows the TAP to select and shift data through one of the two types of scan paths, instruction or data, without accessing the other scan path.

TAP Test Access Port (TAP) is controlled by the test clock (TCK) and test mode select (TMS) inputs. These two inputs determine whether an instruction register scan or data register scan is performed. The TAP consists of a small controller design, driven by the TCK input, which responds to the TMS input as shown in the state diagram in Figure 4.4. The IEEE Std 1149.1 test bus uses both clock edges of TCK. TMS and TDI are sampled on the rising edge of TCK, while TDO changes on the falling edge of TCK.

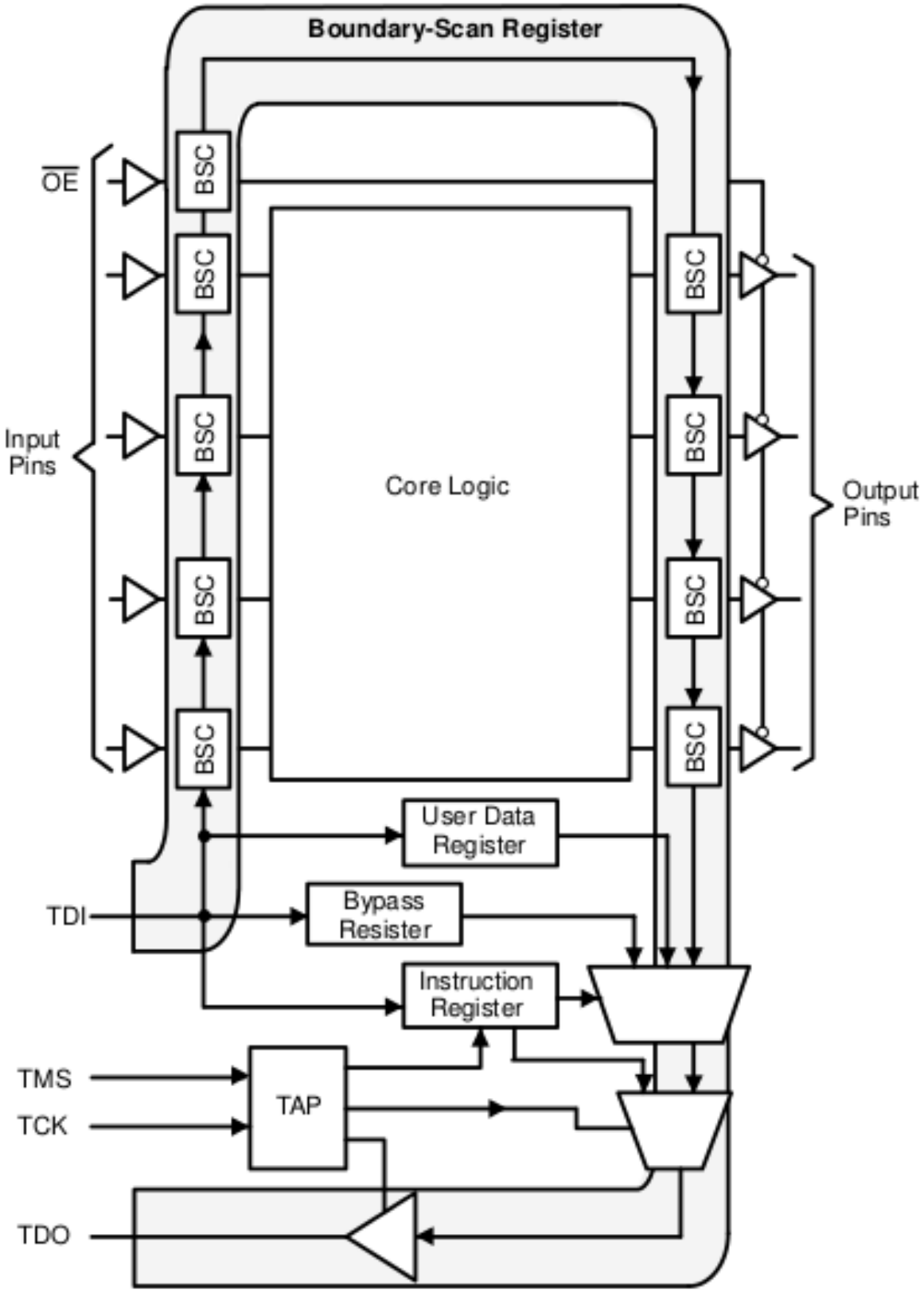


Figure 4.3: Boundary Scan Architecture. Boundary-scan register (BSR), a serially accessed data register made up of a series of boundary-scan cells (BSCs), is shown at the input and output boundary of the IC.

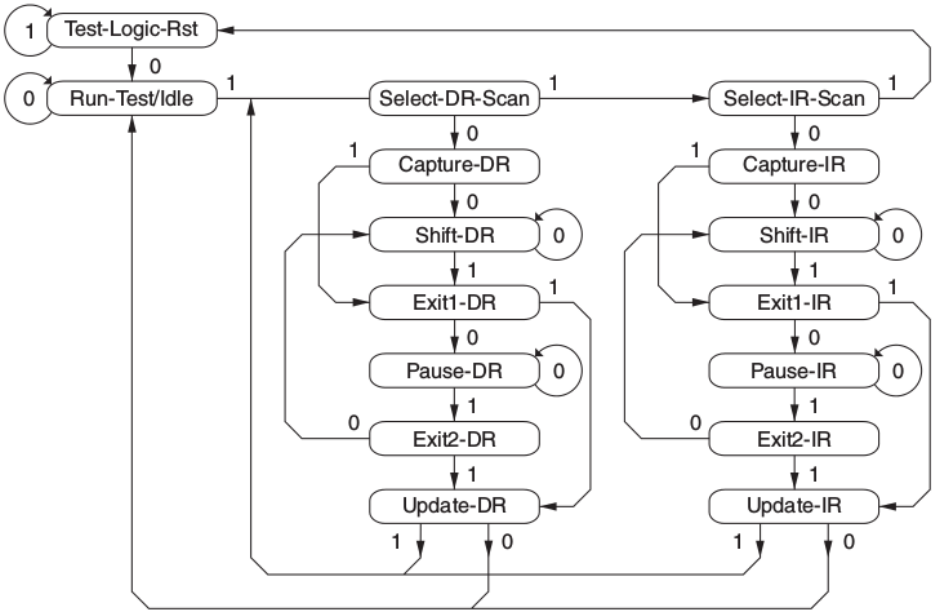


Figure 4.4: TAP Controller State Diagram.

The main state diagram consists of six steady states: Test-Logic-Reset, Run-Test/Idle, Shift-DR, Pause-DR, Shift-IR, and Pause-IR. A unique feature of this protocol is that only one steady state exists for the condition when TMS is set high: the Test-Logic-Reset state. This means that a reset of the test logic can be achieved within five TCKs or less by setting the TMS input high.

At power up, or during normal operation of the host IC, the TAP is forced into the Test-Logic-Reset state by driving TMS high and applying five or more TCKs. In this state, the TAP issues a reset signal that places all test logic in a condition that does not impede normal operation of the host IC. When test access is required, a protocol is applied via the TMS and TCK inputs, causing the TAP to exit the Test-Logic-Reset state and move through the appropriate states.

Upon entering the data register scan or instruction register scan blocks, shadow latches in the selected scan path are forced to hold their present state during the capture and shift operations. The data being shifted into the selected scan path is not output through the shadow latch until the TAP enters the Update-DR or Update-IR state. The Update state causes the shadow latches to update (or parallel load) with the new data that has been shifted into the selected scan path.

Instruction Register The instruction register is responsible for providing the address and control signals required to access a particular data register in the scan path. The instruction register consists of an **instruction shift register** and an **instruction shadow latch**.
The instruction shift register consists of a series of shift register bits arranged to form a single scan path between the TDI and TDO pins of the host IC. During instruction register scan operations, the TAP exerts control via the instruction register shift enable (SHIFTIR) and instruction register clock (CLOCKIR) signals to cause the instruction shift register to preload status information and shift data from TDI to TDO.
The instruction shadow register consists of a series of latches, one latch for each instruction shift register bit. During an instruction register scan operation, the latches remain in their present state. At the end of the instruction register scan operation, the instruction register update (UPDATEIR) input updates the latches with the new instruction installed in the instruction shift register.

Data Register The instruction register supplies the address that allows one of the data registers to be accessed during a data register scan operation. During a data register scan operation, the addressed scan register receives TAP control via the data register shift enable (SHIFTDR) and data register clock (CLOCKDR) inputs to preload test response and shift data from TDI to TDO. IEEE Std 1149.1 requires two data registers; boundary-scan register and bypass register.
The **boundary-scan register** (BSR) consists of a series of boundary-scan cells (BSCs) arranged to form a scan path around the boundary of the host IC. Shadow latches in the BSCs, driving the outputs, remain in their present state during a data register scan operation. At the end of a data register scan operation, the data register update (UPDATEDR) input updates the shadow latches with the new boundary test pattern to be applied from the outputs of the BSCs.
The **bypass register** consists of a single scan register bit. When selected, the bypass register provides a single-bit scan path between TDI and TDO. Thus, the bypass register allows abbreviating the scan path through devices that are not involved in the test.

4.1.4 JTAG Instructions

JTAG IEEE Std 11.49.1 defines nine test instructions:

BYPASS Instruction The BYPASS instruction allows the IC to remain in a functional mode and selects the bypass register to be connected between TDI and TDO. The BYPASS instruction allows serial data to be transferred through the IC from TDI to TDO without affecting the operation of the IC. The bit code of this instruction is defined as all ones.

SAMPLE/PRELOAD Instruction The SAMPLE/PRELOAD instruction allows the IC to remain in its functional mode and selects the boundary-scan register to be connected between TDI and TDO. During this instruction, the boundary-scan register can be accessed via a data scan operation, to take a sample of the functional data entering and leaving the IC. This instruction is also used to preload test data into the boundary-scan register before loading an EXTEST instruction.

EXTEST Instruction The EXTEST instruction places the IC into an external boundary-test mode and selects the boundary-scan register to be connected between TDI and TDO. During this instruction, the boundary-scan register is accessed to drive test data off-chip via the boundary outputs and receive test data off-chip via the boundary inputs. The bit code of this instruction is defined as all zeroes.

INTEST Instruction The INTEST instruction places the IC in an internal boundary-test mode and selects the boundary-scan register to be connected between TDI and TDO. During this instruction, the boundary-scan register is accessed to drive test data on-chip via the boundary inputs and receive test data on-chip via the boundary outputs.

RUNBIST Instruction The RUNBIST instruction places the IC in a self-test mode, enables a comprehensive self-test of the IC's core logic, and selects a user-specified data register to be connected between TDI and TDO. During this instruction, the boundary outputs are controlled so that they cannot interfere with neighbouring ICs during the RUNBIST operation. Also, the boundary inputs are controlled so that external signals cannot interfere with the RUNBIST operation.

CLAMP Instruction The CLAMP instruction sets the outputs of an IC to logic levels determined by the contents of the boundary-scan register and selects the bypass register to be connected between TDI and TDO. Before loading this instruction, the contents of the boundary-scan register can be preset with the SAMPLE/PRELOAD instruction. During this instruction,

data can be shifted through the bypass register from TDI to TDO without affecting the condition of the outputs.

HIGHZ Instruction The HIGHZ instruction sets all outputs of an IC to a high-impedance state and selects the bypass register to be connected between TDI and TDO. During this instruction, data can be shifted through the bypass register from TDI to TDO without affecting the condition of the IC outputs.

IDCODE Instruction The IDCODE instruction allows the IC to remain in its functional mode and selects the optional device identification register to be connected between TDI and TDO. The device identification register is a 32-bit shift register containing information regarding the IC manufacturer, device type, and version code. Accessing the device identification register does not interfere with the operation of the IC.

USERCODE Instruction The USERCODE instruction allows the IC to remain in its functional mode and selects the device identification register to be connected between TDI and TDO. During the USERCODE instuction, the optional 32-bit device identification register captures user-defined information about the IC. Accessing the device identification register does not interfere with the operation of the IC.

4.2 FPGA parallel programming via VME

4.2.1 ROD's FPGA programming

To define the behavior of the FPGA, the user has to provide a Hardware Description Language (**HDL**) or a schematic design. Then, using an electronic design automation tool, a technology-mapped netlist is generated. The netlist can then be fitted to the actual FPGA architecture using a process called place-and-route; the binary file generated is used to configure the FPGA. This file is transferred to the FPGA via JTAG or to an EEPROM, that is used to program the FPGA after booting.
In the ReadOut Driver each FPGA has a JTAG connector (J9, J18, J11 AND J12); however it can be useful to have a single JTAG chain with all the main FPGAs (Spartan 6 slave A, Spartan 6 slave B, Virtex 5 master). This can be arranged by programming the PRM with a special firmware; the PRM is directly connected with the other FPGAs and acts as a JTAG programmer. In this way only the PRM can be accessed from the front panel (Figure 4.5).

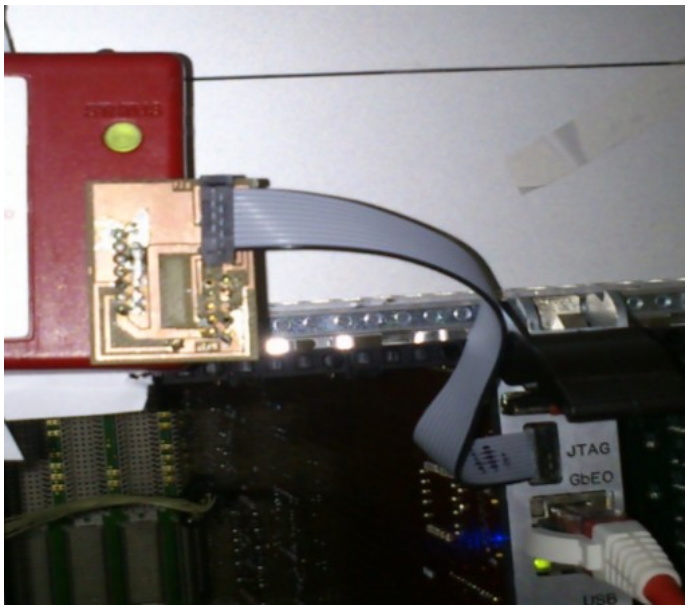


Figure 4.5: PRM JTAG connector as viewed from the front panel.

4.2.2 FPGA VME programming

There is an alternative way for programming the IBL ROD FPGAs: via VME. As already explained the PRM interfaces to the VME bus mastered by the Single Board Computer. The SBC loads in the VME bus STAPL or ACE files (standard for JTAG in-circuit programming of programmable logic devices); those files are received by the PRM that redirects them to the right FPGA.

For the IBL readout chain there are 15 ROD boards; each board has a PRM with his own VME address. In almost all cases all the master or slave FPGAs has to be programmed with the same firmware, so it is useful to program them concurrently. Therefore i added a **broadcast VME address** (0x25) that allows all the PRMs to read data from the bus at the same time. However the broadcast address can be used only for reading data and not for writing them, so a Bus Error (BERR) signal is sent if PRMs try to write in this address.
The program *Ace_Programmer_broadcast.cxx* running in the SBC open an existing ACE file and sends it few bytes a time to the PRMs that memorize them in FIFOs before sending them to the chosen FPGAs. During this process it is necessary to frequently check every FIFO state, so each PRM has to perform a writing operation in the VME bus. This slow up the process (writing operations can't be parallel) and for few FPGAs the serial program-

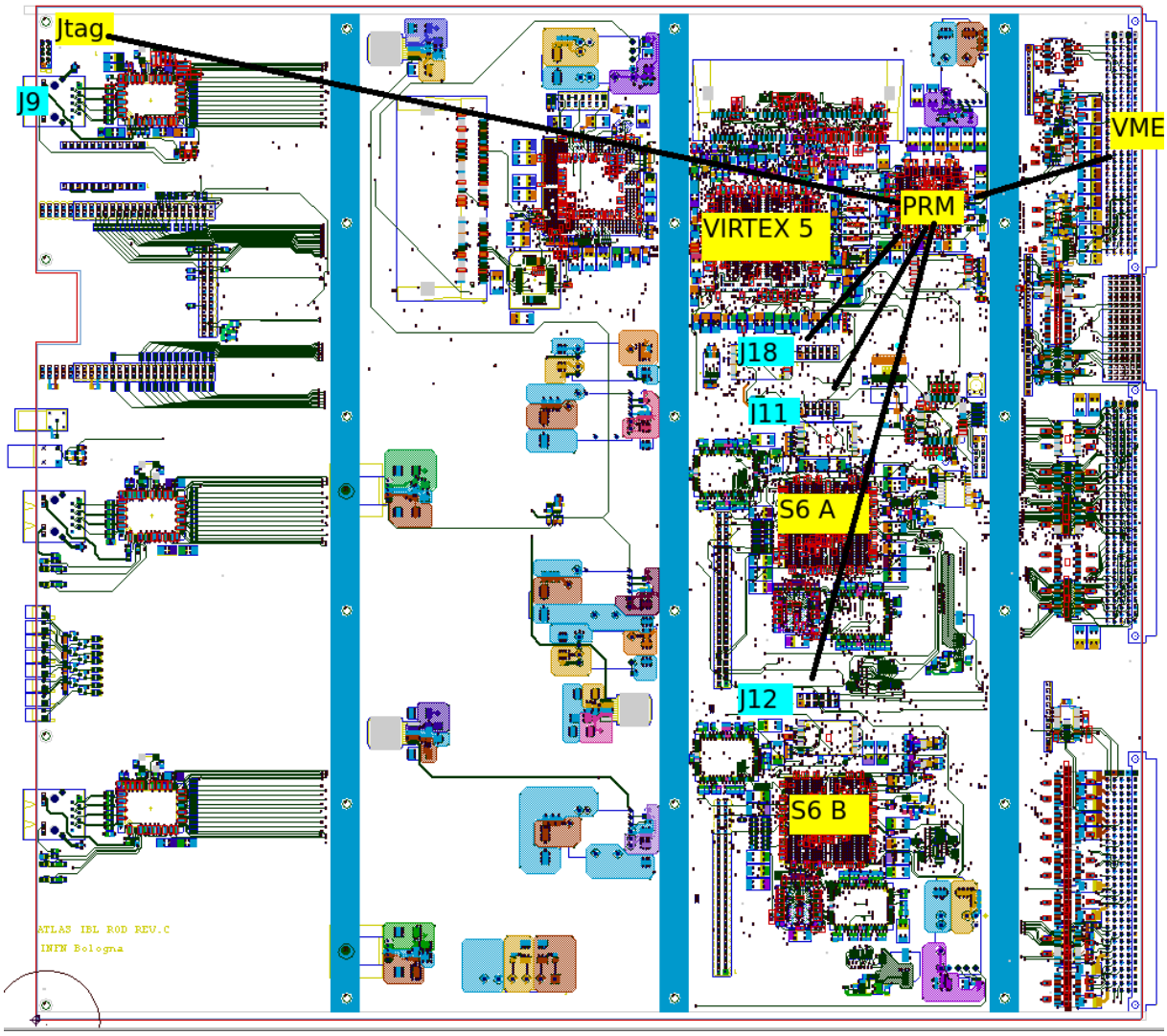


Figure 4.6: FPGA JTAG or VME programming.

ming is faster, but for many FPGAs the parallel programming time gain is remarkable, as shown in Figure 4.7.

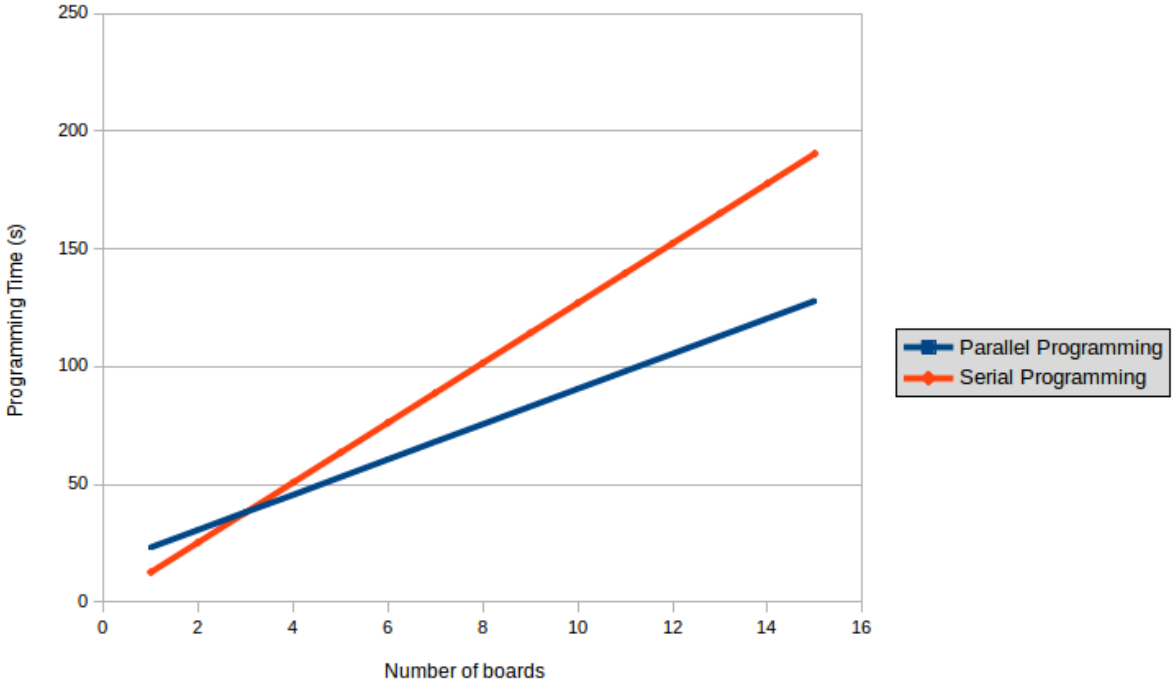


Figure 4.7: Parallel vs Serial programming time.

4.3 PLL resetting via VME

4.3.1 Clock distribution

The ROD board has two main sources of clock: an internal one, used when the board is in standalone mode, and an external one, coming from the BOC card via backplane. A Dip switch controls which of these clock sources drives the whole board. The Phase Locked Loop chip then multiplies and distributes the needed clock sources all over the board. Also the BOC can be configured to lock on the TIM clock, with this set-up all the clocks inside the crate are perfectly in phase. Once the ROD is inserted in the Crate the Dip switch is not visible so, in order to determine which clock source is used, I added a control signal accessible via VME, as explained in next sections.

4.3.2 PLL JTAG chain

The Lattice ispClock 5620 PLL has its own JTAG connector (J8); as with the FPGAs, the PRM can directly connect to the connector creating in this way a JTAG chain.

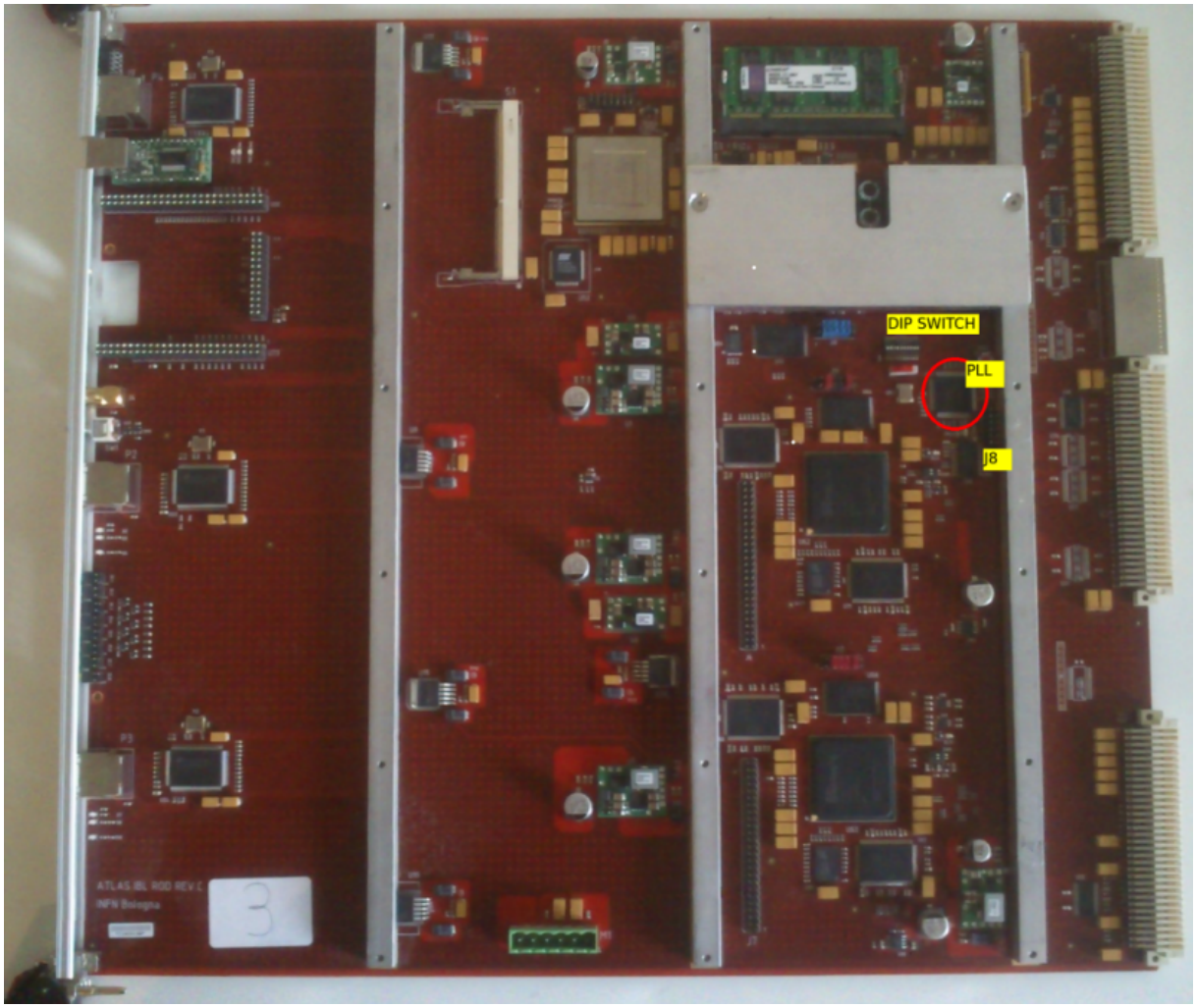


Figure 4.8: ROD board: PLL, JTAG connector J8 and the Dip switch.

Via JTAG it is possible to:

- check the clock source (internal or coming from BOC);
- reset the PLL.

The PRM's clock come from the PLL; when the PLL is reset the clock is no more distributed to the FPGAs so clocking the process that resets the

PLL with the PRM's clock would cause the PLL to froze in a reset state. An independent clock signal is therefore needed. Fortunately the Spartan 6 PRM FPGA has an internal 100 MHz oscillator (used during the booting process); the oscillator generates a clock signal that can be slowed down to 1 MHz and used as TCK; in this way the clock is no longer dependable on the PLL.

4.3.3 Checking the clock source

The sixth switch of the Dip switch controls the Lattice PLL's REFSEL input signal (Figure 4.9). When the signal is "1" the internal clock is used, when it is "0" the BOC clock is used.

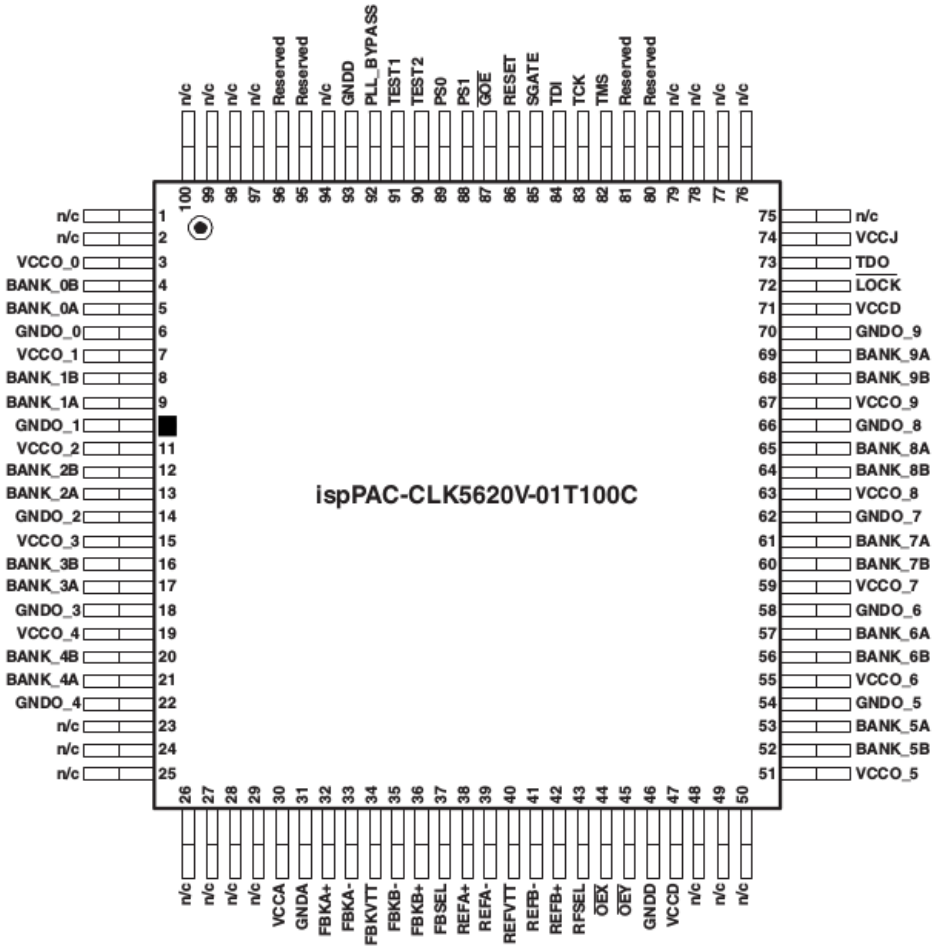


Figure 4.9: Lattice ispClock 5620 PLL pinout.

JTAG IEEE Std 11.49.1 provides an instruction to capture current state of pins to boundary scan register: the **SAMPLE-PRELOAD** instruction.

The procedure consists in the following steps:

1. the TMS signal drives the Test Access Port main state diagram (Figure 4.4) in the **SHIFT-IR** state;
2. while remaining in the SHIFT-IR state, the TDI signal select the **SAMPLE-PRELOAD** instruction (0001 1100) ;
3. the TMS signal drives the Test Access Port main state diagram in the **RUN-TEST/IDLE** state;
4. the TMS signal drives the Test Access Port main state diagram in the **SHIFT-DR** state;
5. while remaining in the SHIFT-DR state, the **TDO** signal, connected to the boundary scan register, sends back to PRM the state of pins captured by the SAMPLE-PRELOAD instruction (Figure 4.10). The state of the REFSEL pin is then memorized into a register.

The register that contains the value of the REFSEL pin can be accessed by the SBC via VME.

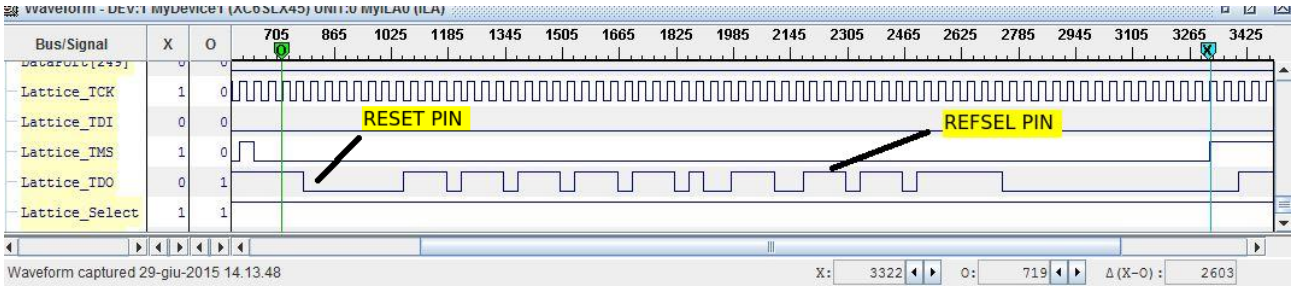


Figure 4.10: The TDO signal shows the state of LATTICE ispClock 5620 pins. In this example REFSEL = 1, so the local clock is used.

4.3.4 Resetting the PLL

Lattice ispClock 5620 can be reset sending an *"1"* signal to the RESET input pin (Figure 4.9). JTAG IEEE Std 11.49.1 allows the user to drive input pins with the contents of the boundary scan register with the **INTEST** instruction so the PRM can reset the PLL. The procedure consists in the following steps:

1. the TMS signal drives the Test Access Port main state diagram (Figure 4.4) in the **SHIFT-IR** state;

2. while remaining in the SHIFT-IR state, the TDI signal select the **IN-TEST** instruction (0010 1100) ;

3. the TMS signal drives the Test Access Port main state diagram in the **SHIFT-DR** state;

4. in SHIFT-DR the boundary scan register is set in order to have a "1" corresponding to the RESET PIN;

5. the TMS signal drives the Test Access Port main state diagram in the **RUN-TEST/IDLE** state where the INTEST instruction is actually executed;

6. after waiting 2 ms (minimum reset time) the **SAMPLE-PRELOAD** instruction is selected (with the procedure described above) in order to restore the normal functioning of the chip.

To start the reset procedure it is necessary to change the value of a PRM register; this can be done by the SBC via VME. Figure 5.1 shows an example of the PLL locking after resetting.

Figure 4.11: PLL locking after resetting.

Chapter 5

Future developments and conclusions

The 15 RODs for the staves of IBL have already been assembled and delivered to CERN and are currently participating in data acquisition. Each board can interface with 32 FEI4 chips, and data-taking and calibration work properly. The ROD firmware is done, but the entire software-firmware system debugging is ongoing so that the ROD code is continuously under development for fine tuning. Further spare boards have also been delivered to CERN and are undergoing system tests.
ROD boards are also going to be used for Pixel Layer 1 and 2.

In fact, the Pixel readout link of the actual detector will suffer from bandwidth limitations due to the luminosity increment of LHC. The link occupancy can be expressed as:

$$L_o = \frac{Throughput}{Bandwidth} \propto \sigma$$

where:

- L_o is the link occupancy;
- the **throughput** is the rate of data transfer *actually used*;
- the **bandwidth** is the maximum rate of data transfer;
- σ is the trigger rate of front-end devices.

So the link occupancy is directly proportional to the trigger rate and inversely proportional to the link bandwidth. With an average number of expected pile-up events $\langle\mu\rangle \approx 50$ (estimated by luminosity, energy and bunch spacing) and trigger rate of 100 kHz, the estimated average link occupancy for Layer 2

is about 90%. With greater pile-up even Layer 1 will get into trouble. High link occupancy brings to synchronization errors (Figure **??**) so it is necessary to reduce this value. The actions that could be taken are different in Layer

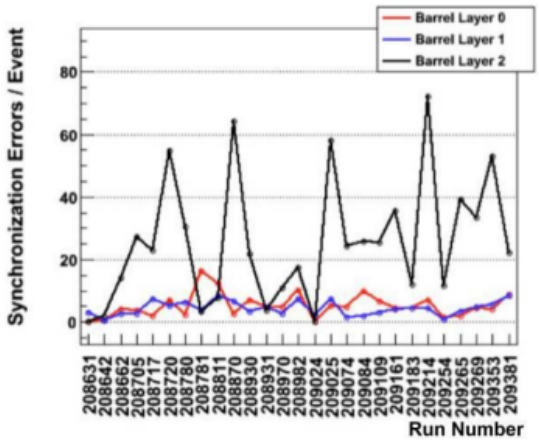


Figure 5.1: Synchronization errors in runs acquired before LHC's shut-down. The y-axis is the maximum number of modules that showed synchronization errors at a given event. As an example, a "Synchronization Error/Event" of 50 means that an inefficiency of 50 out of 1700 (the number of modules in Layer 2) occurred for few seconds. The excess shown by Layer 2 links with respect to the others is due to bandwidth limitation.

1 and Layer 2. Layer 2 is read-out with one link per module at 40 Mb/s. Increasing the bandwidth to 80 Mb/s is a viable solution; it would require producing more BOC opto-electrical plug-ins as well as more BOC-ROD pairs (to support double the bandwidth) and rearranging the link cabling. Since IBL off-detector electronics already manage BOC-ROD transmissions at 80 Mb/s it would be straightforward to adopt IBL cards. Only two minor modifications would be needed: a new firmware to interface the board with FEI3 chip and new custom RX optoelectrical BOC plug-ins.
Layer 1 is already able to manage read-out at 80 Mb/s; therefore, installing a second link per module can increase the bandwidth. As in the previous case, the adoption of IBL cards would require both new firmware and BOC plug-ins, with minor modifications of the connections.
The adoption of IBL ROD-BOC cards would bring also other benefits:

- it will provide a uniform board for most of the Pixel read-out system;
- it will provide common spares for all sub-detectors.

26 ROD will be needed for Layer 2 and 38 for Layer 1.

35 Layer 2 RODs (including spare boards) have already been produced with no modification to the board design and they are ready to be tested and delivered to CERN. The firmware is still under rework; time plan is to have it ready and to have the RODs running by the end of 2015.

ROD boards for Pixel Layer 1 will be produced by the end of 2015 and will be tested in 2015/2016.

Appendices

Appendix A

8b/10b encoding

In telecommunications, 8b/10b is a line code that maps 8-bit symbols to 10-bit symbols to achieve DC-balance and bounded disparity, and yet provide enough state changes to allow reasonable clock recovery. 8b/10b coding is DC-free, meaning that the long-term ratio of ones and zeros transmitted is exactly 50%. To achieve this, the difference between the number of ones transmitted and the number of zeros transmitted is always limited to ± 2, and at the end of each symbol, it is either $+1$ or -1. This difference is known as the running disparity (RD). The control symbols (shown in table A.1) within 8b/10b are 10b symbols that are valid sequences of bits (no more than six 1s or 0s) but do not have a corresponding 8b data byte.

	Input			RD = −1	RD = +1
	DEC	HEX	HGF EDCBA	abcdei fghj	abcdei fghj
K.28.0	28	1C	000 11100	001111 0100	110000 1011
K.28.1	60	3C	001 11100	001111 1001	110000 0110
K.28.2	92	5C	010 11100	001111 0101	110000 1010
K.28.3	124	7C	011 11100	001111 0011	110000 1100
K.28.4	156	9C	100 11100	001111 0010	110000 1101
K.28.5	188	BC	101 11100	001111 1010	110000 0101
K.28.6	220	DC	110 11100	001111 0110	110000 1001
K.28.7	252	FC	111 11100	001111 1000	110000 0111
K.23.7	247	F7	111 10111	111010 1000	000101 0111
K.27.7	251	FB	111 11011	110110 1000	001001 0111
K.29.7	253	FD	111 11101	101110 1000	010001 0111
K.30.7	254	FE	111 11110	011110 1000	100001 0111

Table A.1: 8b/10b K-words.

Appendix B

VME standard

VERSABUS Module Eurocard (VME) is a computer bus standard widely used for many applications and standardized by the IEC as ANSI/IEEE 1014-1987. It was first developed in 1981 and continues to be used today, so, during this time, it has seen a number of extensions and add-ons.
VME modules come in three sizes. 3U x160 mm cards have one backplane connector (J1) and have a 24-bit/16-bit address/data space. 6U x 160 mm cards are the most common ones and have two backplane connectors (J1 & J2) allowing for 32 bits of address/data space. Large 9U x 400 mm cards also have 32 address/data lines and 2 connectors (J1 & J2). Each connector is a 96-pin DIN 41612 (Figure B.1).

BUS Description

Address Lines The VME bus has 31 address lines. The first 23 lines are present on J1 and the remainder being on J2. The lowest address bit (A0) is implied by the transfer cycle and is not present on the backplane.

Data Lines The VME bus has 32 data lines. The low order 16 data lines are on J1, the high order 16 on J2. VME modules with only J1 can only do 16 bit wide transfers, while those with both J1 and J2 can do 32 bit wide transfers.

Bus Arbitration A VME Bus master requests the bus by asserting one of the bus request lines BR0*-BR3*. The slot 1 bus arbiter will grant the bus by asserting the corresponding bus grant signal (BG0OUT-BG3OUT). The arbiter can cyclically scan the BRn* lines (round robin arbitration), or

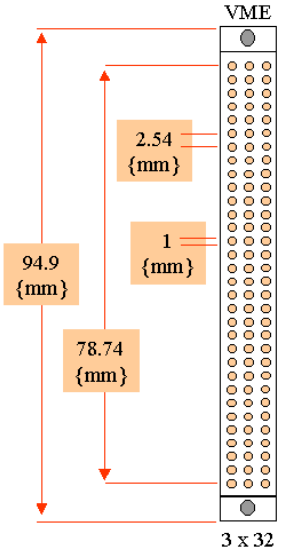


Figure B.1: DIN 41612 96-pin.

treat higher numbered BRn* lines as being a higher priority request (prioritized arbitration). The bus grant forms a daisy chain. Each module monitors BG0IN-BG3IN if it is not requesting the bus it reproduces these signals on BG0OUT-BG3OUTwhich are inputs to the next slot to the right on the backplane. If the module is requesting the bus on the corresponding BRn* it claims the bus by driving BBSY*.

Data Strobe Lines DS0* and DS1* are tri-state signals used in conjunction with LWORD* to indicate how many byte locations are being accessed (1, 2, 3, or 4). For byte transfers these signals imply bit zero of the address. During a write cycle, the falling edge of the first data strobe indicates that valid data is available on the data bus. For read cycles, the rising edge of the first data strobe indicates that data has been accepted from the Addressed slave.

Address Strobe Line The Address strobe Line (AS*) is driven low by a master to indicate it is driving a valid address.

Data Acknowledge Line DTACK* is an open-collector signal generated by slaves. The falling edge of this signal indicates that valid data is available on the data bus during a read cycle, or that the slave has accepted data

during a write cycle. The rising edge of DTACK indicates when the slave's data is no longer present at the end of a read cycle.

Interrupt Handling Any module on the VME bus may request an interrupt by driving one of the interrupt request lines IRQ1*-IRQ7*. Any bus master module can respond to any of the interrupt request lines by arbitrating for the bus, asserting IACK* and echoing the interrupt level on A1-A3. The bus arbiter places the IACKOUT* on an interrupt daisy chain (similar to the bus grant daisy chain). The interrupting module will then provide a status-id on the data bus that allow the interrupt handler to distinguish between interrupters sharing the same interrupt request level.

System Fail Line The SYSFAIL* line is an open-collector signal that indicates when a failure has occurred in the system. Any board in the system can generate this signal.

System Reset The SYSRESET requests that all bus modules perform power-up initialization.

Write Line WRITE* is a three-state signal generated by the master to indicate whether the data transfer cycle is a read or write. A high level indicates a read operation; a low level indicates a write operation.

Address Modifiers VME provides for large number of data transfer types. The VME Address modifier lines (AM0*-AM5*) are asserted by a bus master during an address cycle to indicate the type of data transfer requested. In Table B.1 all address modifiers are shown.

Long Word The LWORD* line is used in conjunction with DS0*, DS1*, to specify the width of a data transfer.

Serial Data The SERCLK and SERDAT lines implement a serial data bus. SERCLK provides a synchronization clock for the serial data that can be transferred on SERDAT.

Bus Busy and Bus Clear The master that has been granted the bus assert BBSY* to indicate the bus is in use. In priority arbitration, the bus arbiter can assert BCLR* if a bus request at a higher priority than the currently granted master is present. The current bus master is then expected

AM	Address	Description
0x3F	24	A24 supervisory block transfer (BLT)
0x3E	24	A24 supervisory program access
0x3D	24	A24 supervisory data access
0x3C	24	A24 supervisory 64-bit block transfer (MBLT)
0x3B	24	A24 non-privileged block transfer (BLT)
0x3A	24	A24 non-privileged program access
0x39	24	A24 non-privileged data access
0x38	24	A24 non-privileged 64-bit block transfer, MBLT
0x37	40	A40BLT [MD32 data transfer only]
0x35	40	A40 lock command (LCK)
0x34	40	A40 access
0x32	24	A24 lock command (LCK)
0x2F	24	CR / CSR space
0x2D	16	A16 supervisory access
0x2C	16	A16 lock command (LCK)
0x29	16	A16 non-privileged access
0x21	32/64	2eVME for 3U bus modules
0x20	32/64	2eVME for 6U bus modules
0x0F	32	A32 supervisory block transfer (BLT)
0x0E	32	A32 supervisory program access
0x0D	32	A32 supervisory data access
0x0C	32	A32 supervisory 64-bit block transfer (MBLT)
0x0B	32	A32 non-privileged block transfer (BLT)
0x0A	32	A32 non-privileged program access
0x09	32	A32 non-privileged data access
0x08	32	A32 non-privileged 64-bit block transfer MBLT
0x05	32	A32 lock command (LCK)
0x04	64	A64 lock command (LCK
0x03	64	A64 block transfer (BLT)
0x01	64	A64 single access transfer
0x00	64	A64 64-bit block transfer (MBLT)

Table B.1: List of address modifiers

to release the bus when convenient by releasing BBSY, to allow the new arbitration cycle to complete.

AC FAIL The ACFAIL line is driven low when there is an AC failure for the VME power supply.

Bus Errors The bus arbiter often implements address timeout logic and asserted BERR* if no module responds to an address cycle within the time-out. Slaves may also assert BERR* if they are not able to honor a requested cycle (e.g. they do not support the requested address modifier).

Timing

Address Cycle During an address cycle (Figure B.2), a VME bus master holds IACK high and places the address and AM [0-5] codes on the bus. Once the lines have been valid for at least 35ns the Master drives the Address Strobe [AS*] indicating a valid address is on the bus. For interrupt acknowledge cycles the IACK line is driven low, the interrupt priority is encoded on A1-A3 and the AM lines are ignored.

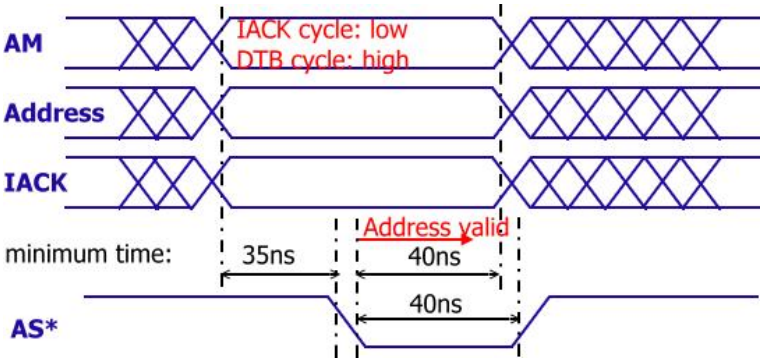


Figure B.2: VME Address Cycle

Data Cycle VME Data cycles (Figure B.3) can be writes (Master to Slave) or reads (Slave to Master). Regardless of the cycle type, the Master uses LWORD*, DS0* and DS1*to indicate the width of the transfer. At least one of DS0*, DS1* will be driven. For a write cycle, DS0* and DS1* also indicate that the Master has stable data on the data bus for the slave. In a read cycle, DS0* and DS1* indicate the master is ready to receive data from the slave. In a write cycle, DTACK* is asserted by the slave when it has accepted the

data transfer. In a read cycle DTACK* indicates the slave has stable data on the bus for the master. Regardless of the cycle type, the release of both DS0* and DS1*, and subsequent release of DTACK* by the slave indicates completion of the cycle.

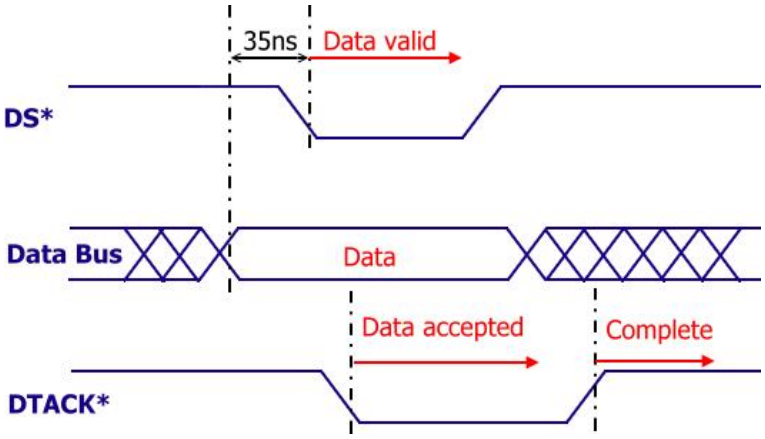


Figure B.3: VME Data Cycle

Data Transfer Data transfer (Figure B.4) requires an address and a data cycle. Address cycles may overlap the previous data cycle.

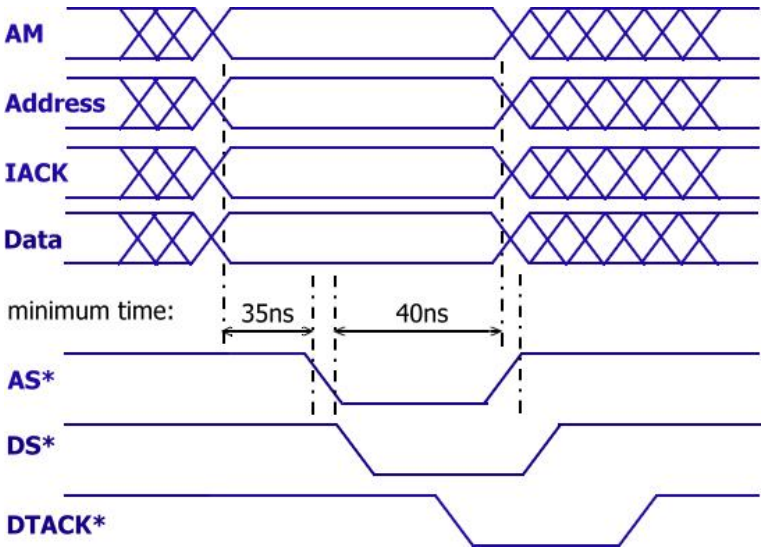


Figure B.4: VME Data Transfer

Block Transfer A VME bus BLock Transfer (Figure B.5) consists of a single Address cycle followed by up to 256 bytes of Data transfer before another address cycle is required. VME64 adds the Multiplexed Block Transfer. MBLT transfer data on both the address and data lines to achieve a 64 bit transfer width.

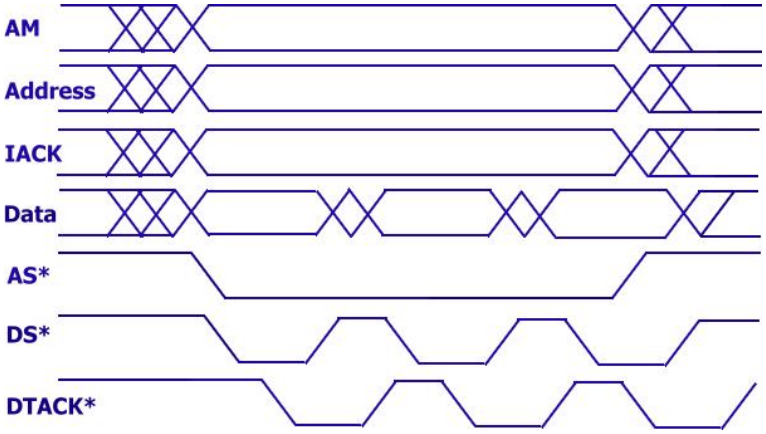


Figure B.5: VME Block Transfer

Bus Request The master requesting the bus (Figure B.6) does so by driving a Bus Request (BR) line low. The VME bus arbiter hands control of the bus to a master by asserting the corresponding BG line.

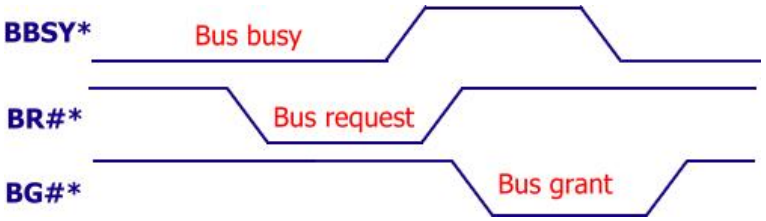


Figure B.6: VME Bus Request

Appendix C

FPGA

A field-programmable gate array (FPGA) is an integrated circuit designed to be configured by a customer or a designer after manufacturing. The FPGA configuration is generally specified using a hardware description language (HDL), similar to that used for an application-specific integrated circuit (ASIC).

FPGAs contain an array of programmable logic blocks, and a hierarchy of reconfigurable interconnects that allow the blocks to be "wired together", like many logic gates that can be inter-wired in different configurations. Logic blocks can be configured to perform complex combinational functions, or merely simple logic gates like AND and XOR. In most FPGAs, logic blocks also include memory elements, which may be simple flip-flops or more complete blocks of memory. An FPGA has three main elements, Look-Up Tables (**LUT**), **flip-flops**, and the **routing matrix**, that all work together to create a very flexible device.

Look-Up Tables Look-Up Tables (LUTs) are how your logic actually gets implemented. A LUT consits of some number of inputs and one output. What makes a LUT powerful is that you can program what the output should be for every single possible input.

A LUT consists of a block of RAM that is indexed by the LUT's inputs. The output of the LUT is whatever value is in the indexed location in it's RAM.

Flip-flops Each LUT's output can be optionally connected to a flip-flop. Groups of LUTs and flip-flops are called slices. These flip-flops are typically configurable allowing the type of reset (asynchronous vs synchronous) and the reset level (high vs low) to be specified. Some of the flip-flops can actually

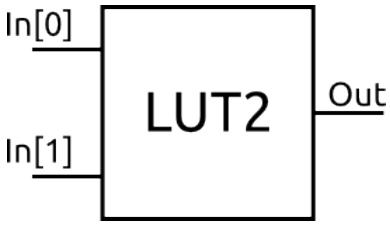


Figure C.1: 2-input LUT.

be configured as latches instead of flip-flops, although latches typically aren't good practice to use as they can lead to timing problems.

The Routing Matrix The next size block in the FPGA is the **Complex Logic Block (CLB)** and each CLB consists of two slices. Each CLB connects to a switch matrix that is responsible for connecting the CLB to the rest of the FPGA. The switch matrix can connect the inputs and outputs of the CLB to the general routing matrix or to each other. That way the output from one LUT can feed into the input of another LUT without having the travel far.

The routing resources in an FPGA are essentially a bunch of multiplexers and wires that are used to define what CLBs and other FPGA resources are connected to each other. These connections are again defined in RAM which is why the FPGA must be reconfigured every time the power is cycled.

There are also special routing sorceress available on the FPGA. The most notable are the clock routing resources. These are basically wires that connect through the entire chip (for global) or sections of the chip (for local) with very little propagation delay. Only inputs from certain pins on the FPGA are allowed to drive a signal on the global clock routing resources.

Appendix D

Programs utilized

ISE

Xilinx ISE (Integrated Synthesis Environment) is a software tool produced by Xilinx for synthesis and analysis of HDL designs, enabling the developer to synthesize (”compile”) their designs, perform timing analysis, examine RTL diagrams, simulate a design’s reaction to different stimuli, and configure the target device with the programmer. The Xilinx ISE (Figure D.1) is primarily used for circuit synthesis and design, while the ModelSim logic simulator is used for system-level testing.

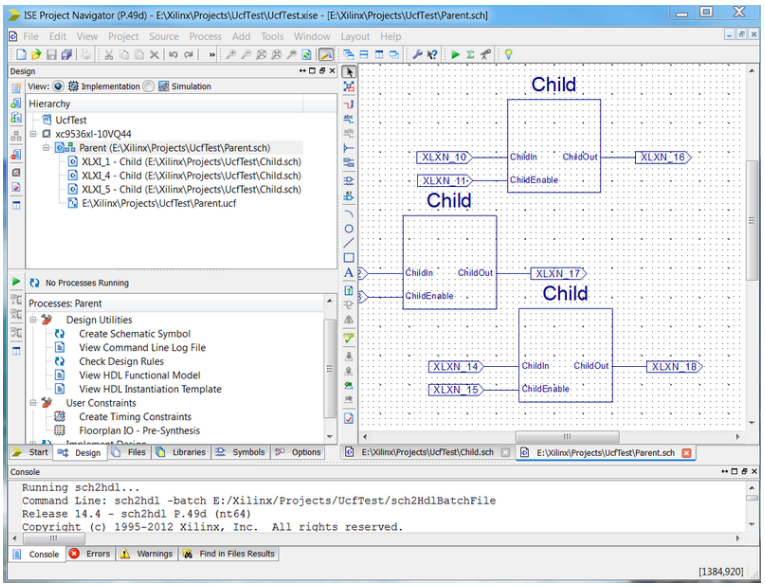


Figure D.1: Xilinx ISE IDE.

EDK

The Embedded Development Kit (EDK) is an integrated development environment for designing embedded processing systems. It Provides:

- **Xilinx Platform Studio (XPS) Tool Suite**: Graphical IDE and command line support for developing hardware platforms for embedded applications;
- **Software Development Kit (SDK) for MicroBlaze and PowerPC**;
- **Real-Time Operating System and Embedded OS Support**: provides design support and board support package (BSP) generation for numerous third party suppliers in the Xilinx ecosystem;
- **Processing IP and MicroBlaze Soft Processor Core**: pre-verified IP catalog, including a wide variety of processing peripheral cores for customizing your embedded systems.

ChipScope

ChipScope tool inserts logic analyser, system analyser, and virtual I/O low-profile software cores directly into your design, allowing you to view any internal signal or node, including embedded hard or soft processors. Signals are captured in the system at the speed of operation and brought out through the programming interface, freeing up pins for your design. Captured signals are then displayed and analysed using the ChipScope Pro Analyser tool (Figure D.2).

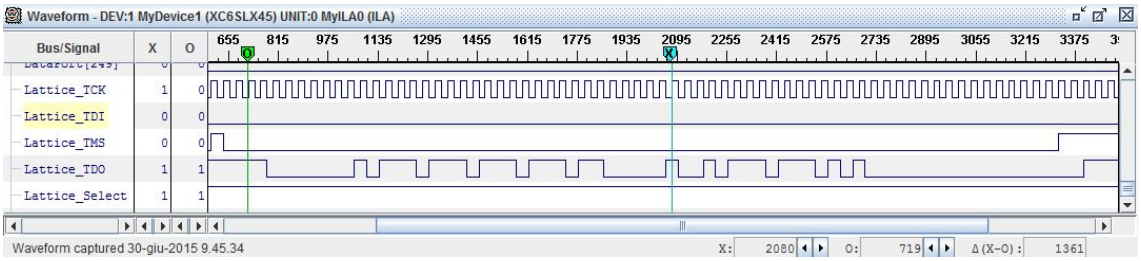


Figure D.2: ChipScope Pro Analyser Tool.

iMPACT

Xilinx iMPACT (Figure D.3) allows the user to download, read back and verify design configuration data as well as to create PROM, SVF, STAPL, System ACE CF and System ACE MPM programming files.

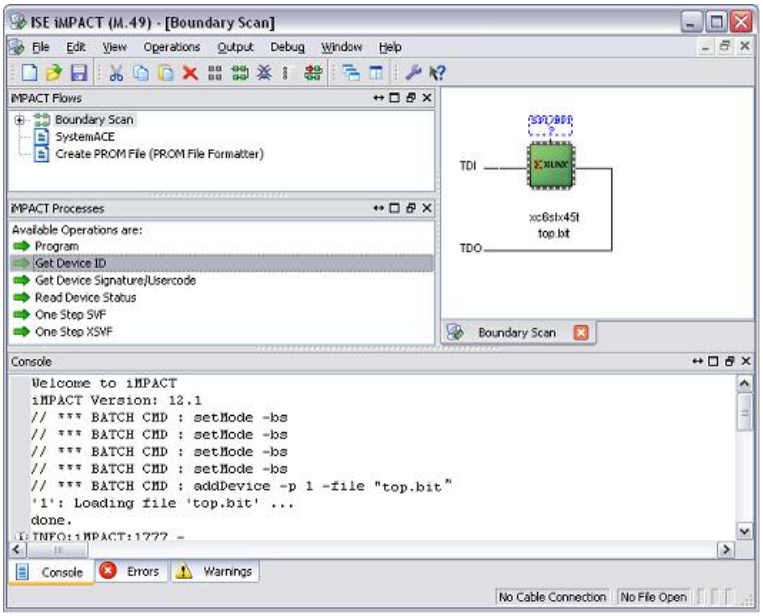


Figure D.3: iMPACT IDE.

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