ALMA MATER STUDIORUM · UNIVERSITÀ DI BOLOGNA

Scuola di Scienze
Corso di Laurea Magistrale in Fisica

Implementation of a VLSI amplifier interfaced with biomedical sensors for Ultra Wide Band data transmission

Relatore:
Prof.Alessandro Gabrielli

Correlatore:
Dott.Ing. Marco Crepaldi

Presentata da:
Gabriele D'amen

Sessione II
Anno Accademico 2013/2014

Sommario

Questa tesi presenta un Amplificatore CMOS con alta Reiezione di Modo Comune progettato in tecnologia UMC 130nm. Lo scopo è quello di ottenere un alto fattore di amplificazione per un ampio range di segnali biologici (con frequenze nella finestra di 10Hz-1kHz) e di rigettare il segnale di rumore di modo comune. Viene presentato un Sistema di Acquisizione Dati, composto da un Modulatore di tipo Sigma-Delta e da un'antenna, fulcro di un sistema radio portatile a bassa complessità; l'amplificatore è progettato in modo da interfacciare il sistema di acquisizione dati con un sensore che acquisisce il segnale elettrico. Il modulatore acquisisce in maniera asincrona e campiona l'attività muscolare umana, inviando un pattern Quasi-Digitale che codifica il segnale acquisito. Utilizzando questo pattern per tradurre l'attività muscolare vi è solo una minima perdita d'informazione se comparata ad una tecnica di codifica che utilizza segnali digitali standard via Impulse-Radio Ultra Wide Band (IR-UWB). I segnali biologici, necessari per analisi Elettromiografiche, hanno un'ampiezza di 10-100μV e necessitano di essere grandemente amplificati e separati dal sovrastante rumore di modo comune di 50mV. Vengono presentati vari test di robustezza del progetto, nonché la prova che il design funziona anche con differenti sensori, come un sensore di radiazione per studi di Dosimetria.

Abstract

This thesis presents a CMOS Amplifier with High Common Mode rejection designed in UMC 130nm technology. The goal is to achieve a high amplification factor for a wide range of biological signals (with frequencies in the range of 10Hz-1KHz) and to reject the common-mode noise signal. It is here presented a Data Acquisition System, composed of a Delta-Sigma-like Modulator and an antenna, that is the core of a portable low-complexity radio system; the amplifier is designed in order to interface the data acquisition system with a sensor that acquires the electrical signal. The Modulator asynchronously acquires and samples human muscle activity, by sending a Quasi-Digital pattern that encodes the acquired signal. There is only a minor loss of information translating the muscle activity using this pattern, compared to an encoding technique which uses a standard digital signals via Impulse-Radio Ultra-Wide Band (IR-UWB). The biological signals, needed for Electromyographic analysis, have an amplitude of 10-100μ*V and need to be highly amplified and separated from the overwhelming 50mV common mode noise signal. Various tests of the firmness of the concept are presented, as well the proof that the design works even with different sensors, such as Radiation measurement for Dosimetry studies.*

Contents

List of Figures

Chapter 1

Introduction

1.1 INFN-IIT Collaboration milestones

Over the last years, the Department of Physics of University of Bologna, along with other international partners, has developed a series of microcircuits to read out signals originated from different types of sensors, and to transmit the information via wireless digital protocols.

In particular, a first research has started in the 2008 by the design and fabrication of a radiation monitor, with an embedded microelectronic sensor, via a strong collaboration with the *Rutherford Appleton Laboratory*, UK, who has financed the project. The initial idea was to fabricate a possible commercial device capable to transmit the absorbed dose of radiation, in a specific point of a (human) body, through an in-vivo implantable device. After that some prototypes were tested in the *Electronics Laboratory of INFN* in Bologna, and continuously modified and tuned with some studies carried out in the electronic group of the Physics Department of the University of Bologna. Then, the interests of the research moved to transmission protocols even more shifted over a high-frequency carrier of the order of some GHz.

It is in this context that this thesis has started. I have personally revisited all the previous microelectronic circuits, from the schematic view to the final layout in a form that was ready to be submitted to the silicon foundry, and studied the conversion of every individual block designed in a first technology node into a different technology. Eventually I designed from scratch a differential amplifier for instrumentation, by paying particular attention to the common mode noise rejection. In more detail, I have scaled part of the entire circuit that was initially designed using the *TowerJazz Silicon Foundry*, CMOS process at 180nm, towards the *UMC* 130nm CMOS process.

In addition, by designing a pre-amplifier for instrumentation, the entire circuit now is capable to directly interface with sensors, whose output voltage is very low, of the order of a few hundreds of μV. This small range of amplitude is what is expected from sensors measuring biological signals: an electrocardiogram, for example, might be created starting from this type of voltages.

Hence, a modified version of the prototypes studied and fabricated over the last years might be applied to measure biosignals for electrocardiograms, electromyograms, electroencephalograms etc. Moreover, if the sensor is read out via a digital circuit able to digitally codify the information, to apply a sensor mark and to transmit the full payload information within a digital packet, many sensors might work in parallel. In this way one unique digital receiver will be able to reconstruct information originated from different positions of the same body. The design and test of a common receiver is the work currently ongoing within the same collaboration group of people that has led the research up to the point which is described in this thesis, and this makes the near future activity and expectations of this research in Bologna.

1.2 Types of signals

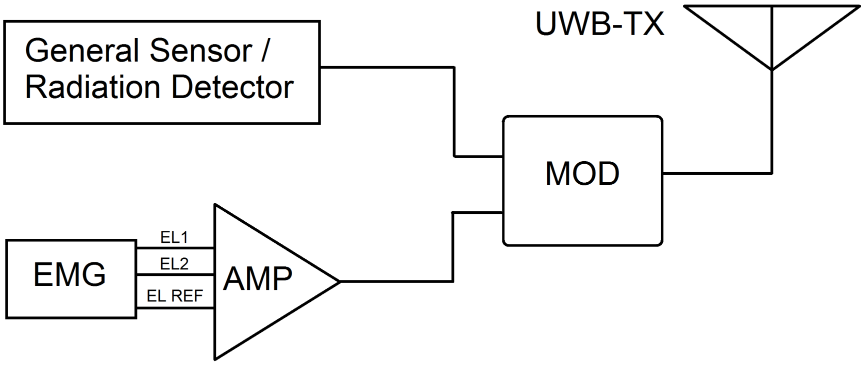


Figure 1.1: Main scheme of the proposed data acquisition system; the modulator described in chapter 3 works indifferently for various types of sensors and acquired data. While a generig sensor (such as the radiation sensor) with high signal amplitude should be directily interfaced with the modulator and readied for transmission, a low amplitude signal needs to be amplified, as described in chapter 4.

The data acquisition system (DAQ) presented in chapter 3 is not focused of studying of particular signals, but allows to obtain data from a wide variety of sensors with different amplitudes and frequencies. The opportunities of study have been addressed so far in implementing this method on biological (*Electromyography*) and environmental (Radiation dose) parameters, allowing a precise analysis of many different signals with an universal device.

Figure 1.1 show a theoretical diagram of the proposed DAQ; the signal modulator (described in chapter 3) could be adapted to different types of sensors (and therefore different signals) via front end electronics which adapts the studied signal parameters (amplitudes and frequencies) to the operational regime of our system.

It is possible to note that we need to split out study in two different types of signals:

- signals whose amplitude order of magnitude is widely different ($\sim 10 - 100 \mu V$) with respect to electronics range. These, must be amplified and processed via a pre-amplifier (as described in chapter 4), like EMG measurements;
- signals whose amplitude order of magnitude is about $\sim 1V$ (same order of electronics), like Radiation Dose measurements;

1.2.1 EMG

The first signal we want to study falls into the category of human biological signals, produced by specific actions executed by human body. The[1] importance of this analysis is the possibility to obtain precise information of important physiological parameters observing the features and the evolution of these signals.

In order to easily access at muscular and neural parameters of an human being one should study the electric signals produced by the voluntary contraction of the muscular fibers: this technique is known as *Electromyography* (from now *EMG*). Every time one needs to accomplish a function, create force, produce movement, an electric signal is created and it travels into muscular tissues in order to transmit the required information and achieve the designed job.

This electric signal is very low, about 10-100μV and frequencies between 10-1000 Hz and is hardly recognized on his carrier of amplitude 50mV and frequency 50Hz. As described in chapter 4 we need to create a pre-amplifier able to independently reject the overwhelming noise and collect our EMG information.

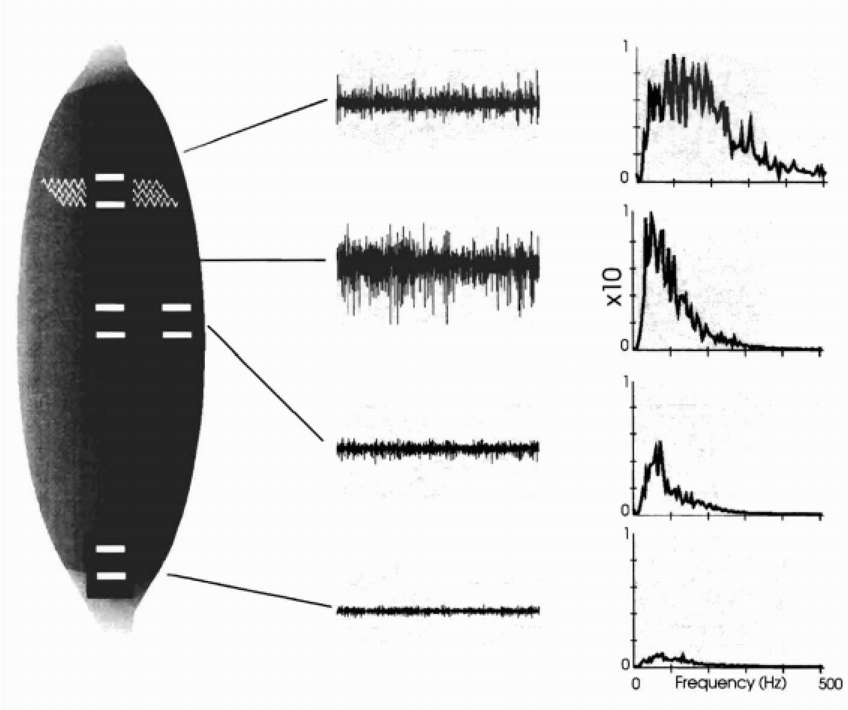


Figure 1.2: The amplitude and frequency spectrum of the EMG signal is affected by the electrode location. It's important to focus in zones of greater strain which leads to higher signals[2].

The signal is therefore highly specific and must bring many informations about the task to obtain and the medium (the specific muscle) that had to produce it.

A damaged nerve will not transmit the correct information, as a damaged muscle will not perform the requested act or it will perform it with minor to greater distortion. Studying the electrical signal detected into a muscle surface (or into the tissue, in some cases) leads to the possibility of evaluate these "errors" and treat the disease in a specific context.[3] It's therefore interesting to consider the interrelated factors underlying the relationship between the EMG signal and the force produced by a muscle: greater muscular contraction leads to higher signals and, as may be seen in fig.1.2, it is possible to focus the measure on specific zones of the tissue in order to increase the signal an so the reliability of the signal; placing three differential surface electrodes on the ventral region of the forearm over the *"flexor digitorum superficialis"*, *"palmaris longus"*, and *"flexor carpi ulnaris"* muscles (as explained in section 2.3.2) it is possible to achieve reliable signals.

1.2.2 Radiation detector

As previously introduced, we should[4] execute measurements directly coupling a sensor (both commercial or custom) and the modulator if the signal parameters fit into voltage range of our electronics. A first prototype design of the device implemented a radiation detector and was designed for specific in-vivo dosimetry applications.

The chip embeds a re-programmable floating-gate transistor configured as a radiation sensor and a read-out circuit; prototype chips have been fabricated and tested exploiting a commercial 180 nm, four-metal CMOS technology (*Towerjazz technology*).

The dosimeter prototype shows the following features:

- estimated sensitivity of 1 mV/rad;
- total absorbed dose range up to 10 krad;
- very low total power consumption (about 165 μW);
- powered with 3.3 V;

.

Verification of the dose delivered to patients is an essential tool for controlling radiotherapy treatments; adding up the possibility of acquiring EMG signals, the idea was to create a portable full check-up chip.

It has been decided to use a floating gate based dosimeter, realized including also a dedicated read-out chain. The proposed read-out circuit is designed to asynchronously trigger an Ultra-Wide Band (UWB) transmitter with a repetition frequency dependent on the dosimeter output voltage level. The carrier frequency of the transmitter was chosen according to biomedical application constraints, where the frequency of *403 MHz* offers the least attenuation of radio waves to human body, mostly composed of water. The specifications of the integrated antenna were defined mainly for testing purposes, resulting in the realization of a small area device ($< 1mm^2$), since frequencies of hundreds of MHz would require much larger antennas. The chip was fabricated by extending the principles of other designs, constructions and measurements performed on similar circuits recently tested at the *Istituto Italiano di Tecnologia, Center for Space Human Robotics in Turin, Italy.*

It is possible, as will be explained, of using a floating gate based sensor in dosimeter and will be show preliminary characterization tests and transmitted power measurements versus distance, as a validation of the feasibility of such a low-power wireless transmission circuit.

The floating-gate based sensor

In MOSFET-based dosimeters the amount of accumulated dose is indirectly measured via the shift of the threshold voltage. In particular, the threshold voltage depends on the trapped charge within the SiO_2 oxide interposed between the control gate and the bulk.

Usually, MOS transistors need to be integrated on the same technology of the readout electronics. Conversely, floating gate devices, commonly used for static memories, can be fabricated using a standard CMOS technology, featuring double polysilicon layers, which is compatible with monolithic fabrication processes of the readout electronics; the floating-gate is initially pre-charged by the injection of electrons–holes, via a tunnelling process.

Then, the charge trapped in the SiO_2 interface by the ionizing radiation discharges the floating-gate preloaded charge and causes a backshift of the MOS's threshold voltage.

The sensor device proposed here consists of a single NMOS transistor. The radiation sensor was characterized via irradiation tests performed providing, at each step, an equivalent dose of *100 rad.* The sensor, which is a floating-gate based MOS transistor, was reprogrammed each time after the charge was removed from the gate; in this way the process was repeated up to an equivalent total irradiation dose of *10 krad.* Within this range, a maximum sensitivity of *1* mV/rad was estimated.

Chapter 2

Signal Sampling

The main goals we proposed to achieve in designing a sampling and transmitting portable device are both the capability of obtaining a signal faithful to the original, that is a signal that maintains the most important and meaningful features of the studied event, and at the same time the possibility to achieve energetic efficient processing and transmission, without "wasting" power in useless tasks. In order to achieve this result it has been used the *Impulse-Radio Ultra Wide Band* technology (explained in section 2.1) that allows a duty cycle at the transmitter of $\sim 0.1\%$ at 1Mbps data rate.

To test the likelihood of implementing this method it has been created a test circuit that allows to evaluate, using commercial components, pros and cons of this kind of the approach.

2.1 Impulse-Radio Ultra-Wide-Band transmission

We use an IR-UWB event-driven transmission, in which information is encoded in digital trigger events delayed with continuous power resolution; the transmission nature is then maintained analog-based but in pulse-based form, which permit orders of magnitude lower energy consumption at the transmitters compared to standard wireless systems.

2.1.1 IR-UWB Basic concept

Impulse radio communication systems and impulse radars both utilize very short pulses in transmission that results in an ultra-wideband spectrum[5]. For radio applications, this communication method is also classified as a pulse modulation technique because the data modulation is introduced by pulse position modulation (PPM).

The UWB signal is *noise-like*, and due to the low-power spectral density, UWB signals cause very little interference with existing narrow-band radio systems. UWB has a number of advantages that make it attractive for consumer communications applications. In particular, UWB systems:

- have potentially low complexity and low cost;
- have noise-like signal;
- have very good time domain resolution allowing for location and tracking applications.

The low complexity and low cost of UWB systems arises from the essentially baseband nature of the signal transmission. Unlike conventional radio systems, the UWB transmitter produces a very short time domain pulse, which is able to propagate without the need for an additional RF (radio frequency) mixing stage. The RF mixing stage takes a baseband signal and "injects" a carrier frequency or translates the signal to a frequency which has desirable propagation characteristics.

2.2 Wireless transmission test circuit

The circuit we intend to test is schematically introduced in fig.2.1: the EMG signal is acquired using two differential electrodes (every signal common to both electrodes is automatically removed) EL_1, EL_2 with an additional electrode EL_{REF} useful to compensate the common mode by connecting it to a muscle-less zone of the human body, such as the elbow.

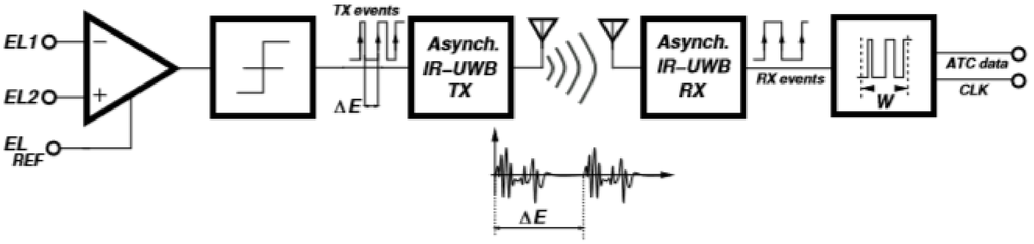


Figure 2.1: Block scheme of the proposed single-channel ATC wireless system.

It's possible to notice that the entire design is divided in two main parts, or nodes, physically and conceptually disconnected: a *Transmitter* (TX) and a *Receiver* (RX). A commercial amplifier for instrumentation (**INA114**) interfaces the transmitter node and the human body, amplifying the EMG signal and generating the 1-bit ATC signal (later explained) that triggers the asynchronous IR-UBW transmitter. An UWB pulse is generated as an ATC positive-edge occurs. At the receiver node, the ATC signal is instantaneously rectified with the asynchronous IR-UWB receiver (which should occupy an area small as $0.21mm^2$), and redirected through an interface module to a laptop or another electronic device for signal processing and real-time force plot.

The test has been conducted in three main steps:

- the creation of the test circuit using discrete components that let us evaluate the feasibility of the hypothesis; (section 2.3)
- the evolution of the first concept in order to simultaneously evaluate multiple different EMG signals; (section 2.4)
- the design of an integrated component (in 180nm CMOS technology) that tests the compatibility of the requested functions with CMOS technology qualities and limitations. (section 2.5)

2.3 Single channel Transmitter (TX) architecture

2.3.1 Average Threshold Crossing (ATC) sampling

In order to significantly[6] reduce power consumption, data are not transmitted in digital form (*i.e.* as a pulse train that encodes numeric data following a binary logic) but in *quasi-digital form*, that is transmitting information as delay between two consecutive digital pulses; this approach significantly reduces the number of processed pulses and therefore the required power.

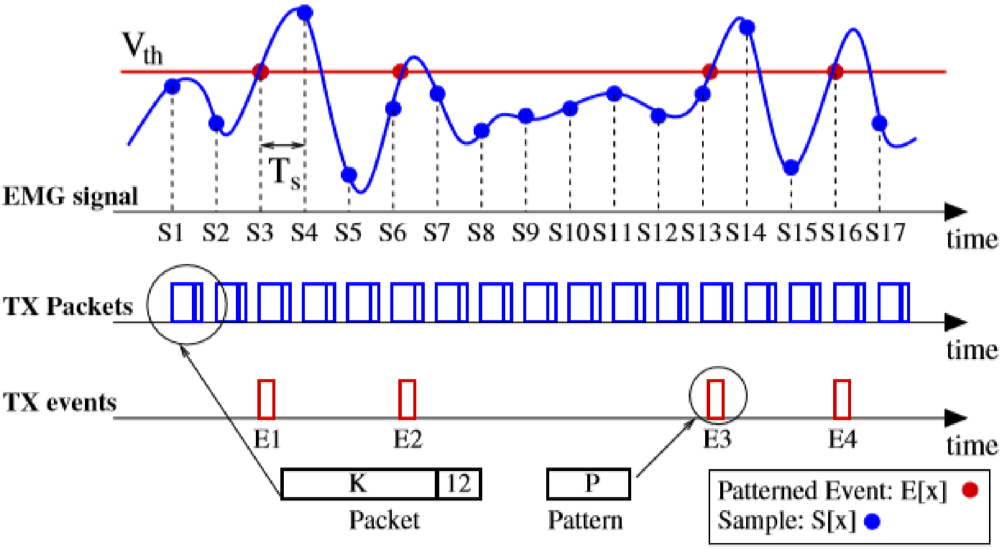


Figure 2.2: An example of ATC sampling: the EMG signal (upper) is continuously compared with a threshold potential (V_{Th}). One should clearly see the difference in term of generated pulses between standard logic (Blue pattern) and ATC (event-driven) logic (Red pattern). The number of threshold crossing is proportional to the applied force.

ATC features

The creation of a "pattern" of signals that encodes the acquired EMG follows the **Average Threshold Crossing** (**ATC**) logic, that is the creation of a logic bit whenever the sampled signal exceed a threshold value V_{th} (see fig.2.2): this *event-driven* method lead to the creation of asynchronous positive-edge signals which pattern is univocally correlated to the original input.

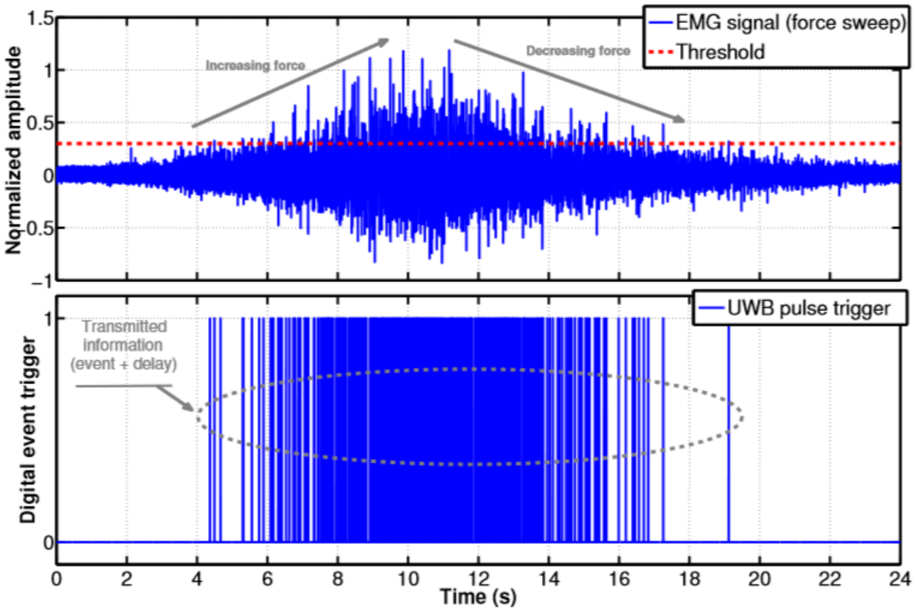


Figure 2.3: Input signal and corresponding ATC generated trigger pattern. The pulse sequence should be read by the RX with a simple sliding windowing.

ATC system bring obvious advantages both in terms of active silicon area and consumed power for wireless transmission: compared to a standard solution comprising *Analog-to-Digital Conversion* (*ADC*) the transmitter area is scaled by a factor:

$$\frac{A_{withATC}}{A_{withADC}} = \frac{A_{EMG} + A_{Th} + A_{TX}}{A_{EMG} + A_{ADC} + A_{Logic} + A_{TX}} \tag{2.1}$$

where the A_i are the active silicon are occupied by:

- A_{EMG}: *EMG amplifier*
- A_{ADC}: *Analog-to-Digital Converter*
- A_{Logic}: *packet generation logic*
- A_{TX}: *IR-UWB transmitter*
- A_{Th}: *asynchronous threshold detector*

In comparison, the ratio between the ATC consumed power and the standard wireless transmission the consumed power is:

$$\frac{P_{ATC}}{P_{Digital}} = \frac{30}{(960 + 60K)} \tag{2.2}$$

assuming a sampling rate of 2kbps, EMG data of 16 bit and K bit packet overhead and considering an energy consumption for IR-UWB transmission of $30\frac{pJ}{pulse}$.

These considerations are actually correct in single-channel electronic systems: out goal is to obtain a multi-channel electronic system which handles multiple inputs. Following these observations we can appreciate the fact that, while increasing the number of channels K a standard system comprising ADC for signal digitizing imply an increase in ADC area, in EMG conditioning circuits and a subsequent increase in the transmitter logic, even in the case of ATC besides multiple EMG inputs plus multiple threshold comparators, the digital logic which coordinates the transmission and the reception of multiple channels is still very small area, and achieves low-power consumption.

Test board ATC pattern generator

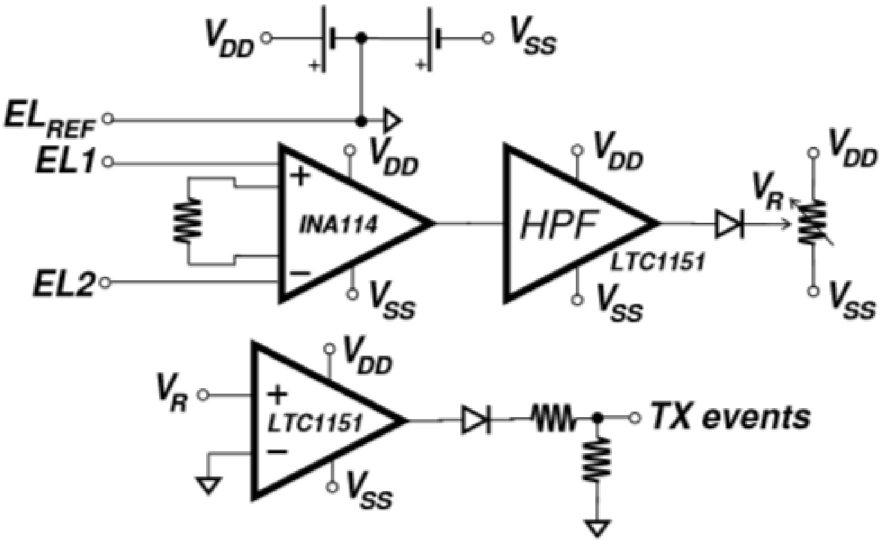


Figure 2.4: Scheme of the ATC signal generator.

To generate the ATC pattern it has been created the circuit shown in the block diagram in fig.2.4 (including EMG signal conditioning).

- Microelectrodes arrays EL_1 and EL_2 acquire electrical signals from the muscle tissues. They are connected to an *INA114* precision instrumentation amplifier, with high *Common Mode Rejection Ratio* (*CMRR*) and dual supply ±9V.
- The ground reference electrode EL_{REF} is connected to the human body, near the tissue we want to test.
- An active *High-Pass Filter* (*HPF*) removes low-frequency components; later the signal ranging between $0V - V_{dd}$ is compared to threshold V_{th}.
- A single commercial device (*LTC1151*), including two general purpose operational amplifiers, implements both the active filter and the voltage comparator.
- A *level shifter*, formed by a voltage divider, changes the voltage level for the components that needs more than ±5V of supply.

Test board additional features

The TX board mounts linear voltage regulators, logic buffers and dedicated trimmers to adjust UWB center frequency and pulse duration. The antenna area is less than $1mm^2$ (3.1-8 GHz) and directly connected to the TX Radio Frequencies output; it has been also used at the RX board and connected to the Radio Frequencies input through a 1nF DC-block capacitor.

In evaluating the signal sampling with ATC, only the positive crossing of the threshold (*i.e.* from under to above the threshold voltage) are considered and triggers the TX; therefore the digital RX output has half switching activity compared to ATC, hence information now is signal toggles. The RX compute the intensity of muscle force by counting ATC pulses on the received transition events by an *Arduino Microcontroller*; the data processed in this way are then transferred to a PC via USB link.

2.3.2 ATC transmission test

Designed the test circuit, the firmness of this approach has to be tested using real EMG data: the sample group is composed by eight healthy male subjects (31.8± 2.2 years). It has been asked to the sample group to hand a dynamometer and to smoothly push up from 0% to 70% of their *Maximum*

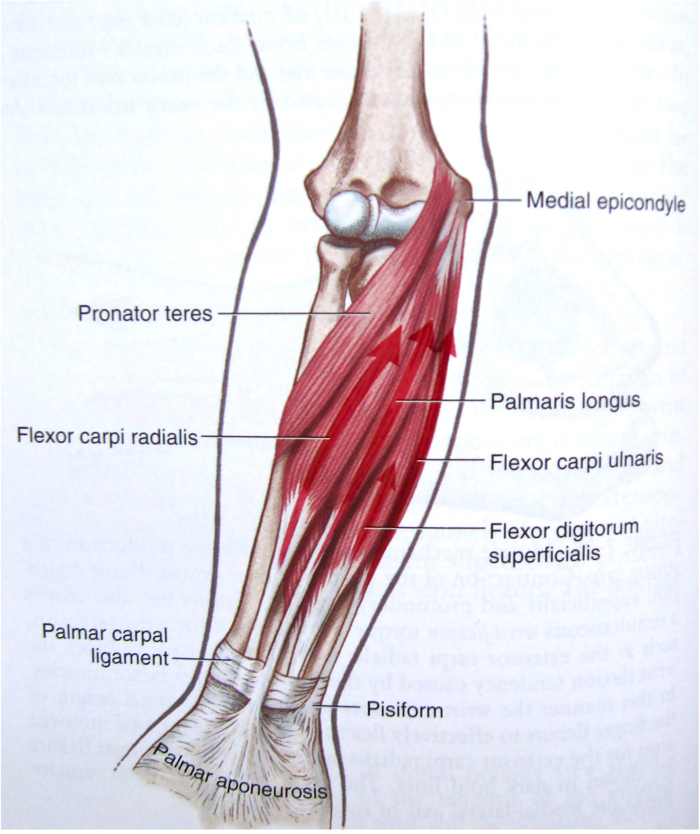


Figure 2.5: Position of the *"flexor digitorum superficialis"*, of the *"palmaris longus"* and of the *"flexor digitorum superficialis"* (on the right); the EMG signals have been acquired by differential electrodes from these muscles.

Voluntary Contraction (*MVC*) and back to 0% using a cylindrical power grip.

The Maximum Voluntary Contraction is a parameter determined placing three differential electrodes on the ventral region of the forearm over the *"flexor digitorum superficialis"*, *"palmaris longus"*, and *"flexor carpi ulnaris"* muscles (fig.2.5) and acquiring data during a sustained (1 second) maximum contraction of the muscles; the MVC is mean value of this signal during this period. and 1000kS EMG signals are acquired using a Biometrics DataLINK device.

For each signal the *Average Rectified Value* (*ARV*)[1] and the Average Threshold Crossing values are computed on a sliding window W lasting 500 ms and is evaluated the correlation to the force signal acquired by the dynamometer. The mean value of the overall rectified signal is used as ATC threshold V_{Th}. The results reported in fig.2.7 show that:

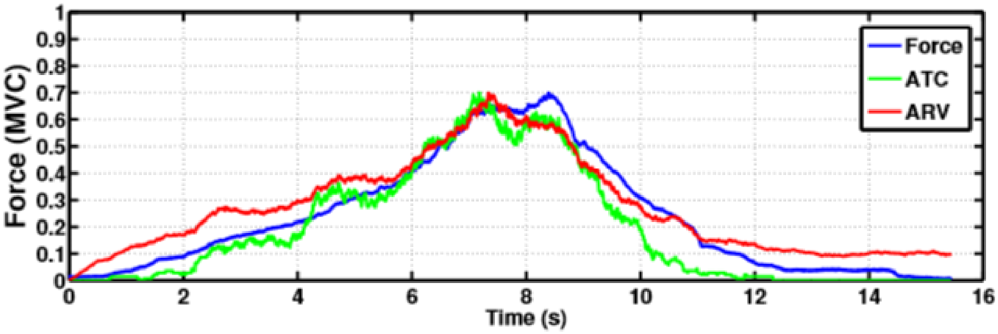


Figure 2.6: Plot of instantaneous force (Blue), its Average Rectified Value (Red) and the Average Threshold Crossing for comparison (Green)[7].

- The average correlation level between the ATC signal and the force signal is 0.95±0.02;
- The correlation level between the ARV and the force signal is 0.97±0.02;
- the correlation is relatively lower for the low-force part of the signals (for the signals below 70%/3 = 23%MVC) and higher otherwise;

the last result in unexpected, if we take account of the relatively low Signal Noise Ratio[2] and the nature of the EMG signals. Although correlation of

---

[1] The Average Rectified Value is the average of the absolute value

[2] At low signals the noise become predominant over the signal. This parameter is expressed in terms of Signal-Noise Ratio $SNR = \frac{Signal}{Noise}$

ATC to force is slightly lower than for ARV, the results show no significant difference. This data suggest that ATC could be used as a reliable estimation of force.

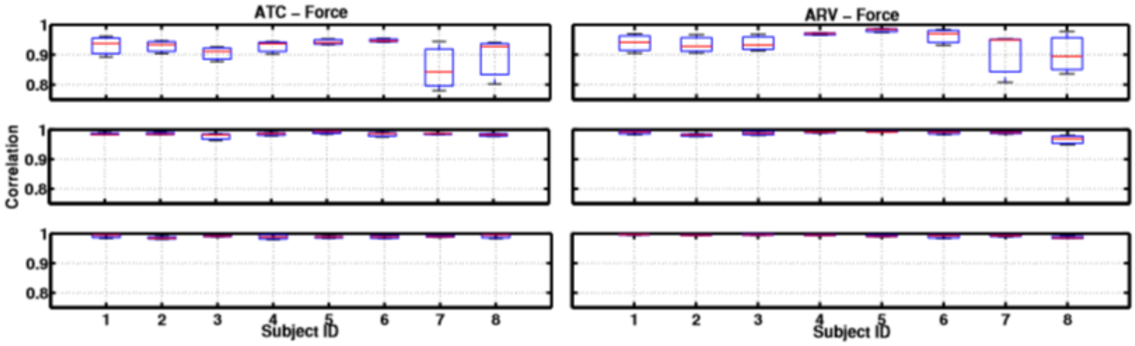


Figure 2.7: Correlation between force measured by dynamometer and ATC/ARV. The graphics are parted in eight segment each for the eight sample subjects. The low force component is on the top and shows a worse correlation; in the medium force (middle) and high force (bottom) components the correlation is strongly near 100%. The signals are plotted in order to account for the largest and smallest observations on maximum and minimum quartile.

The TX radiated power is very low (-72 dBm at 100Hz Pulse Repetition Frequency, PRF), and the RX typically reaches sensitivity of -102.6 dBm at 100Hz PRF (average power).

2.4 Multichannel TX architecture

Having tested[8] the reliability of ATC signal robustness and the functionality of our design, we want to extend our analysis on multiple EMG inputs, in order to account the fact that Electromyographic studies should require the simultaneous examination of the activity of different muscles. The chosen approach is based on the transmission of a single pattern [3] every time in which the corresponding EMG signal overcomes the threshold. In order to achieve this result we obviously need to implement:

- *Multiple EMG input channels front ends*, that simultaneously acquires data from different parts of the subject body;

---

[3] as previously stated in sec.1.2.1, the shape on an EMG signal is unique and function of both the involved muscle and the accomplished action

- An *Event Arbiter*, which manage the data stream of the inputs serializing the events;
- An *Event Encoder*, that forms data packets identifying the input channel;
- A *Modulator*, that acts as connection between Encoder and Transmitter, driving the latest with burst of trigger events.
- An *IR-UWB Transmitter*

The system architecture is presented in fig.2.8: the input stage (*EMG Frontend*) is followed by a digital core (*Event Arbiter, Event Encoder, S-OOK Modulator*) in common for every input. The fact that the proposed system is totally asynchronous and event-based, as well common for every input in the majority, greatly minimize complexity, power consumption and area occupation (digital core and transmitter should be implemented on the same CMOS integrated circuit).

For proposed medical applications we need to implement 10 channels for the analysis of as much tissues, transmitting $\simeq 66.7$ kevents/s per channel for a total of $\simeq 667$ kevents/s. Since the sensed information is encoded as the average threshold crossing (ATC) over time, we can just consider the positive edges as the events which trigger the communication of a tag identifying the source channel. Their timing still hold the information, whereas the content

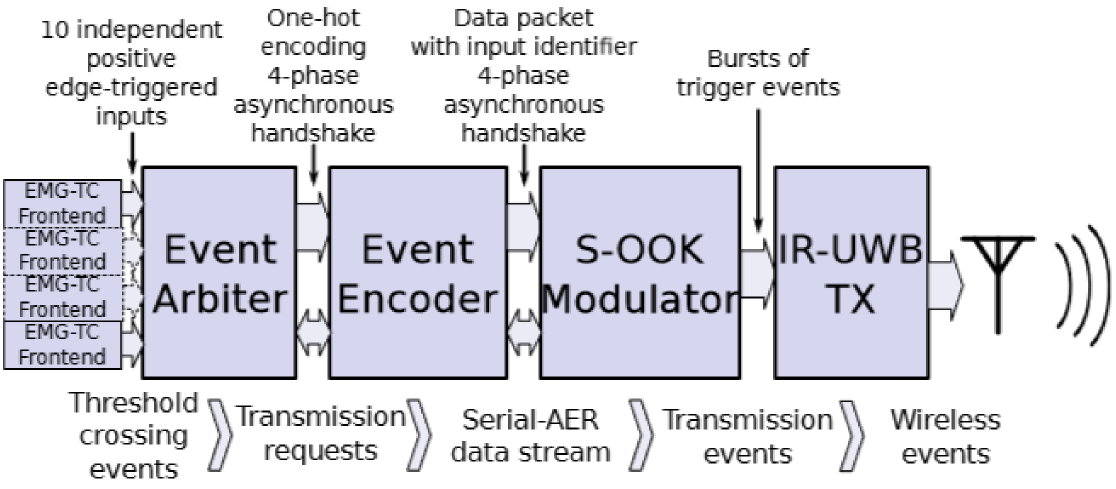


Figure 2.8: The block diagram of the proposed multichannel transmission system.

of each sent data packet allows to distinguish events coming from different sources (*Address-Event Representation, AER*).

Unlike other wireless address-event solutions, we should take advantage of the robustness of the ATC respect to information (*i.e.*, events) loss to further simplify the system by not including an IR-UWB receiver to listen for a "wireless acknowledge" signal. This has the major advantage of minimizing the system complexity, the power consumption, and channel occupancy required for the transmission of the single data packet, despite the difficulty of guaranteeing the event reception.

2.4.1 Event Arbiter

As we have seen we need a device that should "order" the incoming data from different inputs: the arbiter (fig.2.9) manages the data streams serializing the events and sending transmission requests to the following stage (the Encoder).

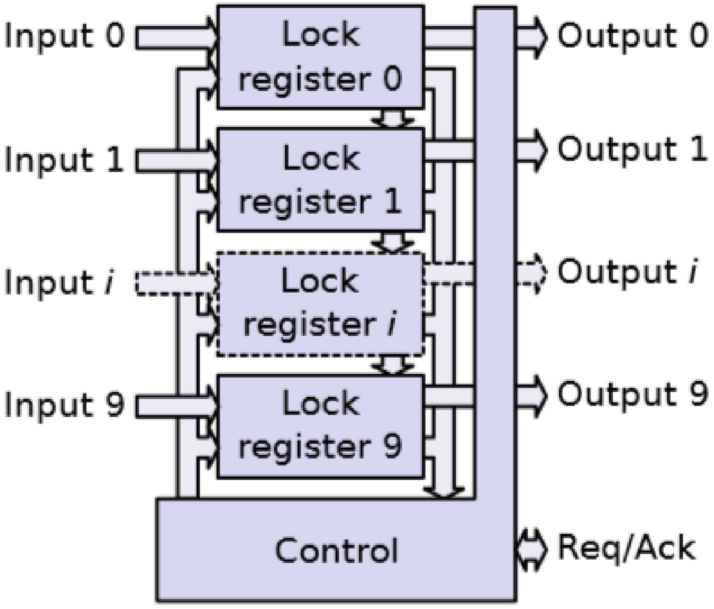


Figure 2.9: Conceptual design of the event arbiter in multichannel (10 inputs) transmission.

The arbiter waits for incoming input and then, if the system is idle, starts a new transmission cycle. In fig.2.9 the proposed event arbiter is depicted a set of lock units (with a daisy-chain topology[4]) implemented as concurrent processes waiting for the inputs and setting the corresponding outputs, while a control process monitors their state and handles the handshake protocol with the following stage.

Since all the input channels are assumed independent of each other and there is no constraint on their timing statistics, a coincidence of multiple events can occur. Moreover the arbiter has to account for events arriving during an already initiated transmission too. The first issue is addressed by giving priorities to the input channels; the second one by simply ignoring (discarding) input events during an ongoing transmission. No event delay occurs, although an event could be thrown away (in case of overlapping transmission requests). In section 2.6 will be show that the ATC signal is barely affected by small loss of events.

2.4.2 Event Encoder

Once a transmission is requested, the event identifier, made of a data packet including both the input channel identifier and the chip address (externally configurable), has to be sent serially to the modulator. This is the role of the encoder, activated by the arbiter and cycling through the binary tag. Each transmitted tag (top of fig.2.10) is divided into:

- *Fixed Header* (4bits)
- *Chip Address* (5bits, externally configurable)
- *Spacer* (1bit)
- *Input Source Address* (5bits)

This schema has been designed to allow the deploy of a wireless sensor network with multiple transmitters (each one connected to multiple sensing transducers) and one receiver collecting all the data. Given that no IR-UWB receiver has been implemented as a part of this solution (none "wireless acknowledge" signal is sent), only forward error correction approaches are allowed.

The implemented error detection code is the *constant-weight code*, which poses a constraint on the validity of a word of **n** bits by limiting the amount of ones to be at most **m**, hence termed *m-out-of-n* code. Fixed m, at most:

$$x = \binom{a}{b} \tag{2.3}$$

---

[4] Units are said to be in Daisy Chain Topology if they are connected in series

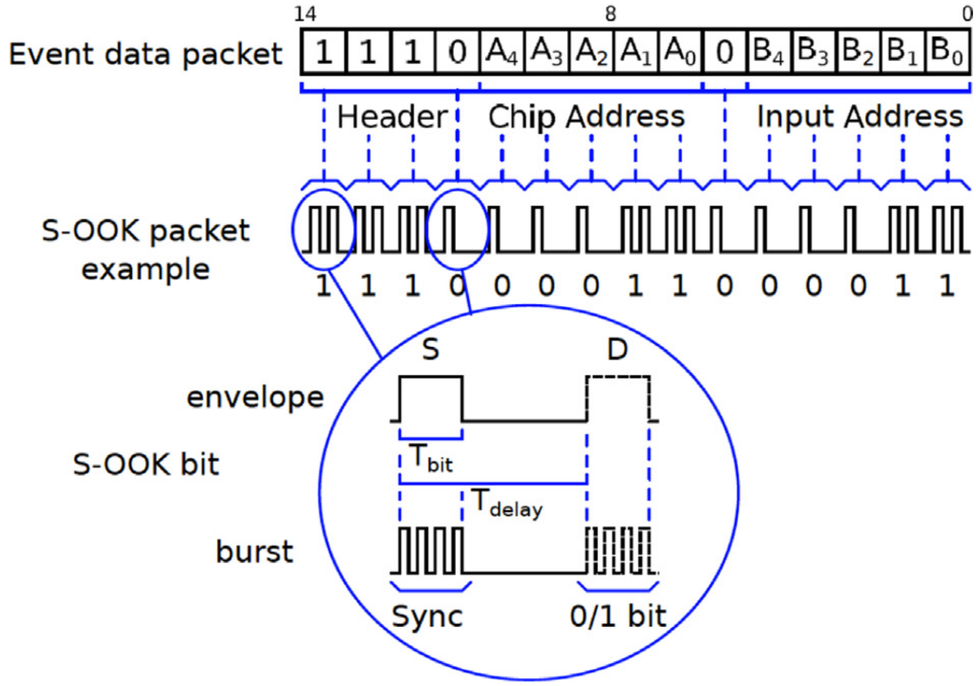


Figure 2.10: Wireless AER protocol detail: **top**) bit template; **bottom**) SOOK modulation

codewords can be encoded within a word of n bits. Looking for the smallest word size to hold ten identifiers:

$$arg\ min_{m,n}\ x = \binom{n}{m}, x \geq 10 \tag{2.4}$$

suitable parameters are $\mathbf{n} = \mathbf{5}$ and $m \in \{2, 3\}$, both resulting in $\mathbf{x} = \mathbf{10}$. The same schema has been adopted both to distinguish different inputs to the same chip and between different chips (respectively $B_4 ... B_0$ and $A_4 ... A_0$ in fig.2.10). An advantage of using constant-weight code with $\mathbf{m} = \mathbf{2}$ (at most two ones in the identifier) is that we can add a packet header with just three ones, being sure not to be confused with an enclosed identifier.

For the same reason we added a zero as spacer between the chip and source identifier. Following this schema, the data packet is a template where the encoded data is inserted and the validity of the whole tag can be easily checked by the receiver.

2.4.3 S-OOK Modulator

The fourth stage of the system is the S-OOK modulator: it accepts the request from the encoder and drives the IR-UWB transmitter with bursts of trigger events. The implemented modulation (bottom of fig.2.10) is perhaps the simplest one: *Synchronized On/Off Keying (S-OOK)*:

S-OOK Protocol

The S-OOK modulation is devoted to "translate" bit transmission requests into transmission trigger events for the following UWB transmitter. Standard OOK maps each 1 into an "*impulse trigger*", and each 0 into a "*space*" that is a delay. S-OOK adds a synchronizing impulse "S" before the data bit "D"(fig.2.10), thus allowing the receiver to know whenever a data bit is being effectively transmitted and hence not requiring to recover any timing information regarding the data stream.

Despite using a synchronizing impulse, this solution allows to design a fully asynchronous event-based receiver, more robust with respect to undesired delays due to the transmission channel. In more detail, any digital series of 0s and 1s, i.e. the modulation sequence of bits, enables or disables the high-frequency oscillator. Hence, the effective transmitted bits were formed by a series of bursts centered at a carrier frequency. Figure 2.10 shows a sequence of 15 bits, each of which composed of a set, or envelop, of high-

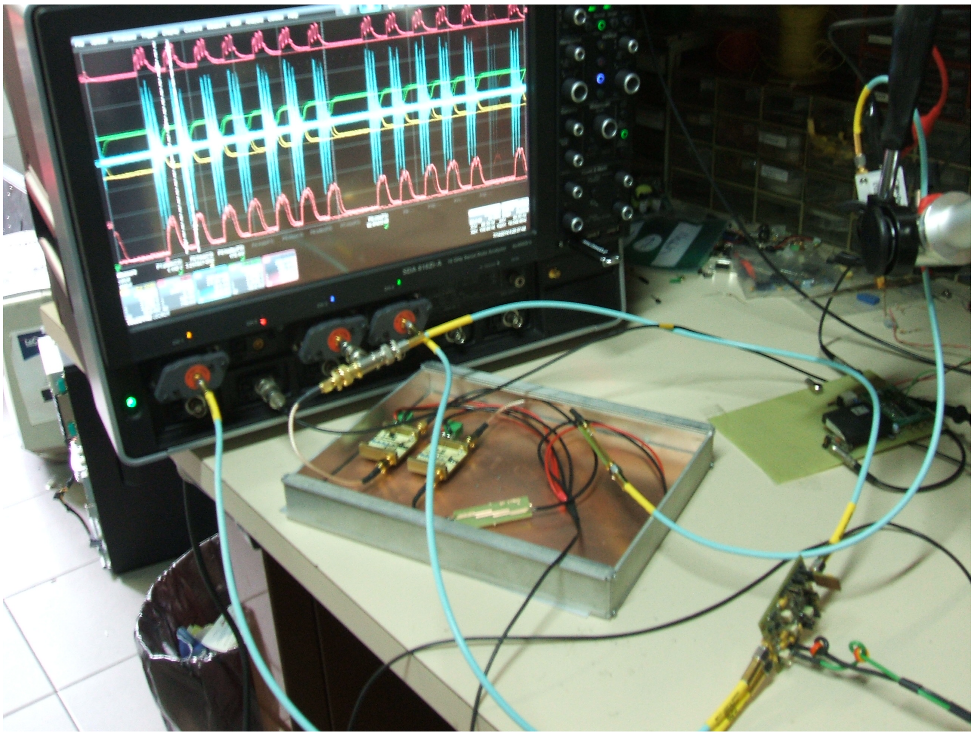


Figure 2.11: Detected burst into the receiver with S-OOK modulation.

frequency pulses that include a header and an address code. In this example the S-OOK modulation carries the information to transmit, via the packet frequency: the higher the 15-bit packet repetition time, the lower the original analog signal level.

A variation of the input signal of the sensor causes a variation on the frequency of the 15-bit packets. The address and coding bits are meant to a multi channel parallel transmission. Eventually, the T-bit and T-delay in the fig.2.10 can be adjusted depending on the signal input bandwidth. By following this approach any information can be transmitted, consuming very low power from the transmitter side.

Modulator implementation

In order to physically implement the modulator four monostable are integrated, two for the synchronizing S impulse and two for the data D one, pairwise configurable externally, the first two with T_{bit} (timespan of each impulse) ranging from 16ns to 64ns (with 16ns steps), and the last two with T_{delay} (interval between the rising edge of two impulses) ranging from 50ns to 200ns (with 50ns steps). This flexibility is required to exploit transmission optimizations, either allowing a communication speedup or helping to avoid undesired effects due to the wireless channel (e.g., multipath effects).

The time $T_{TX,1bit}$ required to transmit a single data bit (from the rising edge of the request signal to the release of the acknowledge signal) is $T_{TX,1bit} = 2xT_{delay}$. Further, each "transmission impulse" is actually a burst of triggers events sent to the IR-UWB, so that the transmitted signal is more robust. The burst generator is derived from a gated ring oscillator circuit, with a fixed period of 8ns (duty cycle 50%); considering the allowed T_{bit} values, a single burst can include between 2 and 8 impulses (with increments of 2).

2.4.4 IR-UWB Transmitter

The last stage of the system is the transmitter; major requirements are low power consumption, low complexity and ease of integration (on the same chip) within the whole system. Given that a data packet is transmitted only whenever an input event occurs, the system can be regarded as a low data rate one, and a natural fit in these cases are IR-UWB. Moreover, recent advances have shown that all-digital IR-UWB transmitters are feasible, thus making their adoption very attractive, considering the area occupation, flexibility (also in terms of scalability with respect to the technology node), and robustness.

The enclosed IR-UWB used has a wide frequency range (0.3-4.4GHz), low power consumption (32pJ/pulse at 4GHz) and area occupation ($0.004mm^2$), and its all-digital design suited for S-OOK modulation. The digital core has been designed with a 130nm RFCMOS technology *one-poly-eight-metal (1P8M)* top metal 20K with high speed (HS) core transistors, and nominal supply voltage of 1.2V; area occupation is $0.0045mm^2$. Simulations show that power consumption (digital core and IR-UWB) is $\simeq$ 0.5mW.

2.5 Microelectronic prototype

The circuit conceptualized in previous paragraphs has been designed and tested in microelectronics flavour, using a 180 nm CMOS process.

As it was the very first prototype the radio-frequency carrier was set at 350MHz instead of the targeted 3.5GHz. After this prototype circuit, others have been fabricated with higher frequencies of the carriers. After the first amplifier that interfaces the human body and the circuit, the signal is feeds a readout chain, used to read out a cardiac signal in this example, and it is interfaced with a *Voltage Controlled Oscillator* (*VCO*) circuit.

The VCO is used to digitize the information by converting the voltage amplitude of the sensor into a variable frequency digital wave (*voltage-frequency conversion*).

Then, the digital signal can interface with a wireless transmitter. As previously, the information is digitally modulated to transmit an Ultra-Wide-Band protocol, balanced around a carrier of about 3.5 GHz. In addition, the example is designed to read out a variety of signals that range from cardiac **Electrocardiogram** (**ECG**), cerebral **Electroencephalogram** (**EEG**) or **Electromyogram** (**EMG**) signals, as well as Radiation Dosimetry.

Once these information have been digitized are treated just as numbers and transmitted via a UWB transmitter (**UWB-TX**)and asynchronously received by an unique device (RX).

2.5.1 Modulator

Hence, it is here described the design of the modulator to interface with the analog output voltage level of a generic sensor. The aim is to be able to read out the sensor output level and convert this voltage variation into a frequency shift over a free-running oscillator. Figure 2.12 shows the basic blocks that implement the modulator:

- a **Sloper** which acts as an integrator since it integrates a voltage level, being successively reset by the output signal of the adjacent comparator;

- a **Comparator** which compares the sensor's output with a predefined reference level;
- a **Toggle** which reads out the output saw-tooth signal of the comparator and generates a more stable square waveform with a frequency range of the order of hundreds of kHz. For this purpose a digital frequency divider was also used;
- an **Enable_ Transmitter** which creates a 100-to-200 ns tunable monostable signal to enable the following Ring_Oscillator;
- a **Ring_Oscillator** that oscillates at 350 MHz, if enabled. It drives the Transmitter for the final antenna coupling;
- a **Transmitter** able to drive, at 3.5 GHz, a 50 Ω antenna. The circuit refers to an input V_{IN} voltage from one sensor. The amplitude varies in this contest of nearly 1 V.

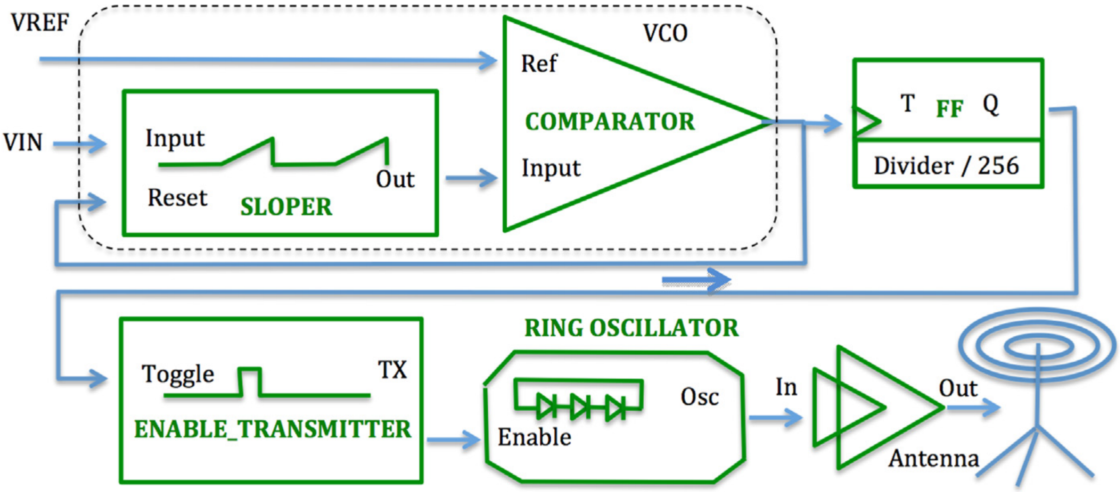
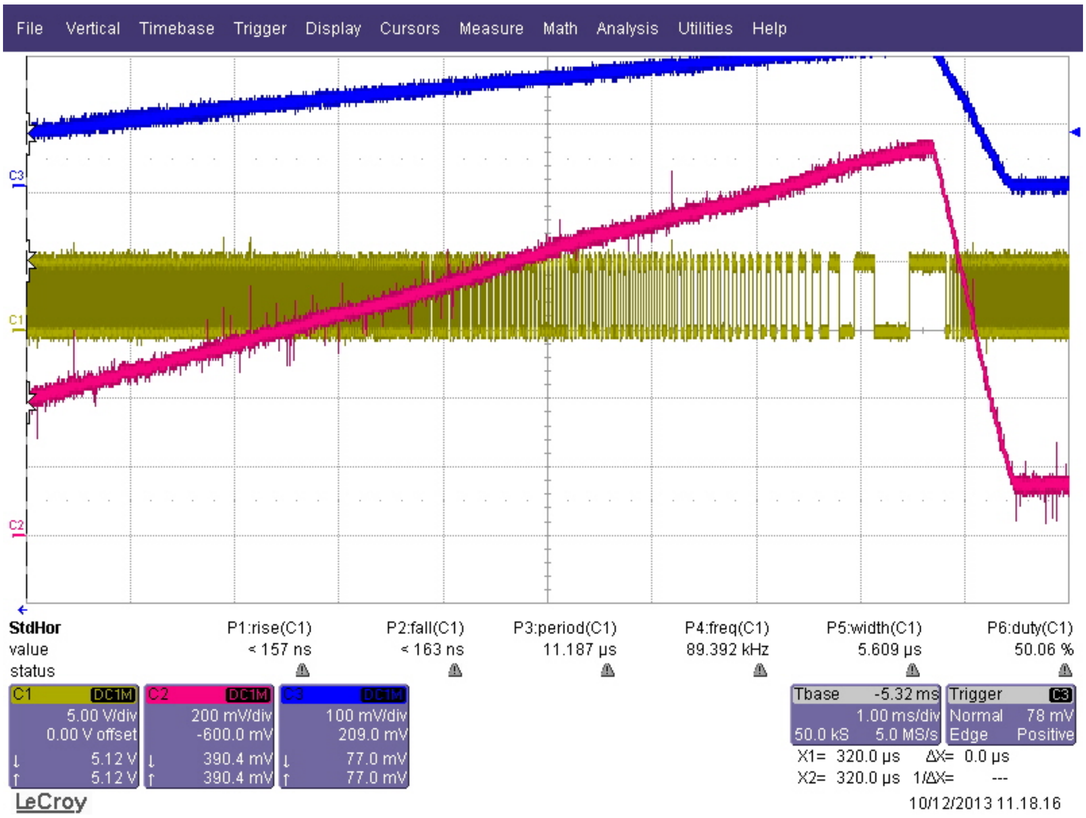


Figure 2.12: Basic blocks of the modulator circuit.

Figure 2.13 shows a frequency variation of the *VCO* (green wave), versus the V_{IN} voltage, red wave. It is apparent that as a consequence of a 1-V amplitude variation of V_{IN} the Toggle circuit produces a square wave with almost decreasing frequency that has been measured from about 85 to 50 kHz. The received and amplified high-frequency waves are visible in fig.2.14:

the upper one (green) is the detected burst at 350 MHz, created via the Ring Oscillator and enabled via the Enable_Transmitter monostable circuit. The same wave is shown in the lower plot (blue) as amplified signal within the receiver. The VCO is part of the modulator (as it is like a serial 1-bit converter) that converts a given analog continuous signal to a digital series of pulses, which are read as a variable-frequency square wave. After that, the S-OOK modulation takes place and, on every rising edge of the VCO output, a series of high-frequency burst, such as that shown in fig.2.14, are generated.

Eventually, the repetition time of these bursts (i.e. how many of these are present in a given period) is inversely proportional to the analog voltage amplitude of the sensor's output.



StdHor	P1:rise(C1)	P2:fall(C1)	P3:period(C1)	P4:freq(C1)	P5:width(C1)	P6:duty(C1)
value	< 157 ns	< 163 ns	11.187 µs	89.392 kHz	5.609 µs	50.06 %
status	⚠	⚠	⚠	⚠	⚠	⚠

C1 DC1M	C2 DC1M	C3 DC1M
5.00 V/div	200 mV/div	100 mV/div
0.00 V offset	-600.0 mV	209.0 mV
↓ 5.12 V	↓ 390.4 mV	↓ 77.0 mV
↑ 5.12 V	↑ 390.4 mV	↑ 77.0 mV

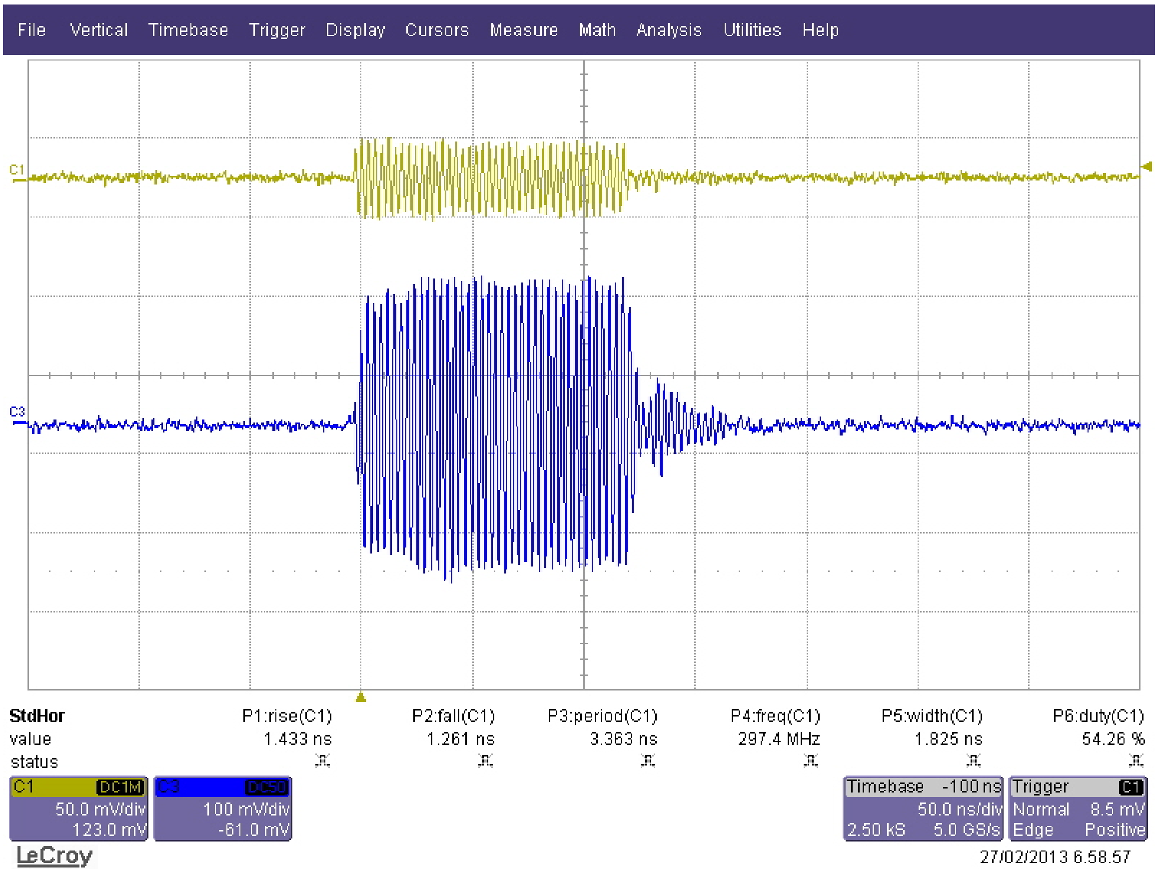
Tbase -5.32 ms
1.00 ms/div
50.0 kS 5.0 MS/s

Trigger C3
Normal 78 mV
Edge Positive

X1= 320.0 µs ΔX= 0.0 µs
X2= 320.0 µs 1/ΔX= ---

10/12/2013 11.18.16

Figure 2.13: Voltage Controlled Oscillator (VCO) signals.



```
StdHor   P1:rise(C1)  P2:fall(C1)  P3:period(C1)  P4:freq(C1)  P5:width(C1)  P6:duty(C1)
value    1.433 ns     1.261 ns     3.363 ns       297.4 MHz    1.825 ns      54.26 %
status
```

```
C1        DC1M   C3        DC50                      Timebase  -100 ns   Trigger    C1
  50.0 mV/div      100 mV/div                                50.0 ns/div   Normal  8.5 mV
  123.0 mV         -61.0 mV                          2.50 kS   5.0 GS/s    Edge    Positive
                                                                   27/02/2013 6.58.57
```

Figure 2.14: Detected and amplified 120 ns wave created by the 350 MHz Ring Oscillator.

2.6 ATC Signal Tests

The same data presented before in section 2.3.2 was artificially modified to test three different possible sources of noise:

- 1) noise was added at different signal-to-noise ratios (SNR);
- 2) the signal was distorted to account for non-linear, saturating amplifiers;
- 3) randomly, threshold transitions were dropped (to account for lost ATC events).

The result of the ATC force estimator is here compared to the one based on ARV.

1) SNR

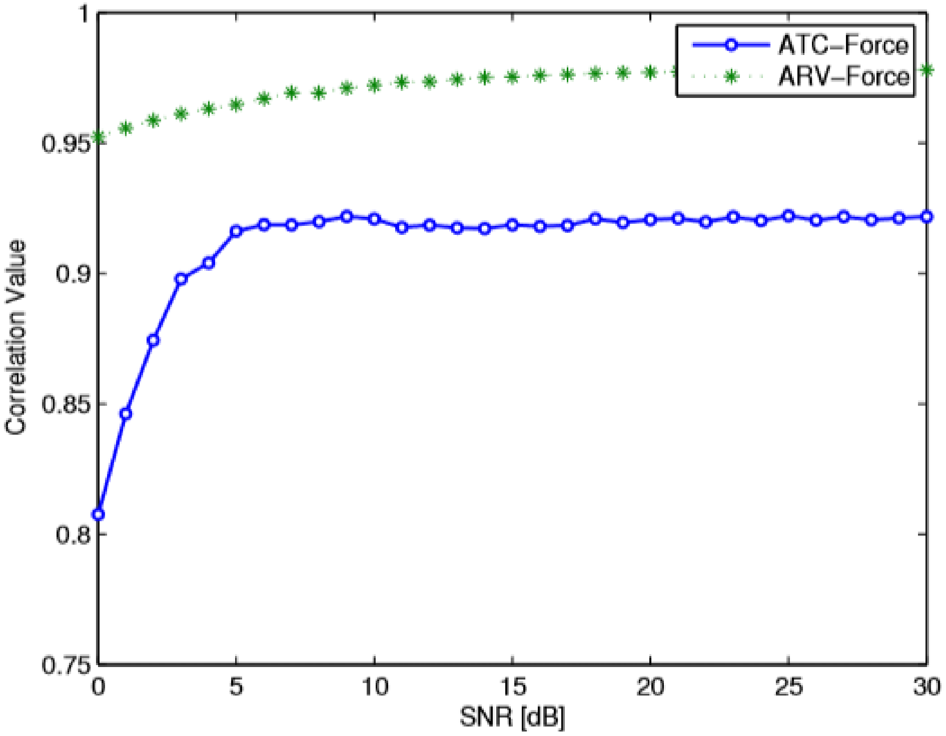


Figure 2.15: Correlation level using ARV and ATC signals increasing acquisition noise.

The first experiment regards the robustness of the ATC signal to increased acquisition noise. To perform this test white noise was artificially added before ATC or ARV computation. We had SNR vary between 0-30 dB: as it can be observed in fig.2.15, 5-6 dB of SNR is already enough for the ATC correlation value to reach is maximum; on the contrary ARV correlation value needs up to 20 dB in SNR to reach the maximum. This suggest that ATC is more robust than ARV to the presence of wideband noise, thus significantly relaxing the requirements on the amplifier.

2) Amplifier distortion

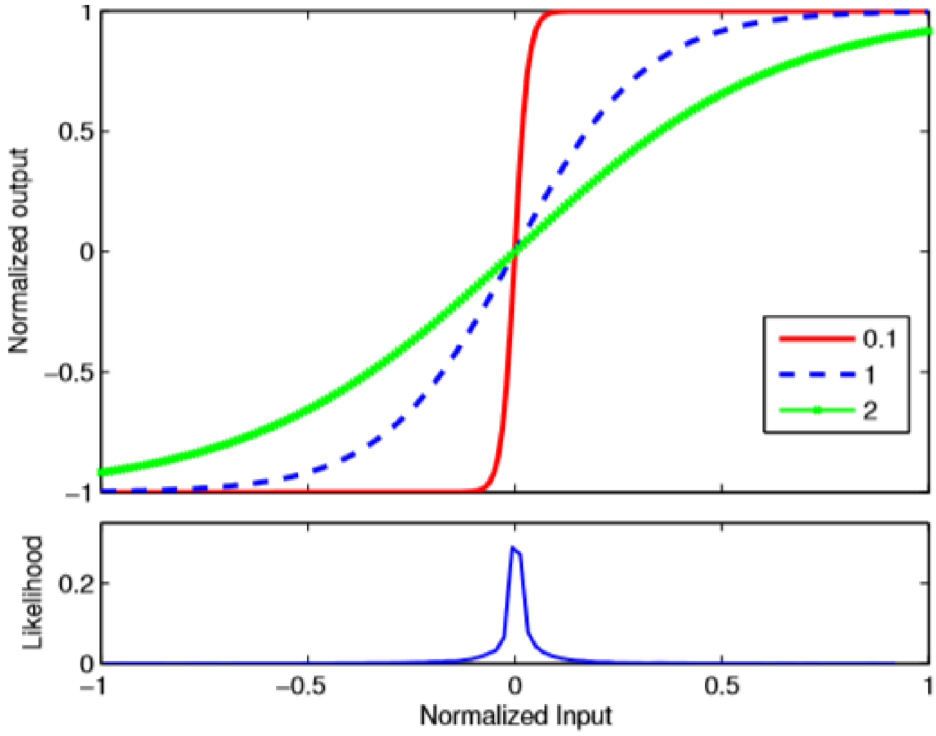


Figure 2.16: Shape for three amplifiers for variable m values.

The second experiment deals with simulating the non-linearities of amplifiers by applying the following function:

$$y = \frac{2}{1 + e^{-2\pi \frac{x}{m}}} \tag{2.5}$$

We simulated different amplifiers by setting m with values ranging from 0.1 to 2 (see fig.2.16); it is possible to denote that for m<1 then (1-m)% of the input signal is saturated to the maximum value.

The result, shown in fig.2.17 demonstrate that the ATC paradigm is practically independent to the distortion of the signal; on the contrary, ARV correlation value is instead damaged when m ≤ 0.5. The bottom half of fig.2.17 shows the probability distribution of the input signals. As it has been expected, the EMG signal is compressed around the 0 value.

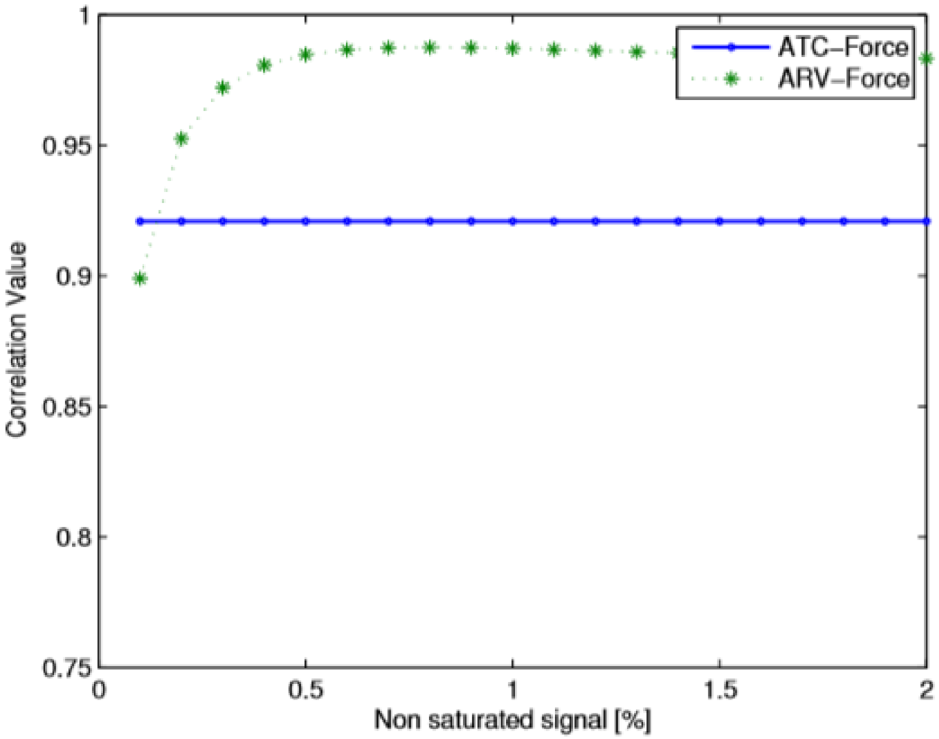


Figure 2.17: Effect of amplifier distortion on correlation to force.

3) Event Loss

Fig.2.18 reports the correlation value for the force estimation as it changes when a percentage of ATC events are lost. The results show that the ATC paradigm is robust to almost 70% event losses. In this section we have shown that the ATC paradigm is very robust to low signal to noise ratios, to low amplifier linearity, and to random ATC event losses.

As it was seen in the previous sections AER over UWB show to be a perfect fit to these characteristics as it is very robust to interferences and can hardly detect false signal pulses. On the other hand, thanks to the ATC robustness to amplifier distortion the requirements for the EMG signal

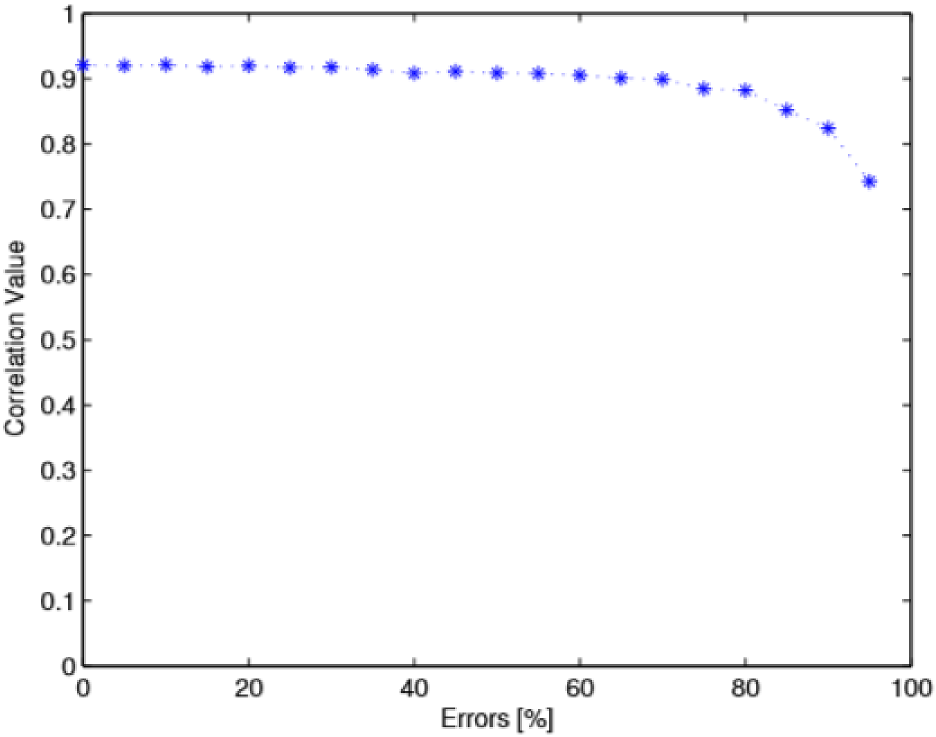


Figure 2.18: Correlation between signal and force in presence of ATC event losses.

amplifier can be relaxed, because it can by-design tolerate large distortion levels, and higher noise factors.

Chapter 3

Modulator design and signal transmission

In this chapter is described the effective implementation of the proposed concept of an integrated component prototype using TowerJazz CMOS 180nm technology. This prototype uses the precautions observed in section 2.5 in creating the microelectronic design and has been produced in two different types (or *"flavours"*) implemented in the same design: the reason of this choice lies in the prototypical nature of this device; different configurations of antenna leads to different effects on signal transmission and needs therefore a "tuning" on physical implementation of the design.

In order to better explain the meaning and functions of the modulator (*Delta-Sigma modulator*) will be show the logic elements that forms the read-out system in both a schematic form (i.e. the symbol representation of circuits) and a layout design (the effective disposition of insulator, conductors and semiconductors used in microelectronics fabrication).

The need of achieving a match between the circuital element "conceptual" representation and the creation, respecting the geometrical rules of the used technology (gate length, etc...), is the fulcrum of microelectronic design.

3.1 Delta-Sigma Modulator composition

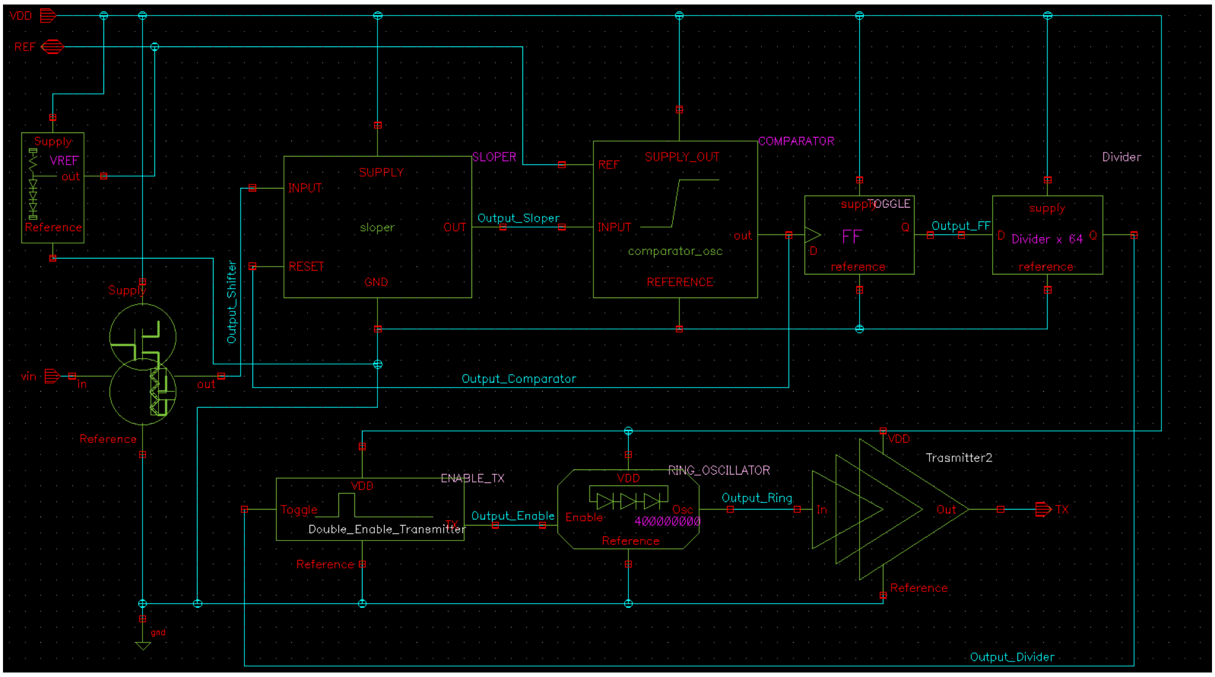


Figure 3.1: Schematic circuit of the Sigma-Delta modulator components.

The modulation of the signal acquired by the pre-amplifier described in section 4 or the dosimeter is therefore described by presenting the integrated circuit in CMOS 180 nm Towerjazz technology and its main components. For every component are presented the Schematic Circuit (*i.e.* its logic functionalities), the Layout Design (the physical implementation of the presented functions) and a brief explanation of the core features of the design (see appendix A for explanations on Layout and Schematic designs).

The sigma-delta modulator is presented in is entirety in fig.3.1 and should also be observed in figure 3.2 in his whole complexity. It is therefore essential to separately explain is main components.

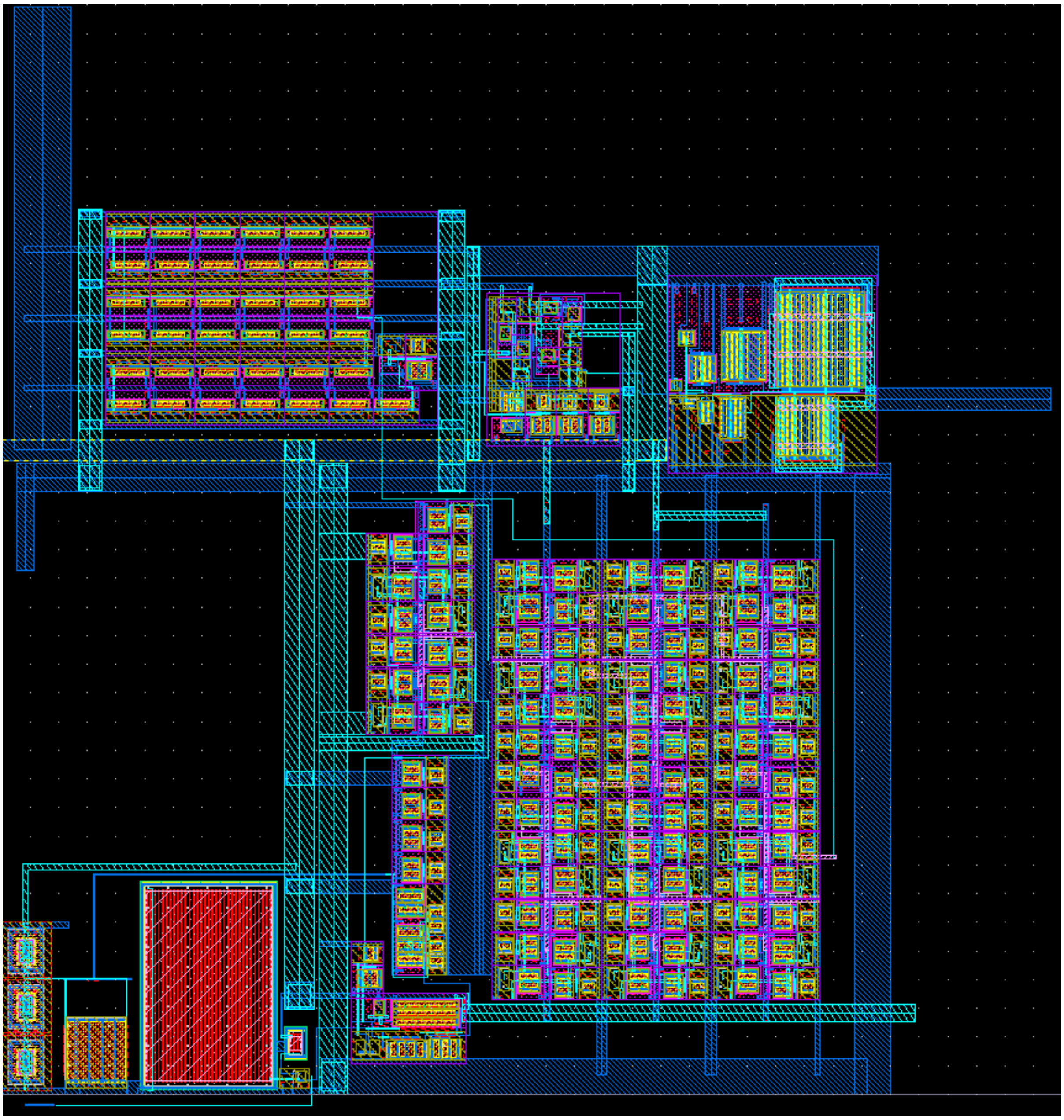


Figure 3.2: Design Layout of the Sigma-Delta modulator.

Level Shifter

The **Level Shifter** circuit shifts down the voltage from a 0-3V range to 0-2V to adapt the input range of the **Sloper** circuit. This level shifter is composed of a source-follower NMOS with a 3.5 MΩ, in parallel with a small capacitor, on its source.

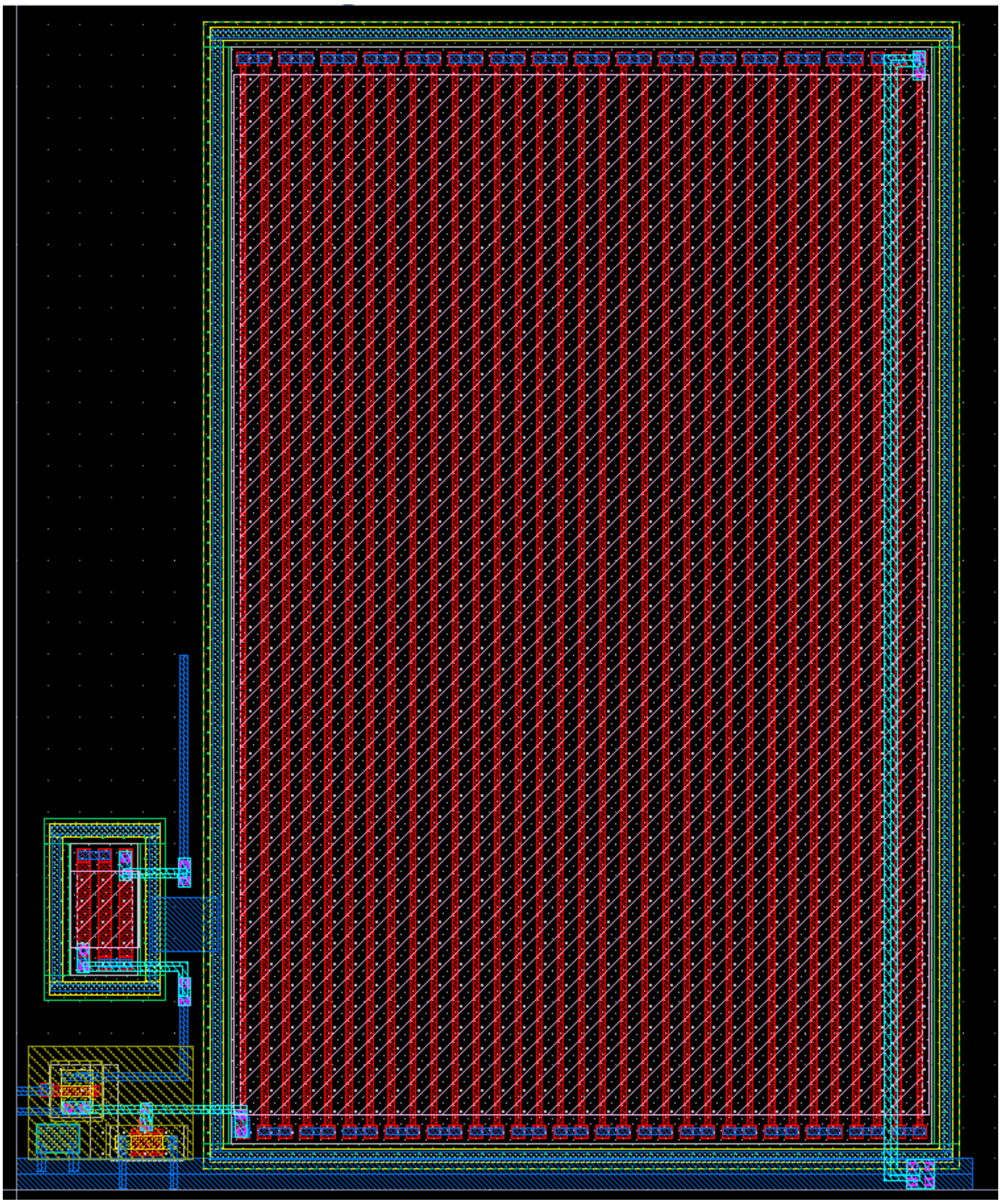


Figure 3.3: Schematic circuit of the Voltage Level Shifter.

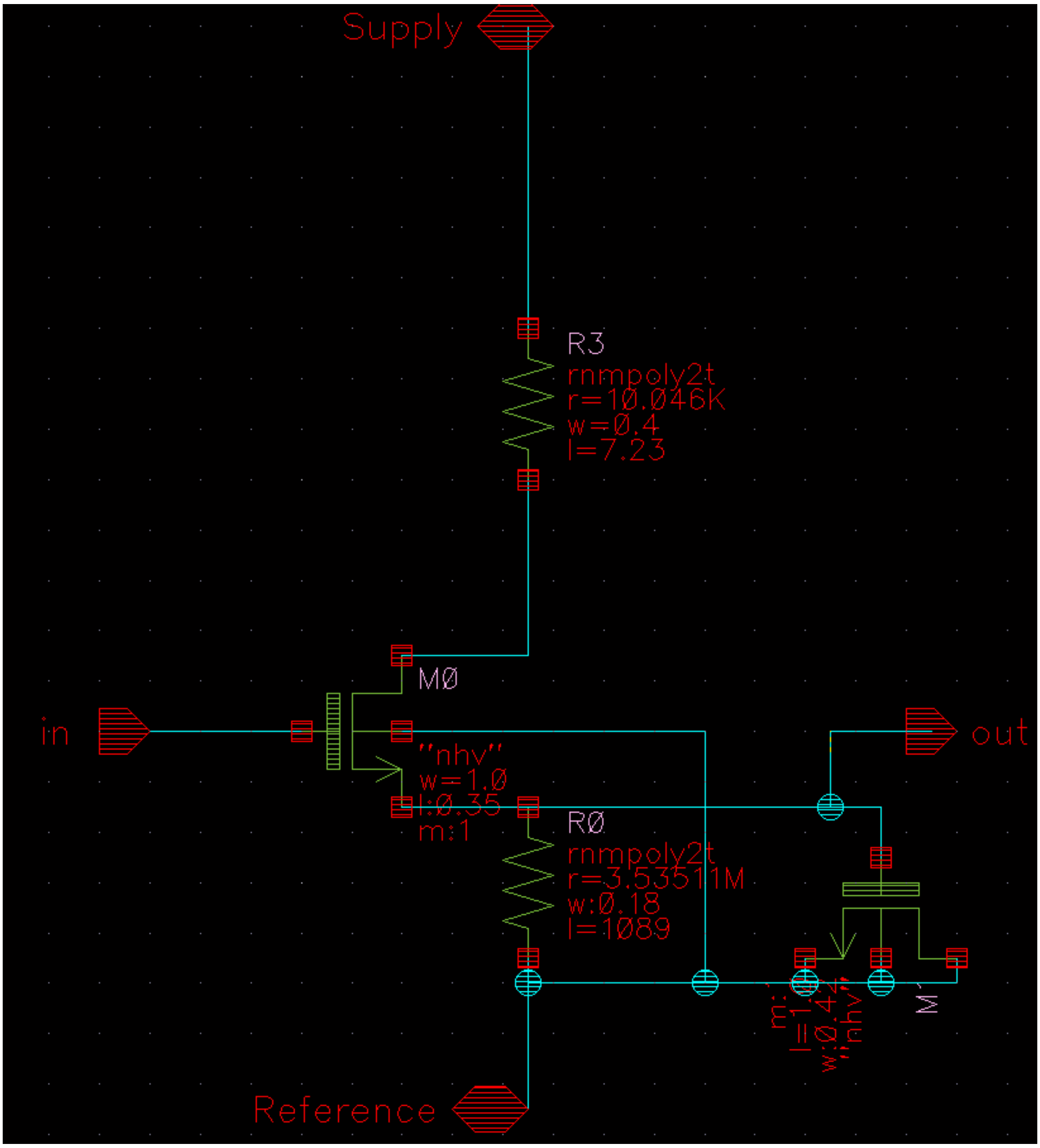


Figure 3.4: Design layout of the voltage level shifter.

Voltage Reference diode

V_{Ref} is a shunt diode-based voltage reference of 2/3 V_{DD}. This circuit should be connected internally or externally (Depending of circuit flavour, see sect.3.3). Cascading three diodes, as in figure 3.6 let us obtain a 2V signal for the comparator (which compares input signals to a threshold of 2 V) very stable and without further need of 2V power sources.

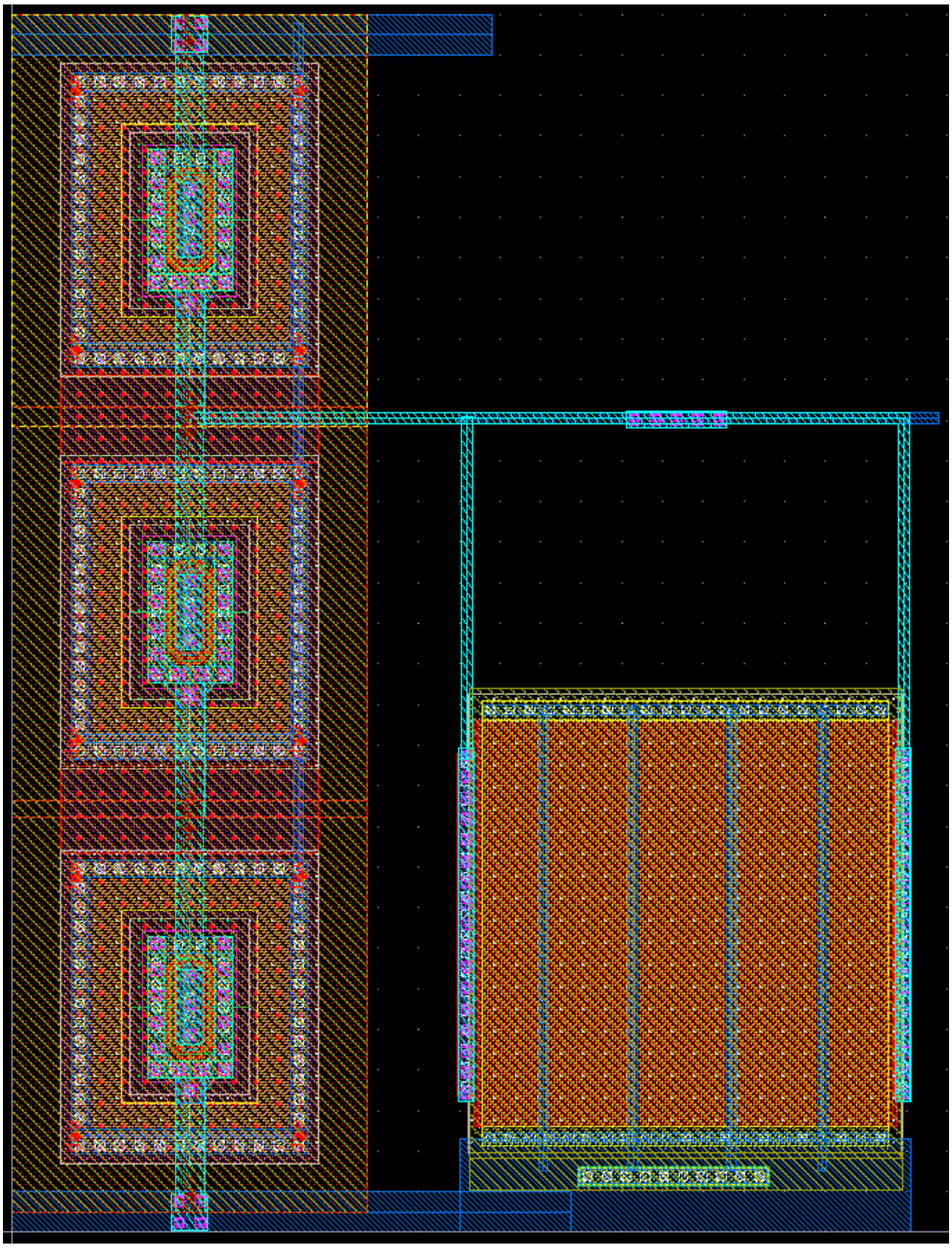


Figure 3.5: Schematic circuit of the Voltage Reference diode.

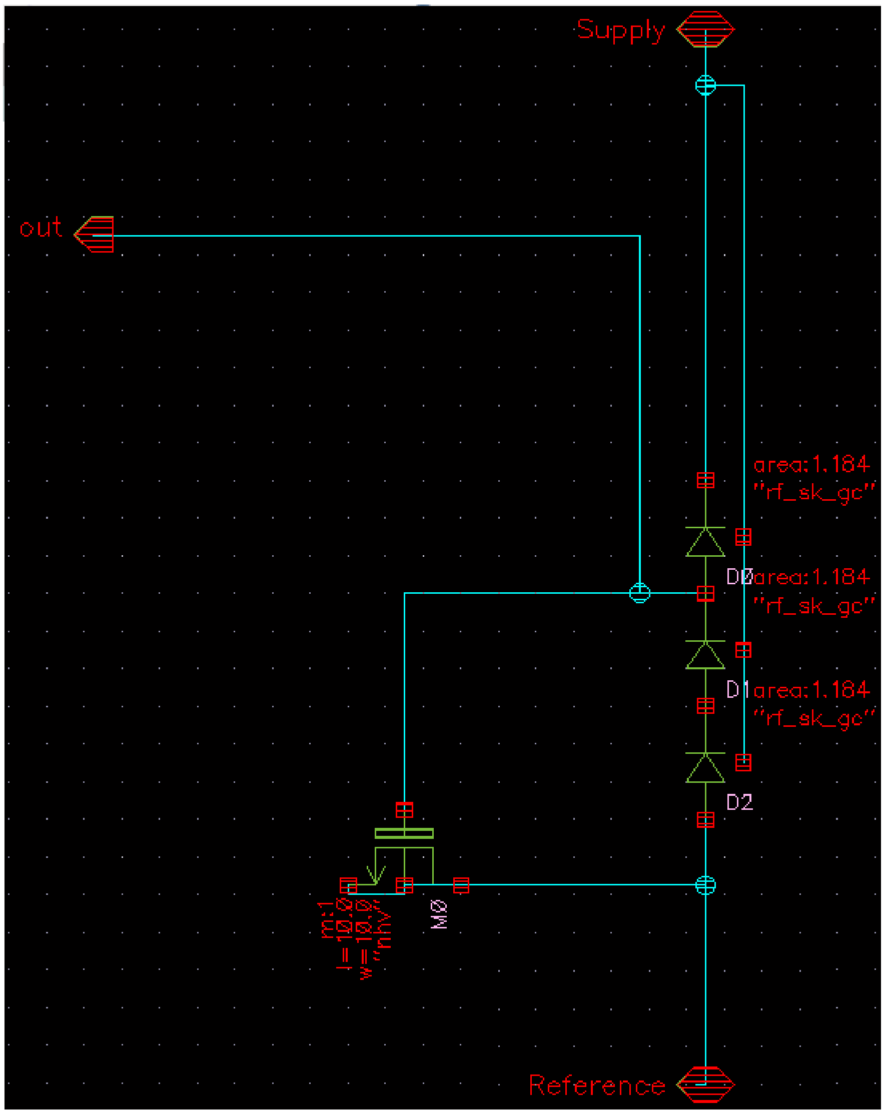


Figure 3.6: Design Layout of the Voltage Reference diode.

Sloper

The Sloper acts as a free-running oscillator since it integrates an external voltage level (the amplified EMG input or the radiation signal); the sloper output act is compared to a fixed value in the adjacent comparator and if, the threshold is crossed, the comparator reset the sloper to start a new integration (as seen in fig.3.21).

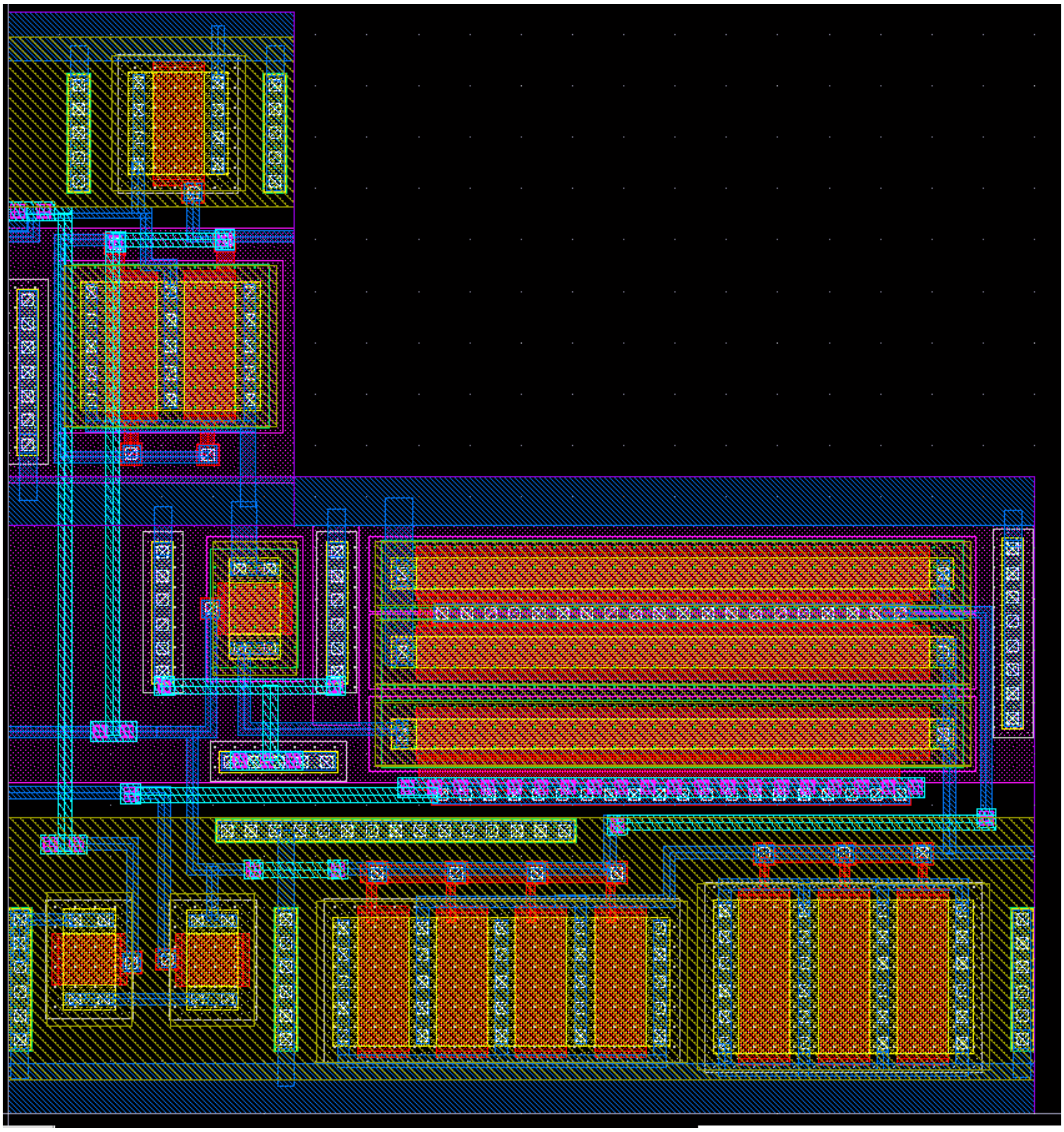


Figure 3.7: Schematic circuit of the Sloper.

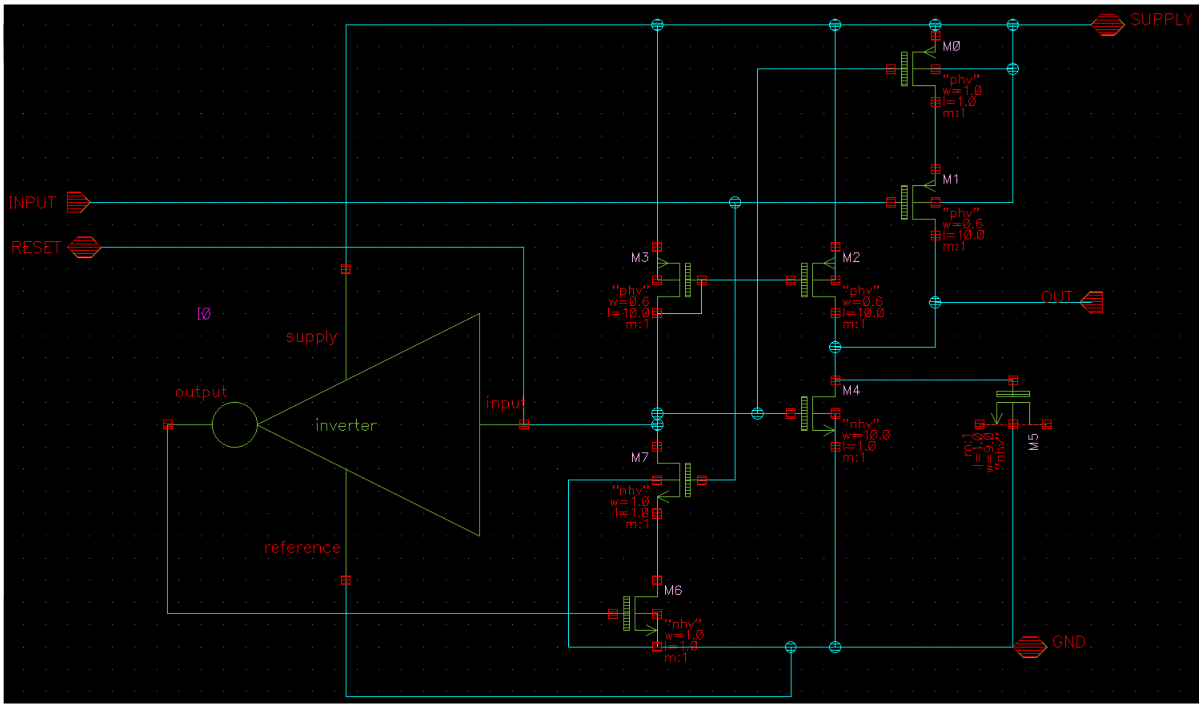


Figure 3.8: Design Layout of the Sloper.

Comparator

The Comparator compares the output level of the sensor integrated by the sloper with a predefined reference level of 2V. Each time the threshold is crossed, it sends a saw-tooth signal (fig.3.21) that enable the Flip-Flop and reset the sloper.

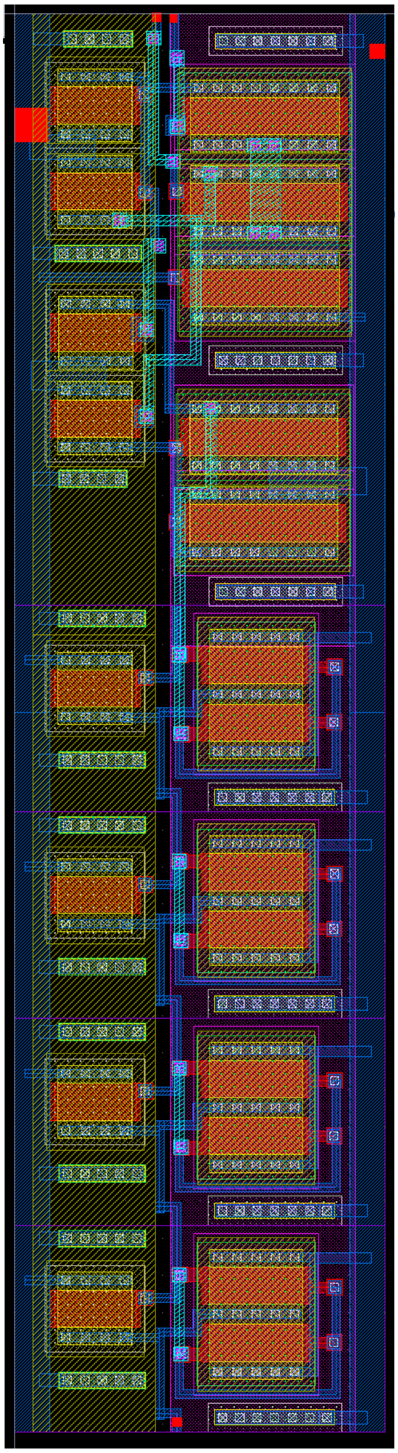


Figure 3.9: Layout design of the level comparator.

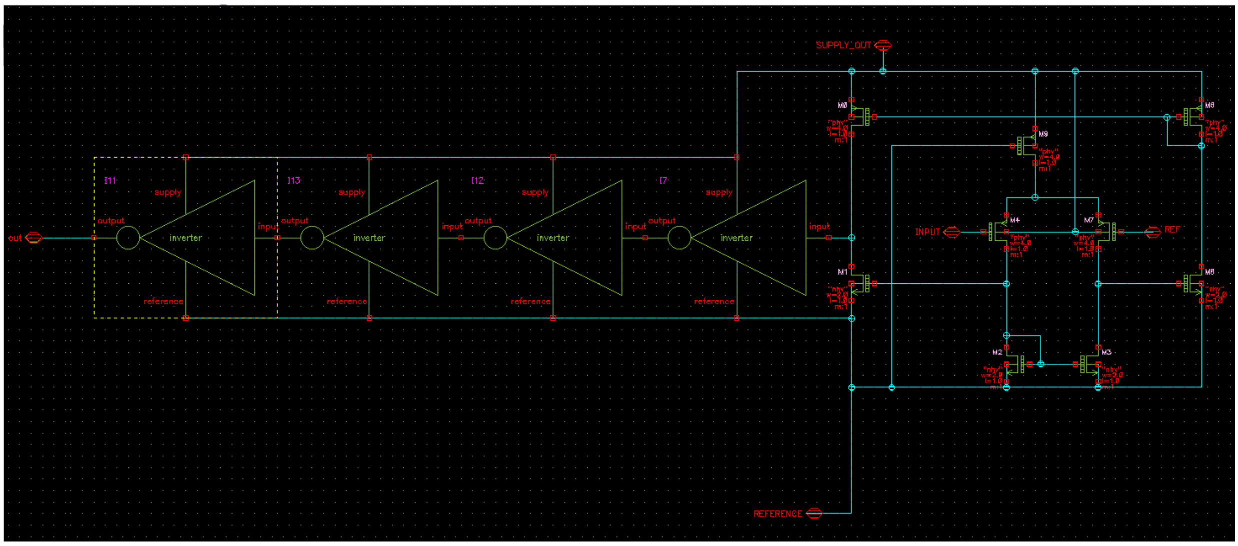


Figure 3.10: Schematic circuit of the level comparator.

Toggle

The Toggle reads out the output saw-tooth signal of the comparator and generates a more stable square waveform with a frequency range of the order of hundreds of kHz.

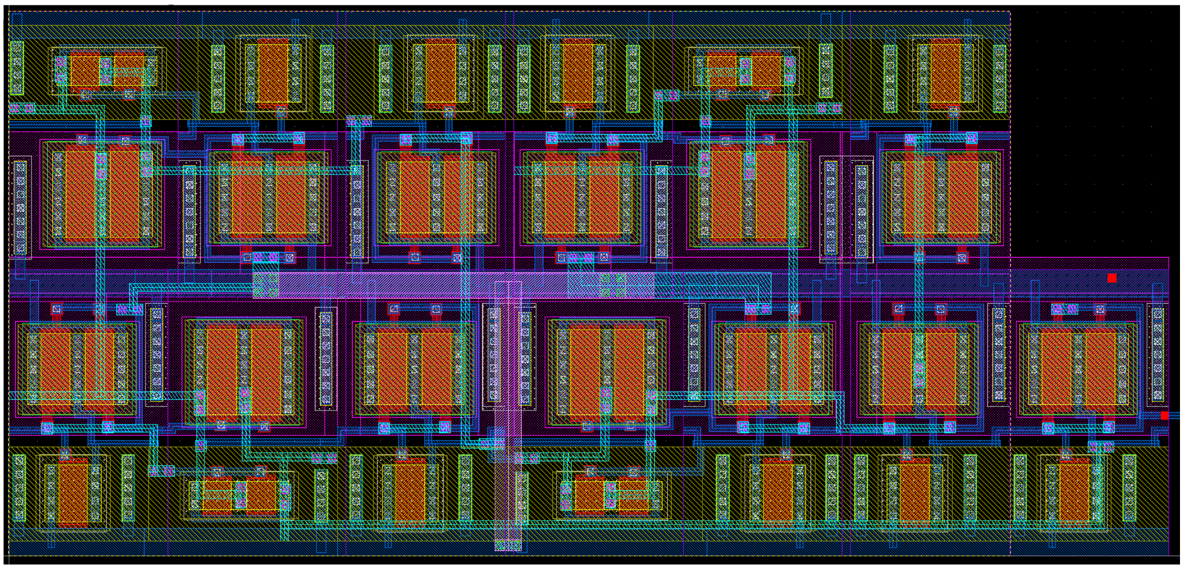


Figure 3.11: Schematic circuit of the Toggle.

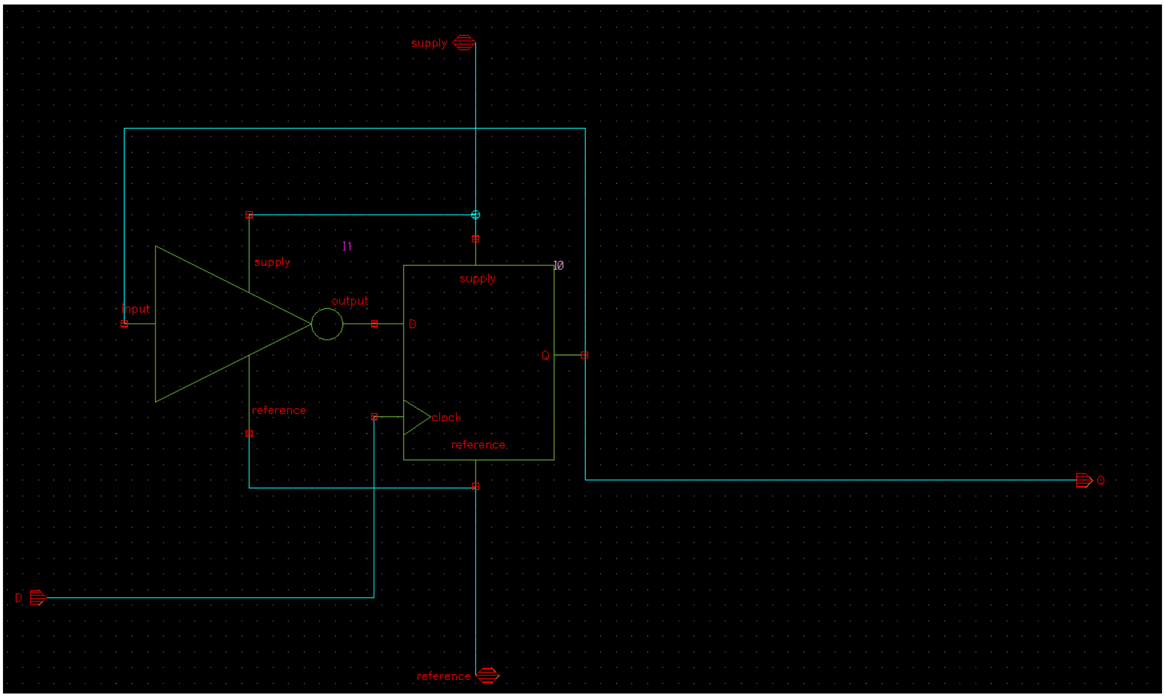


Figure 3.12: Design Layout of the Toggle.

Frequency Divider

The Divider divides the frequency of the Toggle circuit in order to make fit the time duration of the acquired signal into the temporal frame of the transmitter, i.e. in order to extend the information burst length and improve the duty cycle.

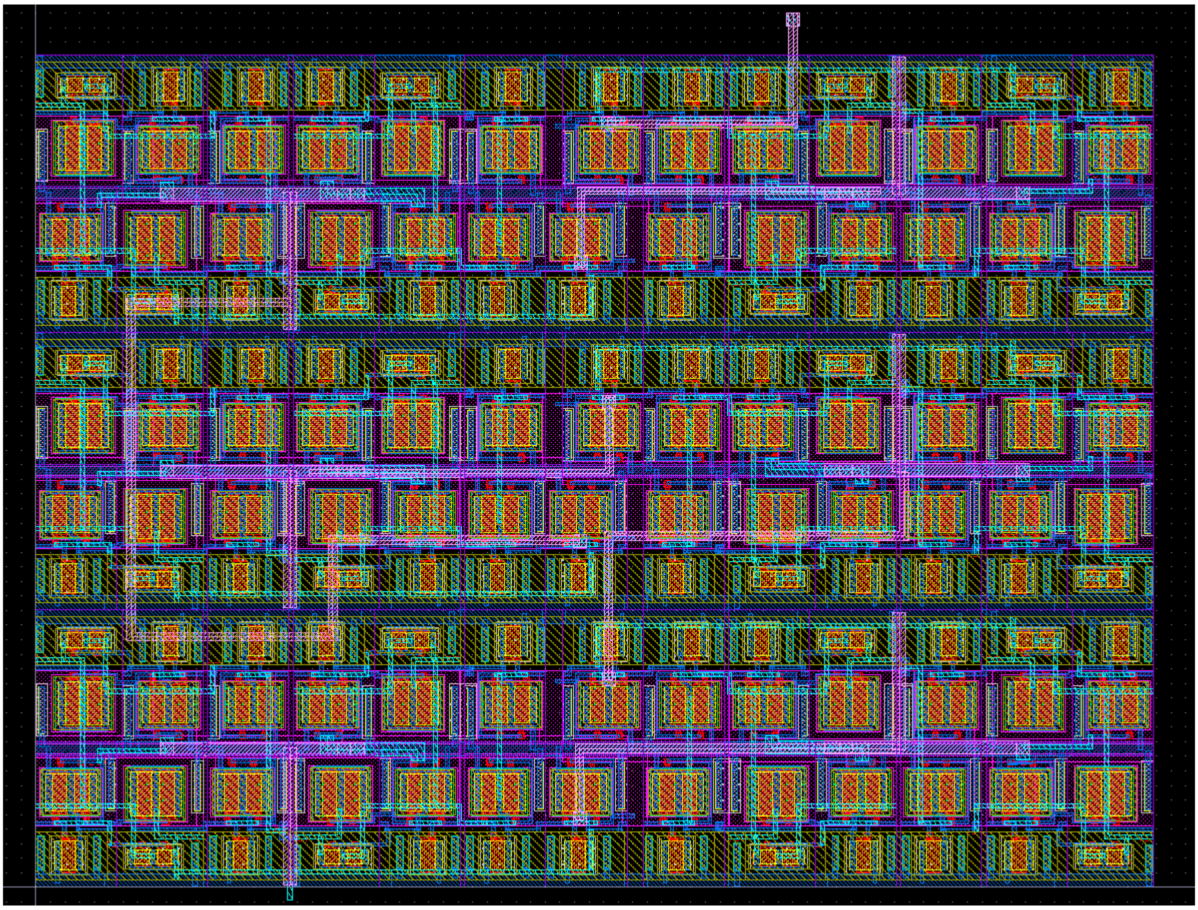


Figure 3.13: Schematic circuit of the Frequency Divider.

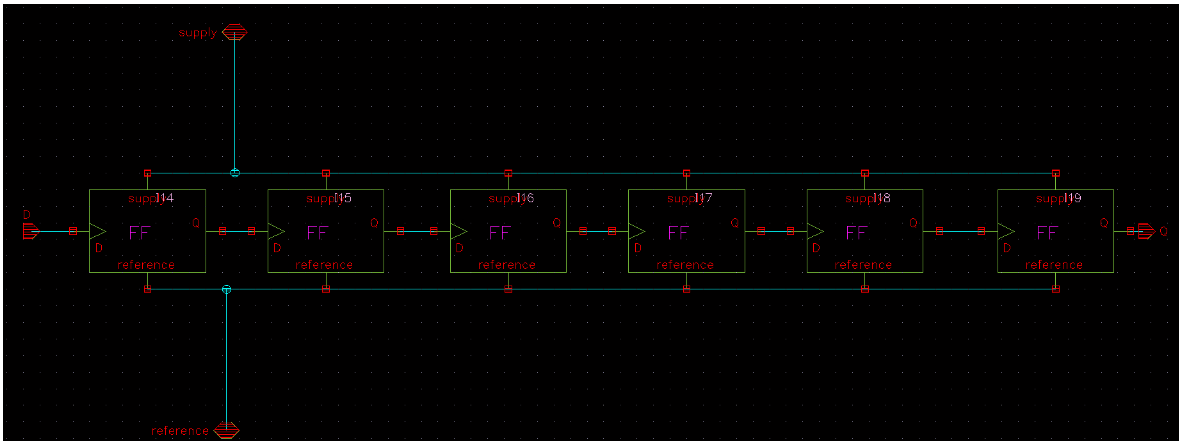


Figure 3.14: Design Layout of the Frequency Divider.

Double Enable Transmitter

The Enable Transmitter creates an about 215 ns monostable signal to enable the following Ring Oscillator.

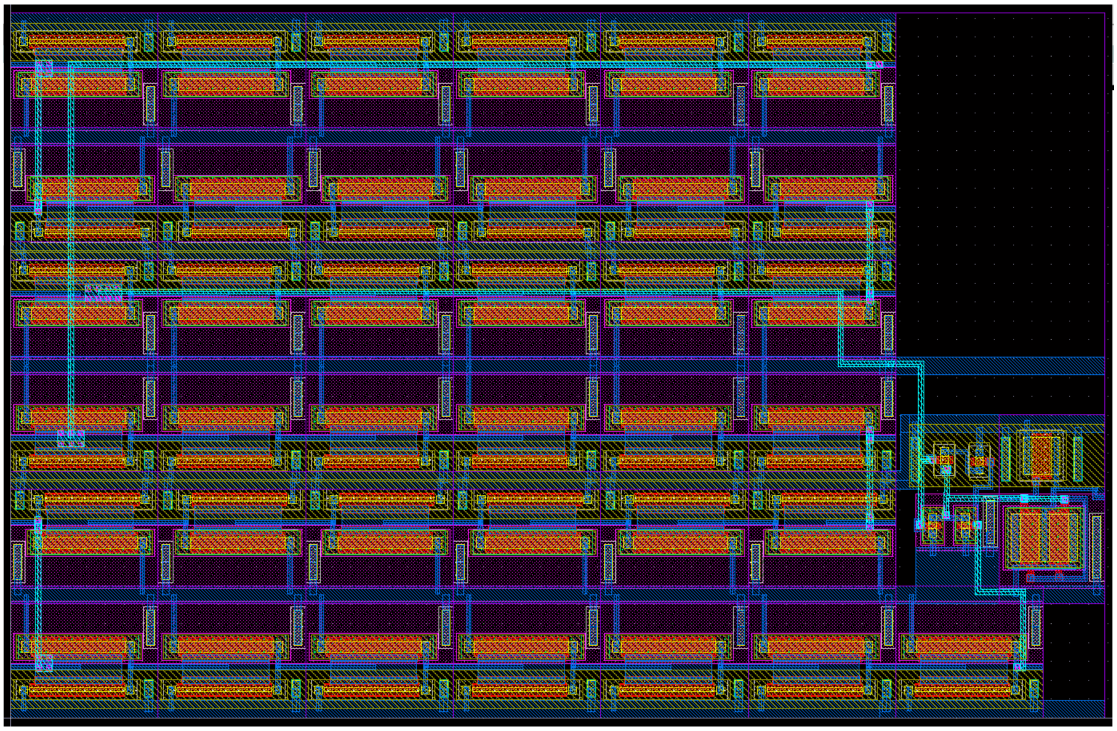


Figure 3.15: Schematic circuit of the Enable Transmitter.

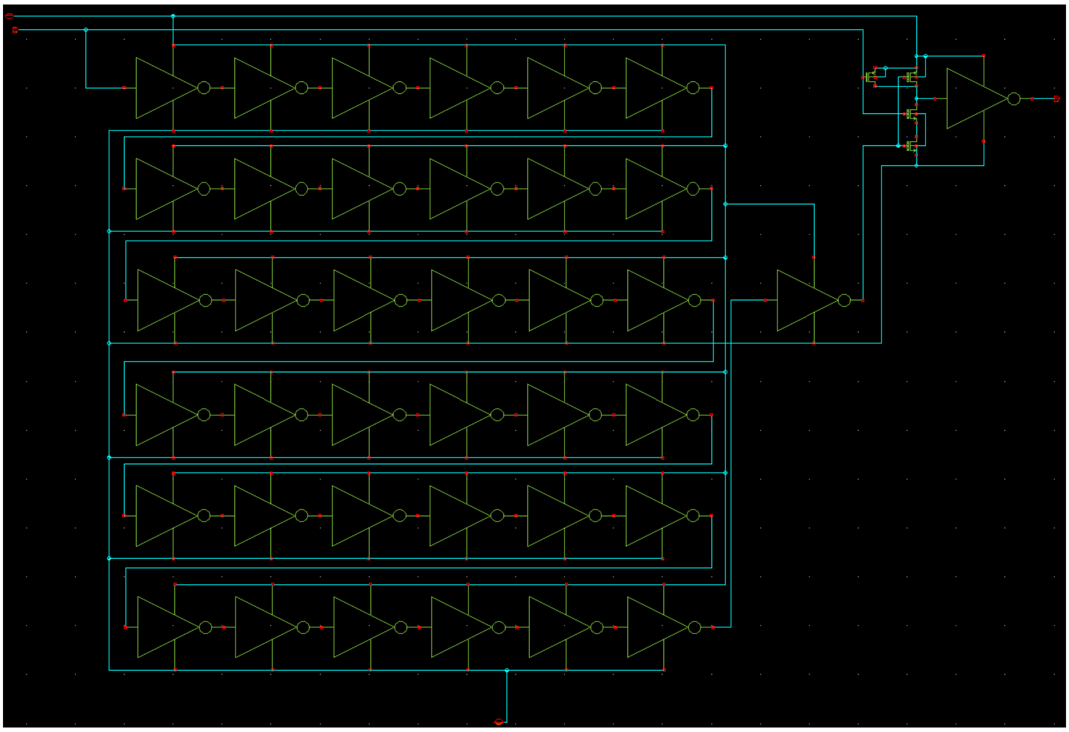


Figure 3.16: Design Layout of the Enable Transmitter.

Oscillator

The Ring Oscillator oscillates at 400 MHz, when enabled.

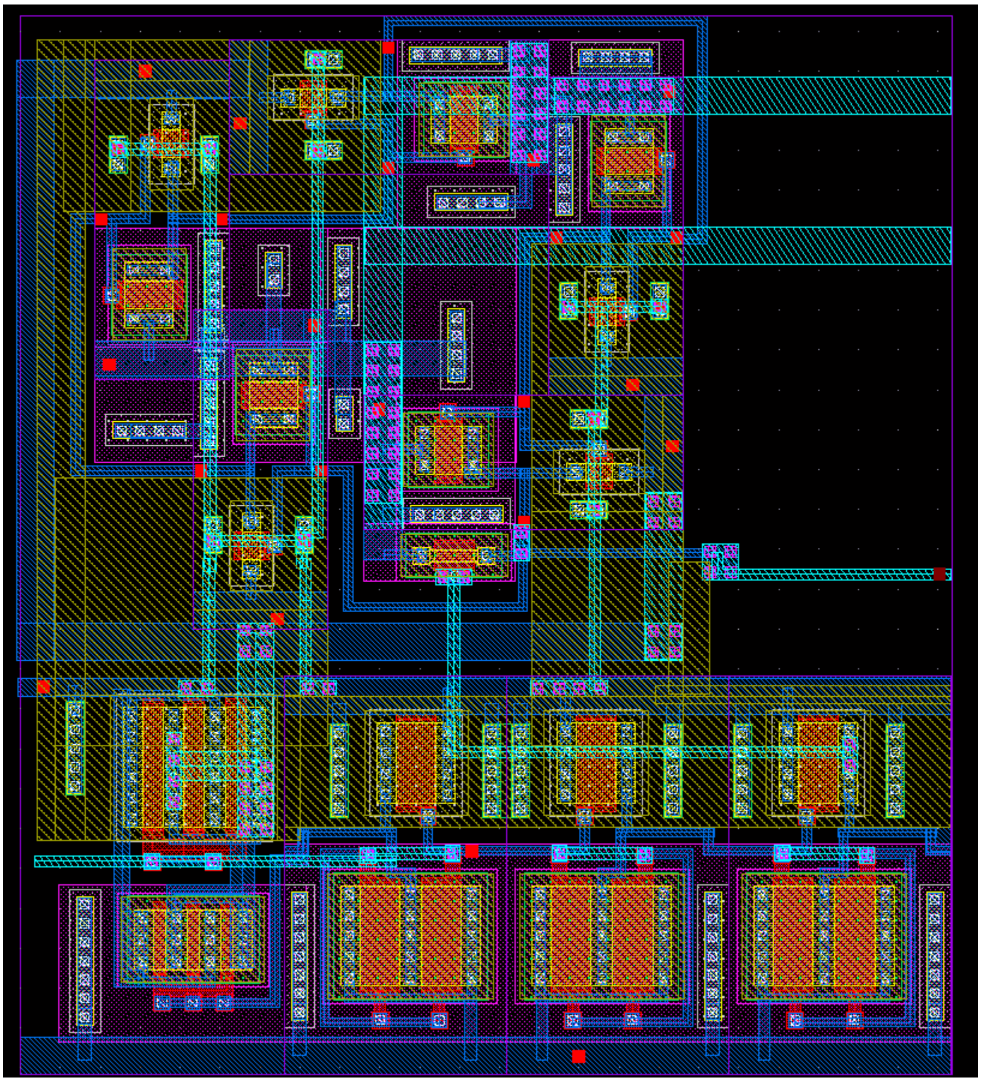


Figure 3.17: Schematic circuit of the Oscillator.

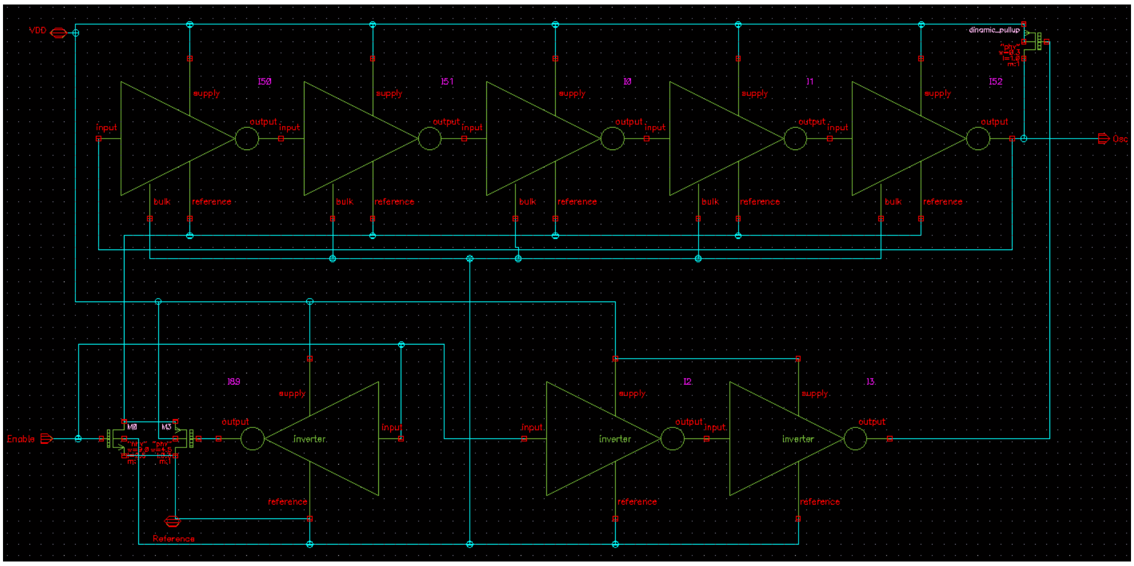


Figure 3.18: Design Layout of the Oscillator.

Transmitter

The transmitter is able to drive, at 400 MHz, a load composed of a parallel 10 pF capacitor 50 Ω resistor, while maintaining a voltage swing of about 2 V being powered at 3.3 V.

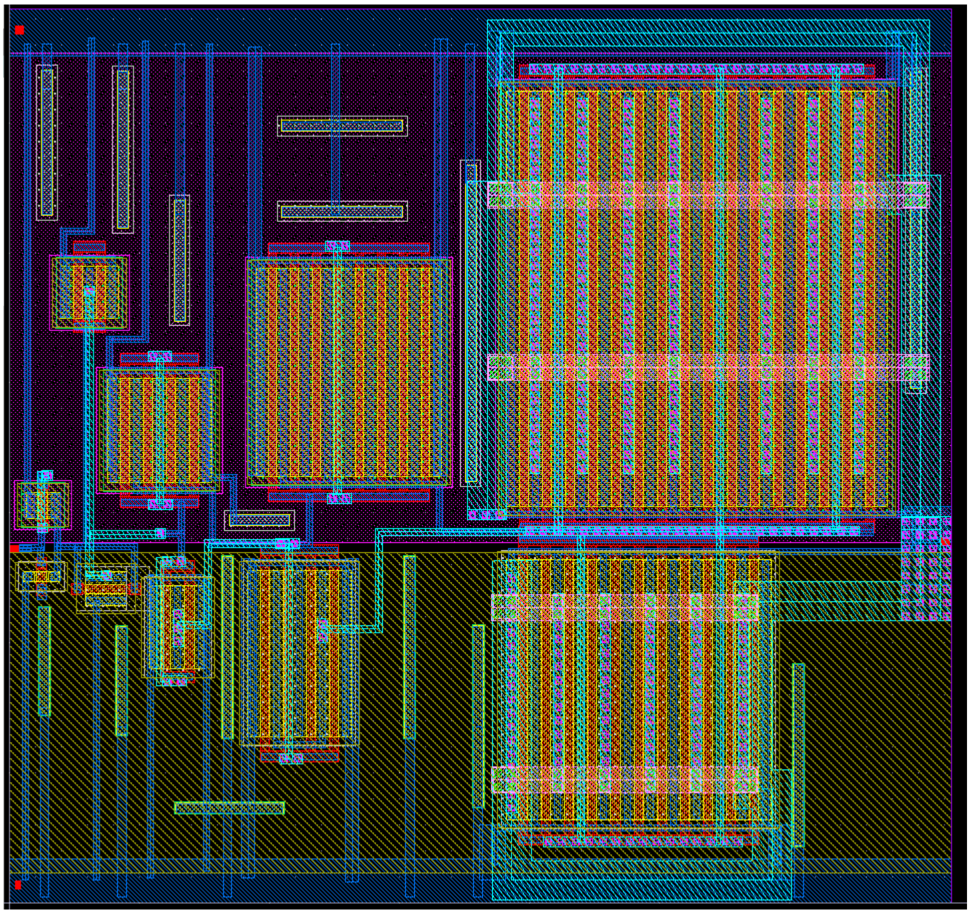


Figure 3.19: Schematic circuit of the Transmitter.

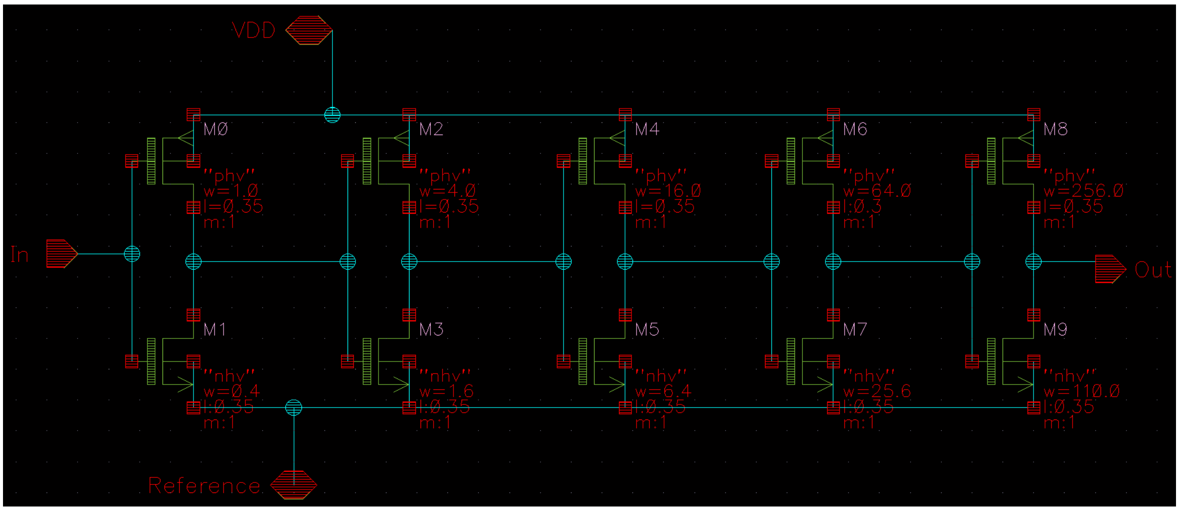


Figure 3.20: Design Layout of the Transmitter.

3.2 Transmission

3.2.1 Simulations and UWB wireless measurements

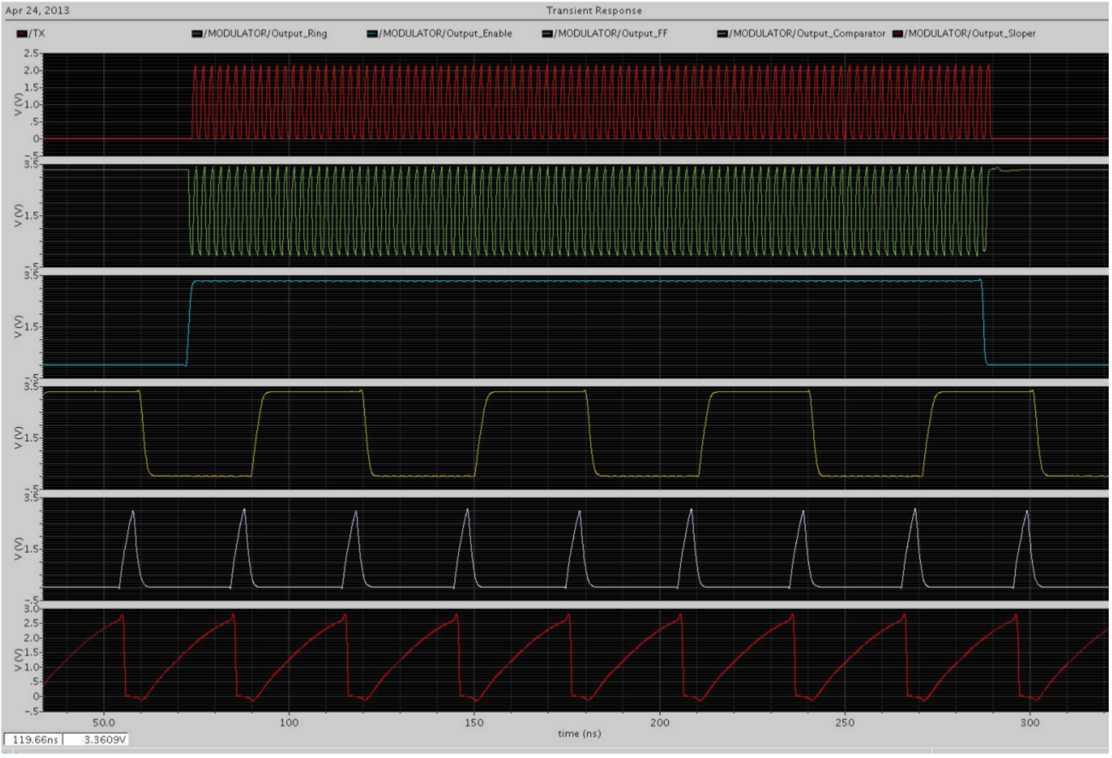


Figure 3.21: Simulation of the Sigma-Delta circuit.

Figure 3.21 shows from top to bottom the waveforms as they respectively come out from the **Antenna**, the **Transmitter**, the **Enable Transmitter**, the **Toggle**, the **Comparator** and the **Sloper**. All the simulations have been carried out using the Cadence Spectre simulator and Spectre model from TowerJazz; also, the RC parasitic extracted parameters were added to the simulation (see appendix A).

Simulations in figure 3.21 are zoomed to show the RF signal on the antenna; here the voltage swing only reaches 1.5 V, but his depends on the type of the load. Using a 10 pF capacitor in parallel with a 50 Ω resistor, the final Transmitter allows a voltage swing of 2 V on the antenna. The RF burst lasts about 213 ns.

3.2.2 Spread of Parameters

Figure 3.22 shows preliminary results about the readout circuit. The Sloper input level (V_{IN}) ranges from 0 to 3 V and the VCO circuit decreases the repetition output frequency quite linearly from 280 kHz to 180 kHz. Here the V_{IN} signal was obtained by programming the dosimeter at different constant values: these results are therefore fully representative of whole integrated devices.

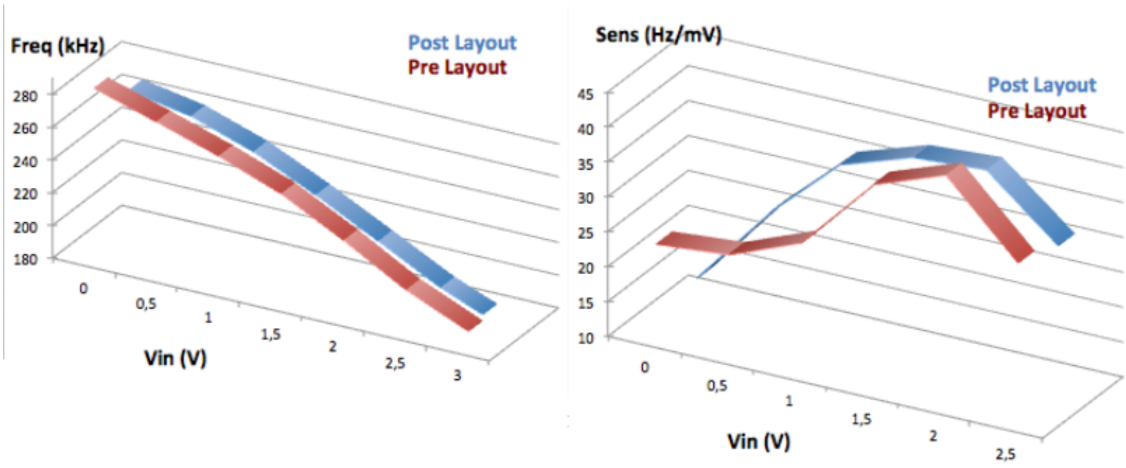


Figure 3.22: Results of the spread of parameters in Vin vs Toggle Frequency simulations. The plot on the left shows how the VCO frequency varies depending on the VIN at the modulator input; on the right is plotted the estimated sensitivity of the circuit, with pre-layout and post-layout simulations. The burst were 213 ns long; the base band was 403MHz; V_{dd} was set at 3.3V and $V_{REF} = \frac{2}{3}V_{dd}$.

The graph is divided into a left plot representing how the output toggle frequency varies upon input voltage, and a second on the right that shows an estimation of the sensitivity of the circuit, in $\frac{Hz}{mV}$.

In detail, this is an estimation on how the output frequency of the transmitted radio-frequency bursts varies upon input voltage; the two plots show both pre-layout simulated data (without including the parasitic extraction) and the circuit with parasitic effects included (see appendix A). In this way we can estimate how the simulations might approximate the actual expected behaviour. The blue and red curves refer to pre and post layout simulations, in any case resulting to similar numbers; this analysis leads to a possible estimation of the sensitivity of the device: the toggle frequency senses about 30 kHz/V.

V_{IN}	**frequency Pre Layout (kHz)**	**frequency Post Layout (kHz)**
0	283	266
0.5	272	259
1	260	246
1.5	246	229
2	226	210
2.5	205	190
3	189	175

A set of measurements was done on the already produced prototypes to evaluate the received UWB signal power, by varying the distance of a spectrum analyzer used as a receiver.

V_{IN}	**sensitivity (Hz/mV) Pre Layout**	**sensitivity (Hz/mV) Post Layout**
0.5	23	14
1	24	26
1.5	28	35
2	39	38
2.5	43	39
3	32	31

A 10 dB/div monitor was set with a 100 kHz input filter to clean up the integrated input signal. The measured power spectrum shown in Figure 3.23 shows the Ring Oscillator working at a lower frequency than expected, i.e. 350 MHz instead of 400 MHz.

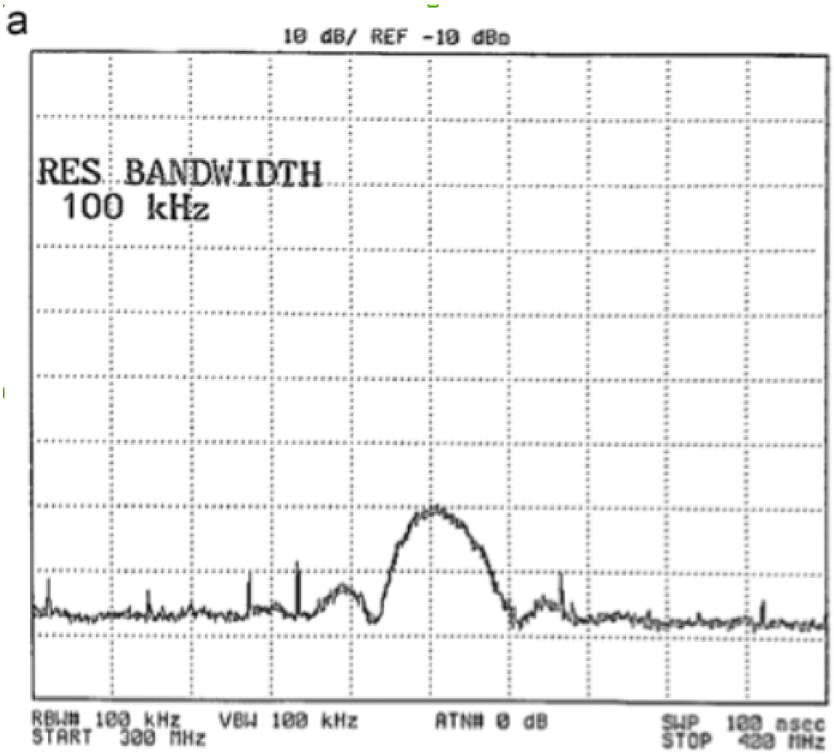


Figure 3.23: Ultra Wide Band bandwidth occupation[9]: the signal is composed by harmonic functions that tower in amplitude over the uniform noise.

This discrepancy can be interpreted in terms of both parasitic effects on the oscillator, which were not entirely under control during the design, and of the antenna inefficiency due to its being not optimized with respect to the carrier frequency.

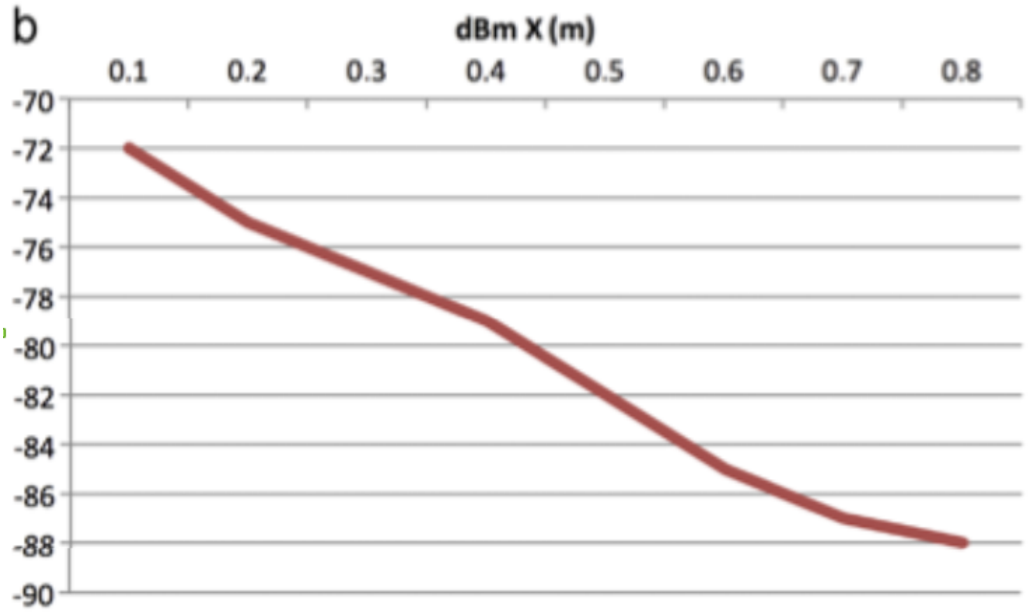


Figure 3.24: Power distribution of the transmitted signal versus distance.

Nevertheless, the transmission concept is confirmed and the signal is detectable at various distances in the range of 10 cm to 1 m from the chip as illustrated in Figure 3.24. During these measurements the total average current consumption was also evaluated to be about 50 μA (165 μW at 3.3 V), which is fully compliant with low-power and remotely powered wireless applications.

3.3 Circuit Flavours

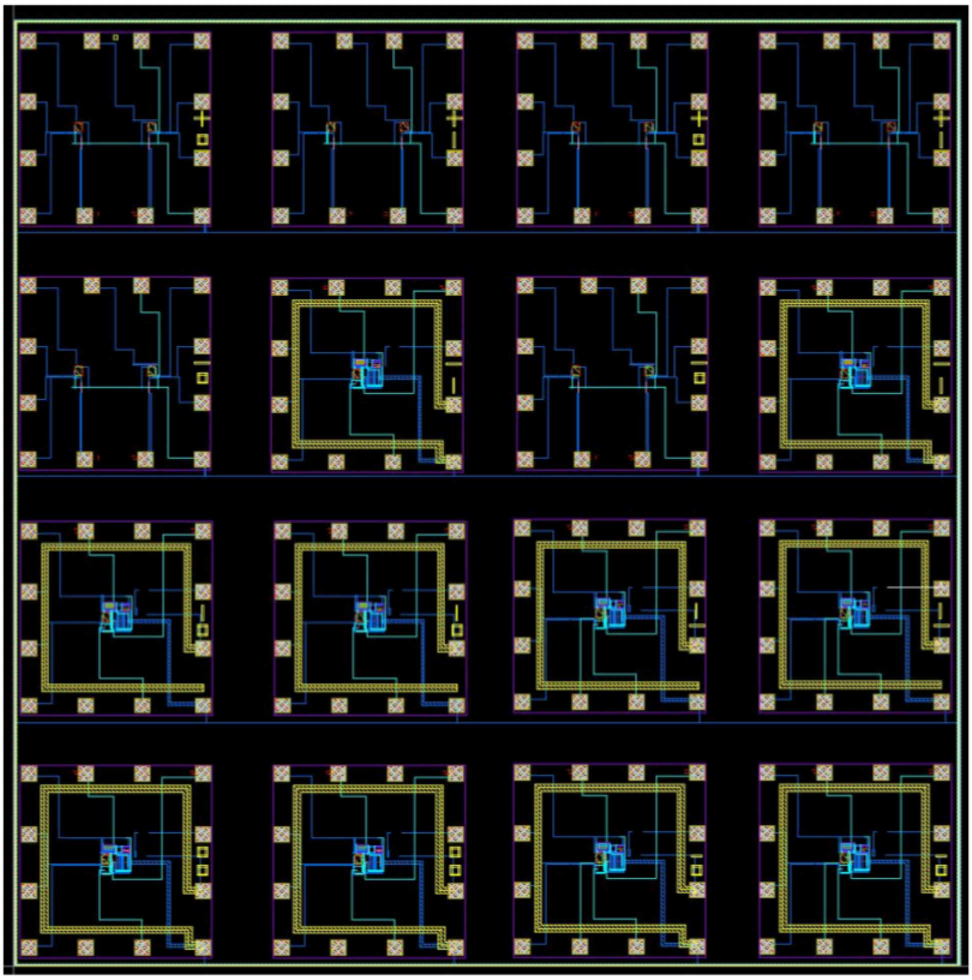


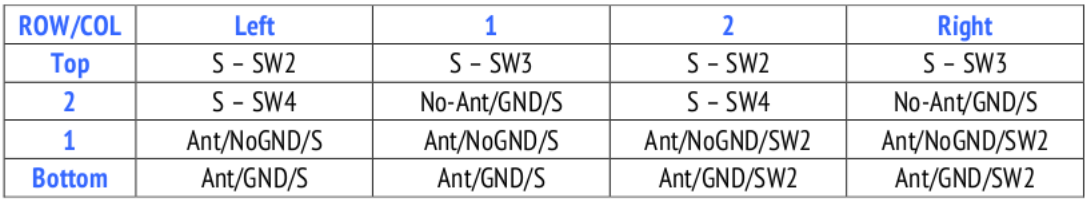
Figure 3.25: Distribution of the 16 items on the physical chip. The chip are divided in two flavours.

Due to antenna tuning, the same circuit has been created in different "*flavours*" corresponding to different component disposition and connection, as explained below; the items distribution is show in fig.3.25. The flavours differ first in two main options:

- **First Option:** used in top and 3^{rd} row, 1^{st} and 3^{rd} column from the left, implements two sensors only;
- **Second Option:** implements one full sigma-delta modulator with one-only-ring antenna close to the circuit.

The flavour belonging to two options differ internally to the same option depending on how the antenna is connected and for the presence of an additional metal layer on top of the sensor, for better testing the sensibility.

The two flavours have necessarily different pin-outs, however the **GND** and **PWR** share the same pads. Thus, eventually, it is like having copied and pasted the left column twice. The flavours differs for the following characteristics:



ROW/COL	Left	1	2	Right
Top	S - SW2	S - SW3	S - SW2	S - SW3
2	S - SW4	No-Ant/GND/S	S - SW4	No-Ant/GND/S
1	Ant/NoGND/S	Ant/NoGND/S	Ant/NoGND/SW2	Ant/NoGND/SW2
Bottom	Ant/GND/S	Ant/GND/S	Ant/GND/SW2	Ant/GND/SW2

- **S:** Regular sensor with L/2W form factor, without any additional metal on top;
- **SW2:** Regular sensor with L/2W form factor, with additional metal **M2** on top;
- **SW3:** Regular sensor with L/2W form factor, with additional metal **M3** on top;
- **SW4:** Regular sensor with L/2W form factor, with additional metal **M4** on top;
- **ANT:** Top side of antenna connected to the modulator's output;
- **NoANT:** Top side of antenna not connected to the modulator's output;
- **GND:** Bottom side of antenna connected to the **GND** pad;
- **NoGND:** Bottom side of antenna not connected to the **GND** pad;

Base circuit is ANT/GND/S (row/col 00 and 01) so with antenna connected on both sides, no metal on top of the floating gate and VREF internally connected.

3.3.1 Flavour 1 Pinout

Here are summarized the chip pin-out, along with fig.3.26 for the first flavour option:

- 1 - **VDD 1** supposed at 3.3V;
- 2 - Sensor control gate 1;
- 3 - Tunneling Gate 1;
- 4 - Deep NWell 1;
- 5 - Sensor 1 out;
- 6 - Sensor 2 out;
- 7 - **GND**;
- 8 - Deep NWell 2;
- 9 - Tunneling gate 2;
- 10 - Sensor control gate 2;
- 11 - Metal plate on the sensor 2, to be externally biased;
- 12 - **VDD 2** supposed at 3.3 V;

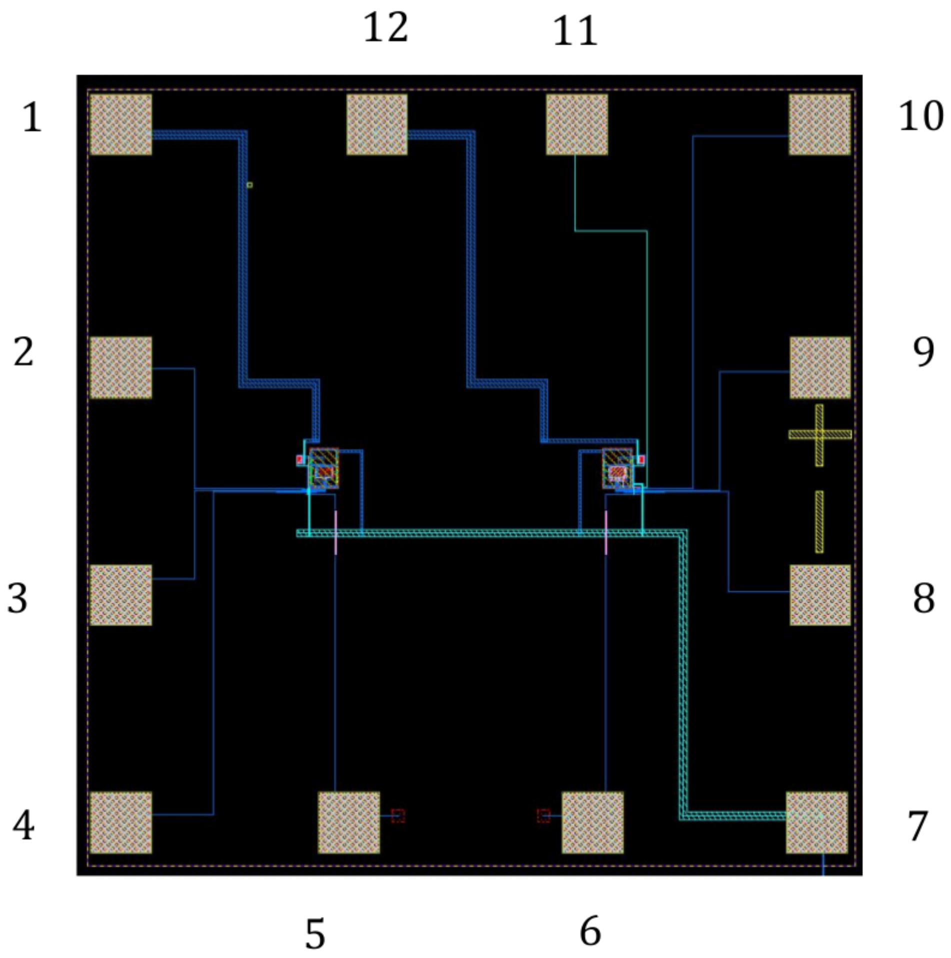


Figure 3.26: Pin-out of the first flavour chip.

3.3.2 Flavour 2 Pinout

Here are summarized the chip pin-out, along with fig.3.27 for the first flavour option:

- 1 - **VDD** supposed at 3.3V;
- 2 - Sensor control gate;
- 3 - Tunneling Gate;
- 4 - Deep NWell;
- 5 - Metal plate on the sensor, to be externally biased;

- 6 - Vref-out, output of the 3-diode voltage divider from VDD to 2/3 VDD;
- 7 - **GND** - Antenna Bottom (if connected);
- 8 - Antenna top - RF out (if connected);
- 9 - RF out signal at 400 MHz via Transmitter;
- 10 - **Vin,** that enters into the Sloper, output of the Level Shifter;
- 11 - not connected;
- 12 - **VCO/64**, output of the Divider;

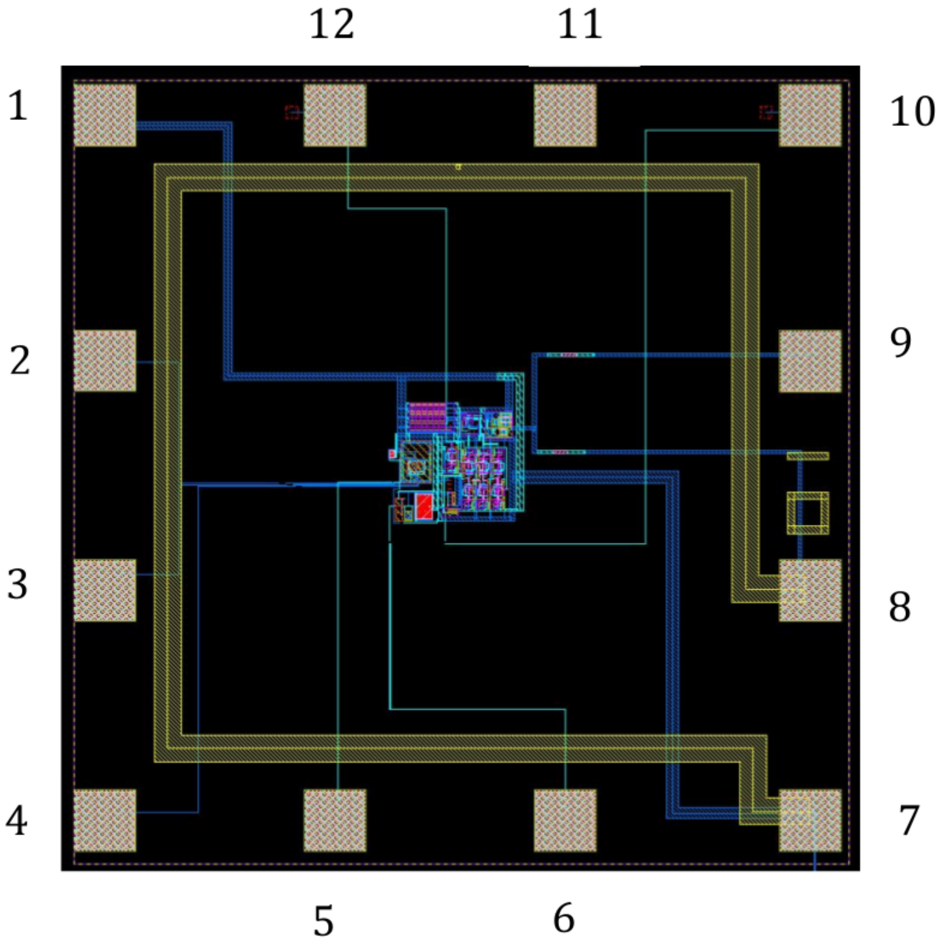


Figure 3.27: Pin-out of the second flavour chip.

Chapter 4

Amplifier Design

In this chapter is presented one of the fundamental components of our chip, the pre-amplifier for the input signal. The importance of this element lies on the fact that it operates the first and most important investigation on the input signal. In fact, the study of the electrical propagation of signals within the circuit and of the stability of the pre-amplifier are essential parameters in the optimization of functionalities of our design and in how our requirement might be fulfilled.

In more detail, using a commercial component (such as INA114 amplifier used in tests) will increase the dimension of the entire circuit over the allowed dimension compatible to in-body applications. Moreover, commercial components are mainly designed for general purpose applications, i.e. not really suitable to a specific task.

Also, the gain [10]of commercial components is too low (G=1.000 for INA114[11], while we need to amplify microvolt signals in a range of few volts, i.e. a factor 1.000.000) as well as the common mode rejection ratio, making the EMG signal overwhelmed by the common-mode signal. As it will be described below, using a 130 nm technology we can increase the frequency of the data acquisition, by exploiting Ultra-Wide-Band transmission.

The pre-amplifier design is an advanced step with respect to other parts of the presented chip and represents an upgrade in the new direction of scaling the entire detector from TowerJazz 180nm CMOS technology to UMC 130nm technology. For clarification regarding schematic and layout design (presented in sections 4.3 and 4.2) see appendix A.

4.1 Goals

4.1.1 Amplification

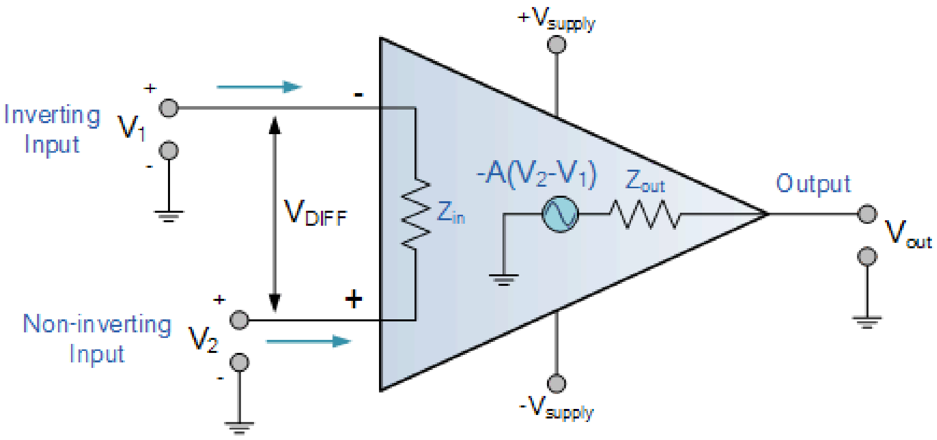


Figure 4.1: Conceptual circuital scheme of an operational amplifier.

A general operational amplifier (or *Op-Amp*) is a device with three terminals: two high impedance inputs (V_1 and V_2) and a low impedance output.

The output[12] is the difference between the two input signals multiplied by a value **A**, called *Amplifier Gain*. An ideal operational amplifier has a:

- **Very high (infinite) amplification factor:** real values range from about 20.000 to 200.000 of A;
- **Infinite input impedance:** in an ideal op-amp no current enters the amplifier, but in real ones there is an input leakage of the order of [pA-mA];
- **Zero output impedance:** an ideal op-amp act as a perfect voltage generator, while real amplifier output resistance should be as high as 20 kΩ;

The voltage gain should be expressed as:

$$A = \frac{v_{OUT}}{v_{IN}} \tag{4.1}$$

or, in decibels:

$$A = 20log\frac{v_{OUT}}{v_{IN}} \tag{4.2}$$

We should then adapt our gain, and therefore the order of magnitude of the V_{OUT}, by acting on the output adding different resistances (or a trimmer) to select different amplification factor.

For example, the INA114 amplifier used in test in chapter 2 have a Gain equation of:

$$A = 1 + \frac{50k\Omega}{R_G} \tag{4.3}$$

where the 50kΩ factor is temperature dependant and R_G is an output trimmer.

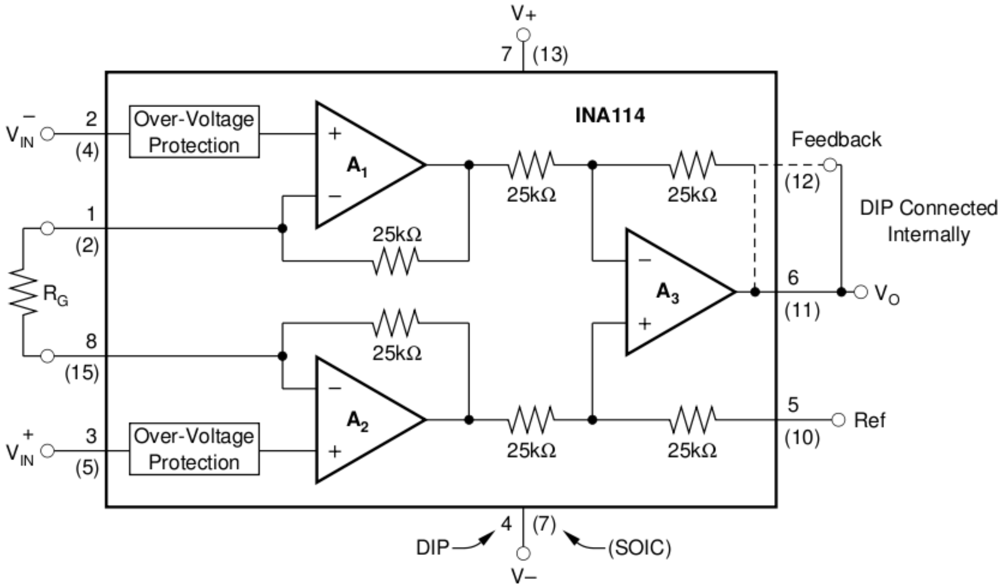


Figure 4.2: Circuital scheme of the commercial INA114 operational amplifier.

4.1.2 Common Mode signal rejection

Unfortunately, the output voltage of a real amplifier contains components in addition to a scaled replica of the input voltage:

$$V_{OUT} = A * V_{in} + components = A * (V_1 - V_2) + components \tag{4.4}$$

In particular[13], a real amplifier also respond to the signal that is in common to both inputs, called [14] the *common-mode input voltage* v_{ic}, defined as:

$$v_{ic} = \frac{v_1 + v_2}{2} \tag{4.5}$$

The common-mode input signal is amplified by the common-mode gain A_{cm}, and the output voltage is therefore:

$$v_{OUT} = A(v_1 - v_2) + A_{cm}\left(\frac{v_1 + v_2}{2}\right) \tag{4.6}$$

This equation should be expressed in terms of *CMRR*, or *Common-Mode Rejection Ratio*:

$$CMRR = \frac{A}{A_{cm}} \tag{4.7}$$

as:

$$v_{OUT} = A\left[v_{in} + \frac{v_{ic}}{CMRR}\right] \tag{4.8}$$

the common mode signal in EMG study is obviously[15] overwhelming in respect of the differential input signal v_{in}: the have a high common mode rejection ratio is therefore a main goal in designing the amplifier.

4.1.3 Power dissipation

The power dissipation of an operational amplifier in not easy to describe; many effect come at different voltage or frequency values, and a direct theoretical approach is then deterred.

We should anyway consider that a good description of how the dissipated power vary in respect of important parameters of the used transistors (and the entire amplifier as well) is:

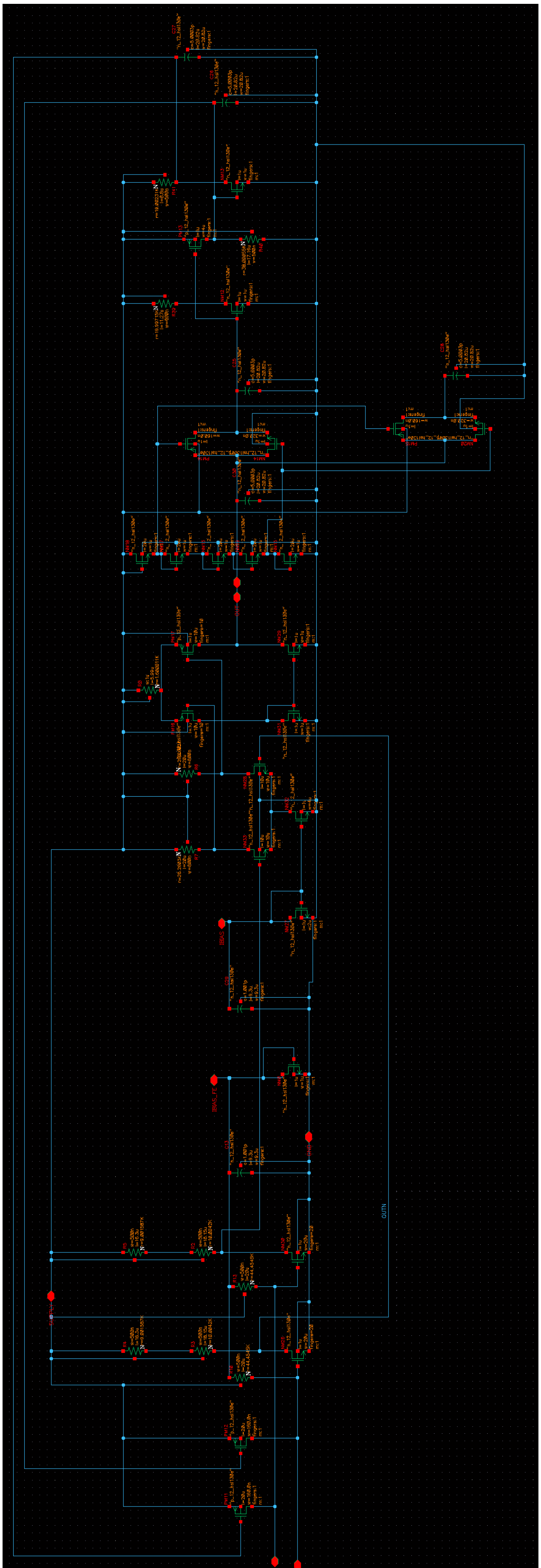
$$P \simeq C\ \nu\ V^2 \tag{4.9}$$

where **C** is the entire *Capacitive Load* to the circuit, ν the working frequency and **V** the voltage applied to the transistors. Using 130 nm technology node permits to lower the applied voltage from 3.3 V to 1.2 V, dropping the dissipated power by 7.6 times and with a minor decrease in terms of applied load.

The total dissipated power, keeping the frequency constant, is reduced by a factor $\sim$10. We should then keep the dissipated power constant, increasing by 10 times the working frequency, and making feasible the scaling from 403 MHz (working frequency of the radiation detector) to $\sim$ 4 GHz, and allowing the use of Ultra Wide Band technology.

4.2 Circuit diagram

The amplifier is presented in figure 4.3;


IBIAS
IBIAS_FE
GND
OUTN

4.2.1 Main components

Resistances and capacitors

As shown in figures 4.4 and 4.5, both resistances and capacitors have three terminals, instead of two: the third terminal (the middle one) is an Isolation terminal, and is a carefulness in order to avoid parasitic effects.

- Resistances needs to connected to V_{dd};
- Capacitors needs to be connected to Grounds;

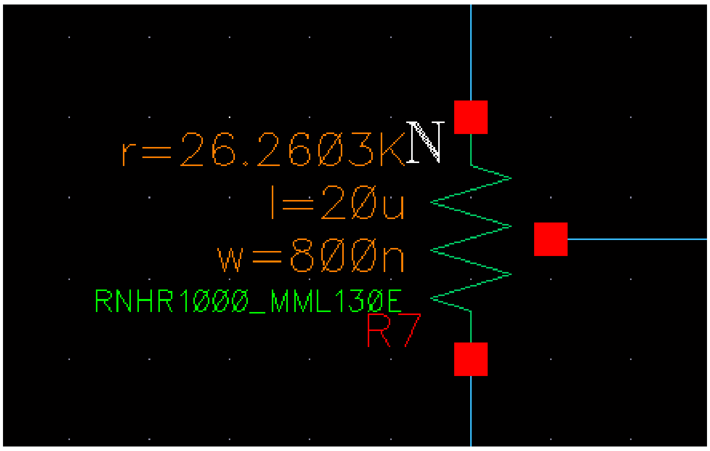


Figure 4.4: Three terminal resistance, used in the design of UMC 130 preamplifier; the third terminal is needed to avoid parasitic effects and improve the insulation of the component.

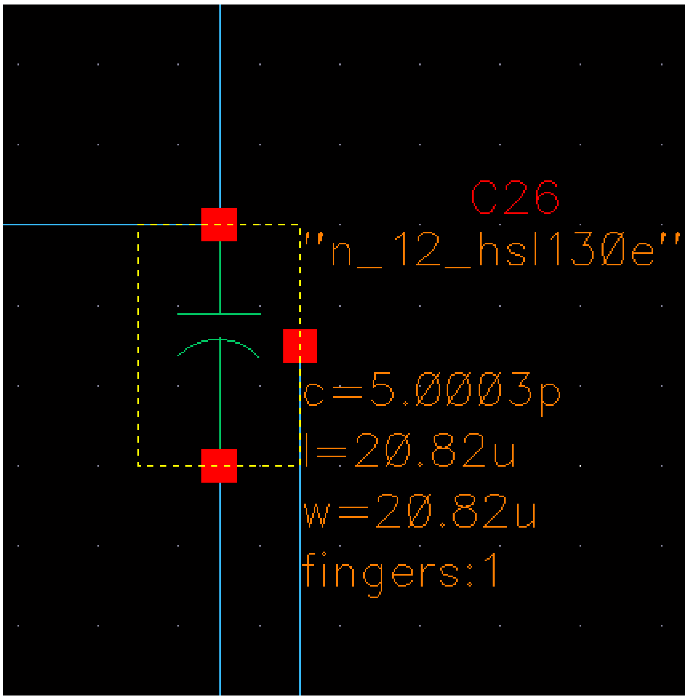


Figure 4.5: Three terminal capacitor, used in the design of UMC 130 pre-amplifier; the third terminal is needed to avoid parasitic effects and improve the insulation of the component.

Current Mirrors

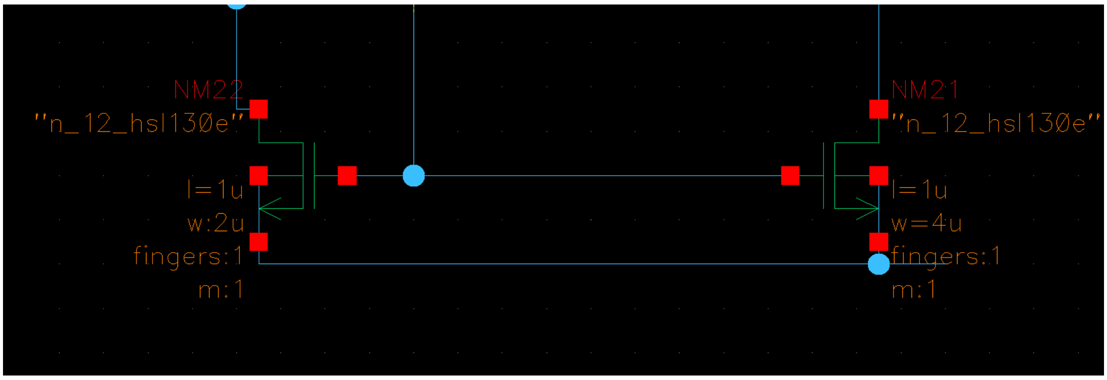


Figure 4.6: A current mirror, composed by two Nmos, leads to a great improvement in terms of stability of the currents.

The disposition presented in figure 4.6, called "*Current Mirror*", leads to and improved (more stable) drain current, by reading a current entering in a node and mirroring the current (like an unitary gain amplifier) to another node.

4.3 Layout diagram

The effective physical layout is shown in figure 4.7. The squared part in the right is the capacitor, and is clearly the bulkiest part of the design. While technology should be scaled in order to diminish area occupation of mos and resistances, the capacitance of a capacitor is tightly coupled with its dimensions; decreasing the capacitor area leads to a decrease in terms of capacitance.

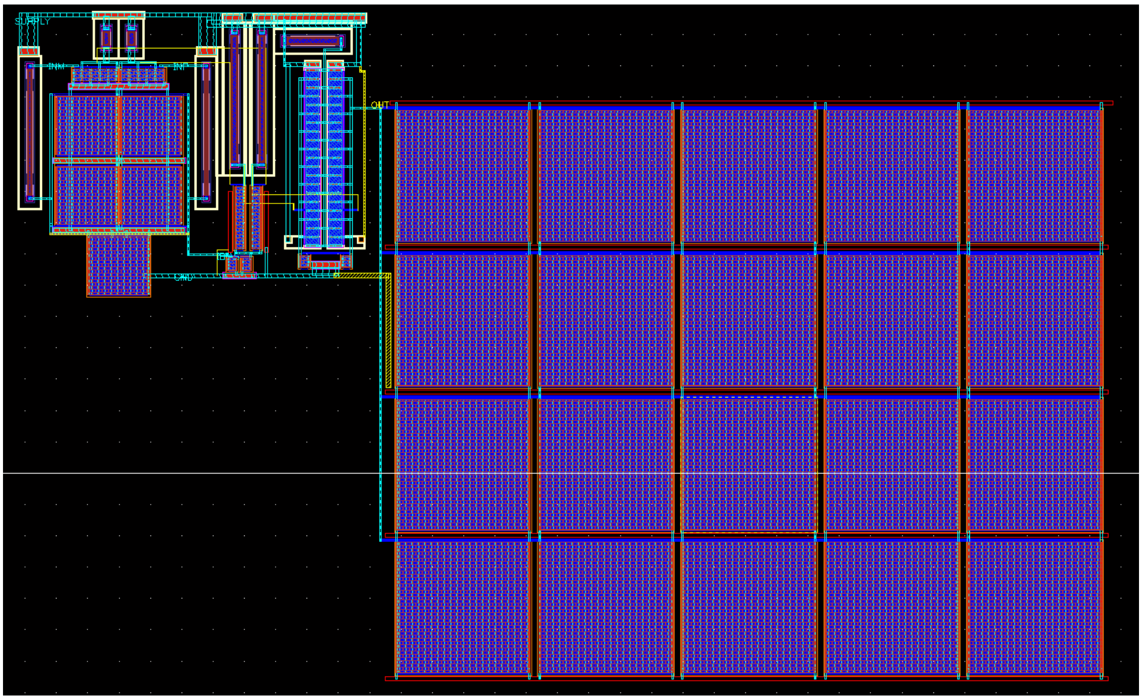


Figure 4.7: Total layout of the pre-amplifier prototype in UMC 130 nm technology.

In order to better figure the effective layout composition of the proposed prototype, in figure 4.8 is presented the upper-left part of the entire design; most of the area is occupied by resistors and capacitors, while transistors occupy (thanks to scaling) just a small portion of the entire design.

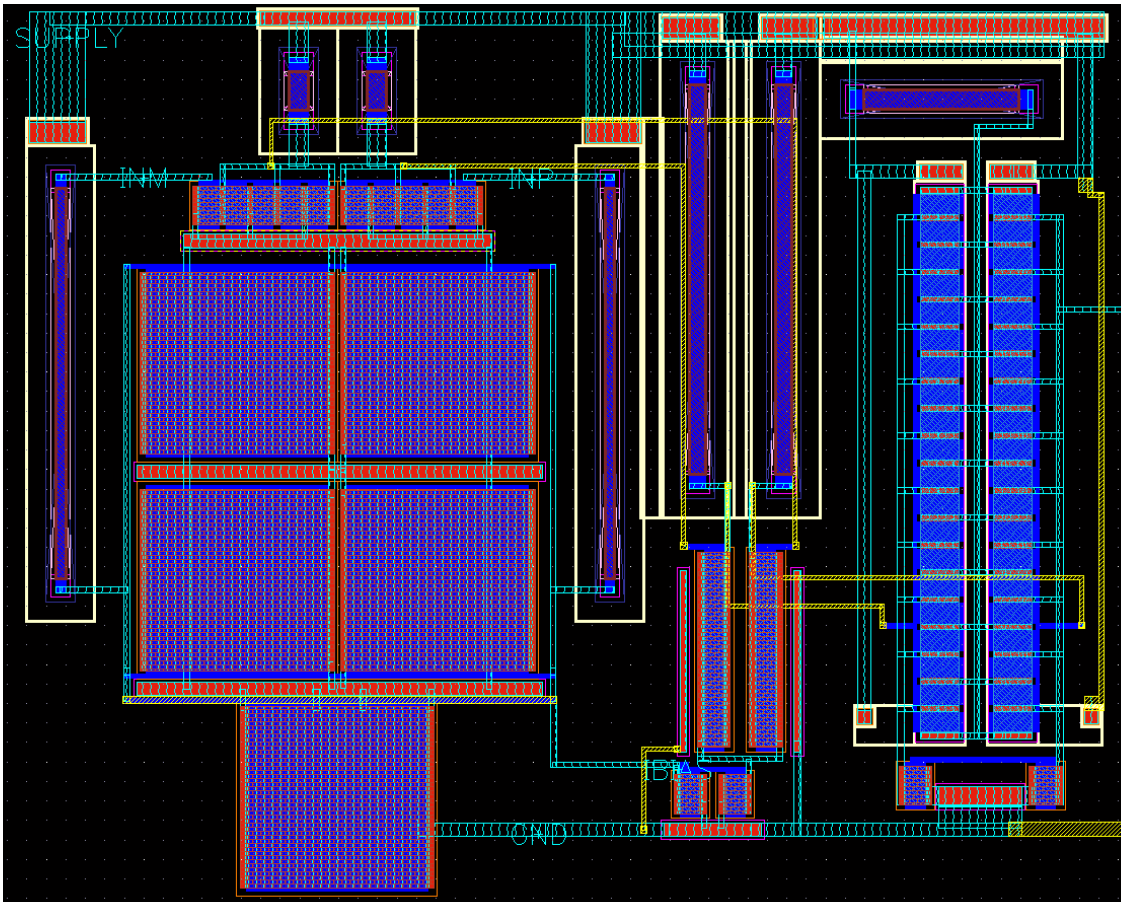


Figure 4.8: Partial layout of the pre-amplifier prototype in UMC 130 nm technology, focusing on mos and resistances.

Chapter 5

Conclusions

The present thesis is a summary of the work in design, research and development of microelectronic technology applications for sensor reading and signal processing, in collaboration with the Istituto Nazionale di Fisica Nucleare (INFN), the Istituto Italiano di Tecnologia (IIT) of Torino, the Politecnico in Torino and the Rutherford Appleton Laboratory (RAL), UK. Research focus are the miniaturization of the components, in order to create low-cost and portable devices, power dissipation reduction, improvement of signal over noise ratio and efficient transmission of the data via wireless digital protocol, exploiting a Impulse-Radio Ultra Wide Band technology.

The proposed device, a Sigma-Delta like modulator, has been described in detail, including circuital schemes and physical design layout of every main functional element that composes the system.

Signals studied during the device development have been presented (Electromyographic signals and Dosimetric measurement of radiation) and methods to analyse both types of signal have been proposed.

The proposed design for data acquisition system has been tested using commercial technology in order to establish the feasibility of the idea. The circuits were eventually fabricated as integrated circuit, using TowerJazz 180 nm technology; after many successful test realized in electronic laboratory at INFN, Bologna in order to tune and improve the original design, the project have been upgraded by modifying the transmission protocols in order to use a high-frequency carrier wave (some GHz using Ultra Wide Band).

My work focused in upgrading the system: scaling from TowerJazz 180 nm to UMC 130 nm technology. This upgrade allows a significant containment of costs and energy consumption while permitting a higher frequency of the carrier without increasing power dissipation, thanks to the diminishing of both supply power from 3.3 to 1.2 V and capacitive load on circuit. By following a deepened study of the entire circuit, I designed and tested a new component in 130 nm technology, the pre-amplifier that interfaces EMG electrodes with the Sigma-Delta Modulator; otherwise, signals from the electrodes would have been not measurable using the modulator alone because of the low wave amplitude of the EMG signal(order of 10-100 μV).

Results obtained thanks to this research put the foundations for a further scaling of the entire modulator design in the new UMC 130 nm technology, in order to broaden the benefits to the entire system.

Appendix A

Cadence Virtuoso

Cadence Design System is an ECAD (*Electronic Computer-Aided Design*) software suite used in integrated circuits design. The platform used to elaborate schematic circuitry, layout designs and test the parameters of our composition is part of this suite, called Virtuoso; Virtuoso comprise the possibility of testing the designed hardware, verifying eventual logic or conceptual errors of the physical chip before the fabrication itself. In between many fundamental features of the suite, an function essential in design microelectronics has been implemented: the possibility of parasitic effect extraction.

Design follows three main stages:

- **Schematic phase:** the schematic phase is the creation of the logic circuit prototype, i.e. the implementation of the required features at symbolic level;
- **Layout phase:** is the creation of a physical implementation of the Schematic concept by superimposing layers of different materials, such as Polysilicon, Conductive metals, etc. and following the geometries required for the creation of every component (e.g. the placement of the gate in the correct place and with correct sizes in a MOS transistor);
- **Simulations and extractions:** Schematic and Layout design are compared, in order to link every symbolic element (e.g. a specific transistor or capacitor) to an area of the layout that implement the corresponding function. Parameters of the layout geometry are evaluated ad resistance and capacitances related to the materials geometry (such as the resistance of a conductor metal trail) and information are stored for better simulations.

Test operations use many different tools included in Cadence suite, but three of them are of main importance:

- **Assura DRC (Design Rule Checker)**: this tool analyse the layout project, verifying that the Design Rules (construction and operational parameters) are followed, e.g. the distance between two metal trail to avoid parasitic effects. Assura did not forecast on the functionality of the design, and an eventual project that pass DRC test should not have the required features.
- **LVS (Layout Versus Schematic):** LVS is a secondary ECAD that verifies if the created Layout match the required operations detailed into the schematic design.

Schematic

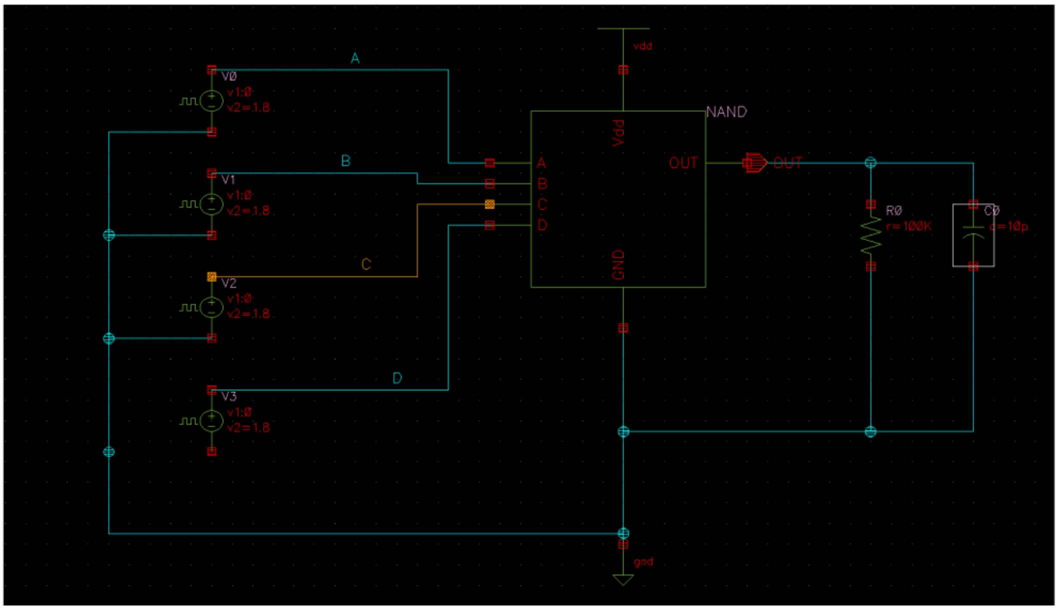


Figure A.1: Schematic representation of a 4-terminal NAND gate, as well a RC parallel circuit for test reasons.

Layout

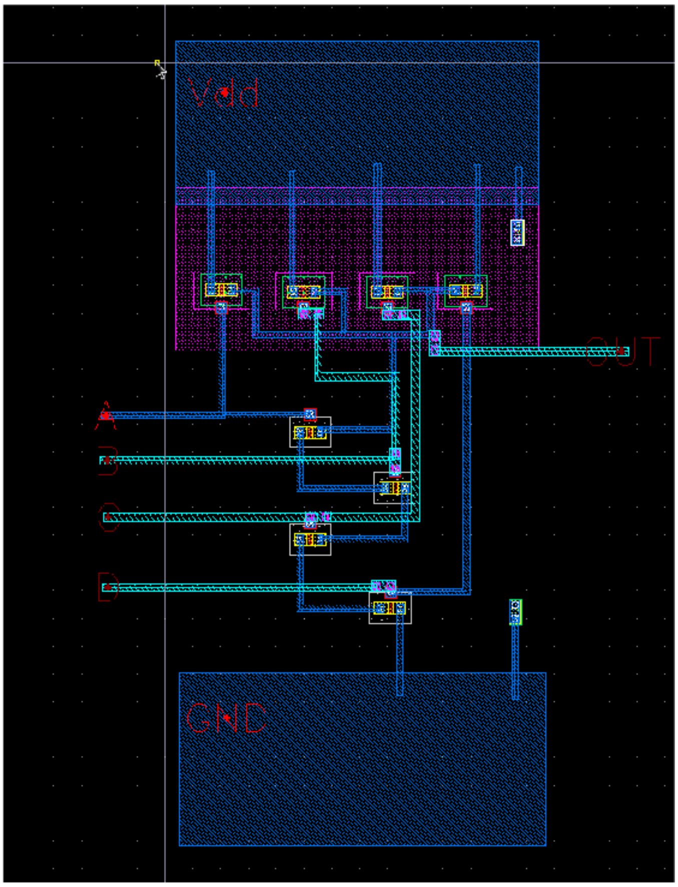


Figure A.2: Layout of a 4-terminal NAND gate, designed in TowerJazz 180nm technology.

Parasitic effects extraction

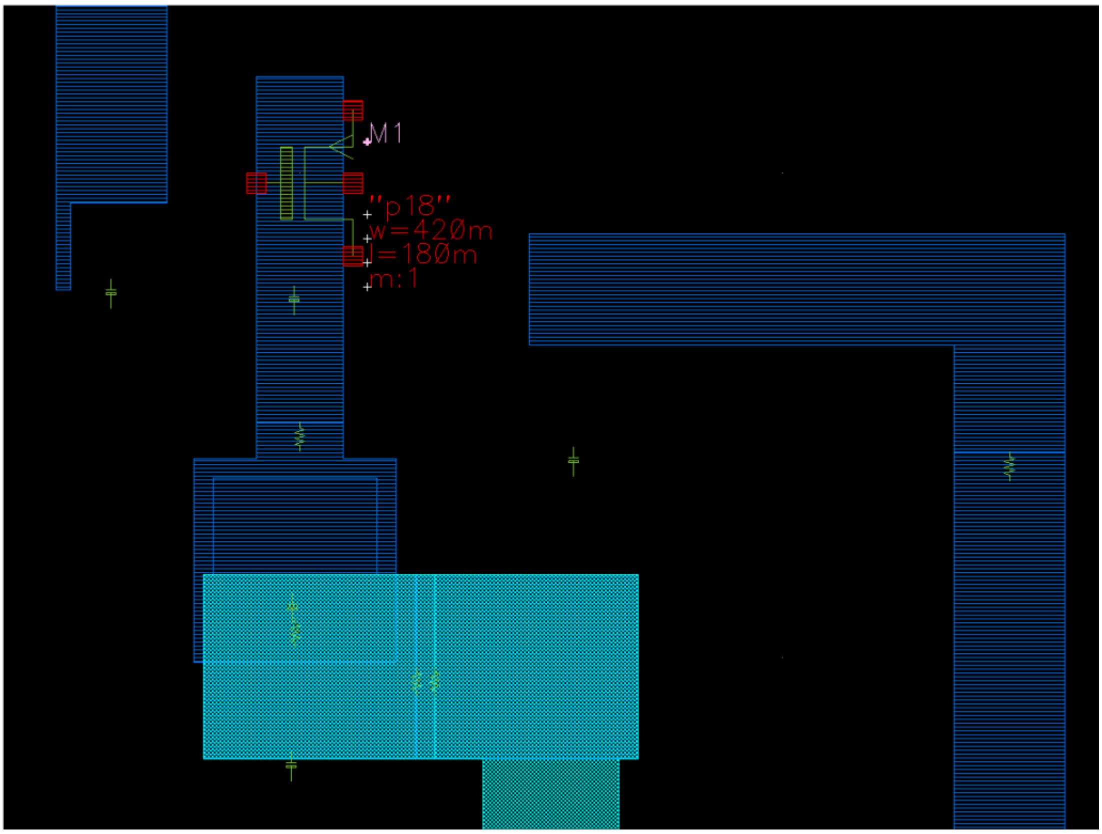


Figure A.3: Parasitic effects extracted from layout of the NAND gate. It is possible to see capacitances and resistances of the construction geometries.

Simulation using schematic circuit is only approximately descriptive of the designed circuit behaviour; using Parasitic extraction on layout design and therefore obtaining a more precise description of the designed component, leads to the possibility (non before having linked schematic and layout using LVS function) of achieving more faithful results in schematic design simulation (as seen in section 3.2.2).

Abbreviations

ADC	Analog-to-Digital Converter
AER	Address-Event Representation
ARV	Average Rectified Value
ATC	Average Threshold Crossing
CMOS	Complementary Metal Oxide Semiconductor
CMRR	Common Mode Rejection Ratio
DAQ	Data Acquisition System
DRC	Design Rule Checker
ECG	Electrocardiogram
EEG	Electroencephalogram
EL	Electrode
EMG	Electromyography
GND	Ground
HPF	High-Pass Filter
IR-UWB	Impulse Radio - UWB
LVS	Layout Versus Schematic
MVC	Maximum Voluntary Contraction
OpAmp	Operational Amplifier
PPM	Pulse Position Modulation
PWR	Power (source)
REF	Reference
RF	Radio Frequency
RFCMOS	Radio Frequency CMOS
RX	Receiver
S-OOK	Synchronized On/Off Keying
SNR	Signal-Noise Ratio
TX	Transmitter
UWB	Ultra Wide Band
VCO	Voltage Controlled Oscillator

Bibliography

[1] Mark Halaki and Karen Ginn, *Normalization of EMG Signals: To Normalize or Not to Normalize and What to Normalize to?*

[2] Donald A. Neumann and Mosby Elsevier, *Kinesiology of the Musculoskeletal System, Foundations for Rehabilitation* Second Edition, 2010

[3] De Luca, Carlo J., *The Use of Surface Electromyography in Biomechanics* . Journal of applied biomechanics,1997, **13**, 135-163, Human Kinetics publisher, Inc.

[4] F.Fuschino, A.Gabrielli, G.Baldazzi, R.Campana, M.Crepaldi, D.Demarchi, G.Villani, *A Wireless transmission low-power radiation sensor for in-vivo dosimetry*

[5] Ian Oppermann, Matti Hämäläinen Editor, Jari Iinatti *UWB: Theory and Application* Wiley, 2004

[6] Paolo Motto Ros, Marco Paleari, Nicolò Celadon, Alessandro Sanginario, Alberto Bonanno, Marco Crepaldi, Member, Paolo Ariano and Danilo Demarchi, *A Wireless Address-Event Representation System for ATC-Based Multi-Channel Force Wireless Transmission*

[7] S.Bastianini, M.Crepaldi, G.D'Amen, D.Demarchi, A.Gabrielli, P.Motto Ros, G. Zoccoli, *Low power wireless ultra-wide band transmission of bio signals*

[8] Marco Crepaldi, Marco Paleari, Alberto Bonanno, Alessandro Sanginario, Paolo Ariano, Duc Hoa Tran, Danilo Demarchi, *A Quasi-Digital Radio System for Muscle Force Transmission Based on Event-Driven IR-UWB*

[9] S.Bastianini, M.Crepaldi, D.Demarchi, A.Gabrielli, M.Lolli, A.Margotti, G.Villani, Z.Zhang, G.Zoccoli, *A 0.18 μm CMOS*

low-power radiation sensor for asynchronous event-driven UWB wireless transmission, Nuclear instruments and methods in physics research A 730 (2013) 105-110

[10] H. W. Smit, K. Verton, C. A. Grimbergen, *A Low-Cost Multichannel Preamplifier for Physiological Signals* IEEE Transaction on Biomedical Engeneering, VOL. BME-34, NO. 4, April 1987

[11] *INA114 Precision Instrumentation Amplifier Datasheet*

[12] J.Millman, A.Grabel, *Microelectronics* , Seventh edition, McGraw Hill Higher Education

[13] Richard C.Jaeger, Travis N.Blalock *Microelectronics Circuit Design* Fourth Edition, 2011

[14] Daniel Dzahini, Hamid Ghazlane , *Auto-zero stabilized CMOS amplifiers for very low voltage or current offset*

[15] Yuhwai Tseng, Yingchieh Ho, Shuoting Kao,and Chauchin Su, *A 0.09 μW Low Power Front-End Biopotential Amplifier for Biosignal Recording* IEEE Transactions on biomedical circuits and systems ,VOL.6,NO.5, October 2012