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TESI DI LAUREA

in

Sistemi a Portante Ottica

CONTROLLO OTTICO AUTOMATIZZATO DI CIRCUITI FOTONICI INTEGRATI: PROGETTAZIONE, REALIZZAZIONE E VALUTAZIONE

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Sessione III

Homo faber ipsius fortunae

Appius Claudius Caecus

Abstract

Nei prossimi anni le reti di telecomunicazioni dovranno affrontare un drastico aumento del traffico dati. L'attuale trasmissione su fibra ottica, con commutazione a pacchetto effettuata tramite switch elettronici, non potrà sopperire a tale incremento. Una soluzione promettente è la commutazione di pacchetto ottica, in cui la funzione di instradamento è svolta da circuiti fotonici integrati (Photonic Integrated Circuits, PICs). Le funzionalità dei PIC sono notevolmente aumentate negli ultimi anni. Tuttavia, la complessità e la lentezza della verifica delle funzionalità ottiche ne limita lo sviluppo: sono quindi necessarie procedure di controllo affidabili, veloci ed economiche.
Nel progetto di tesi che viene di seguito presentato, è stata ideata, realizzata e valutata una procedura innovativa di verifica automatizzata delle funzionalità ottiche dei circuiti fotonici integrati. Partendo dall'analisi delle criticità delle procedure attuali, sono state individuate le seguenti specifiche da realizzare come obiettivo: automatizzazione, flessibilità, affidabilità, semplificazione dell'allineamento e velocizzazione delle operazioni di misura. Il banco di misura si compone di una griglia di microlenti, una matrice di fotodiodi e due programmi di controllo, acquisizione e analisi dei dati. I componenti sono stati studiati e calibrati, attraverso numerose prove che ne hanno determinato le caratteristiche. I due programmi sono stati sviluppati allo scopo di controllare l'intero banco di misura, dal PIC, al ricevitore, effettuando infine un'analisi dei dati. L'affidabilità del nuovo banco di prova è stata verificata con successo con riferimento ad un prototipo di PIC a 16 porte, del quale sono state analizzate: la posizione dei fasci, le curve corrente-potenza, la distribuzione spazio-temporale della potenza e la continuità ottica da porta a porta. Inoltre, sono state analizzate la precisione e la complessità delle operazioni di allineamento, dimostrando affidabilità e flessibilità inalterate a fronte di una drastica riduzione dei tempi di effettuazione delle misure.

Contents

Chapter 1

Introduction

Since the beginning of the new millennium, the telecommunications have faced one of the most significant challenges [1]. The Internet and the social networks have changed the technological trends faster than ever [2]. The network services have drastically increased their subscribers and coverage. As shown in Figure 1.1, the machine-to-machine (M2M) applications, high definition video playing [4] and wi-fi spots have dealt with an impressive growth in demand, providing greater data traffic than ever before. Every subscriber wants to be connected everywhere: therefore, large coverage, high mobility and on-line connectivity have become ubiquitous requirements for the wireless networks.
The futurable services and paradigms, e.g. the Internet of Things [5], are stressing these requirements: data traffic models provide an increasing bandwidth demand during the next decade, with an approximate doubling every year [6], [7].

The integration of optical fibre and wireless networks have become an essential technology for the provision of access to broadband wireless links [8], [9]. Its uses include last-mile solutions, improvement of radio coverage and capacity and backhaul of current and next-generation wireless networks.

As long as the optical fiber medium is future-proof, since its current bit

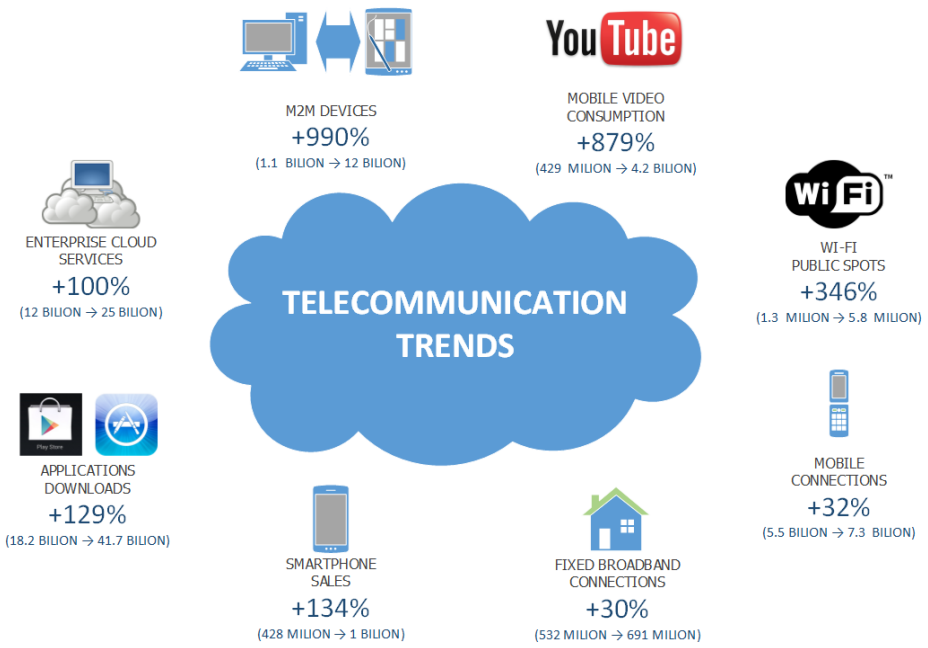


Figure 1.1. Technological trends between the 2011 and 2015: percentage growth and users (users in 2011 → users in 2015) [3].

rate is conservatively estimated to be $1Tb/s$ over a single fiber and with thousand kilometres between regenerators. As a consequence of this scenario, the pressure on transport network nodes is increasing [10], [11]. Indeed, they perform the routing and switching functions in the electrical domain: current routers redirect each optical channel, i.e. wavelength, to an ingress line card where the optical signal is converted to the electrical domain. Once the control information, as destination and priority, is retrieved, the data is processed and up converted again to the optical domain.

The transformation to the electrical domain in the intermediate nodes involves great limitations. The electronics speed is limited to $40Gb/s$: consequently, the speed limitation generates a bottleneck incapable of absorbing the traffic throughput coming from the optical fibers. Additionally, the processing time in the electrical domain adds extra latency to the end-to-end communication. On the other hand, the optics-electronics-optics (O-E-O) conversion equipment augments decisively the intermediate node cost [12],

[13].

A promising solution is represented by all-optical networks: the intermediate O-E-O transformations are avoided and the signals remain in the optical domain from end-to-end.
Techniques providing optical circuit-switched network are the only solutions deployed [14]. Although, another technology is under research: the optical packet switching network [15]. It represents a very promising solution for next generation all-optical networks [16]: such a network would be able to offer virtual circuit or datagram services [17], [18], much like what is provided by IP networks, using photonic integrated switches [19].

The COBRA Research Institute of Eindhoven University of Technology has recently set the world-record for routing 320 Gb/s in a multi-stage optical integrated switch [20]. The complexity of state-of-the-art integrated chips is keeping growing: the number of components per chip reaches now hundreds [21], [22]. Nevertheless, the fast photonic integrated switch technology is not yet fully competitive with the electronic counterpart [18]. One of the greater limitations is the test complexity, which increases the analysis time and cost.

Since the '70 the automated test methods for electronic integrated circuits have been demonstrated to be solid and standardized procedures [23]. These reliable techniques have been exploited to provide hundreds of connections at one go.
Photonic integrated chips (PICs) will be competitive with electronic technology if a fast and reliable test procedure is developed. Photonic integrated switch facets integrity, as well as electrical connections quality after bonding, have been shown by visual inspection and automated electrical tests [24]. However, the optical test of these sophisticated chips is still very slow and complex.

In this master thesis project an automated test-bed for reliable optical assessment is conceived and provided, in order to hasten the photonic integrated circuit optical test. The thesis framework is reported below:

1. the current optical test problems and the project requirements are analysed in chapter 2;

2. the selection and the test of the components and the assembly of the test-bed is described in chapter 3;

3. the verification of the test-bed optical test capabilities, performed by flip chip bounded photonic integrated switch trials is reported in chapter 4;

4. the critical problems observed during the assembly and assessment are discussed and solutions are proposed in chapter 5;

5. finally, the conclusion and the outlook are shown in chapter 6.

Chapter 2

Concept

The photonic integrated switch optical tests, which constitute the core of this master thesis work, are based on beam reception by fiber lenses. These are placed and aligned toward the waveguides. Therefore, the beams are collected and the data are processed by the receiver.
The critical problems are represented by the setup time and procedure complexity. The alignment requires strict placement tolerances due to the distance between the devices, which is $10\mu m$ [25]. Consequently, all the device placements must be performed by microscope visual inspection in order to avoid the optical lens collision into the photonic waveguide. Moreover, the alignment precision is $\simeq 100nm$: this requires that all the fiber lenses are placed one at a time and the position must be corrected every hour in order to balance the chip thermal drift. Therefore, the test-bed set-up time depends on the number of fiber lenses positioned.
The other time-consuming step is the photonic integrated switch control because the test inputs are provided by manual input due to the lack of automated test controller.
The test setup time, for the 16×16 ports PIC, is conservatively estimated in 4 months.

The envisaged test-bed should reduce the time-consumption related to

the setup and to the trial stages. The first step should decrease the time necessary for obtaining the photonic integrated circuit alignment toward the optical receiver and, to this purpose, it is desirable to relax the positioning precision. Moreover, it should simplify the placement complexity, avoiding the microscope visual inspection and introducing more practical feedback tools for the operator.
Furthermore, the trial step must also be time optimized: the test-bed should be able to perform multiple waveguide assessments in the same test and the operator intervention should be limited due to the increase of the test-bed automation.
Finally, the test-bed should be as layout independent as possible, reducing the test-bed changes necessary to test different waveguides and PICs, achieving lower setup time.
These concepts drive to the envisaged automated optical test, which must satisfy few fundamental requirements to make it valuable for effective optical test of sophisticate photonic integrated circuits. The specifications are following:

1. relaxed precision and still reliable alignment;
2. multiple port assessments at the same time;
3. independence from the chip layout;
4. real-time alignment and measurements;
5. high automation via software control;

Chapter 3

Test-bed setup and components

In this chapter the selection of the components for the test-bed is illustrated.
Each device is studied in 3 stages: firstly, its requirements are defined, secondly, a comparison between different choices is made and, finally, the component performances are analysed with proper test-bed.
The methodology used is a bottom up approach: the project requirements are analysed starting from the photonic integrated circuit and its control, then the best available solution to carry the optic beam toward a theoretical optical receiver is studied. Subsequently the best optical receiver is defined and, finally, the data process and test control algorithms are programmed and optimized.

3.1 Photonic integrated switch

In this section are defined the PICs suitable to be verified with this test-bed and the prototype is used during the assessment.

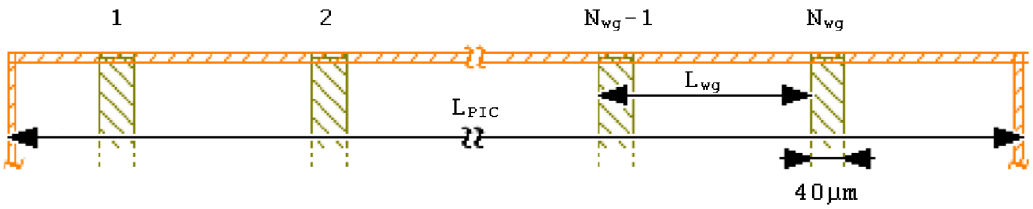


Figure 3.1. Photonic integrated circuit, horizontal plane view, and mechanical parameters: $L_{PIC} \simeq N_{wg} \cdot L_{wg} = 8mm$, in green the waveguides and in orange the edges.

3.1.1 Mechanical and optical requirements

This optical test-bed is designed to inspect any multiport photonic integrated switch, following with layout shown in Figure 3.1 and the characterization:

- all the ports are defined on the front facet;
- waveguide pitches (L_{wg}) same of $250\mu m$;
- number of waveguides (N_{wg}) less or equal to 32;
- $1600nm$ wavelength;
- divergent waveguides with numerical aperture (NA) on horizontal plane equal to 0.5;
- maximum estimated transmitting power $0dB_{mW}$.

3.1.2 Photonic integrated switch prototype

The PIC used during the test-bed assessment is here defined. The photonic integrated circuit is placed and bounded on the tile with flip chip bounding technique, as shown in Figure 3.2. The electrical connections between the PIC and the PCB connectors have been already tested [24]. The circuit is a 8×8 optical switch ($N_{wg} = 16$) and satisfies all the requirements at page 8.

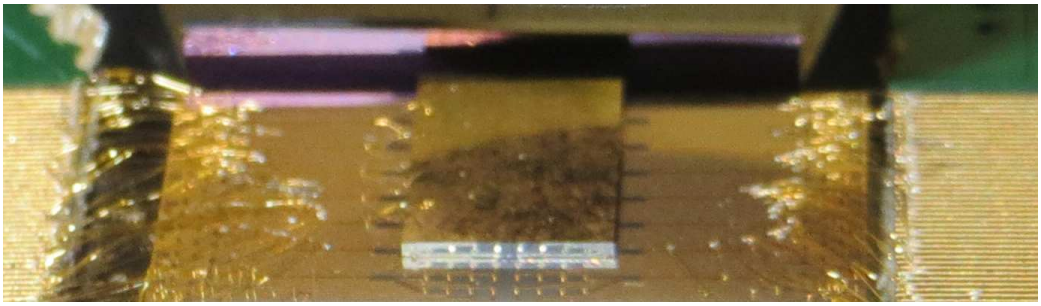


Figure 3.2. Photonic integrated switch 8×8 used during the test.

Photonic integrated switch control

The switch function is provided, in an optical integrated circuit, by a matrix of SOAs [26]: they must be univocally identified in order to control the circuit.
A SOA is classified by its index and current value. As shown in Figure 3.3, there are 96 pads, divided in 12 groups with 8 tracks each one. The index is specified by matrix notation: $index_{group}.index_{track}$. There are, at least, 2 pads per SOA while others are not connected, for instance: pad 1.1 and 1.2 are connected to the same metallization and 1.7 is not connected.

Current controller

The PIC needs an interface in order to be controlled. A specific circuit (henceforth defined as current controller) and software were designed [27].
As shown in Figure 3.4, the operator inputs the SOA indices and their currents by the software, the information are sent, through USB, toward the Arduino and this enables the output pins by means of 2 current drivers, each one can control up to 32 SOAs.
The software is provided with source code and the programming language is $C++$.

The setup is performed using a laboratory power supply: firstly a rack power supply was used, due to high current absorptions (about $6A$ in idle

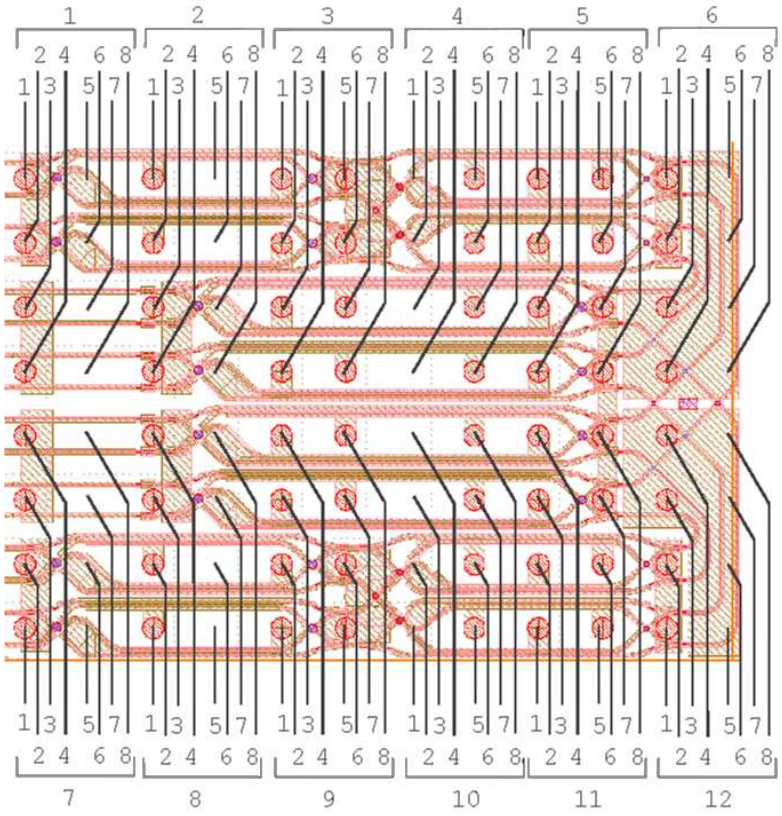
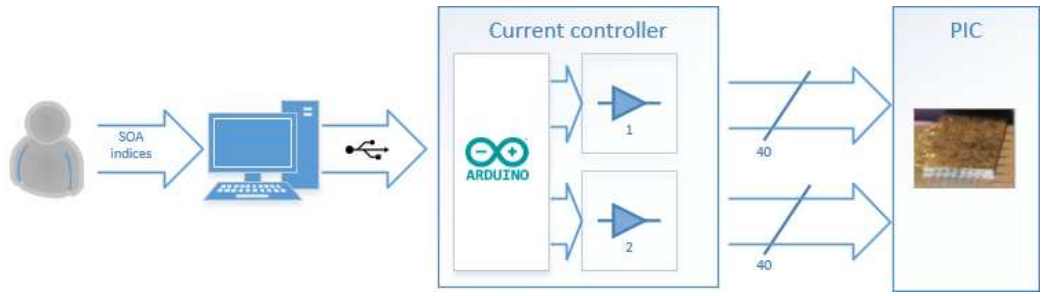
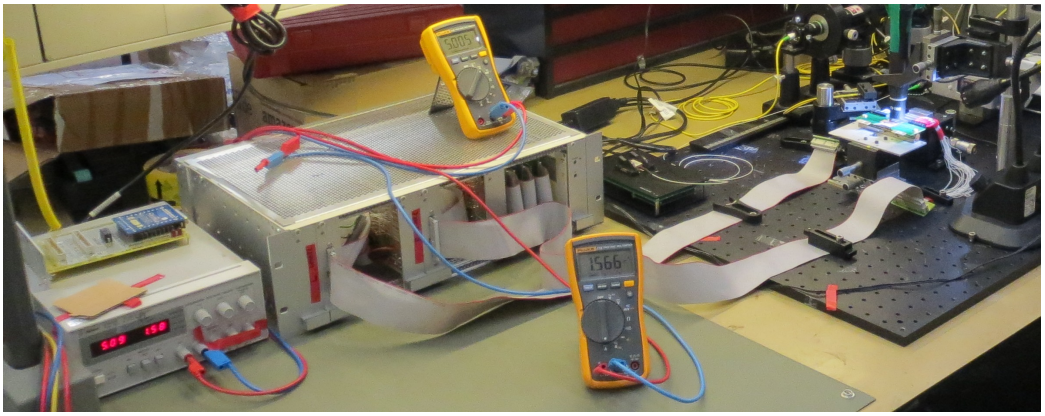


Figure 3.3. Photonic integrated switch 8×8 layout and track indices.



(a)



(b)

Figure 3.4. The current controller; block diagram (a), setup, from left to right (b), the power supply, current controller (metallic rack box at the centre), the ammeter and voltmeter, the ribbon cables (one for each driver) and the PIC on optical board.

mode) and overheating, a laboratory power supply is used instead, therefore the problems are solved.
Current absorption spikes and voltage are monitored at board supply line through ammeter and voltmeter.
The connection between the drivers and PIC requires PCB plug adapters: electrical tests are performed to check the electrical continuity and the pin mapping.

3.2 Microlens array

3.2.1 Divergent multiple beams

The photonic integrated switch is a multiple port divergent source. This implies 2 problems: power distribution decreases with distance due to divergence (the path-loss is neglected) and a mutual interference is present between the beams.

Firstly, the simplest case is taken in account: only 1 PIC waveguide is enabled and in front of it the observer is positioned.
The received power decreases with the distance [28], while in transmission it is limited, therefore it is necessary to decrease the gap in order to increase the signal strength. If the observer is an optical receiver (photodiode or camera), this means decrease the placement tolerance and enlarge the positioning time, key features of this project.

Now a second case is considered: 2 more PIC waveguides are turned on, ray tracing is used to represent the beams and rectangular aperture diffraction [28] is assumed to be negligible. As shown in Figure 3.5, the beams start to interfere at the distance D_{if}(henceforward called beam crosstalk). It can be demonstrated by trigonometry as D_{if} depends on the distance between the enabled waveguides, in the worst case they are adjacent, consequently $D_{if} = 466.5\mu m$.
The crosstalk can be reduced, even neglected, decreasing the distance between the PIC and the receiver and this introduces the same problems of the

previous case.
It is clear the trade-off between received power, crosstalk and positioning tolerance: a solution could come from collimation.

A collimated beam is defined as a beam which has all the rays parallel one to the other [29]. Regarding the previous 2 cases, as shown in Figure 3.6, the great advantages are: the collimated beams can travel for longer distances than the divergent ones and crosstalk does not depend on the distance between lens and receiver, therefore this can be placed more distant from the PIC, with relaxed precision. This solution also increases the flexibility of the test-bed: more devices could be placed between the photonic integrated circuit and the receiver to perform different tests.

3.2.2 Linear lens array

An array of lenses (hereafter called microlens array, MLA) is preferred to overcome the divergent beam trade-off.
The array features are: each lens can achieve the collimation only if it has the same axis of waveguide, all of them must be collimated at the same time, the reflection loss must be minimized and the device must be placed with relaxed tolerance. The lens array following with the constraints:

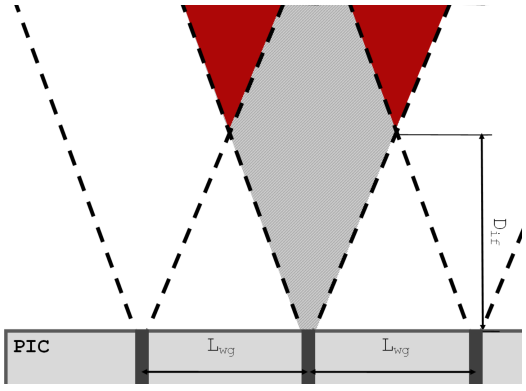


Figure 3.5. Mutual interference between 2 waveguides which emit at the same time. The 3 beams are displayed as triangles on the horizontal plane.

- lens pitches equal to L_{wg};
- array of at least 32 lenses;
- circular lenses;
- AR coating to minimize the reflection loss;
- good trade-off between focal distance and alignment tolerance.

The first parameters taken in account are the lens pitches, the number of lenses and their geometry. Besides, the Fresnel number (FN) is considered: higher values are preferred than the smaller ones, to decrease the diffraction effect on flat-top profile of lenses [30].
A *Matlab* script is written to compare the selected models, it takes as input: model code, radius of curvature (ROC), refractive index and NA. As shown in Figure 3.7, it displays and saves in a file: model, crosstalk condition fulfilment, focal distance, number of lenses and FN.

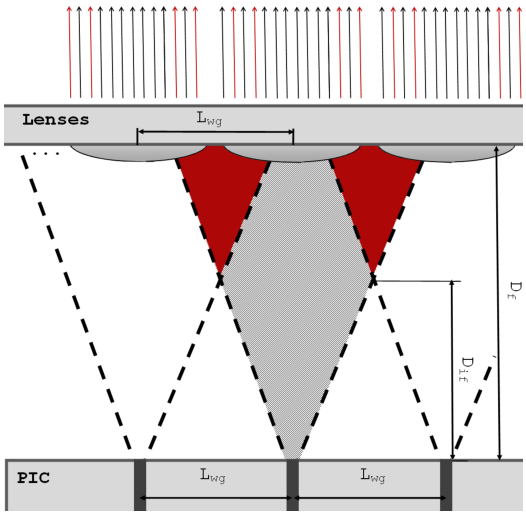


Figure 3.6. Top view of lens array collimation: the red rays are the interferences, the black ones are the useful signals and D_f denotes the lens focal distance.

Table 3.1. The MLA model at the final selection.

	Fused Silica Lenses (18-0092)	Silicon Lenses (18-00284)
Type	circular	circular
Focal distance	$744.9\mu m$	$665.9\mu m$
Pitch	$250\mu m$	$250\mu m$
Num. Lenses	48	48
AR coating	$1.25 - 1.65\mu m$	$1.2 - 10\mu m$

The final choice is, as shown in Table 3.1, between two models with shortest focal distance. The best option is the microlens array, Silicon Lenses, model 18-00284, whose mechanical layout is shown in Figure 3.8.

The small positioning distance and the size of the microlens array require a customized holder. As shown in Figure 3.9(a), the compatibility with other optical board holders and components and the high precision manufacturing led to a customized version of *HFV002 - Tapered V-Groove Fiber Holder for Multi-Axis Stages* [31] by *Thorlabs*, customized by *Equipment & Prototype Center*, TNO lab. located in Eindhoven, Figure 3.9(b).
As shown in Figure 3.9(c), web-cam microscope is used to have a visual feedback during the MLA movement and avoid collision between the components.

```
cod.     overlapping     focal distance [um]     numb. lens   FN
18-00046             Y           1099.32280       40.0         8.6
cod.     overlapping     focal distance [um]     numb. lens   FN
18-00092             Y            744.92099       56.0         13.9
cod.     overlapping     focal distance [um]     numb. lens   FN
18-00284             Y            665.85956       56.0         13.9
Maximum distance without interference = 4.665064e+02[um]
```

Figure 3.7. Microlens array available models, *Matlab* .txt output file.

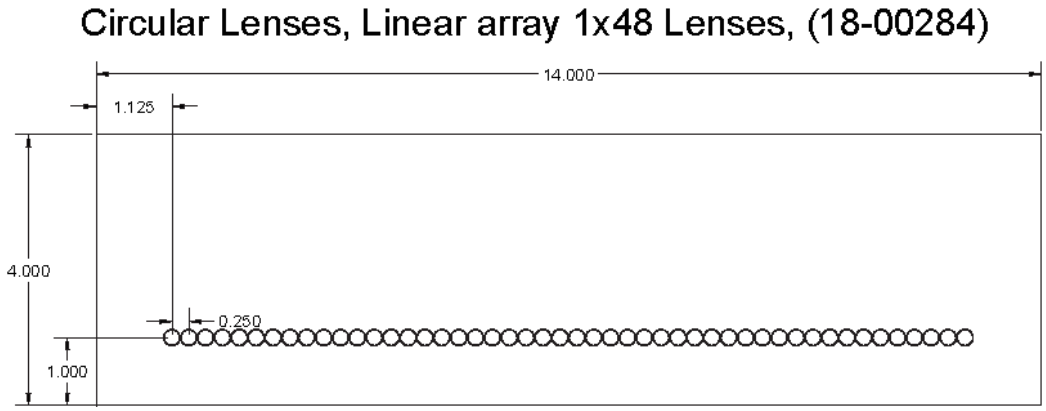
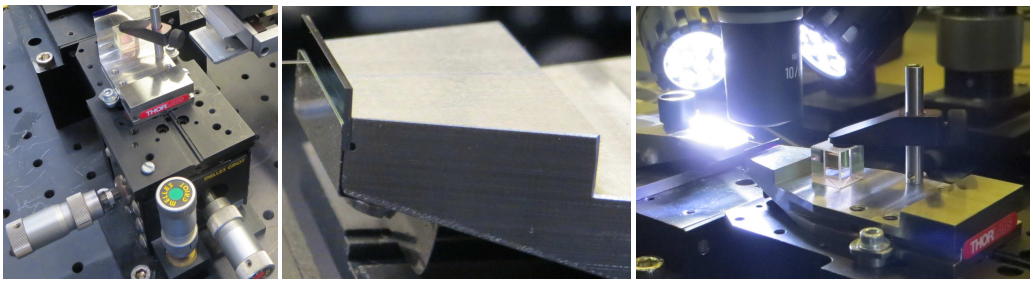


Figure 3.8. Microlens array mechanical layout, vertical view, all the dimensions are in mm. The MLA thickness is $0.5mm$.



(a) (b) (c)

Figure 3.9. The microlens array: full view of the holder and positioner (a), a detail of MLA and its holder (b) and the 3-axis stage used and web-cam microscope (c).

Tests

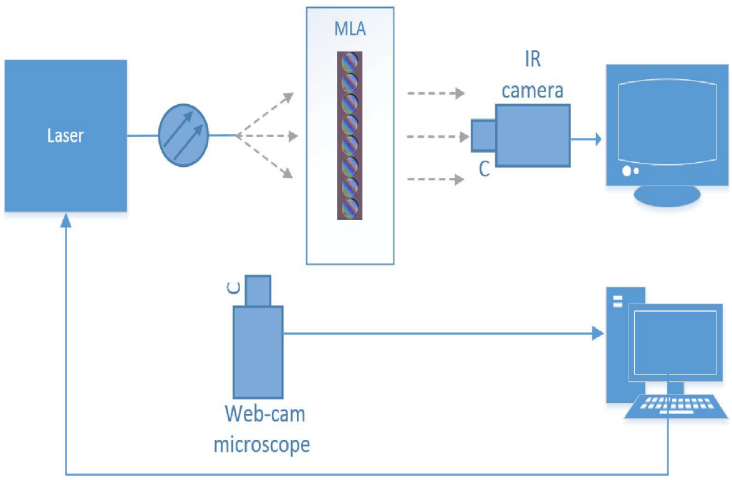
The microlens array is tested: the alignment procedure and the collimated beam are verified.
As shown in Figure 3.10(a) and Figure 3.10(b) the test-bed uses a laser [32] and an optical fiber as transmitter, the IR camera [33], displayed in Figure 3.10(c), as receiver; a red dot laser is also used during the alignment.

The collimation is performed in 3 steps: firstly the microscope is used to align the optical fiber at focus distance with precision of few μm, secondly the MLA position is adjusted on vertical plane by the red dot laser (or IR card detector is used to shown the optical beam) and, finally, the fine collimation is performed by IR camera feedback, as shown in Figure 3.10(c).

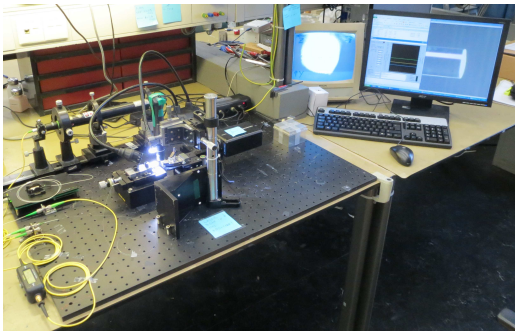
Lens magnification problem. The magnification of the beam caused by mismatch of focus point is discovered and studied.
The lens magnification is a well known phenomenon: a lens of MLA is considered, which in general is defined the vertical and horizontal planes, but is analysed on only one of these two planes (the analysis is the same for the other one). As shown in Figure 3.11, the optical fiber beam can be represented as a spot on plane, near the focal point, at distance d_0. The IR camera is on the lens focal axis, behind it at distance d_i.
Defined h_0 the gap between the spot height and the focal point:

- if $h_0 = 0$ the spot is in focus point, the beam is collimated, and its image is at infinity;
- otherwise magnification occurs: the image is at finite and shifted from the focal axis. The distance h_i between the receiver and the image spot depends on d_i by the transverse magnification $M_T \equiv -\frac{d_i}{d_0} = \frac{h_i}{h_0}$ [34], therefore, the beam is in a different position from the expected one.

The magnification is more important when the receiver is far away from the lens and when it has a small width (for instance, the IR camera $d_i \simeq 190mm$).



(a)



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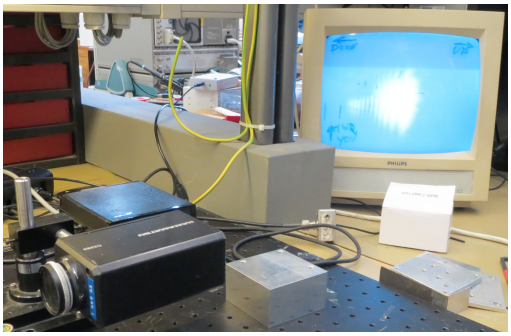


(c)

Figure 3.10. The test-bed scheme (a) and setup (b), from left to right: the $1550nm$ and red dot lasers, the optical fiber, MLA and IR camera, the screen used to display the camera output and the computer to control the laser and microscope display. A detail of the receiver (c): the white spot on screen is the almost collimated MLA beam.

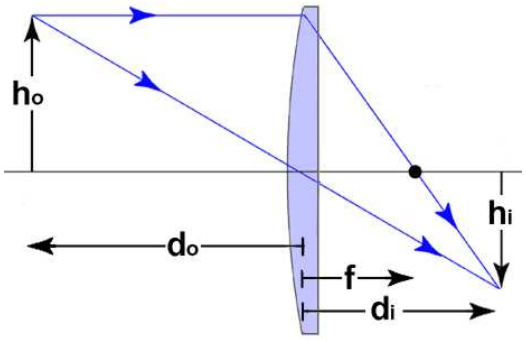


Figure 3.11. Lens magnification in a coordinated plane.

The problem occurs both on vertical and horizontal plane, producing a spot out of camera sensor. This is the reason to use the red dot laser: it allows to perform a first raw and fast alignment, and, secondly, the fine adjustment is performed by IR camera.

Performances

The alignment and the collimation are performed in a few hours. A great advantage is given by red dot laser which allows the placement without IR card detector and through immediate visual feedback. The microscope is used only for the first alignment and for safety reasons, avoiding optical fiber crack on MLA surface. The focal distance allows the fine adjustment without optical feedback through microscope and reduces the alignment time.

3.3 Optical receiver

The beam acquisition is one of the most important features of the test-bed and is performed by an optical receiver. It follows with characterization:

- peak wavelength at $1600nm$;
- incoming beams collection at the same time;
- power distribution recording along the PIC waveguides line;

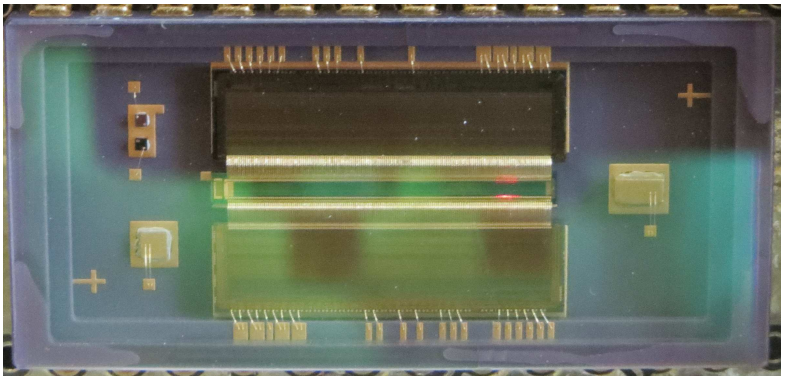


Figure 3.12. Photodiode array *PDA-640 SFF InGaAs Photodetector Sensor* by *Princeton Lightwave Inc.* in place on PCB slot.

- calculation of maximum power positions (peaks) and the total emitted power.

The receivers based on optical fibers are discarded immediately: the precision required in positioning increases placement time and placement precision. The optical power linear distribution along the PIC waveguide alignment direction is the useful one, therefore a linear array of photodetector is chosen. As a further advantage, if the array is selected with a sufficient sensor area, the alignments will require higher tolerance.

3.3.1 Photodiode array

The previous requirements lead to choose the linear array 640 pixels *PDA-640 SFF InGaAs Photodetector Sensor* (PDA) by *Princeton Lightwave Inc.*, as shown in Figure 3.12, following with characterization.

Maximum power. The PDA maximum received power (denoted as $P_{rx,max}$) is calculated and is equal to $11.67 dB_{mW}$, as verified at page 99.
The highest value used during the experiment is $7.52 dB_{mW}$ over 150 pixels.

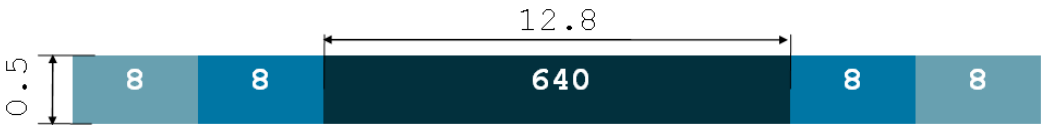


Figure 3.13. PDA pixel arrangement layout: all the dimensions are in mm.

Photodiode arrangement. The PDA provides, as shown in Figure 3.13, a row of 640 active pixels, 8 dark pixels and 8 disconnected pixels on each side. The dark pixels record the power provided by dark current and the disconnected ones give unreliable values which must be deleted during data processing.
The pixel dimension are $20 \times 500\ \mu m \times \mu m$ which is sufficient to acquire the collimated beam of diameter L_{wg}. The total array length is $12.8mm$ and is adequate to acquire all the photonic integrated switch beams at the same time.

Inputs and outputs

The most important inputs and outputs are here described. The other data and timing specification are in datasheet at page 77. The signal functions are the following:

- clock, from 0.01 to $5MHz$;
- Integrate, input signal which control the integration and readout;
- Even Video 1 and Odd Video 1, pixel video reference levels outputs, updated on falling and rising clock edge, respectively;
- Even Video 2 and Odd Video 2, pixel video level outputs, updated on falling and rising clock edge, respectively;

when the integrate signal is activated the photodiode array starts to acquire the optical signal, thereafter the data are output: each pixel is provided with readout circuit which provides the signals (in parallel), the PDA puts these values in serial on Even and Odd Video pins. The sampling time and pixel

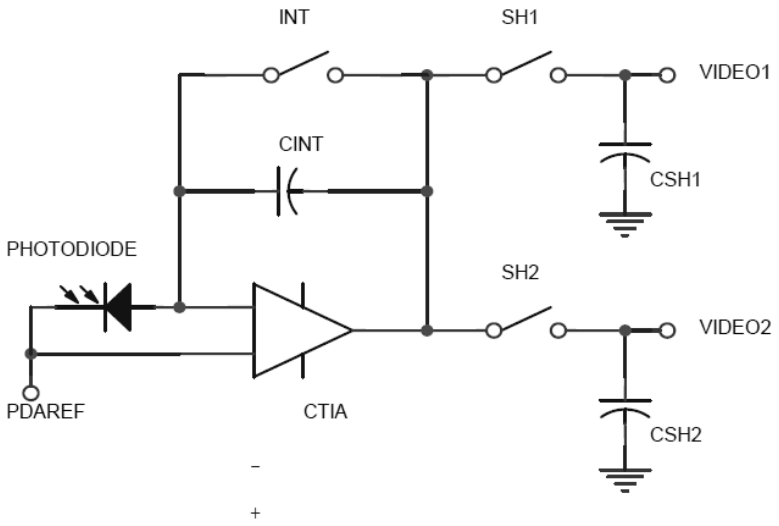


Figure 3.14. PDA electrical scheme from the datasheet at page 77.

rate depend on the clock frequency.
The relation between output voltage and optical power $P_{rx}(t)$ is calculated by analysing the electrical scheme shown in Figure 3.14. The readout circuit is an integrator operational amplifier followed by a sampler. The sampler input voltage (V_{out}) is defined in (3.2): the V_{Ref}, C_{INT}, T_{int} and $i_p(t)$ are, respectively, the voltage reference, the capacitor used in the integrator, the integration duration and the photodiode current. This depends on $\mathcal{R}$, I_{dark} and $I_{ng,opt}$, which denote respectively the responsivity, dark current and negative-going current of pixel photo-detector.

$$i_p(t) = \mathcal{R} \cdot P_{rx}(t) + I_{dark} + I_{ng,opt} \tag{3.1}$$

$$V_{out} = V_{Ref} - \frac{1}{C_{INT}} \int_0^{T_{int}} i_p(t)dt \tag{3.2}$$

3.3.2 Interface board

The photodiode array must be controlled and interfaced toward the computer. Therefore, the following functions must be provided:

- clock generation;

- 6 input signals processing and voltage supply;
- analogue-to-digital conversion of 5 output signals;
- computer interface handling and software library for the test-bed software.

The *640 Pixel Linear PD Array Demo Board* (henceforward called PDA-board) by *Princeton Lightwave Inc.* is chosen as computer interface.
The data loggers by *Pico Technology* were also considered: the limited output voltage range, the dearth of software library which directly supports the PDA and the estimated time necessary to design a reliable receiver led to select the *Princeton Lightwave Inc.* solution.

PDA-board

The PDA-board provides all the requirements previously defined: it converts the input parameters into the proper PDA signals and performs the analogue-to-digital output conversions, providing the number of samples for each pixel. As shown in Figure 3.15, the board requires the power source, computer link (via USB interface) and the PDA connection. All the other signals are generated inside.

From the software support perspective, the board is supplied with a graphical user interface (GUI) software and dynamic-link library (DLL) function set. The provided software, whose graphical user interface is shown in Figure 3.16, is able to set all the PDA parameters. Moreover, it provides the test function which checks the link between the board and computer and the possibility to save the output on a tab delimited text file.
Both the graphic and the output file provide the power distribution along the sensor line: the output is a 672 element vector. The i^{th} value of this vector is the optical power received by the i^{th} pixel. The power values are expressed in samples, a quantity which represents the number of samples used during the analogue-to-digital conversion performed by PDA-board. The relation be-

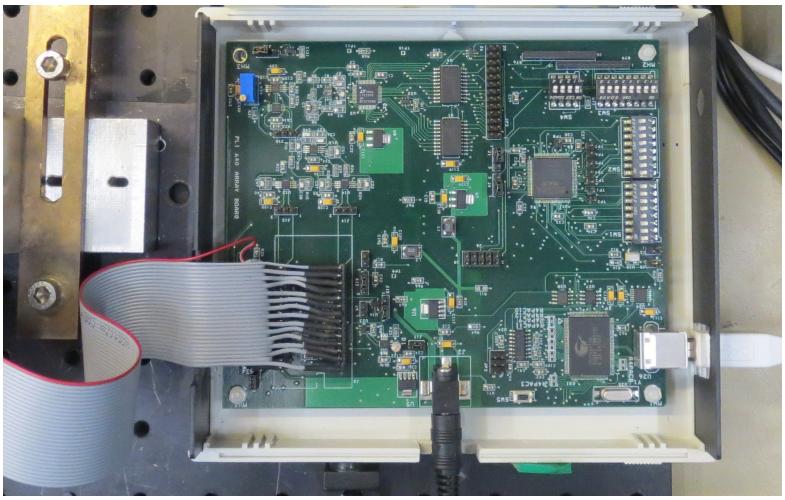


Figure 3.15. Interface board: top view of PDA-board, from left to right, the ribbon cable used to connect the photodiode array, the power supply and the USB cable.

tween power in samples and Watt units is studied and the linear dependence between these quantities is demonstrated in section II.

3.3.3 Tests

Test-bed setup

The photodiode array performance is tested to establish the simulation and environmental parameters affect the measurements. The T_{int} and the number of measurements (N_{Lines}) are studied as well as the high and low frequency electromagnetic (EM) interferences and the minimum distance between beams recognized through the photodiode array. Finally, an unexpected problem in PDA-board output is studied and solved.

As shown in Figure 3.17, the test-bed configuration is similar to the one described at page 17: the optical source is the same, collimated by MLA, the web-cam microscope and the beamsplitter are still positioned. As displayed in Figure 3.17(a), the IR camera is moved to place the PDA, the beamsplitter [35] allows to divide the beam, as a result the IR camera is moved in front

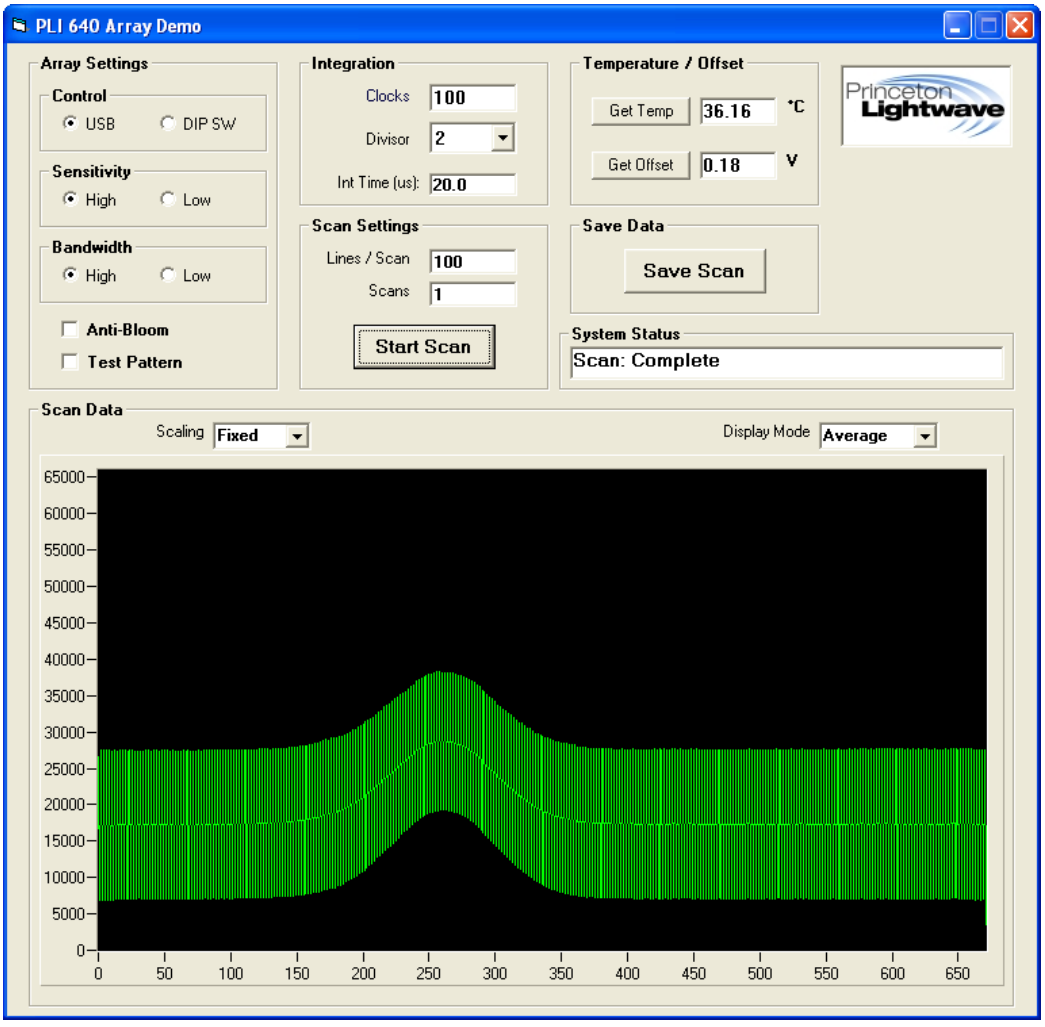
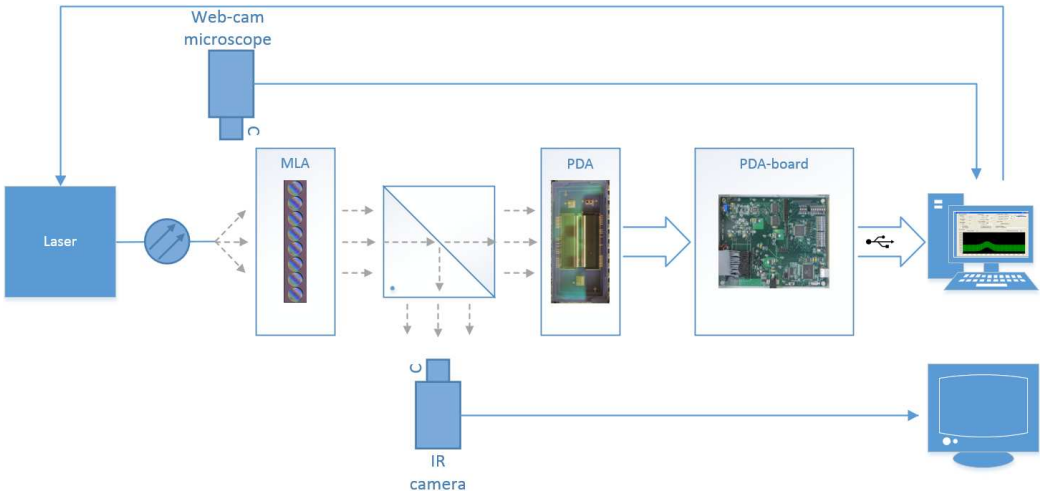
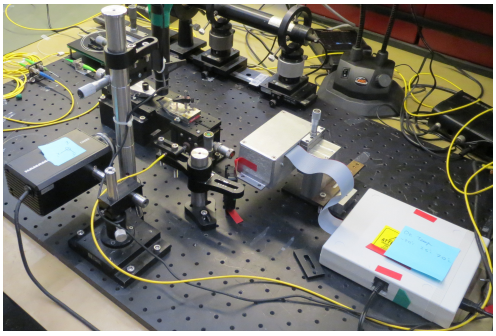


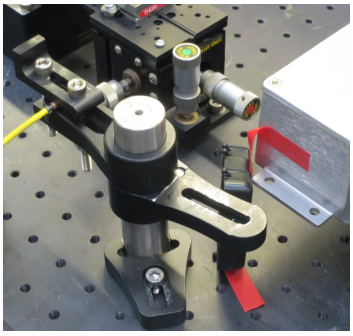
Figure 3.16. The graphical user interface provided with PDA-board.



(a)



(b)



(c)

Figure 3.17. Test-bed used during PDA trials: diagram scheme (a) and setup (b). The PDA is placed in the metal box on the vertical positioner, in the centre of the image, and is connected through a ribbon cable to the PDA-board. The red dot positioner is reported in (c). The bottom post mount fixes the altitude, the upper one rotates in order to point, firstly, the MLA and, finally, the PDA performs the alignment.

of the second output in order have an extra optical receiver.

The alignment procedure is divided in 2 steps: horizontal and vertical positioning. The first stage is simplified by the fact that the photodiode array width is bigger than the beam diameter and is performed by rough visual alignment. The similar dimension of PDA pixel pitch and optical

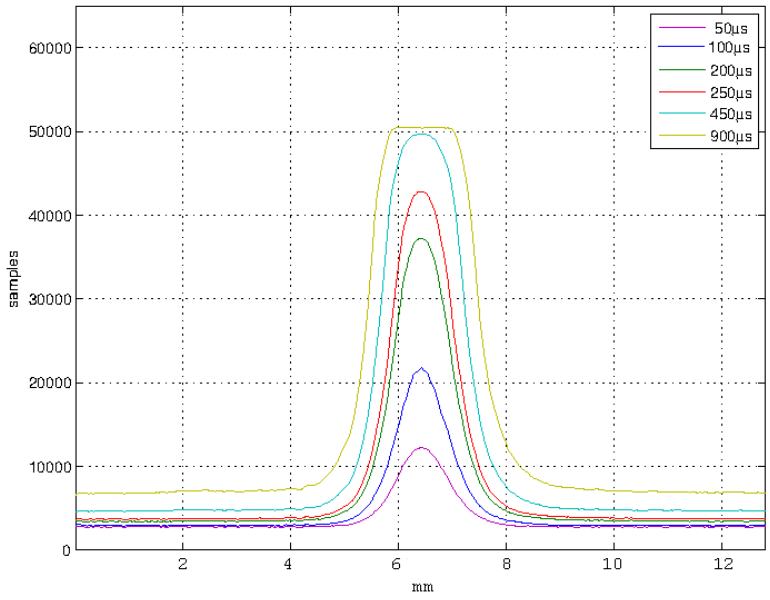


Figure 3.18. Saturation effect versus T_{int}.

beam wavefront increases the vertical alignment time. The solution is to use a red dot laser pointer, as shown in Figure 3.17(c). In this way, the time required is reduced to few minutes.

Measurement time versus saturation

The effect of T_{int} variation on the photodiode array output is measured. As shown in Figure 3.18 and as already defined by the mathematical model of (3.2), the received power rises for increasing T_{int}, up to the level corresponding at $\simeq 50000$ *samples* ($Count_{max}$). Values of optical power greater than $Count_{max}$ are analogue-to-digital converted equal to $Count_{max}$. This phenomenon is denoted as PDA saturation.
The T_{int} can be set by different parameters, such as the clock divisor and the integrate clock number, and the power distribution behaviour does not change from the response reported in Figure 3.18. Same data and conclusion are provided by the tests performed changing the C_{INT}.

Number of measurements versus data reliability

The variation of the optical received power was discovered during the tests, for the same transmitted signal and test-bed conditions. As shown in Figure 3.19, the number of measurements N_{Lines} influences the reliability of the output data. Indeed, the relative error of the maximum between $N_{Lines} = 1$ and $N_{Lines} = 2047$ is 6.574%, while it decreases to 0.29% between $N_{Lines} = 1000$ and $N_{Lines} = 2047$. As consequence N_{Lines} determines the number of reliable digits in all the output data, and the possibility to reveal the minimum power change is not caused by the random variation of the received optical power.

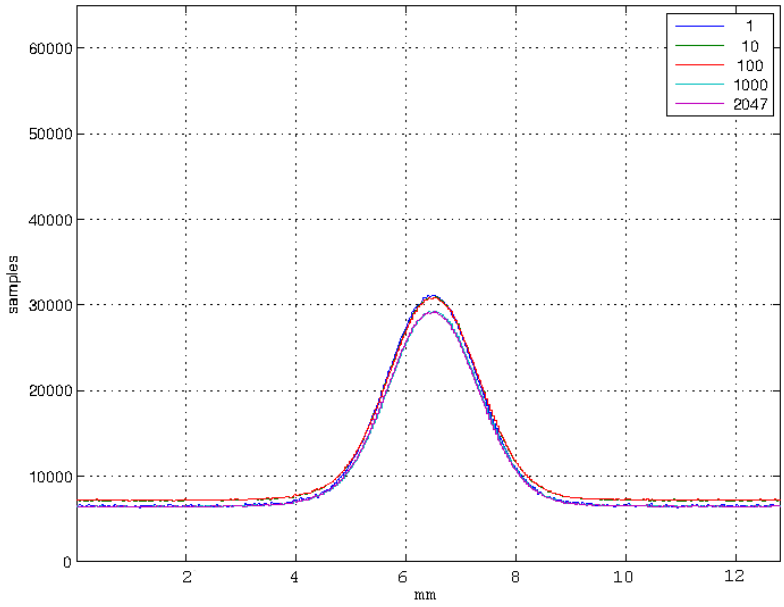


Figure 3.19. Power distribution variation versus N_{Lines}.

Electromagnetic interference

The possible interference by electromagnetic fields at low and high frequencies was studied as well.

The electrical grid interference was studied to know if the other test-bed devices affect the photodiode outputs: the CRT monitor and red dot laser

current spikes during the enabling are used as burst EM interference sources. As shown in Figure 3.20, the device interferences do not affect the PDA data reliability, since the three cases provide negligible variation of the average power.

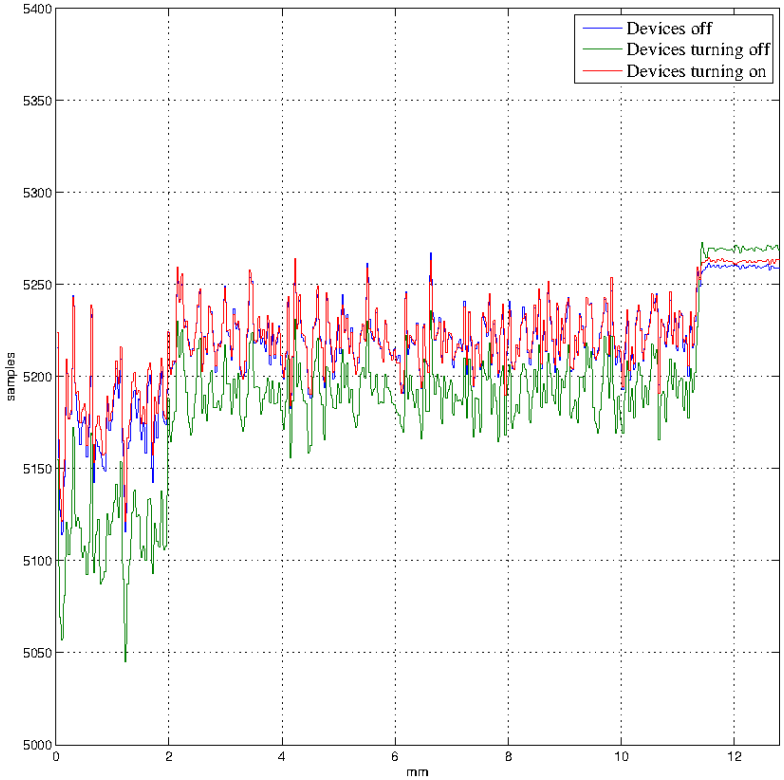


Figure 3.20. Comparison between optical power distribution with and without electromagnetic interference caused by electric grid. The mean values for the blue, green and red curves are, respectively, 5221, 5193 and 5223 *sample*.

The high frequency interference are also tested, in particular, environmental light (especially the microscope light) produces a flat interference pattern which becomes more important with the increase of T_{int}.

However, this interference does not affect the output values, inasmuch it can be recognized and erased by software algorithm during the data processing. The interference adds power to the optical beams received, reducing the number of samples available for the useful signal or, as well as, saturating the

PDA.
As shown in Figure 3.21, the interference is sensibly reduced using a dark-room for PDA. Indeed, the environmental light interference, in this condition, is negligible, inasmuch the darkroom provides as environmental interference as the ideal condition, which is no light in the laboratory.

Spatial resolution

The photodiode array length is sufficient, as written at page 21, to acquire all the photonic integrated switch beams. This simplifies the measurements but, more important, allows to recognize the position of each beam and distinguish it from the others. This feature makes possible to perform new tests on the PIC: optical crosstalk, measure erroneous waveguide routing and SOA mapping.
The position identification depends on the spatial resolution of the PDA. This quality can be defined as the minimum distance between the maximum

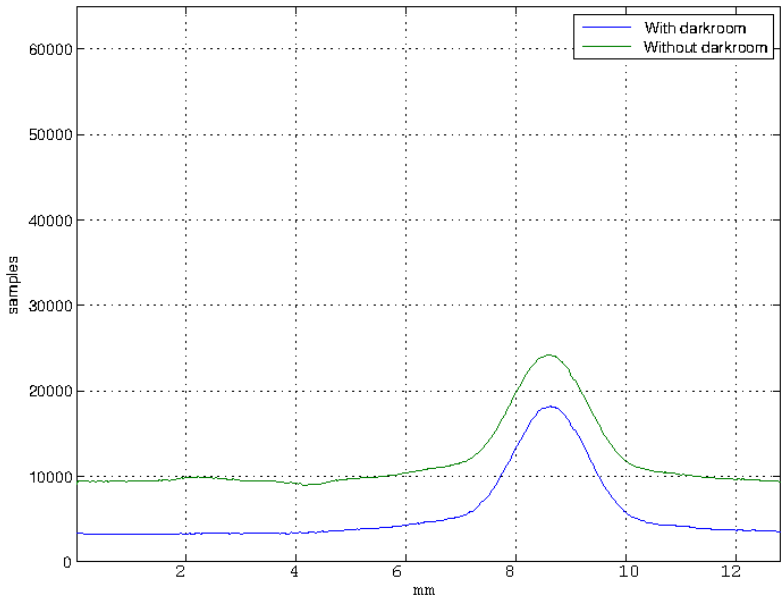


Figure 3.21. Environmental light ($T_{int} = 1.5ms$) interference: the dark-room effect.

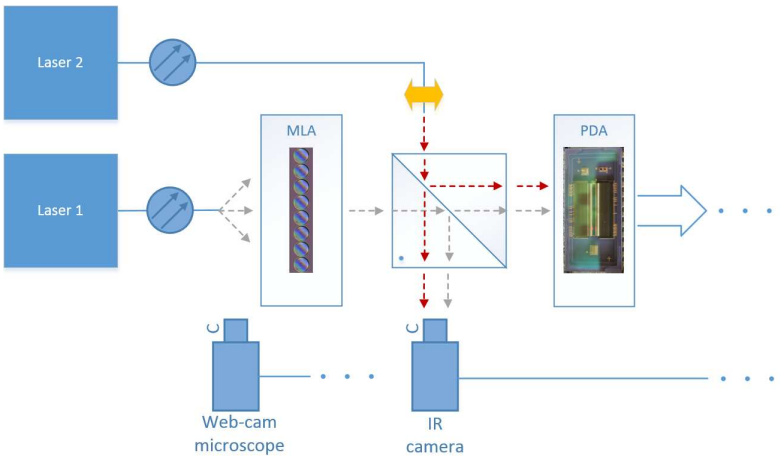


Figure 3.22. Spatial resolution test-bed changes: the optical fiber connected to Laser 2 is collimated and can shift along the yellow arrow direction.

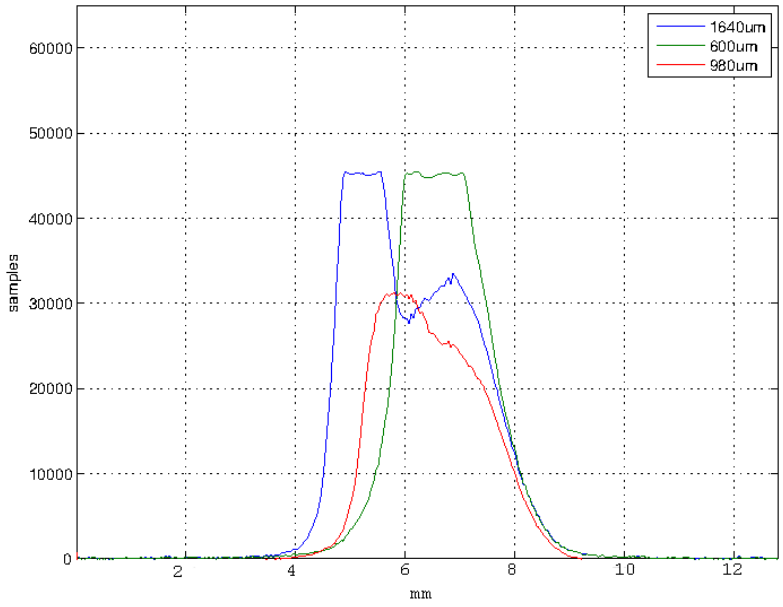


Figure 3.23. The spatial resolution results: the second beam is saturated by purpose in order to display more clearly the signal collimated by the MLA. The displayed distances are the relative gaps.

of 2 beams. The peak and its position are necessary to calculate the mean value and the variance of the theoretical gaussian curve.

As shown in Figure 3.22, the trial is performed adding a second collimated optical fiber in the test-bed. The results obtained are shown in Figure 3.23, where the microlens array collimated signal is the lower peak in each curve and where the second beam is saturated in order to increase the measurement precision. Therefore the minimum recognizable distance is $980\mu m$.

Offset equalization

The PDA-board data ripple problem is here defined and solved.
As shown in Figure 3.24, the trials performed with PDA-board provide a power distribution with an unexpected ripple and the same issue is verified also with the provided DLL function set.
The output curve generated by the PDA-board software allows a more detailed analysis. In this way, it is discovered that the ripple is present between the odd and the even values: the output elements with even indices do not have ripple, since the datum variations are consistent with the expected beam, and the same is verified with reference to the odd index elements. Consequently, the ripple is limited between 2 envelopes defined by the even and the odd vectors.

The problem cause is then analysed. At first, the optical source is investigated as a possible cause of the ripple but it is still present when the photodiode array is shut and the photocurrent is constituted by the noise of the receiver. Moreover the ripple is present also in the dark pixel values. Consequently, the cause is not the external source. Secondly, a possible photodiode array malfunctioning is supposed, but the ripple is also present in test pattern generated by the PDA-board, without regard for the photodiode array. It is then concluded that the ripple must be related to the board.
The photodiode array data are supplied through Odd Video ad Even Video outputs (see at page 21) and a mistaken PDA-board offset compensation calibration of these pins generates the ripple [36]. This ripple cannot be

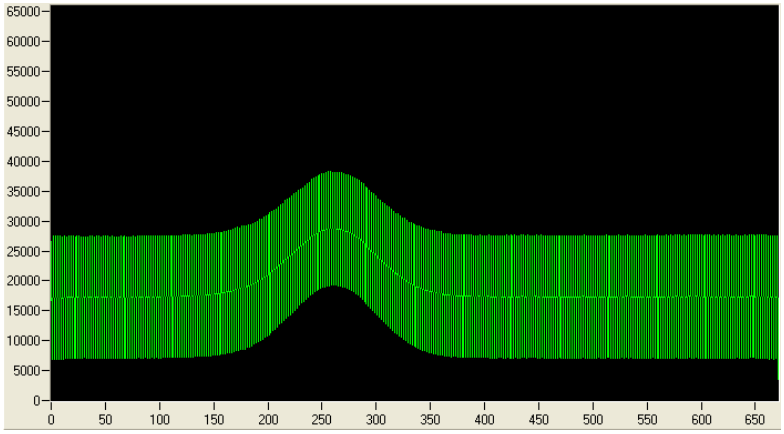


Figure 3.24. Screen shoot of the PDA-board software in which the power distribution ripple is shown. On the abscissae and ordinates are displayed, respectively, the pixel index and the power in samples.

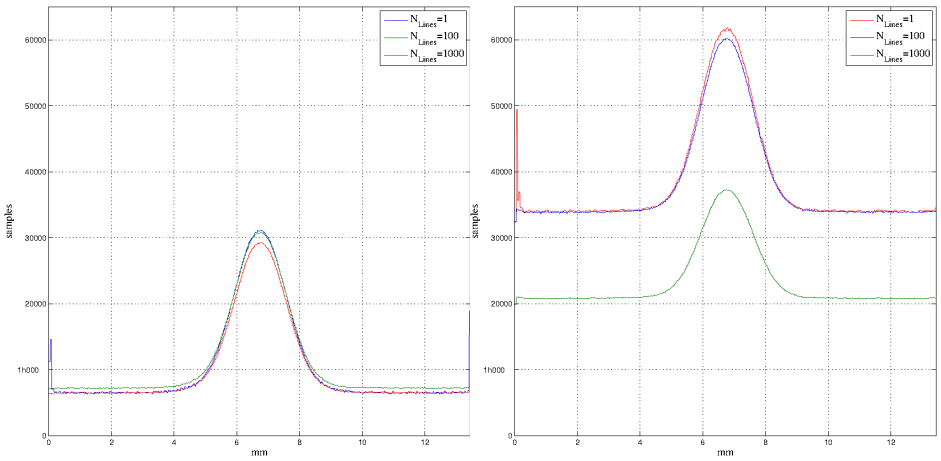
tuned through a circuital calibration. Anyway, the data are still reliable [37], therefore the offset equalization is performed by software during the data processing.

The equalization algorithm is based on odd and even indices separation, the 672 elements vector provided by the PDA-board ($\overline{v}$) is split in $\overline{even}$ and $\overline{odd}$ vectors as shown in (3.4) and (4.1), respectively.

$$even_i = \begin{cases} i = 2, \ldots, 672 & \\ v_i & \text{if i is even or i=1,} \\ \frac{v_{i-1}+v_{i+1}}{2} & \text{otherwise.} \end{cases} \tag{3.3}$$

$$odd_i = \begin{cases} i = 1, \ldots, 671 & \\ v_i & \text{if i is odd or i=672,} \\ \frac{v_{i-1}+v_{i+1}}{2} & \text{otherwise.} \end{cases} \tag{3.4}$$

The $\overline{even}$ and $\overline{odd}$ vectors describe 2 different power distribution envelopes. Therefore the photodiode array parameters influence on them are studied and the most reliable vector is selected. As shown in Figure 3.25, $\overline{even}$ is chosen due to the smaller offset introduced, which means a reduced probability of PDA saturation and increased reliability against the N_{Lines} variation.



(a) (b)

Figure 3.25. Power distribution versus N_{Lines}: $\overline{even}$ (a) and $\overline{odd}$ (b), the offset in smaller in the first case than the second, as well as the relative error decreases faster with N_{Lines} for $\overline{even}$ than $\overline{odd}$.

3.4 Software

The project goals require to write the software necessary to control the test-bed: 3 programs are written to this purpose.

The communication between PDA-board and computer is achieved by the supplied DLL function set. The connection toward the current controller is performed by the function set developed in the same project [27].
The software is development using the following tools:

- *Windows XP* operating system, service pack 3;
- *Standard C++* programming language;
- *NetBeans IDE 7.3.1 (Build 201306052037)*;
- *MinGW* C++ 4.6.2 compiler;
- *Matlab* release 2013a (version 8.1.0.604).

3.4.1 *Data displayer* software

The first software is *Data displayer*: as shown in Figure 3.26, it is a graphical user interface program for the real-time display of recorded power distribution curve, total power, maximum and peak position.
The *Data displayer* main purpose is to enable the operator to use the photodiode array as a linear IR camera, providing the immediate PDA data without performing multiple acquisition, the *Data displayer* is designed to simplify the alignment step through the photodiode array feedback, leaving the operator focused on the device alignment procedures.

The software is written by the programming language *Standard C++*, moreover the *Qt* and *QCustomPlot* [38] – [40] graphical user interface libraries are used.
As shown in Figure 3.26, the graphical user interface has 3 buttons and 4 displays: the peak position and peak value windows, the total power and the power distribution displays. All the power values are declared in samples and the power distribution is shown in pixels versus samples.
The button actions call the function declared in Listing 3.1. The graphical interface provides then the buttons, *start*, *stop* and *capture* with the following functions:

- when for the first time *start* is clicked, the function start () is called and performs the photodiode array initialization. Otherwise, if *start* is clicked meanwhile the measurement is stopped, it will start again the acquisition.
- When the *stop* button is clicked, the function stop() performs the disconnection.
- When *capture* button is clicked the displayed distribution is saved in Value.csv file by the function capture().

The procedure result is shown in the display below the buttons through the messages: 'connected' (green background) or 'error' or 'disconnected' (red

Listing 3.1. *Data displayer* class declaration of public functions.

```
class PDA−GUI : public QDialog {
 Q_OBJECT
 public:
 PDA640SFFBoard_H();
 virtual ~PDA640SFFBoard_H();
 public slots:
 // connect the board
 void start ();
 // disconnect the board
 void stop ();
 // display pattern
 void updateCurve();
 // save in .csv file the pattern
 void capture();
};
```

Table 3.2. *Data displayer* input, output files: name and description.

File	Type
SimParameters1.csv	Input: define low sensitive PDA parameter
SimParameters2.csv	Input: high sensitive PDA parameter
Value.csv	Output (optional): generated by *capture()*
LogFile.txt	Output: logfile

background). Furthermore, a logfile is written to report all the errors occurred.
The typical *Data displayer* usage is: start the program, clicking *start* button, and in this way the graph displays the different patterns. When a distribution needs to be saved: *stop* button is clicked, the pattern remains in the graph, and with *capture* button it is saved, the measurements restarts, newly, clicking the *start* button.
The real-time visualization is obtained by a timer: when the count is finished the curve is updated and displayed by the function updateCurve() and then the timer starts again to count.

Dark values cancellation. The dark current offset by dark pixels is deleted. After the acquisition, the program discards the values provided by the disconnected pixels. To this purpose it calculates the mean value of dark pixel elements in order to find the dark offset, then it subtracts the result from the active pixel vector. Finally, the power values provided do not depend on the dark current.

Parameter autoset. Some tests are performed changing the laser power in a wide range, the PDA acquisition parameters must be set frequently in order to better display the data. An automatic setting of the simulation parameters is needed (autoset): this feature is programmed in order to recognize when the pattern is badly displayed and, in case, to change automatically the PDA

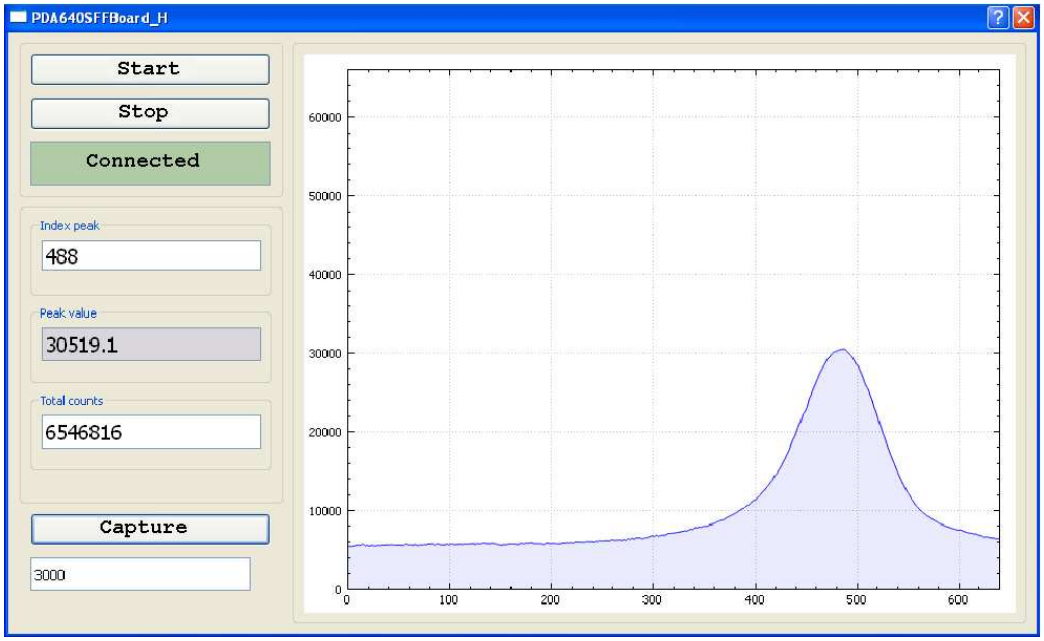


Figure 3.26. Data displayer: the graphical user interface.

parameters between 2 different configurations avoiding saturation or low peak values.

Inputs and outputs. All the input and output procedures are performed by the file shown in Table 3.2, in which SimParameters1.csv and SimParameters2.csv are the files used for the autoset feature. No output is generated unless the function *capture()* is invoked. The logfile is generated to record all the software activities and failures.

3.4.2 *Test controller* software

The second, and main, test-bed software is the *Test controller*: as shown in Figure 3.27, it is a command line interface developed in *Standard C++*. The main purpose of the *Test controller* is to supply a software able to manage all the test-bed during the trials, from the photonic integrated switch transmission to the photodiode array acquisition. It is designed to perform automatically all the operations of a typical photonic integrated switch op-

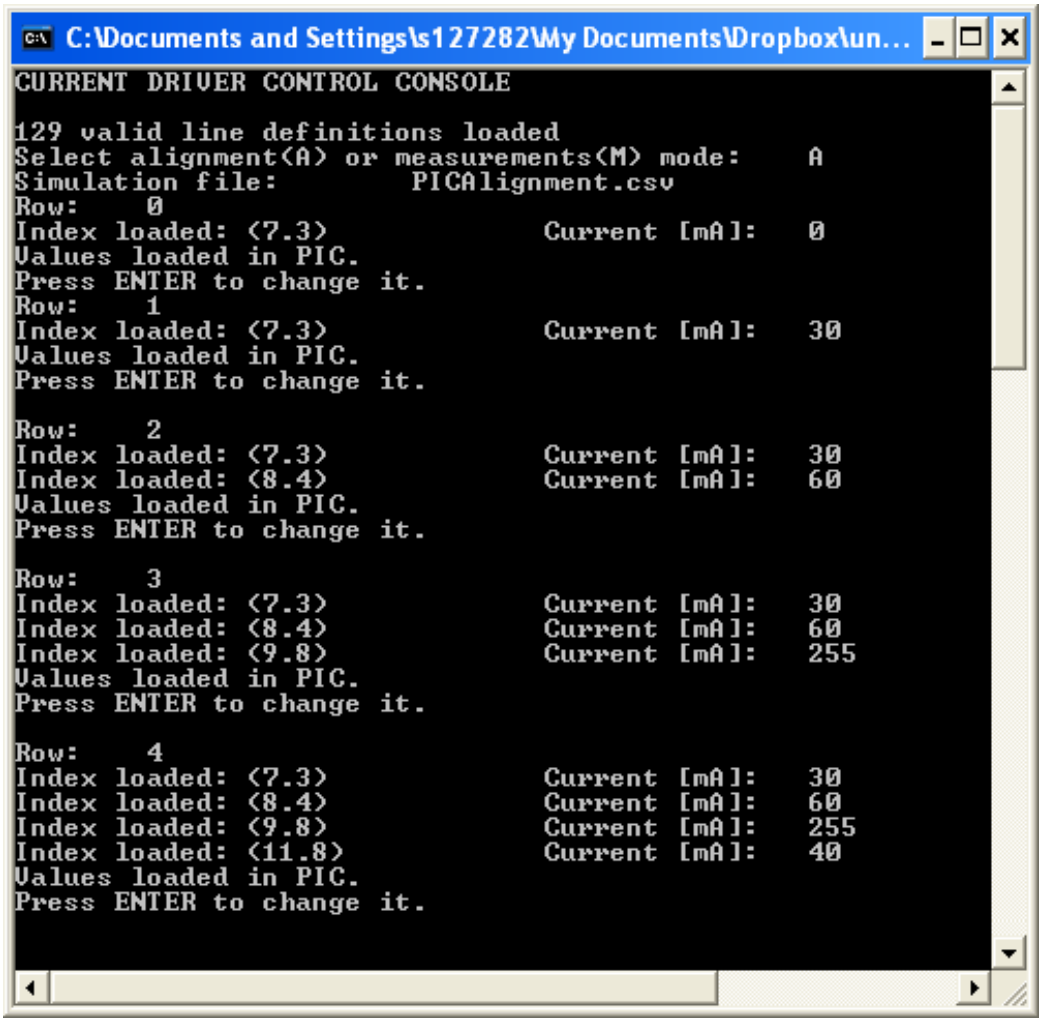


Figure 3.27. Test controller: example of alignment sequence.

tical test (PIC enabling, PDA acquisition and data saving) without the operator control. Moreover, a semi-automatic mode is implemented in order to control the PIC during the alignment procedures.
The sequence of SOAs, their currents, as well as all the PDA parameters are specified by *Comma Separated Value* (.csv) files listed in Table 3.3. The output values and the status flags are not shown on screen but saved in output and log files.

Table 3.3. *Test controller* input and output files and folder: name and description.

File and folder	Type
SimParameters1.csv	Input: define low sensitive PDA parameter
SimParameters2.csv	Input: high sensitive PDA parameter
PICAlignment.csv	Input: SOA sequence
PICMeasureSequence.csv	Input: SOA sequence
OutputParameters.csv	Output: maximum and power
patterns/	Output: recorded patterns directory
LogFile.txt	Output: logfile

The program provides two operating modes: alignment and measurements.

- The alignment mode is designed for the photonic integrated switch positioning steps. The software loads from PICAlignment.csv the photonic integrated switch SOA current and indices: neither the photodiode array, nor the output recording are controlled. They are instead managed by the *Data displayer*.

- The measurements mode manages both the current controller and the PDA-board. In particular, it initializes the devices, loads the set of SOA from PICMeasureSequence.csv and enables it. Subsequently, the

Listing 3.2. *Test controller* PIC class declaration of public functions.

```
class Controller{
 public:
Controller ();
~Controller ();
// initialization function
string Init ();
void getSimData(int & NumCopiedEntry,
                string & InputFile);
 // set read input
 int SetOutput(int & SimIndexEntry,
                bool & ReturnedValue,
                bool & CalibrationMode);
};
```

program performs the data acquisition and saves the read values in OutputParameters.csv and in the *patterns* folder. Thereafter, the next set of SOA is loaded and the same procedure is repeated. No operator control is required.

The modes are based on 2 classes: *Controller* and PDA640SFFBoard_H. *Controller* manages the photonic integrated switch and its public functions are shown in Listing 3.2.
When the *Test controller* starts, three functions are called, which are listed below.

1. The function Init () is called to initialize the current controller outputs, therefore the operator chooses a mode: alignment or measurements.

2. The function getSimData(**int** & NumCopiedEntry,string &InputFile) loads the photonic integrated switch SOA sequence: InputFile speci-

Listing 3.3. *Test controller* PDA class declaration of public functions.

```
class PDA640SFFBoard_H {
public:
 PDA640SFFBoard_H();
 virtual ~PDA640SFFBoard_H();
 //connect the board
 void start  ();
 // disconnect the board
 void stop();
 // check temperature
 void checkStatus();
 // save data
 void capture(bool & CalibrationMode);
};
```

fies the name of the file to load (PICAlignment.csv or PICMeasureSequence.csv) and returns the number of imported rows by NumCopiedEntry, the data are saved in a private array.

3. The function through which the software sends the SOA information to the current controller, which is the function SetOutput(**int** & SimIndexEntry, **bool** & ReturnedValue, **bool** & CalibrationMode). The sequence which has to be set is specified by the parameter SimIndexEntry. All the specified SOAs are enabled and the result is returned by ReturnedValue, and will be true if the procedure returns correctly, false otherwise. Besides, the function returns CalibrationMode=**true** if the first SOA index has current equal to zero. The meaning of this parameter is explained below where the PDA640SFFBoard_H is described.

As shown in Listing 3.3. The second class PDA640SFFBoard_H controls the photodiode array. When measurement mode is activated the *Test controller*

in addition manages the photodiode array through PDA640SFFBoard_H, following with the algorithm:

1. the constructor PDA640SFFBoard_H() initializes the object and loads the default measurement parameters by SimParameters1.csv.

2. The connection and disconnection are performed, respectively by the functions start() and stop(). In case of failure the functions write in LogFile.txt and exit the program.

3. The function SetOutput() is called.

4. A delay of $10s$ is waited in order to be sure that the photonic integrated switch outputs are stable.

5. The function checkStatus() is called to check the temperature of the PDA-board. If the temperature is greater than $65°[C]$ the board will be disconnected, the logfile is updated and the program is terminated.

6. The function capture(**bool** &CalibrationMode) saves the acquired distribution. CalibrationMode is a flag which communicates if the next power distribution is a interference pattern. This is used to perform the interference cancellation. Usually the special entry is specified in the first row, but it can be written more times in the file in order to update it. In this case the software recognizes each time the entry and updates the interference array. This procedure works as follow:

   - if CalibrationMode=**true**, the function sends the measurement parameters to the board, starts the acquisition, receives the distribution from PDA, performs the autoset and memorizes the distribution in a particular array as interference pattern. The entire array is saved in the file *<measurement time>.csv* in the *patterns* folder;

- if CalibrationMode=**false**, the function performs the same operation of the previous point and from the received distribution the interference array is subtracted. Besides the maximum, its position and the total power are calculated;

The function saves other values in OutputParameters.csv: these are SOA index, current, peak position and value, total power, measurement PDA file used and time.

The *Test controller* flowchart is shown in Figure 3.28. The PDA class also performs the dark power cancellation in the same way provided by *Data displayer* software as explained at page 37.

3.4.3 Data analysis

The data supplied through the photodiode array must be processed in order to extract the searched information. The data elaboration is then performed by a *Matlab* software. The script developed allows to display the current versus the power, the full width at half maximum and the current-space power distribution.

The script performs the following steps:

1. the program copies *patterns* folder, OutputParameters.csv, LogFile.txt, SimParameters1.csv and SimParameters2.csv from *Test controller* to the specified target folder.

2. The program reads from OutputParameters.csv, currents, total and maximum power and memorizes these values in 3 different arrays.

3. The software imports all the power distribution in *comma separated variable* files from the *patterns* folder and saves them in the $PowerPatterns$ ($640 \times NumberOfMeasurements$ matrix).

4. The current versus power curve is then obtained displaying the current and total power arrays with the *plot()* function. The figure obtained is saved in .fig, .eps and .jpeg formats in the target folder.

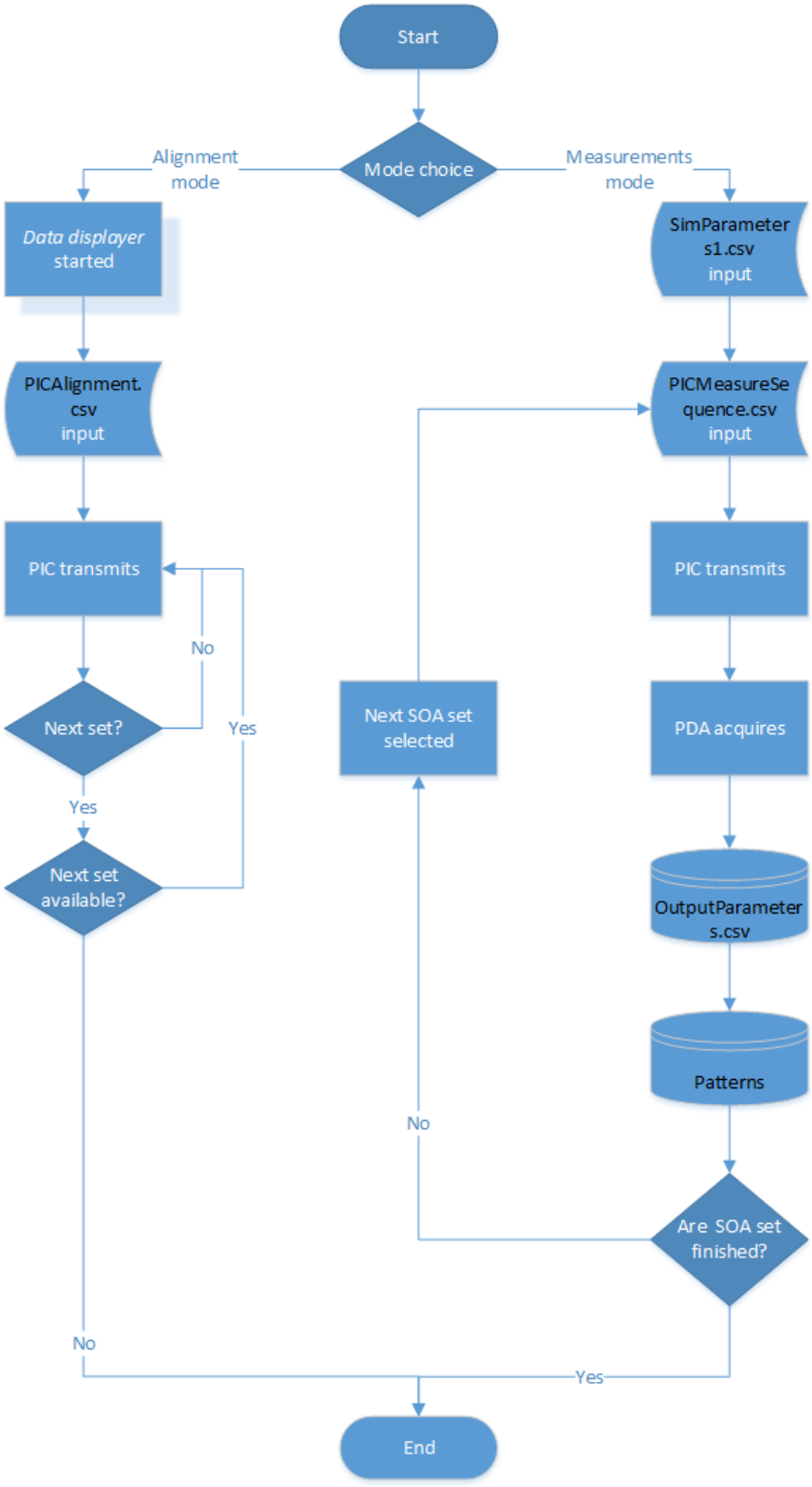


Figure 3.28. Algorithm of a typical use of *Data displayer* and *Test controller* in alignment and measurement procedures.

5. The full width at half maximum versus SOA current is then calculated. The theoretical half maximum power is calculated for each SOA current, then the closest real values are searched in the array and their positions are returned. The indices are 2: one on the left and one on the right of the peak. The full width is calculated making the difference of these two values. The full width versus current arrays are displayed and saved in .fig, .eps and .jpeg formats in the target folder.

6. The power distribution is displayed in function of the pixels and the SOA currents. These two are shown in abscissae and ordinates axes, respectively, and the power values are represented through a color scale. The color-bar graph, which is a 2 dimensional graph, exploiting the script normalizes the $PowerPatterns$ 50000 samples value to 255 (maximum of RGB color scale), in order to have the same scale for all the graphs, the behaviour of the curves is displayed with the function *image()* and saved in the .fig, .eps and .jpeg formats in the target folder.

7. The script deletes all the read data from the software folder making it ready for the next test.

Chapter 4

Test-bed assessment

In this chapter the test-bed evaluation, performed by photonic integrated switch trials, is reported. The prototype used is described in subsection 3.1.2. The tests performed are two: waveguide characterization and optical continuity.
The methodology used is a bottom up approach. Initially, the current controller outputs are verified, the photonic integrated switch is positioned and collimated in section 4.1. Then, the first, simple test is performed: one outer photonic integrated switch SOA at a time is enabled and studied in section 4.2. Finally, the second trial is performed, the complexity is increased inasmuch multiple inner SOAs are enabled in the same measurement and the continuity of a PIC optical path is analysed in section 4.3.

4.1 Preliminary operations

The photonic integrated switch optical tests require that all the test-bed devices are verified before the trials, in order not to affect their reliability. The only component to be checked is the PIC, because all the other devices are already tested in chapter 3, therefore it is assured that they work correctly. The photonic integrated switch check is divided in two stages: current controller output and PIC collimation.

The photonic integrated switch SOAs are identified by their indices and currents, as explained at page 9. Therefore it is necessary to match the values provided by *Text controller* with the current controller pinout and currents, in order to be sure to enable the correct SOAs.
The pinout test is performed verifying that the SOA indices input in *Test controller* match the PIC connector tracks of the trial sample: this allows to emulate all the test-bed from the program up to the PIC ceramic tile. The check is accomplished measuring the track voltages: if they are supplied to the given pads the test is passed, otherwise the pinout is wrong and is changed by software.
The current output is verified for each SOA with the following procedure. The test is based on providing a current value by *Test controller* and measuring the output current of the power supply when a diode connected in series to 5Ω resistive load is used as SOA model. The measurement algorithm is composed by the following steps:

1. the PIC output are disabled $\rightarrow$ the current measured is the idle current controller value;

2. the SOA is enabled by $0mA$ $\rightarrow$ the measured current is the reference value;

3. the SOA current is increased $\rightarrow$ the power supply current is measured;

4. the real SOA current is calculated as difference between the measured and reference values.

As shown in Table 4.1 and Table 4.2, if the load has a finite resistance the measured value will be valid, otherwise it is an open circuit and the current is not matched, theoretically it tends to zero. This method gives a great advantage, since it allows to check the photonic integrated switch SOA status before performing the optical test and in a shorter time: if the measured current for a SOA is not matched, this will be broken.

The photonic integrated switch collimation is the second, and last, stage. The chip is positioned on a two axis positioner ables to move in vertical direction and toward the microlens array. Neither the red dot laser, nor the IR detector card can be used, due to photonic integrated switch characteristics: a new collimation procedure is designed. As shown in Figure 4.1 and Figure 4.2, the alignment is performed in 3 steps: firstly, a coarse placement is performed by IR viewer [41], secondly the IR camera with diaphragm is used and, finally, the photodiode array performs the fine alignment. As displayed in Figure 4.1(a), the IR viewer is placed in front of microlens array. When the PIC spot is displayed (Figure 4.1(b)) the diaphragm is narrowed and the PIC moved to see it again, finally, the beam spot is limited to a few squared mm. As shown in Figure 4.2(a), in the second stage the IR viewer is moved backward on the positioner rail and the camera is mounted in front of it, the two sensor centres are aligned one with respect to the other and the PIC is collimated with greater precision, therefore the third step is performed. As displayed in Figure 4.2(b), in this stage the IR camera is moved backward on the rail and the photodiode array is placed and aligned through the feedback of *Data displayer*. As a result the PIC beam is collimated.

During the entire procedure and the optical tests the following PIC safety rules and advices are strictly followed:

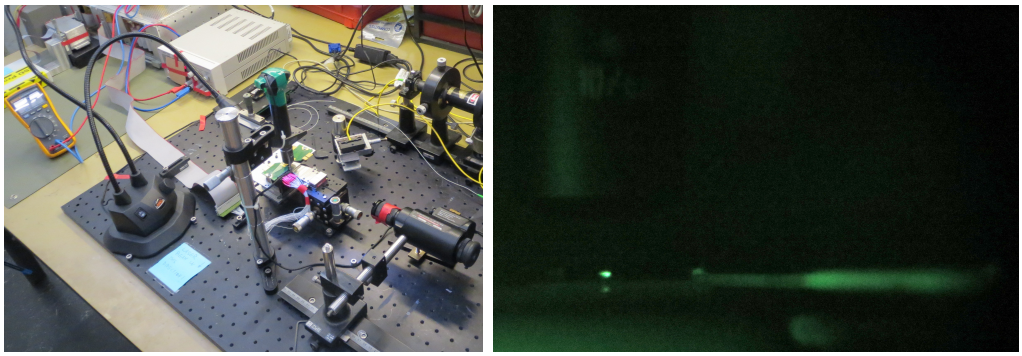
1. typical current values, lower than $30mA$ for alignment and lower than $80mA$ for measurements.

2. Limit of the SOA enable time, it depends on the current, according to the following relationship.

$$time = \begin{cases} 30Min. & \text{if SOA current } < 35mA, \\ 15Min. & \text{if SOA current} \in [35, 70]mA. \end{cases} \tag{4.1}$$

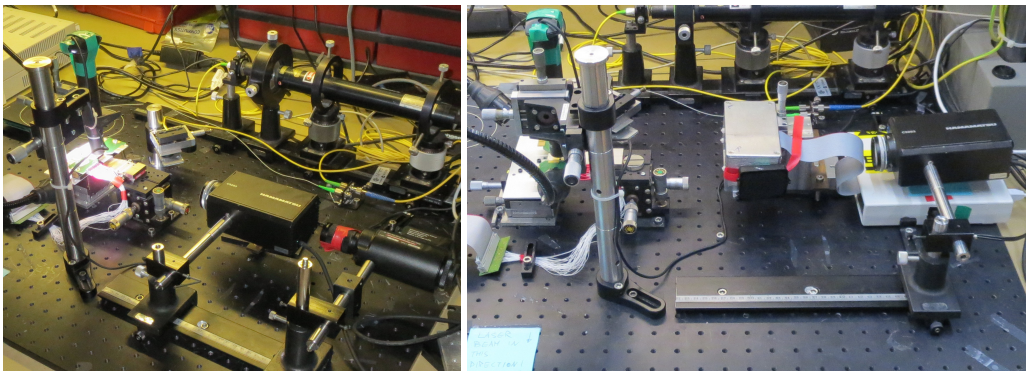
3. Turn-off period between each session $5Min.$.

4. In front of a drastic power decrease (which is due to overheating) the input current must be immediately switched off.



(a) (b)

Figure 4.1. The first step of the PIC collimation procedure: the IR viewer test-bed setup(a). The IR view of the PIC beam by IR viewer(b): the green dot is the beam through the MLA, the microscope lens can be recognized over the MLA.



(a) (b)

Figure 4.2. The second and third step of the PIC collimation procedure: the IR camera is used for the fine adjustment (a) and, in the next step, the photodiode array is placed (b).

5. During the alignment procedure, only one pad at a time must be enabled for the same SOA.

6. The red dot laser must not be pointed toward the photonic integrated switch ports.

Table 4.1. The SOA 1.1 current check: the variations are valid. The idle current is 1.548[mA].

Input [mA]	Current at power supply [mA]	pin output [mA]
0	1.564	0
10	1.575	11
30	1.594	30
45	1.608	44

Table 4.2. The SOA 1.3 current check: the variations are not valid and the connection is broken. The idle current is 1.545[mA].

Input [mA]	Current at power supply [mA]	pin output [mA]
0	1.5556	0
10	1.557	-7
30	1.559	-5
45	1.561	-3

7. The PCB PIC connector must not be crushed into the microlens array holder.

Finally, the test-bed setup is ready. As shown in Figure 4.3, the test controller manages the PIC input as well as the photodiode array acquisition, the output files are saved in *OutputParameters.csv* file and *patterns* directory, the *Matlab* processes the data and the curves and data are shown.

4.2 Waveguide characterization

The photonic integrated switch optical tests are performed acquiring the beam transmitted. Therefore it is necessary verify if, and how, its waveguides emit the signal. This can be achieved enabling the first SOA of each PIC port: as shown in Figure 3.3, these are the SOAs 1.1, 1.3, 7.3 and 7.1 (from now on they are called edge SOAs).

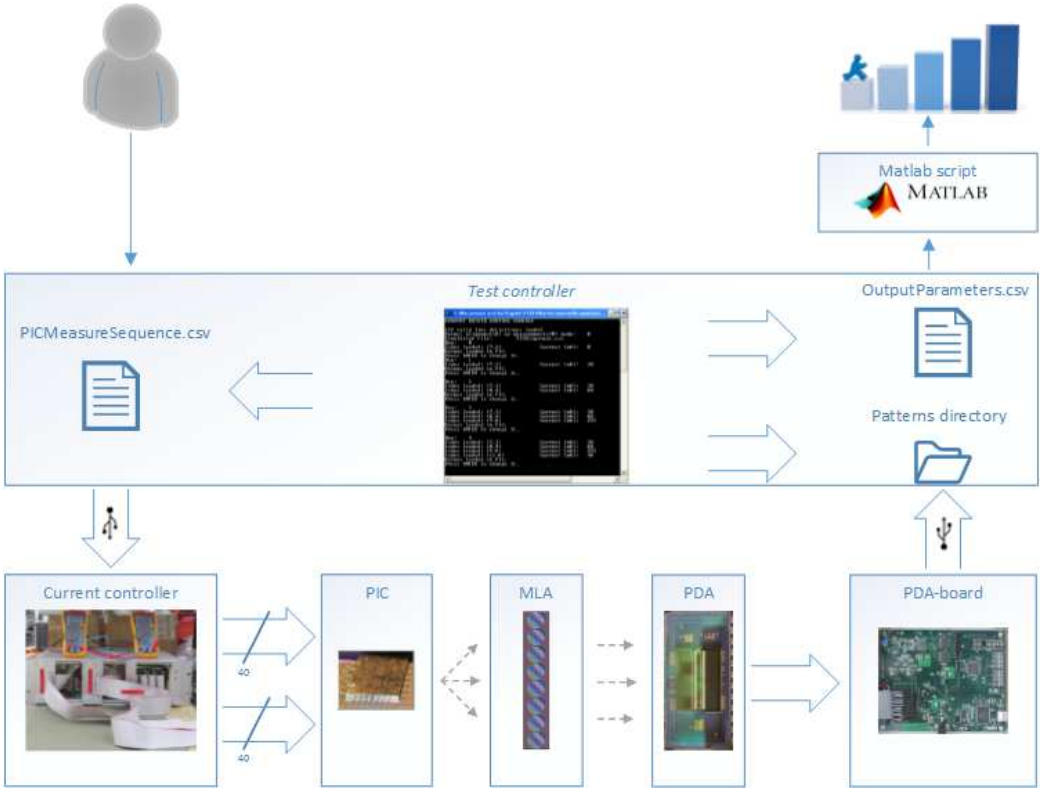


Figure 4.3. Schematic diagram of test-bed used during the photonic integrated switch trials.

The port capability to transmit is proved verifying the waveguide position, and finding the relation between current and optical power as well as measuring the beam width. The first trial recognizes the beam positions and checks the correctness of the photonic integrated switch inner routing. The current versus power test inspects the SOA efficiency to convert the electrical signal into optical power. Finally, the beam width analysis verifies the signal power spreading measuring its full width at half maximum (FWHM) at different currents.

4.2.1 Waveguide positions

The test is designed to verify the PIC beam positions: it is performed, firstly, enabling the edge SOA, secondly, the photodiode array acquires the power distribution and, finally, the peak position is controlled.
As shown in Figure 4.4, the beam spatial disposition is, from left to right: 1.1, 1.3, 7.3 and 7.1. The port order is reversed, if it is compared with the PIC layout, due to the photodiode array placement. However, this does not influence the measurements.

Microlens array tilt. On the vertical and horizontal planes a relative tilt is found between the microlens array and the PIC waveguide lines. Consequently, they are not parallel and the MLA must be collimated in vertical direction: each time a different edge SOA is enabled.
The device visual inspections through microscope allow to calculate the tilt angle on horizontal plane which results equal to 2.245°. The vertical tilt angle is estimated with a different procedure: to this purpose is used the microlens array vertical movement necessary to collimate each waveguide is used. As shown in Table 4.3, the vertical position adjustments require some tens of μm movements and are not constant between the waveguides.
The relative tilt is not observed during the optical fiber preliminary tests since more than one optical source is necessary to experience the problem.

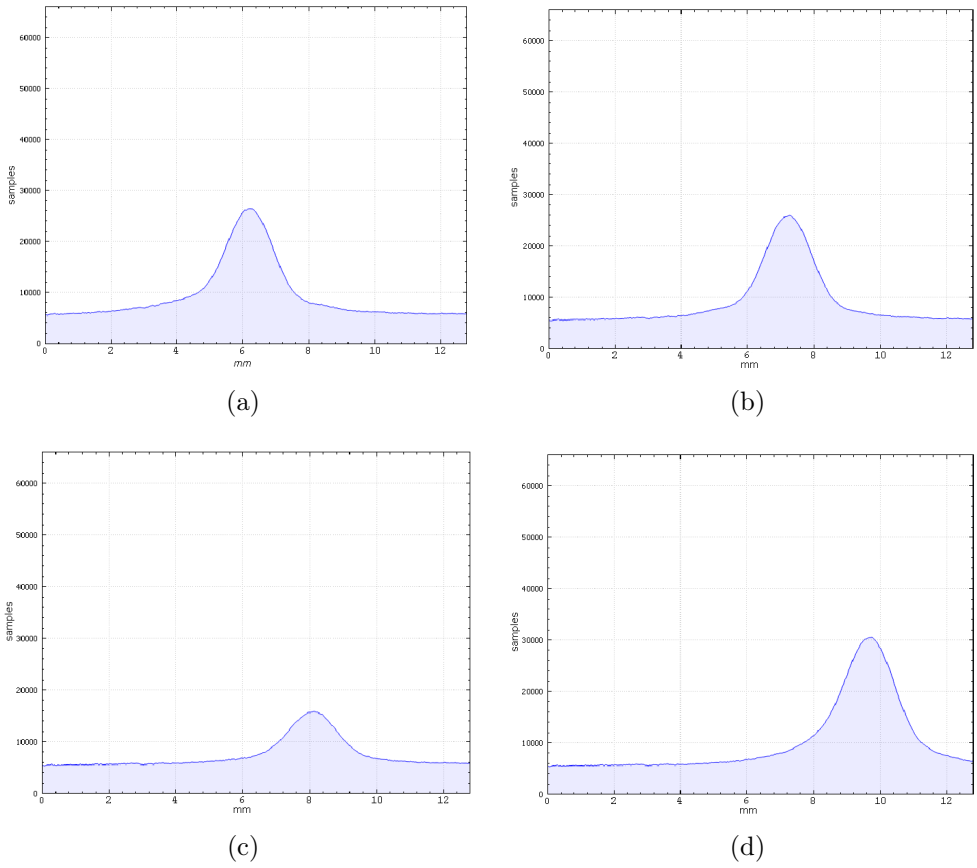


Figure 4.4. SOA power distributions at $30mA$: 1.1 (a), 1.3 (b), 7.3 (c), and 7.1 (d). Maximum position, in mm: 6.24, 6.8, 8.16, 9.76, respectively.

Table 4.3. The SOA indices versus the vertical position variation: for each SOA position change is shown the estimated correction on vertical MLA position.

SOA index change	Vertical adjustment [μm]
$7.1 \rightarrow 7.3$	62.5
$7.3 \rightarrow 1.4$	25
$1.4 \rightarrow 1.1$	50
$1.1 \rightarrow 7.1$	37.5

4.2.2 Current versus power characteristic

The trial finds also the relation between SOA current and its optical power as well ass the beam width. The test is performed in two stages: firstly, the SOA is enabled with current going from 0 to 75(mA), with step of 1(mA), and the power is acquired. Then, the data are processed in order to provide the behaviour of the current versus the optical power and the full width at half maximum curves, as explained at page 44.

The color-bar graph gives, at the same time, the information about the current versus power distribution and the peak. It shows the maximum power changes with current, abscissae axis, and the spatial power distribution, ordinates axis. As shown in Figure 4.5, the SOA 1.4 cannot work properly: this was discovered previously by the current checks at page 48, confirming the validity of current absorption as a valid connection verification method. Besides, the same SOA is not working correctly with the other connector, 1.3: the waveguide position trial shows different results but after few starts its performance decreased.

As shown in Figure 4.5, the SOA 1.1 and 7.1 have better performances than 7.3, due to the higher optical power reached for the same supplied current. The current versus power curve is illustrated in Figure 4.6: the 1.1 and 7.1 better performances are confirmed, furthermore the curve behaviour at low current values are shown.

The full width at half maximum graph is displayed in Figure 4.7: it remains almost constant for all the currents. The spikes at the lowest current values are caused by post-processing mismatch. At those currents the distributions are flat and the error caused by theoretical and real half maximum discrepancy are greater than for the other current values.

4.3 Optical continuity test

The photonic integrated switch function is to address the optic beam from the input toward the desired output port. The optical integrity is a fundamental requirement for the correct operation.
The photonic integrated switch optical paths are defined as the paths between two edge SOAs. An optical path in which the beam propagates from one side to the other of the way is defined as continuous.
The trial here performed verifies the test-bed capability to analyse the continuity of an entire PIC optical path.

4.3.1 Optical path structure

As shown in Figure 4.8, the most simplified PIC optical path model is defined as a sequence of stages, each one composed by a SOA (active component) and passive devices (coupler, etc.).
The stage working point definition is introduced as the current for which the SOA amplified spontaneous emission (ASE) balances the stage loss. Therefore, each stage has 3 states:

1. continuous path and current lower than working point. The current supplied to the SOA is insufficient, therefore the emitted photons cannot balance the stage loss [42], and its link budget is negative (the stage output power is lower than the input value).

2. Continuous path and current greater or equal than working point. The SOA emission balances the loss and the power contribution of the stage

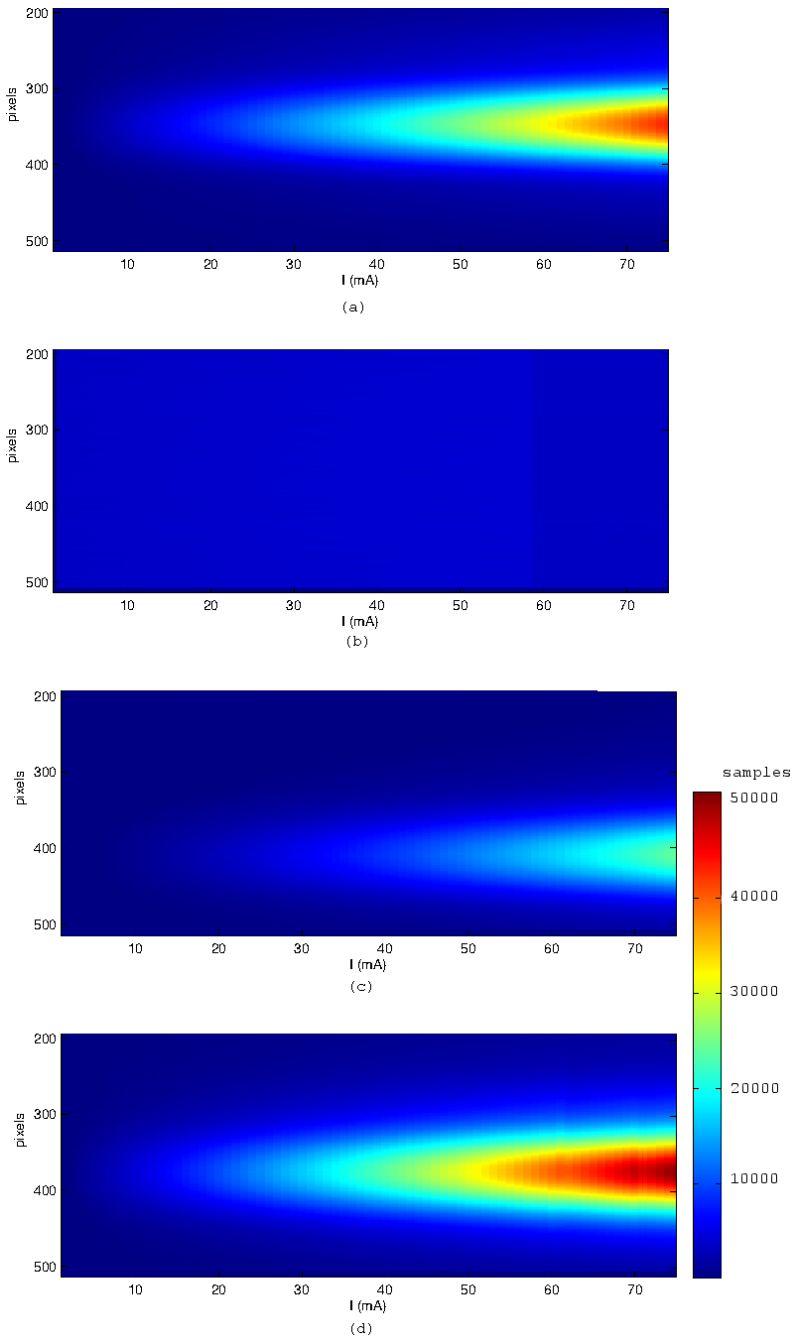


Figure 4.5. Time-spatial power distribution SOA 1.1 (a), 1.3 (b), 7.3 (c) and 7.1 (d), on abscissae and ordinates axes are shown the supplied current and the array line in pixel, respectively.

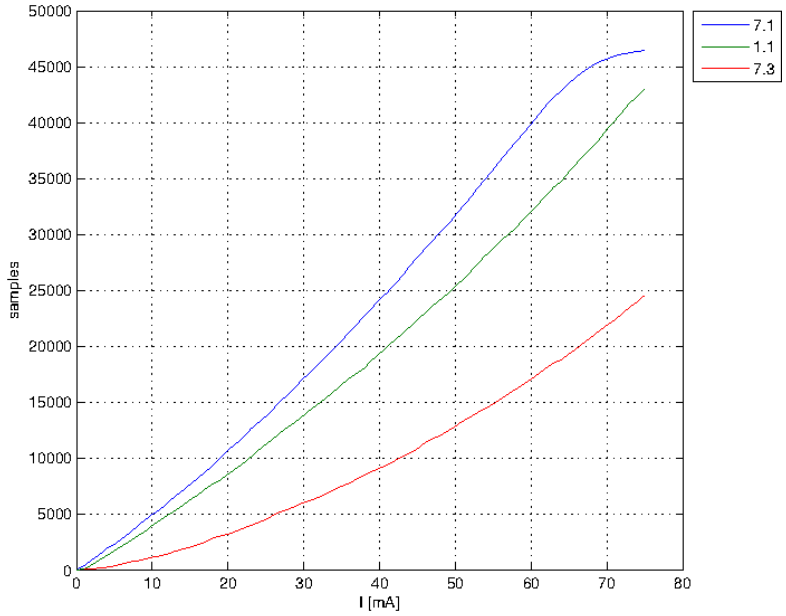


Figure 4.6. Edge SOAs current versus power.

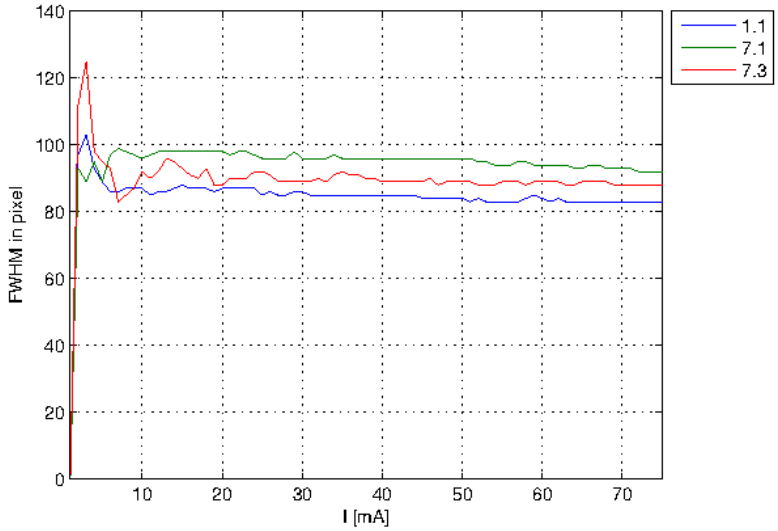


Figure 4.7. Edge SOAs full width at half maximum (FWHM).

is not negative.

3. Optical discontinuous stage, no matter which current is supplied, the stage loss is not balanced;

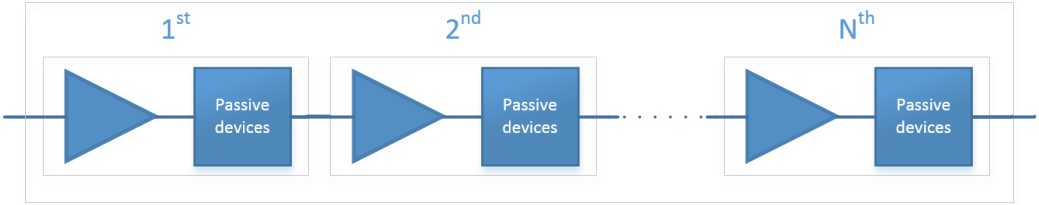


Figure 4.8. Schematic diagram of a photonic integrated switch optical path, the N stages and their model (SOA and passive components): the 1^{st} SOA is an edge SOA.

4.3.2 Working point survey

The suitable current to determine the working point must then be found. This requires two steps: finding the maximum SOA current and ranging it in order to discover the working point.

Firstly, the upper range bound is calculated for each stage. The edge SOA maximum current and their contact areas are known, therefore the current density is calculated which is equal to $9.66 MA/m^2$. The surface of the stage SOA is known, therefore the maximum current is computed and matched during the trials.
Denoting the i^{th} SOA as SOA_i with $i = 2, ..., N$, its working point is found studying the current versus power curve. As shown in Figure 4.9, an iterative algorithm is used:

1. the SOA_1,..., SOA_{i-1} are enabled with their known working points;
2. the SOA_i is enabled with the current in the calculated range;
3. the current versus power is computed and analysed, as shown Figure 4.10;

the step 1 is performed in order to bring the beam to the photonic integrated switch port. The trial can be performed when the i^{th} SOA beam travels up to the photonic integrated switch port and reaches the photodiode array. Therefore, a continuous optical path must be provided between the port and

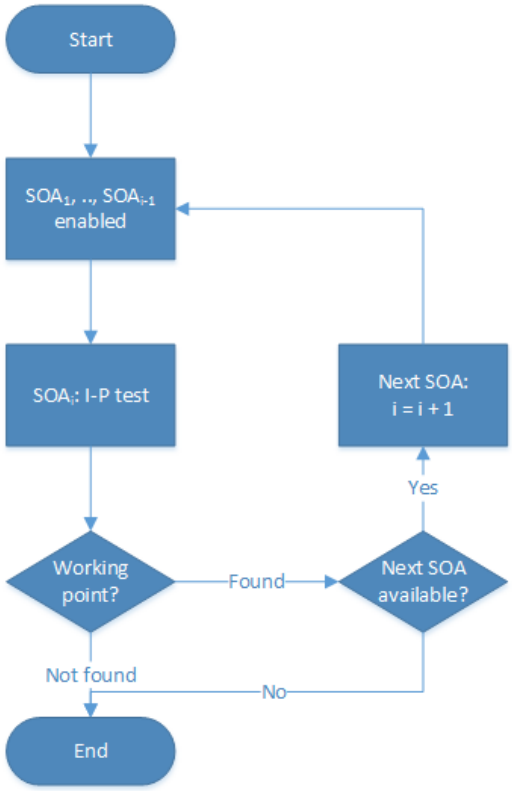


Figure 4.9. Working point survey flowchart: I-P test denotes the current versus power trial.

Table 4.4. SOA working points: switches with similar surface areas have comparable currents.

SOA	7.3	8.4	9.8	11.8	12.4	12.2	11.6	9.6	8.2	7.1
Current $[mA]$	30	60	255	40	255	28	20	40	60	30

the studied inner SOA, the step 1 provides the necessary way.
As shown in Figure 4.11, the tested photonic integrated switch optical path and the SOA indices are defined. Consequently, the working point survey results are found and shown in Table 4.4: the SOA 12.4 reaches the maximum supplied current ($255mA$), without a clear working point.
Besides, during the test, the current absorption check of page 48 is performed: no broken SOAs are found.

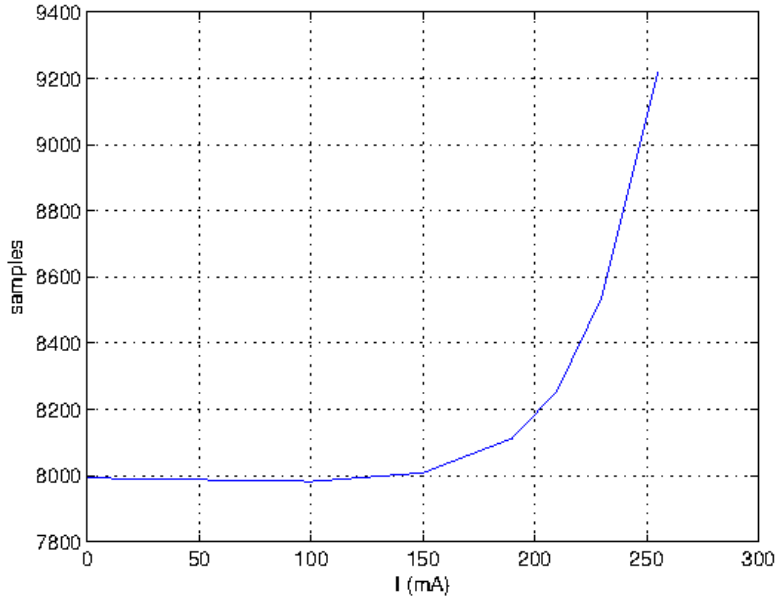


Figure 4.10. Power versus current curve of SOA 9.8, the loss is balanced for $I \simeq 200mA$, as a result the working point is select equal to $255mA$.

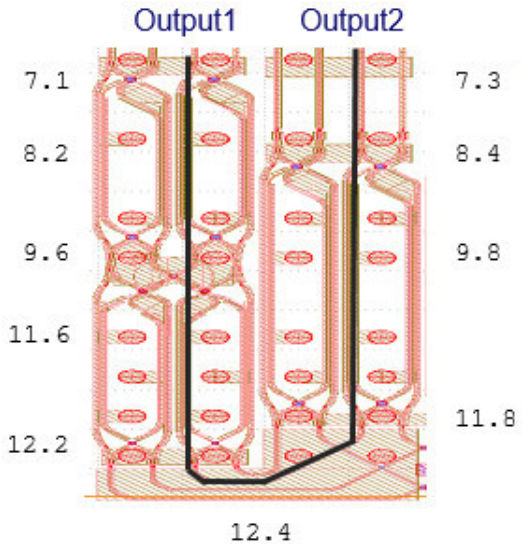


Figure 4.11. The optical path under test and the SOA indices.

4.3.3 Optical path continuity

The entire path must be verified in the same test-bed conditions, therefore it must be performed in one trial.
Under the hypothesis that each stage works in state 2 or 3 defined at page 56, the continuity is verified by the stage gain: if its value is no negative, the stage will be continuous.
The procedure used is similar to the working point survey: the total beam power is acquired and no current versus power curve is evaluated.
As shown in Figure 4.12, the algorithm is based on the *Test controller* software in measurements mode. The program loads the given SOA sequence, then the set of SOAs is enabled and the photodiode array acquires the incoming beam, saving the total power in OutputParameters.csv file. If the next sequence is available, it will be loaded, otherwise all the output files are processed by *Matlab* and the data are displayed.

The test is performed twice. Firstly, the beam is emitted by port Output1 and the SOA enable starts from 7.1 up to 7.3 (denoted as Test1). Secondly, the signal is transmitted by port Output2, enabling the SOA with reverse sequence (denoted as Test2).
The loaded sequences are shown in Table 4.5 and Table 4.6: the rows are the sets of SOAs enabled in the same measurement, while the columns represent the SOA indices. The cell contains the current supplied to that SOA in that measurement.

The results are here returned. As shown in Figure 4.13(a), Test1 shows that the SOAs from 12.4 attenuate, leading to the hypothesis that the optical path is broken from that stage. Nevertheless, as shown in Figure 4.13(b), from the path opposite direction, Test2, the SOAs from the 12.4 however attenuate. This leads to the conclusion that only the SOA 12.4 attenuates, as will be better specified in the chapter 5.

The tests are also repeated breaking the optical path between photonic integrated switch and photodiode array: the obtained optical distribution is equal to the noise pattern, this proves that the collected data are not

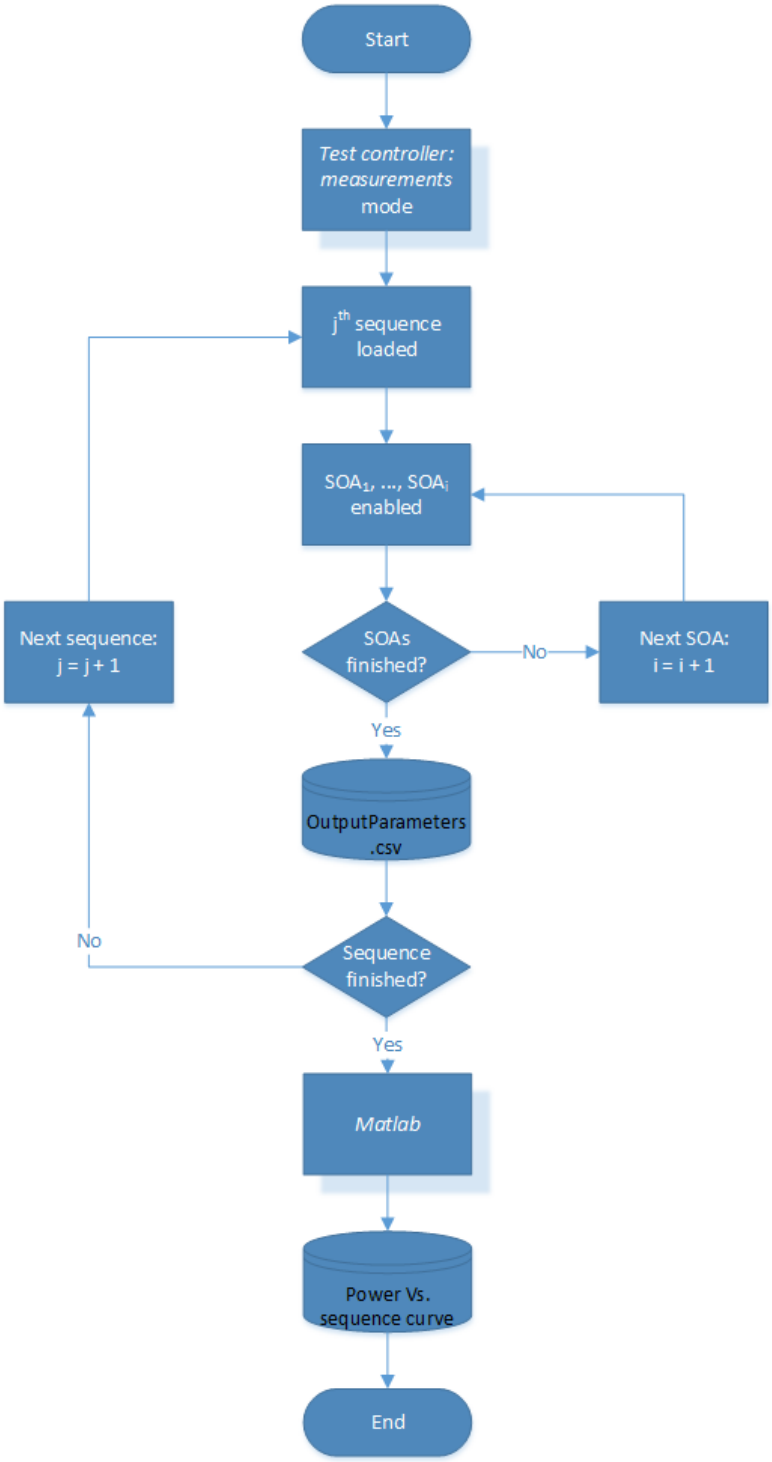


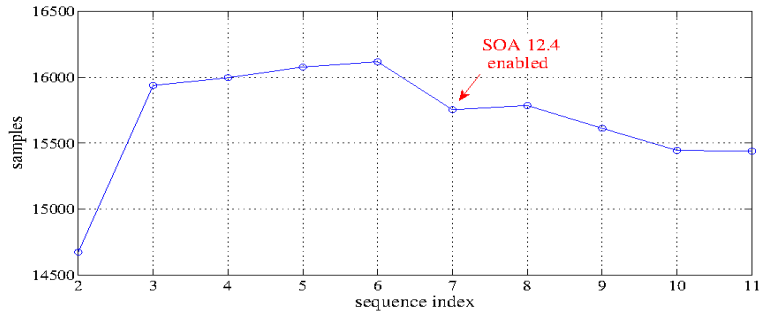
Figure 4.12. Flowchart of optical continuity test.

Table 4.5. Test1, SOA test sequences from 7.1 to 7.3: the rows indicate the input sequences, the columns show the SOA indices, the cells contain the current supplied in mA.

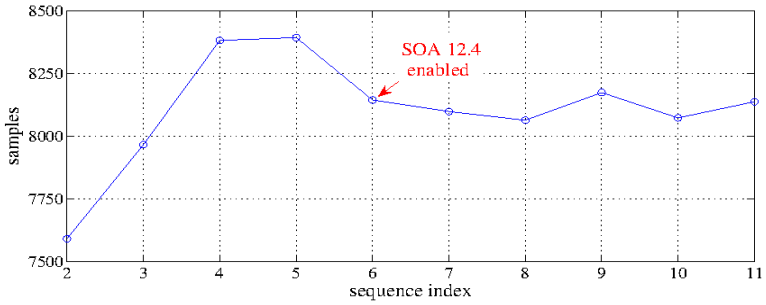
Sequence	SOA									
Index	7.1	8.2	9.6	11.6	12.2	12.4	11.8	9.8	8.4	7.3
1	0									
2	30									
3	30	60								
4	30	60	40							
5	30	60	40	20						
6	30	60	40	20	28					
7	30	60	40	20	28	255				
8	30	60	40	20	28	255	40			
9	30	60	40	20	28	255	40	255		
10	30	60	40	20	28	255	40	255	60	
11	30	60	40	20	28	255	40	255	60	30

Table 4.6. Test2, SOA test sequences from 7.3 to 7.1: the rows indicate the input sequences, the columns show the SOA indices, the cells contain the current supplied in mA.

Sequence	SOA									
Index	7.3	8.4	9.8	11.8	12.4	12.2	11.6	9.6	8.2	7.1
1	0									
2	30									
3	30	60								
4	30	60	255							
5	30	60	255	40						
6	30	60	255	40	255					
7	30	60	255	40	255	28				
8	30	60	255	40	255	28	20			
9	30	60	255	40	255	28	20	40		
10	30	60	255	40	255	28	20	40	60	
11	30	60	255	40	255	28	20	40	60	30



(a)



(b)

Figure 4.13. Optical continuity test results. The power in sample curves versus the sequence index is shown. The first sequence is not shown because it is the interference pattern and is used for interference cancellation: Test1 (a) and Test2 (b) results.

provided by low frequency EM interferences.

4.4 Test performances

The optical test speed is one of the most important project requirements. Therefore, in this section the time performances are analysed for each assessment step. Moreover the time consumption causes are studied. The times required are shown in Table 4.7.

Preliminary operations. The calibration and collimation procedures are the most time-expensive steps.

Table 4.7. Time consumption of test procedures.

Test	Step	Time
Preliminary operations	Calibration	$\simeq 10h$
	Collimation	$\simeq 4h$
Waveguide characterization	Waveguide position	$2Min.$
	Current vs. power	$29Min.$
Optical continuity	Current calculation	$\simeq 5h$
	Working point survey	$8Min.$
	Optical path continuity	$8Min.$

The current controller calibration required about $10h$. The collimation was performed, the first time, in few days: this time was necessary to define the correct procedure. The second attempt needed less time: few hours instead of days.
The IR camera and photodiode array positioning are the most time-consuming stages, although the rail used to move them simplifies the procedure. Finally, the preliminary operations are performed only once for each PIC prototype. Therefore the time required is not related with the further test types.

Waveguide characterization. The tests on the waveguide position are performed in $8Min.$. The most important delay is introduced by the cooling down time introduced by the safety rules at page 49. The vertical alignment needed for the unwanted tilt is not time-consuming, because, it is performed during the cooling down pause, without optical source.
The current versus power characteristics with 75 current samples required $29Min.$ per SOA by virtue of the *Test controller* totally automated procedure.

Optical continuity test. The maximum current calculation time was $5h$. Each working point survey required, in average, 4 measurements of $8Min.$, in order to avoid the PIC overheating. However, the maximum current de-

pends on SOA dimensions, and on the working point of the PIC prototype: therefore, these steps are performed only once for each photonic integrated switch architecture.

Finally, the test of the entire paths are completely automated by the *Test controller*. Therefore the total measurement time is less than $8Min.$.

Chapter 5

Discussion

The purpose of this chapter is to separate the results and the data collected during the project from their interpretation. Here, the issues observed during the entire project are analysed and their causes and possible solutions are discussed. Moreover, the results provided in chapter 4 are interpreted. The topics are dived into sections, each one of which is named after the test which provided the data discussed.

5.1 Spatial resolution

The photodiode array spatial resolution is provided by two separated tests: the one on the Photodiode array spatial resolution, described at page 30, and the one on the Waveguide positions, described at page 53. The first trial provides the minimum recognizable distance between two beams equal to $980\mu m$. This value is contradicted by the second test, in which the minimum distance between the SOAs 1.1 and 1.3 is equal to $560\mu m$.
The reason of these different results could be the misalignment of the second source used during the Photodiode array spatial resolution. As shown in Figure 5.1, if the incoming beam is not perpendicular to the beamsplitter facet ($\beta \neq 0°$), the outgoing beam will not be parallel to the MLA beam ($\alpha \neq 45°$). Therefore, the beams acquired by the PDA are not parallel and

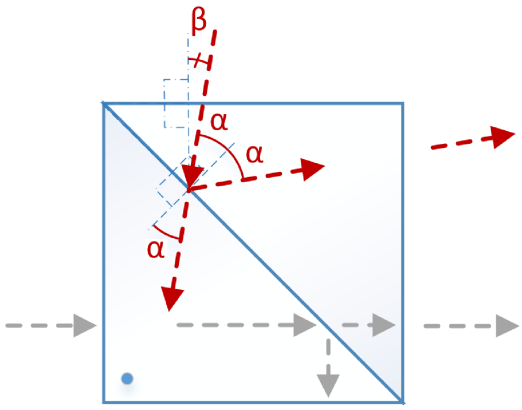


Figure 5.1. Source tilt diagram scheme, referred to Photodiode array spatial resolution test-bed: grey arrows show the MLA collimated beam, while red arrows illustrate the second laser beam. Regarding this one: β is the angle between the real and theoretical wavefront directions, α is the angle between the incident ray and the normal to the interface [43].

the recorded peak distance is not significant of the real spatial resolution. The Waveguide positions test is performed using two photonic integrated switch waveguides and the provided beams are in this case parallel: therefore, the reliable minimum spatial resolution should be $560\mu m$.

5.2 Waveguide positions

The Waveguide positions test at page 53 provides different peak pitches. The causes could be the following:

1. the real waveguide pitches are not equal to L_{wg};

2. a mechanical crosstalk and hysteresis is present in the positioners used during the test-bed setup;

3. Possible presence of different beam magnifications for the different waveguides.

The first reason could not be verified due to the fact that the PIC is flip chip bounded, preventing the visual inspection. The second cause could be verified changing the positioner.
Finally, the beam magnifications are originated by the tilt between the microlens array and the photonic integrated switch, defined at page 53. This could cause an unwanted different magnification for each waveguide. Specifically, the horizontal and vertical tilts could place each waveguide near the focal point but in various positions, producing magnified beams with different traversal magnifications. Therefore, the beams are not parallel providing various peak pitches.
The problem could be verified moving backward the PDA: if the new peak distribution is changed, the beams will diverge with different magnifications, it proves the magnification problem and could be solved avoiding the tilt issue.

5.3 Microlens array tilt

The tilt problem is defined at page 53, where a relative tilt on horizontal and vertical plane between the MLA and the photonic integrated switch is described. The solutions could be the change of PIC positioner, with a holder able to control the tilt angle, for instance a 6 axis stage.

5.4 Current versus power characteristic

The results provided by the Current versus power characteristic at page 55 show the SOA 1.3 fault. This fault could be caused by SOA deterioration. Besides, the same trial shows the better performance of outer edge SOAs (1.1 and 7.1) than the 7.3 as displayed by higher curve slants.
Furthermore, the considerable curve slopes at lowest current shown in Figure 4.6 should be underlined. They could be caused by the enable of all the 4 waveguides of each edge SOA.

5.5 Optical continuity

The optical continuity test, performed at page 56, provides results able to prove the test-bed capability to study an entire PIC optical path. However, the cavity resonant effect did not take place due to the SOA 12.4 loss. Its working point was not found, due to the fact that the maximum current controller output current was reached. The solution could consist in using the 12.3 pad in order to supply a greater current and find the working point. Nevertheless, as shown in Figure 4.13, the power drop after the SOA 12.4 enabling could not be caused by the missing working point but by the overheat. Indeed, the SOA 12.4 supplied current is lower than the working point but it increases the PIC temperature. Consequently the optical power decreases. It is possible that the power reduction is caused by 2 reasons: mismatch of 12.4 working point and overheating originated by the largest SOAs in the optical path. The solution to this problem could be the PIC heat sink installation, which allows to control the PIC temperature and limits the power drop. Otherwise, the produced heat could be decreased by a drastic reduction of the SOA 12.4 enable time.

Chapter 6

Conclusion and outlook

In this master thesis work a new automated optical test of photonic integrated switches is assembled and evaluated.
The report has been organized in 3 stages: firstly, the test requirements are defined in chapter 2, secondly, the selection and verification of the test-bed components are reported in chapter 3 and, finally, the test-bed performances are evaluated by trials of the photonic integrated switch in chapter 4.
All the project requirements of:

1. relaxed precision and still reliable alignment;
2. multiple port assessments at the same time;
3. independence from the chip layout;
4. real-time alignment and measurements;
5. high automation via software control;

have been achieved.
The test-bed components are the microlens array, the photodiode array and its interface, the *Test controller* and the *Data displayer* software. The microlens placement distance allows relaxed precision and reliable alignment. The *Data displayer* software is a trustworthy tool aiding the operator during

the PIC alignment and drastically reducing the microscope use.
The *Test controller* program is capable to manage the entire test-bed: from the photonic integrated switch emission, through the photodiode array control, to the data acquisition. Furthermore, it can manage the photonic integrated switch and PDA in 2 modes: manual, for alignment procedure, and automated, for the tests, performing hundreds of measurements without operator intervention.
Besides, the test flexibility has been verified in terms of multiple ports assessment and chip layout independence: the MLA and the photodiode array are designed to allow multiple port assessments, up to 48 waveguides, at the same time, while the PIC change requires only to redefine one look-up table of *Test controller* software. Furthermore, the beam collimation increases, even more, the test flexibility allowing to add more components to the test, as verified during the spatial resolution analysis at page 30.

The result is a complete fulfilment of test-bed requirements with reduced time-consumption, since the test duration becomes few hours instead of few months of the previous procedure.

The test configuration results also very promising to support more complex procedures. The future developments could move in 4 directions:

1. optical input. The actual studied beams are produced by SOA amplified spontaneous emission, while the next step could be to transmit an external optical input toward the photonic integrated switch ports.

2. Improved test-bed automation. The operator intervention could be indeed further reduced. The next steps could be the support for self-alignment and self-collimation procedures through the software control of motorized positioners. Moreover, the current absorption test could be performed by automated software procedures providing the current value to the *Test controller* program.

3. Further test hasten. The trial time-consumption could be optimized

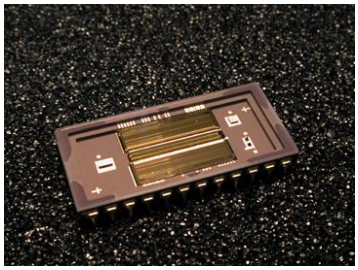
reducing the delays. The cooling down pauses could be reduced, or avoided, implementing proper heat sink system in order to control the photonic integrated switch temperature.

4. Advanced data processing. The software futurable developments are innumerable and very promising due to its high flexibility. Improved features for theoretical gaussian beam calculation and matching, as well as multi peak recognition and improved test-bed management features are only few examples of the software capabilities.

Appendix I

Component Datasheets

In this chapter is reported the datasheet of *PDA-640 SFF InGaAs Photodetector Sensor* [44] and the datasheet of *640 Pixel Linear PD Array Demo Board* [45] by *Princeton Lightwave Inc.*.



PDA-640-SFF
Small Form Factor 640 Pixel, InGaAs Photodetector Sensor with High Speed Readout

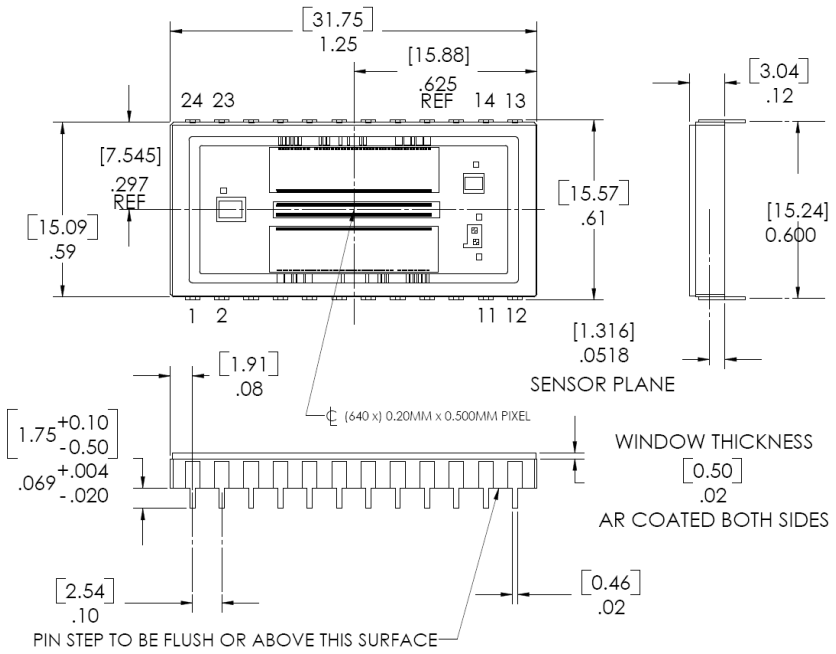
The Princeton Lightwave 640 pixel detector consists of an InGaAs photodetector array hybridized with a high speed, low noise readout circuit. The hybridized array is mounted on low profile ceramic leaded package, with an optical window. Optically black pixels are provided for real-time dark voltage offset correction. This device is ideal for low noise spectroscopy in industrial sensing, telecommunication and defense applications. It is qualified to t Telcordia 468 CORE.

ABSOLUTE MAXIMUM RATINGS

Parameter	Unit	Min.	Typ.	Max.
VDD / Analog supply voltage		4.75	5.0	5.25
Operating temperature range	deg C	-20	25	70
Storage temperature range	deg C	-40		85

Mechanical Layout

(Dimensions are in [mm] / inches)



Pin Designations

Pin	Signal	Pin	Signal
1	VDD_D	24	N.C.
2	VDD_A	23	RESET
3	VSS_D	22	C_{INT} SELECT
4	VSS_A	21	VSS_A
5	Even Vid1	20	Odd Video 2
6	Even Vid2	19	Odd Video 1
7	VSS_A	18	V_{REF}
8	Case Gnd (VSS_D)	17	V_{PDA}SET
9	Integrate	16	VSS_A
10	Clock	15	BW
11	Anti-bloom	14	R_{THERM2}
12	N.C.	13	R_{THERM1}

Princeton Lightwave 640 Pixel Small Form Factor InGaAs Sensor

Sensor Performance

Specifications at VDD=5.00, VSS=0V, T_{CHIP}=25°C, unless otherwise indicated.					
Parameter	**Units**	**Condition**	**Min**	**Typ**	**Max**
Active Pixels	pixels	-		640	
Pixel Dimensions – Pitch and Height	um x um			20 x 500	
Optically Black Pixels - note 1	pixels	-		16	
Inoperable Active Pixels	pixels	-			0
Peak Wavelength	nm	-		1550	
Quantum Efficiency	%	1100-1700 nm		70	
Responsivity	nV/photon	C_{INT} =HIGH C_{INT} =LOW	10 75	12 90	14 105
PRNU	%	80% V_{SAT}		±5	±10
Linearity	%	20-80% V_{SAT}, T_{INT}=50mS			5
VDD	V		4.75	5.00	5.25
IDD	mA			85	120
VSS	V			0	
R_{THERM}	ohms		4900	5000	5100
VRef	V		3.15	3.25	3.35
Clock					
HIGH	V			VDD	
LOW	V			VSS	
Frequency	MHz		0.01		5.00
Duty Cycle	%		45	50	55
Integrate					
HIGH	V			VDD	
LOW	V			VSS	
WIDTH			10 Clocks or 20 usec.		
C_{INT} Select					
HIGH (High Dynamic Range)	V			VDD	
LOW (High Sensitivity)	V			VSS	
Full Well Capacity					
C_{INT}=LOW	pC e-			3.19 2.00 X 10^7	
C_{INT}=HIGH (default)	pC e-			24 1.50 X 10^8	
Gain					
C_{INT}=LOW	nV/e-		105	120	135
C_{INT}=HIGH	nV/e-		14.0	16.0	18.0
V_{SAT}	V		2.0	2.4	2.8
Dark Rate	V/Sec			0.3	1.9
Readout Noise					
C_{INT}=LOW	e-/rt-scan			1000	1600
Dynamic Range	dB	F_{CLK} = 250KHz	41	43	
C_{INT}=HIGH	e-/rt-scan	BW Select = LOW		3800	6000
Dynamic Range	dB		44	46	
Crosstalk	dB				-30
Video Output					
Impedance	ohms				2000
Settling time (to 16-bits)	ns				100
Pixel Rate - note 2	MP/S		0.1		10

Note 1: Dark pixels are optically opaque pixels provided for real-time dark offset correction.

Note 2: Maximum rate of 5MPS per video output, 2 interleaved video outputs, (10MPS total).

Signal Descriptions

Pin	Type	I/O	Signal	Description
1, 2	Power	Power	V_{DD}	Device power supply, +5.0V nominal. Bypass capacitors of 0.1uF and 10uF close to the package pins are recommended for optimum noise performance.
3,4,7,16,21	Power	Power	V_{SS}	Device power supply return.
5	analog	O	Even Video1	Even pixel zero video reference level. May be used for differential subtraction of video offset level. Signal is typically 3.25V
6	analog	O	Even Video2	Even pixel video signal. Pixel video levels are updated on the clock falling edge. Dark signal is approximately 3.25V, saturated signal is approximately 1.25V
8	Power	Gnd	Case GND	May be connected to power supply ground in the user's application
9	digital	I	Integrate	Integration and readout control. Integration begins 5.5 clock cycles after the rising edge and ends 3.5 clock cycles after the falling edge. (Integration time=T_{INT}-2 Clk). Active pixel video readout begins with pixel #1, 12 clock cycles after the falling edge. Minimum high time is the greater of 20us or 10 clocks.
10	digital	I	Clock	Pixel readout clock
11	digital	I	Antibloom	Antibloom Enable - active high. Internal pull-down for disabled state if left unconnected.
13	analog	passive	R_{THERM1}	5Kohm thermistor connection
14	analog	passive	R_{THERM2}	5Kohm thermistor connection
15	digital	I	BW Select	CTIA Bandwidth Select. Internal pull-down. For best noise performance with pixel clocks of <1MHz, this pin should be tied low or left unconnected. For pixel clocks above 1MHz, this pin should be tied high for faster video settling time.
17			V_{PDA}SET	Controls reverse bias to the InGaAs photodiode array. No connection required for 0V bias, may be bypassed with 0.1µF to ground for lowest noise performance. 3.25V nominal (0V Bias), More positive drive voltage causes negative PDA bias.
18	analog	O	V_{REF}	Video reference level, typically 3.25V. May be bypassed externally with 0.1uF for improved noise performance.
19	analog	O	Odd Video 1	Odd pixel zero video reference level. May be used for differential subtraction of video offset level. Signal is typically 3.25V
20	analog	O	Odd Video 2	Odd pixel video signal. Pixel video levels are updated on the clock rising edge. Dark signal is approximately 3.25V, saturated signal is approximately 1.25V
22	digital	I	C_{INT} Select	Integration capacitor select - Internal pull-up for high dynamic range mode (10pF Cint) if left unconnected.
23	digital	I	Reset	Device reset - active low. Device contains a 0.1µF reset capacitor to ground and a 70µA pull-up current to provide power-on reset function (Reset for ~5ms at power-on). Pin may be left unconnected, or driven low by the user for device reset.
12, 24		-	no connection	Pins should be left unconnected.

1. Principles of Operation

The PLI 640 linear array contains an InGaAs photodiode array with 640 “active” pixels on a 20um pitch and 16 “dark” pixels available for user dark offset correction. The CMOS read-out integrated circuit architecture consists of capacitive transimpedance amplifiers (CTIA), in which the photocurrent is buffered, amplified and stored, and a video multiplexer for read-out of the integrated charge values. The CTIA architecture is illustrated in Figure 1.

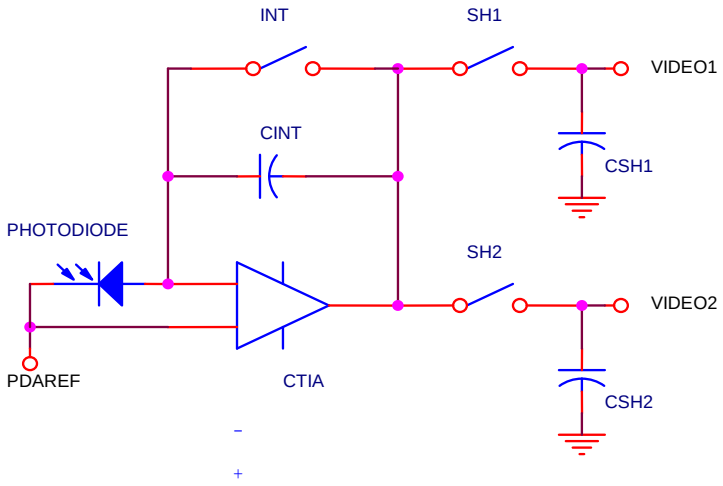


Figure 1. PLI 640 array pixel integration architecture.
PDAREF and control signals for INT, SH1, and SH2 are generated internally.

Within each read-out pixel is a CTIA with the photodiode at the input. During the integration period, the photocurrent is integrated on the feedback capacitor CINT. Two values of feedback capacitor are available, (1.33pF and 10.0pF), and can be selected externally

Nominally, there is a –5mV bias across the photodiodes. Referring to Figure 1, the level of this bias is set at PDAREF. PDAREF is generated internally as a fixed offset to the VREF potential. VREF is nominal fixed at 3.25 V by a built-in bandgap reference. The actual bias across the photodiode can vary ±5 mV from the 5mV nominal set-point. Each pixel will exhibit a dark current of; Idark = (VPDAREF-VREF)/Ro; (the pixel's bias divided by that pixel's shunt resistance). Photodiode dark current appears as a fixed pattern noise (FPN) that deviates both positively and negatively from the zero signal level ($\mathbf{V_{REF}}$).

There are two sample-and-hold circuits at the output of the each pixel's CTIA. This allows the array to operate in a parallel-in, serial-out "snapshot" mode. Between exposures, all of the pixels are held in reset (CINT discharged), then released so that the "zero" levels can be captured with the first sample-and-hold capacitors (CSH1). Following the integration time, the total charge levels are captured with the second sample-and-hold capacitors (CSH2). The pixels are then read out sequentially through a video multiplexer stage. Both the initial signal (**Video 1**) and the final signal (**Video 2**) will deviate from $\mathbf{V_{REF}}$ with bipolar dark current and negative-going photocurrent.

In a typical application, **Video 1** and **Video 2** can be differentially amplified as a form of external correlated double-sampling. This technique eliminates much of the multiplexer related switching noise.

The Integrate/Read-Out sequence is shown in Figure 2.

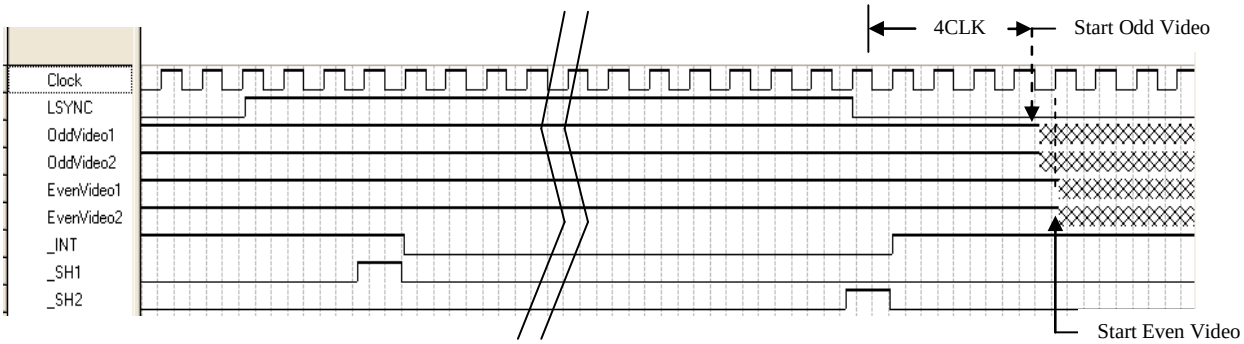


Figure 2. PLI 640 Array Integrate/Read-Out sequence
Clock & Integrate and are provided by the user. _INT, _SH1, and _SH2 are generated internally.

- While waiting for a line sequence to be initiated, the CTIA feedback capacitors are held in reset. Upon assertion (the rising edge of **Integrate**), the following events occur:

  1. The INT switch is opened, which allows charge to accumulate.
  2. SH1 is activated to sample the signal at the beginning of charge integration.
  3. Charge continues to integrate on the feedback capacitor.

- When the line sequence is terminated (on the falling edge of **Integrate**), the following events occur:

  1. SH2 is activated to sample the signal at the end of charge integration.
  2. The INT switch is closed, draining charge from the feedback capacitors.
  3. The shift registers begin operation so that the pixel-by-pixel pre-integration and post-integration charge signals appear at **Video 1** and **Video 2** serially.

All of the above functions are generated internally.
The user need only provide a continuous master clock (**Odd Clock/Even Clock**) and a line-trigger/integrate pulse (**Integrate**).

2.0 Operating the PLI 640 Array

2.1 General Considerations

1. Power Supply: 5.0VDC ±5%

2. Power Supply Decoupling: It is recommended to decouple the power supply using 0.1uF and 10uF capacitors in parallel, mounted close to the $\mathbf{V_{DD}}$ and $\mathbf{V_{SS}}$ pins.

3. V_{REF} is an internally generated bias. It may be bypassed using a 0.1uF capacitor to signal ground for best noise performance.

4. Reset contains a 0.1uF reset capacitor with a weak pull-up to provide automatic power-on reset function. Nominal power-on reset time is 5ms. The pin may be driven externally to force a reset or alter power-on reset timing.

3. Timing is derived from a continuous master clock (**Odd Clock/Even Clock**). A single control line (**Integrate**) is used to initiate the integration, end the integration, and initiate the serial video readout.

4. To avoid transients at the start of video readout, the output amplifiers are clamped to the **V_{REF}** potential when the video readout circuitry is inactive. This reference potential is approximately 3.25 V, and represents the true zero signal level.

5. Observe video setup and hold times (t_{VS}, t_{VH}) to ensure the acquisition video sampling point has allowed the signal to settle to full accuracy.

6. The default integration capacitance is 10.0 pF which is the high dynamic range mode. If **C_{INT} Select** is tied LOW, the integration capacitance is 1.33 pF, which is the high sensitivity mode.

2.2 Pixel Configuration

1. Odd Video 1 & 2 outputs are updated on each Odd Clock falling edge.

2. Even Video 1 & 2 outputs are updated on each Even Clock rising edge.

3. Even Clock and Odd Clock are normally tied together.

4. Video read-out is initiated by the rising edge of the Integrate signal (end of integration).

5. “Active” Pixels: 640 active pixels on 20um pitch, (12.8mm line width). Video information is inverted, where a signal level about 3.25V represents the dark level and about 1.25V represents full scale brightness.

6. “Dark” Pixels: 16 dark pixels are provided, 8 on each side of the active array. Dark pixels are integrated with all active pixels and appear in every line read-out. Dark pixels may be used for systematic dark offset correction.

7. “Buffer” Pixels: 14 buffer pixels between active and dark pixels. Buffer pixels provide an optical margin between the active pixels and dark pixels. Video output values of buffer pixels are indeterminate.

Pixel Sequence of Video Outputs

Assumes common **Even Clock** and **Odd Clock**.
Pixel positions are in reference to the falling edge of Integrate (End of Integration)

		---> Start of Dark Pixels									---> Start of Buffer Pixels							---> Start of Active Pixels					
Channel	O	E	O	E	O	E	O	E	O	E	O	E	O	E	O	E	O	E	O	E	O	E
Type	DRK1	DRK2	DRK3	DRK4	DRK5	DRK6	DRK7	DRK8	BUF1	BUF2	BUF3	BUF4	BUF5	BUF6	1/640	2/640	3/640	4/640	5/640	6/640
Clock	4F	5R	5F	6R	6F	7R	7F	8R	8F	9R	9F	10R	10F	11R	11F	12R	12F	13R	13F	14R

Clock numbers are in reference to falling edge of of L_{SYNC} and indicate the clock edge on which the pixel value is updated in the video stream

- 1st Dark Pixel appears on the odd channel at the 4th falling edge of **Odd Clock** after the falling edge of L_{SYNC}.
- 1st Buffer Pixel appears on the odd channel at the 8th falling edge of **Odd Clock** after the falling edge of L_{SYNC}.
- 1st Active Pixel appears on the odd channel at the 11th falling edge of **Odd Clock** after the falling edge of L_{SYNC}.

	End of Active Pixels--->|								End of Buffer Pixels--->|										End of Dark Pixels--->|	
Channel	O	E	O	E	O	E	O	E	O	E	O	E	O	E	O	E	O	E	O	E
Type	637/640	638/640	639/640	640/640	BUF7	BUF8	BUF9	BUF10	BUF11	BUF12	BUF13	BUF14	DRK9	DRK10	DRK11	DRK12	DRK13	DRK14	DRK15	DRK16
Clock	329F	330R	330F	331R	331F	332R	332F	333R	333F	334R	334F	335R	335F	336R	336F	337R	337F	338R	338F	339R

- Last Dark Pixel appears on the even channel at the 331st rising edge of **Even Clock** after the falling edge of L_{SYNC}.
- Last Buffer Pixel appears on the even channel at the 335th rising edge of **Even Clock** after the falling edge of L_{SYNC}.
- Last Active Pixel appears on the even channel at the 339th rising edge of **Even Clock** after the falling edge of L_{SYNC}.

2.3 Timing

The only control signals required to operate the ROIC are a continuous master clock (CLK) and an exposure time signal (Integrate).

1. **Odd Clock** and **Even Clock** pins are normally tied together.

2. **Clock** should run continuously to allow internal timing functions to occur. If the clock has not been run for an extended duration, or power has been recently applied, the device should be run through an integration/read-out cycle to completely reset the device.

3. The clock frequency should not exceed 5 MHz. Odd pixels are read-out at the falling edges of **Odd Clock**, and even pixels are read-out on the rising edges of **Even Clock**. (Two pixels are delivered every clock period, for a maximum composite readout rate of 10 million pixels per second.

4. **Integrate** should rise and fall on the rising edge of the clock. The minimum duration of **Integrate** high time is 10 clock cycles or 20 µs; whichever is longer. The actual integrated exposure time is three clock cycles less than the total duration of **Integrate** high period.

5. Active pixel #1 video levels will appear at the **Odd Video 1 & 2** pins beginning at the 11th falling edge of **Odd Clock** after the falling edge of **Integrate**.
   Active pixel #2 video levels will appear at the **Even Video 1 & 2** pins beginning at the 11th rising edge of **Even Clock** after the falling edge of **Integrate**.

6. The next exposure can begin anytime after the readout of the previous exposure is complete. (The minimum duration of **Integrate** LOW between integrations is 340 CLK cycles to ensure complete read-out of the previous integration line).

7. **Video1** and **Video2** outputs are clamped to $\mathbf{V_{REF}}$ level between active readout periods.

2.3.1 Clock and Integrate Timing

The Clock and **Integrate** timing requirements are shown in Figure 3:

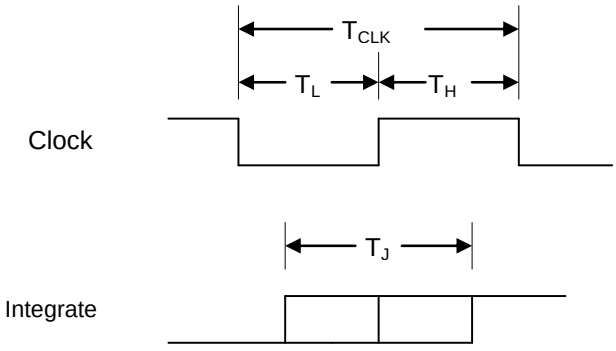


Figure 3. Timing relationships for Integrate and CLK.

1. T_{CLK} is the master clock period. It must be at least 200ns long (maximum clock freq is 5 MHz) and no longer than 100us (minimum clock freq is 10 kHz).

2. CLK will typically have a 50% duty cycle, however, what is explicitly required is that both T_H (the high half period) and T_L (the low half period) be a minimum of 90 ns.

3. Both the rising and falling edges of **Integrate** should occur on the rising edge of the clock. The allowable **Integrate** edge jitter (T_J) is $\pm T_{CLK}/3$.

2.3.2 Video Timing

The timing of the pixel video output is summarized in Figure 4:

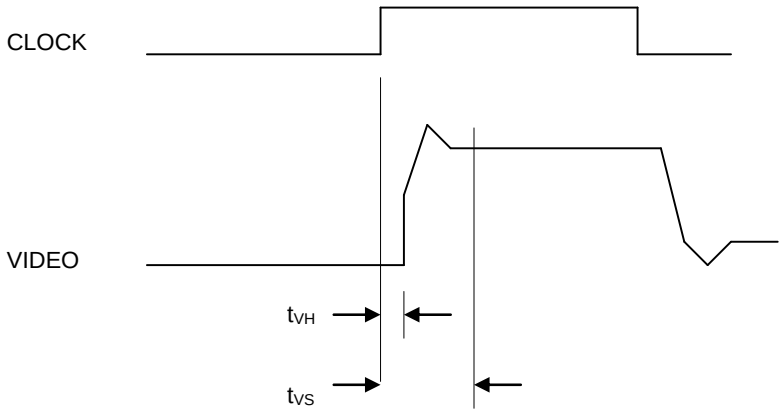


Figure 4. Pixel video timing

1. Video Hold Time: (t_{VH}): The minimum time between detection of a clock edge and the beginning of the transition to the next pixels video level. It is less than 50 ns.

2. Video Setup Time (t_{VS}): The maximum time required after detection of a clock edge until the video signal is sufficiently settled so that it can be digitized with 16 bit precision. It is less than 100 ns.

2.4 Thermistor

The sensor module incorporates a thermistor for monitoring the temperature of the photodiode array and electronics.

Thermistor: Negative temperature coefficient (NTC) type with a nominal value of 5Kohms at 25°C.
Thermal Coefficients: Alpha = -4.39%, Beta = 3892±1.0%
Steinhart-Hart Coefficients: $A=1.28745 \times 10^{-3}$, $B=2.357394 \times 10^{-4}$, $C=9.5052 \times 10^{-8}$

PRODUCT HANDLING NOTES

Semiconductor devices are sensitive to electrostatic discharge (ESD) and should be handled with appropriate caution, including the use of ESD protective equipment such as grounding straps and anti-static mats.

640 Pixel Linear PD Array Demo Board

Overview

The 640 Pixel Linear Array Demo Board is supplied with a demonstration program to exercise the array. The demo program uses the supplied dynamic link library, DemoDLL.dll. This library can be used to develop a custom end-user application.

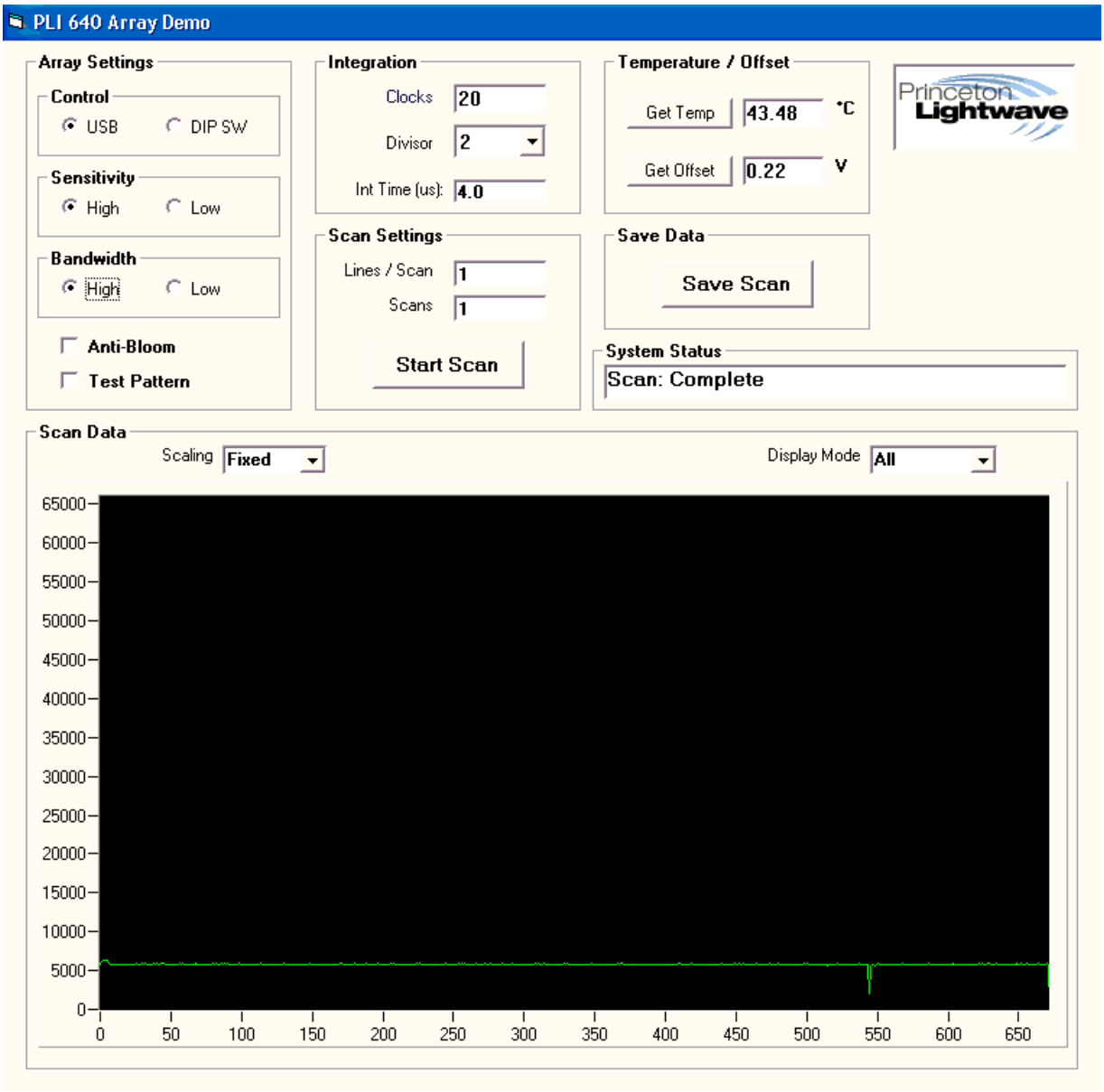
Preparing the Demo Board and Software

This Demo is designed specifically for use on a USB 2.0 "High Speed" port and will not work properly with older USB V1.0 "Full Speed" ports.
This Demo has been verified with Windows XP and Vista systems.

1. Open the folder "Package" on the supplied media, and run Setup.exe. This will install the demo program,PLIDemo640, in the Start Programs group.
2. Plug in the included module power supply and connect to the Demo Board barrel style plug.
3. Connect the supplied USB cable between the PC and the Demo Board.
4. If this is the first use, the PC will indicate New Hardware Detected - QuickUsb. Direct this wizard to the Support folder to select QuickUsb.sys.

Running the Demo Program in USB mode

Go to the Start Programs group and select program "PLIDemo640". The following screen should appear:



The Array operating parameters may be set as follows:

- High or Low Sensitivity.
- High or Low Bandwidth.
- Anti-Bloom On or Off.
- A Test Pattern may be selected instead of an array output for the scan. The Test Pattern has a square wave appearance, and can be used to test the Demo Board to PC communication.

The Integration and Clocking may be set as follows:

- Integration Exposure Clocks may be set to a maximum of 65535.
- The divisor for the master clock used to make the Array Clock may be 2, 4, 8, 16, or 32.
  As supplied, the on-board 10MHz master clock is used and gives a 5MHz Array Clock when a divisor of 2 is selected.
- The Integration time resulting from these settings is displayed.

The Scan parameters may be set as follows:

- The number of lines per scan may be set from **1 to 2047**.
- The number of scans to perform may be set from **1 to 32767** scans.
  The Scan indicator will count down with each scan performed.

Clicking the Scan button begins the exposure and acquisition sequence with the selected parameters.
The acquired data may be saved to a tab delimited text file for easy import into the user's data analysis software. The saved data filename can be specified.

The Get Temp button displays the Array temperature, and the Get Offset button displays a DC offset voltage set by the offset potentiometer on the Demo Board. This voltage is nominally .22VDC and gives about a 5000 count offset to the dark array data. This offset allows measurement of the forward and reverse dark pixel leakage.

The System Status area indicates normal Array/Demo operation or error codes as appropriate.

The Control buttons should be selected for USB or Manual (DIP Switch) operation.

Data Acquisition will begin by pressing the **Start SCAN button**.

The Scan Data may displayed having a Fixed or AutoScale amplitude as selected with Scaling control.

The Display Mode may be:

- All, which displays all the lines in the scan as a long array.
- Last Scan, which displays only the last line of the scan.
- Average, which displays the average pixel values over the number of lines in the scan.

Note
Do not unplug the Demo Board from the USB or the power supply while the Demo Program is running, the Demo program will report operation errors. If this happens, exit the program, plug in the Demo Board and re-start the program.

Demo Board Operating Mode Configuration

The Demo Board contains jumpers and DIP switches which can be used to set board operation modes. This section describes these settings and their use. Default settings are for USB operation where all operating parameters are controlled by the demo software.

J1 - A/D Clock Source. 1-2 on-board source. 2-3 External 2x Clock supplied at JP3-22.

J3 - On-board 10MHz Master clock select, disabled when installed.

J4 - Scan Trigger Source. 1-2 selects USB control. 2-3 selects external trigger supplied at JP3-24.

J5 - External Master Clock Input at pin 1 and Ground at pin2.

J7 - Array Integration Capacitor Select. Position 2-3: (default) USB selection. Position 1-2: selects High Sensitivity. Open (no jumper): selects High Dynamic Range.

J11 - Array Bandwidth Select. Position 2-3: (default) USB selection. Position 1-2: selects High Bandwidth. Open (no jumper): selects Low Bandwidth.

J12 - Array Anti-Bloom Select. Position 1-2 (default): USB selection. Position 2-3: Anti-Bloom enabled. Open (no jumper): Anti-Bloom disabled.

J15 - Array Clock Source. Position 2-3: (default) on-board source. Position 1-2: External Array Clock supplied at JP3-20.

J16 - Array LSYNC Source. Position 2-3: (default) on-board source. Position 1-2: External Array LSYNC supplied at JP3-18.

J17 - TEC Power. Position 1-2: enables TEC power. Open (no Jumper): disables TEC power.

J18 - Odd/Even Switch Select. Position 2-3: (default) selects on-board source. Position 1-2: External 2x Clock supplied at JP3-22, inverted on-board.

J19 - Array TEC Temperature Select. Open (default) selects 25°C. Position 1-2: selects 42°C. Used with J17.

SW4-1 Off (default) selects USB controlled settings. On is for manual operation with DIP Switch and jumper settings.

SW4-4 Off (default) sets USB communication. On selects non-USB operation.

SW1 - The 8 LSB's of the Integration clocks setting. SW1-1 is the LSB.

SW2 - The 8 MSB's of the Integration clocks setting. SW2-8 is the MSB.

The number of integration clocks should be set as N - 1 where N clocks of integration are desired.

SW3 settings:

SW3 -1 - oscillator divisor bit 0, On = 0, Off = 1.
SW3 -2 - oscillator divisor bit 1, On = 0, Off = 1.
SW3 -3 - oscillator divisor bit 2, On = 0, Off = 1.

Example: for 10MHz Master Clock (internal),
0 yields 5MHz Array clock, 10MHz A/D Clock, (SW3-1,2,3 ON)
1 yields 2.5MHz Array clock, 5MHz A/D Clock, (SW3-2,3 ON, SW3-1 OFF)
2 yields 1.25MHz Array clock, 2.5MHz A/D Clock, (SW3-1,3 ON, SW-3-2 OFF)
3 yields 625KHz Array clock, 1.25MHz A/D Clock, (SW3-3 ON, SW3-1,2 OFF)
4 yields 312.5KHz Array clock, 625KHz A/D Clock. (SW3-1,2 ON. SW3-3 OFF)

Note: Divisor must yield an A/D Clock of 625KHz or greater for proper operation.

SW3 -4 – ALWAYS OFF.

SW3 -5 - On selects Test Pattern. Off selects array video.

SW3 -6 - On selects Low BW. Off selects High BW.

SW3 -7 - On selects high sensitivity. Off selects high dynamic range.

SW3 -8 - On disables Anti-bloom. Off enables Anti-bloom.

Common User Configurations:

A. USB with onboard 10MHz oscillator, (default)
Settings: J4 SET1-2, J15 SET 2-3, J16 SET 2-3, J12 SET 1-2, J11 SET 2-3, J7 SET 2-3, J1 SET 1-2, J5 OPEN, J3 OPEN, SW4-1 OFF,SW4-4 OFF, J18 SET 2-3.

B. USB Controlled with External Oscillator
Settings: Same as **A** except, J3 SET 1-2, use external 50% duty cycle square wave applied at J5-1 with Ground at J5-2.
External clock, for operation with USB, should be 1.25MHz to 10MHz.

C. Manual Control with onboard 10MHz Oscillator
Settings: SW4-1 ON, SW4-4 ON, J3 OPEN, J5 OPEN, J7 select, J11 select, J12 select, J1 SET 1-2, J4 SET 2-3, J18 SET 2-3..
1. SW1 sets LS Byte of integration cycle count, and SW2 sets MS Byte of integration cycle count. The number of integration cycles should be set as N - 1 where N clocks of integration are desired.
2. SW3 Sets:

SW3 -1 - oscillator divisor bit 0, On = 0, Off = 1.
SW3 -2 - oscillator divisor bit 1, On = 0, Off = 1.
SW3 -3 - oscillator divisor bit 2, On = 0, Off = 1.

Note: Divisor must yield an A/D Clock 625KHz or higher for proper operation.

SW3 -4 – ALWAYS OFF.
SW3 -5 - On selects Test Pattern, Off selects array video.
SW3 -6 - On selects Low BW, Off High BW.
SW3 -7 - On selects small integration capacitor, Off the larger capacitor.
SW3 -8 - On selects No Anti-bloom, Off enables Anti-bloom.

3. The External Trigger from JP3-24 rising edge begins operation.

D. Manual Control with External Oscillator
Settings: Same as **C** except J3 SET 1-2 and external square wave applied at J5-1 and ground at J5-2.

E. Manual Settings with USB Control
Settings: Same as **A** except set SW4-1 On, and SW4-4 OFF,
Operation: Same as **A** except switches SW1, SW2, and SW3 select array timing and pin settings. The DLL function GetTemperature should not be used in this mode, as it uses USB control for selecting Array data or temperature data.

F. External Drive Mode
Settings: J1 SET 2-3, J15 SET 1-2, and J16 SET 1-2, J18 SET 1-2..
Operation: The user supplies TTL level External CLOCK for the array at IDC-20, LSYNC for the array at IDC-18, and a continuous 2X_CLK for the A/D converter and video switch at IDC-22. In this mode, it is the user's responsibility to supply these in a correct timing sequence, and to externally capture the array samples. The 2X_CLK is used to trigger the A/D converter on the falling edge. This should occur several nanoseconds before the CLOCK edge transitions to allow for sufficient settling time of the signals into the A/D converter. A delayed A/D CLK_OUT with data valid on the rising edge is available at IDC-26.

Demo Board Outputs

A. 16 Bit digital data at IDC Pins 1-16, along with a delayed sample clock at IDC-26. This clock is suitable for use to clock data into an external memory.

B. J13: Raw Analog array Odd video data
J14: Raw Analog array Even video data

C. J10: Buffered analog Odd video data and Even video data. Signal range is approximately 0V to 2.5V (fullscale)

D. TEC Locked LED indicator lights when the TEC controller is locked

E. In USB operation, a test signal is available as alternating TEC V_Temp thermistor voltage and a dark offset voltage. These are digital 16 bit numbers spanning the range of 0V to 2.5V. The offset voltage may be changed from the nominal .22V with potentiometer R34.

640 Array Demo Board Functional Specification.

The 640 Array Demo Board will allow a user to evaluate the 640 array, in the lab or in a system, by adding a light source and optics.

Size

6" X 5" PCB with .15" holes at each corner for mounting.

Power

Power is provided by the included power supply module. The board also uses USB power from the PC host for USB operations.

Interface

The USB 2.0 High Speed Interface allows full speed operation of the array. Windows drivers, the demonstration program, and a USB cable are included. Up to 2047 scans at up to a 13.5KHz scan rate maximum can be acquired and transferred via the USB port.

The board can also be operated without using USB, by setting Dip switches on the board for manual control operation.

Array Operation

Integration time - selectable from 10 clocks to 65535 clocks
Bandwidth Select - High or Low
Integration Capacitor Select – High sensitivity or High dynamic range mode
Anti-Bloom select – Enabled / Disabled
Analog to Digital Clock rate - 10MHz, 5MHz, 2.5MHz, 1.25MHz, 625KHz internal.
Array Clock rate - 5MHz, 2.5MHz, 1.25MHz, 625KHz, 312.5KHz internal.
TEC controller - to keep the array at 25°C/42°C, with LED temperature lock indicator.

Resolution

A 16 bit A/D converter is used, unsigned binary format.

Modes

USB - as above.
Non-USB - All modes selected by DIP switch setting.
- External logic input for edge triggering operation.
- External logic inputs for array CLOCK, LSYNC and 2X A/D converter clock input.

Outputs

- 16 bit A/D data output and a rising-edge-valid clock derived from the 2X A/D converter clock.
- Headers for raw array Odd and Even video output before black level subtraction.
- Header for array Odd and Even video output with black level subtraction.
- LED indicator for TEC lock
- Test video signal for communication interface testing.

External Inputs

- Master Oscillator - input, 3.3V max, 625KHz to 10MHz square wave. 50%duty cycle nom.
- Array Clock - input, at JP3 Pin 20, TTL, 5.5V max
- Array LSYNC - input, at JP3 Pin 18, TTL, 5.5V max
- Converter 2X_CLK - input, at JP3 Pin 22, TTL, 5.5V max
- Ext Scan Trigger - input, at JP3 Pin 24, TTL, 5.5V max. Rising edge triggers an array scan within 1.5 Array Clock periods. Minimum trigger interval is 688 Array Clock periods. Minimum trigger width is 3 Array Clock periods.
-Clock Out - JP3 Pin 26, TTL 3.3V max, rising edge for external latching of 16 Bit A/D data.

Dynamic Link Library Specifics - DemoDLL.dll

The Demo program uses the supplied custom DLL. This DLL is normally placed in the windows/system32 folder.

long FindDemoBd(char *str)
Detects the presence of the Demo Board on a USB and places the deviceName in the char array **str** if found or empty if not found. Returns Error Code.

long GetHiSpeedCapable(long *UsbSpeed, char *deviceName)
Detects the speed capability of the attached USB connection **deviceName** . If **USBSpeed** bit7 is high then the USB connection is High Speed, otherwise it is not. High Speed connection is required. Returns Error Code.

long SetDemoBdTimeout(long timeout,char *deviceName)
Allows the Demo Board Time Out setting **timeout** to be between 100 milliseconds and 60000 milliseconds for **deviceName**. The Demo program uses 20000 milliseconds. Returns Error Code.

long GetTemperatureAndOffset(double *Data, char *deviceName)
Places Temperature and Voltage Offset in **Data** from **deviceName. Data**[0] is the temperature in degrees C. **Data**[1] is the offset voltage in volts. Returns Error Code.

long Scan(unsigned long NumLines,long *Data, char *deviceName)
Performs an Array Scan on **deviceName** of **NumLines** and places the values in a one dimensional array **Data.** The calling program should allocate 672***NumLines** space to hold the **Data**. Returns Error Code.

long SetArrayParams(int ClockDivisor,int SetAntiBloom,int SetHighBandwidth,int SetLargeCapSize,int SetTestPattern,char *deviceName)
Sets Array operating parameters: **ClockDivisor** 1..5. Array Clock frequency is (Master Clock Frequency)/(2^**ClockDivisor).** Settings use 1 to **Set** or 0 to not set. Returns Error Code.

long SetExposureClocks(long clks,char *deviceName)
Sets the number of exposure clocks to **clks** -1 on **deviceName.** The maximum value for **clks** is 65535. Returns Error Code.

Error Codes:

NoError = 0
DemoBdNotFound = 1
ParamOutOfBounds = 2
TimeOut = 3

FifoNotEmpty = 4

Sample Visual Basic Declarations:

Declare Function SetExposureClocks Lib "DemoDLL" (ByVal clks As Long, ByVal devName As String) As Long

Declare Function SetArrayParams Lib "DemoDLL" (ByVal ClockDivisor As Integer, ByVal SetAntiBloom As Integer, ByVal SetHighBandwidth As Integer, ByVal SetLargeCapSize As Integer, ByVal SetTestPattern As Integer, ByVal devName As String) As Long

Declare Function FindDemoBd Lib "DemoDLL" (ByVal str As String) As Long

Declare Function SetDemoBdTimeout Lib "DemoDLL" (ByVal TimeOut As Long, ByVal devName As String) As Long

Declare Function Scan Lib "DemoDLL" (ByVal NumLines As Long, ByRef Data As Long, ByVal devName As String) As Long

Declare Function GetTemperatureAndOffset Lib "DemoDLL" (ByRef TData As Double, ByVal devName As String) As Long

Declare Function GetHiSpeedCapable Lib "DemoDLL" (ByRef UsbSpeed As Long, ByVal devName As String) As Long

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Appendix II

Calculations and demonstrations

Photodiode array maximum received power

The estimation of photodiode maximum received power is here calculated. The *Princeton Lightwave Inc.* recommends a intensity power (I) lower or equal to $I_{max} = 3\frac{mW}{px}$ for a limited fraction of the entire sensor surface [46]. Defined A_{tot} the total pixel surface hit by the beam and assuming the power distribution to be constant along the beam wavefront, the total received power P_{rx} is calculated by (II.1).

$$P_{rx} = I \cdot A_{tot} \leq I_{max} \cdot A_{tot} = P_{rx,max} \tag{II.1}$$

The pixel dimensions are $20 \times 500\ \mu m \times \mu m$, therefore $I_{max} = 300\frac{KW}{m^2}$.
In case of only 1 source enabled, its maximum beam wavefront area will be equal to the MLA lens surface. Indeed, even if the divergent beam has an area greater than that, the only part on the lens surface is collimated and reaches the PDA. As a result, $P_{rx,max}$ is calculated through (II.2).

$$P_{rx,max} = I_{max} \cdot \pi\Big(\frac{L_{wg}}{2}\Big)^2 = 14.7mW = 11.67dB_{mW} \tag{II.2}$$

The maximum transmitted power $P_{tx,max}$ is calculated by the link budget equation since the 50 : 50 beamsplitter [35] loss ($L_{bs}[dB]$) is equal to $3dB$ and the path-loss is negligible ($L_A[dB] = 0dB$), the result is calculated by

(II.3).

$$P_{tx,max}[dB_{mW}] = \begin{cases} 14.68dB_{mW} & \text{if beamsplitter is used,} \\ 11.67dB_{mW} & \text{otherwise.} \end{cases} \quad \text{(II.3)}$$

The $P_{tx,max}$ here defined cannot be achieved by the PIC but only through the lasers used during the preliminary tests. This makes the hypothesis of only 1 source valid.

Relation between samples and optical power

The linear relation between optical power in samples and Watt units is here demonstrated.
The received power P_{rx} is calculated by its relation with the received energy (II.4).

$$P_{rx} = \int_0^{T_{int}} E_{rx}(t)dt \quad \text{(II.4)}$$

Planck relation [47] for a photon defines the energy given by each photon indicating with h the Planck constant, c the speed light in free-space and λ_0 the wavelength of electromagnetic field associated with the photon, the energy of a received photon is given by (II.5). The i^{th} pixel receives in the interval time t $N_\gamma(t,i)$ photons, therefore $E_{rx}(t)$ is the sum of received pixel energy which is given by the product between E_γ and $N_\gamma(t,i)$ (II.6).

$$E_\gamma = \frac{h \cdot c}{\lambda_0} \quad \text{(II.5)}$$

$$E_{rx}(t) = E_\gamma \cdot \sum_{i=1}^{640} N_\gamma(t,i) \quad \text{(II.6)}$$

The V_{out} in (3.2) is analogue-to-digital converted. The number of samples $N_{sample}(t,i)$ of i^{th} pixel at time t is linked with the number of photons $N_\gamma(t,i)$ by the number of samples of each photon $N_{\gamma/sample}$ by the relations (II.7):

$$N_\gamma(i) = N_{sample}(t,i) \cdot N_{\gamma/sample} \quad \text{(II.7)}$$

Where:

$$N_{\gamma/sample} = \frac{\mathcal{R}}{G_E} = 220.18 \cdot 10^{-6} \left[\frac{photon}{sample}\right] \tag{II.8}$$

is defined by the ratio between the pixel responsivity and the electrical gain [48]. Finally, the received power is given by:

$$P_{rx} = E_\gamma \cdot N_{\gamma/sample} \int_0^{T_{int}} \sum_{i=1}^{640} N_{sample}(t,i)dt \tag{II.9}$$

The operator of integration is linear and $E_\gamma \cdot N_{\gamma/sample}$ is constant. Therefore the linear relation between power and number of samples is demonstrated.

Appendix III

Eindhoven University of Technology final paper

In this chapter is reported the paper presented at the master thesis project defence held at the Eindhoven University of Technology, Eindhoven, The Netherlands on the 30 September, 2013.

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Automated Optical Test of Photonic Integrated Chips: Assembly and Assessment

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Automated Optical Test of Photonic Integrated Chips: Assembly and Assessment

F. Forni

***Abstract*—In this paper a new automated optical test for next generation of photonic integrated circuits (PICs) is provided by the test-bed design and assessment. After a briefly analysis of critical problems of actual optical tests, the main test features are defined: automation and flexibility, relaxed alignment procedure, speed up of entire test and data reliability. After studying varied solutions, the test-bed components are defined to be lens array, photo-detector array, and software controller. Each device is studied and calibrated, the spatial resolution, and reliability against interference at the photo-detector array are studied. The software is programmed in order to manage both PIC input, and photo-detector array output as well as data analysis. The test is validated by analysing state-of-art 16 ports PIC: the waveguide location, current versus power, and time-spatial power distribution are measured as well as the optical continuity of an entire path of PIC. Complexity, alignment tolerance, time of measurement are also discussed.**

***Index Terms*—Photonic integrated circuit, Automatic test equipment, Semiconductor optical amplifiers, Semiconductor device testing, Optical waveguides.**

I. Introduction

THE importance of photonic integrated circuits is known and it is continually increasing [1], [2]. The complexity of state-of-the-art integrated chips is keeping growing. The number of components per chip reaches now hundreds of them [3], [4]. In order to make it competitive with electronic technology, it is essential to develop fast and reliable test procedure.
Since the '70 the automated test methods for electronic ICs have been demonstrated to be solid and standardized procedures [5]. These reliable techniques have been exploited to provide hundreds of connections at one go.

Visual inspection and automated electrical tests have shown integral chip facets and good electrical connections after bonding [6]. However the optical test of these sophisticated chips is still very slow, and complex, because it relies on strict alignment tolerances between the fragile optical waveguides, in the chip, and the fiber lenses [7].
In this paper an automated test-bed for reliable optical assessment is conceived and provided, in order to hasten the photonic integrated circuit optical test [8].

The main test features are defined, and analysed in section II. The test-bed is assembled and evaluated in section III. The assessment is performed for the flip chip bounded photonic integrated in section IV. Finally the conclusion are shown in section V.

II. Concept

The envisaged automated optical test must satisfy a few fundamental requirements to make it valuable for effective optical test of sophisticate photonic integrated circuits (PICs). The specifications are:

- high automation via software control;
- relaxed precision and still reliable alignment;
- real-time alignment and measurements;
- multiple ports assessment at the same time;
- independent of the chip layout.

The base idea is carrying the optical beam from the PIC waveguides to the receiver.
A first studied solution is to bring the beams directly to the receiver. The beams are divergent so the receiver must be placed to few tens μm far from the PIC. This requires high precision alignment, in contrast with requirements.
A second solution is proposed: beam collimation. The collimated beams can travel for longer distance than the divergent ones, furthermore the receiver can be placed more distant from the PIC, with relaxed precision. This solution also increases the flexibility of the test-bed: more devices could be placed between the chip and the receiver to perform different tests.

The second task is how to acquire the PIC beams. The receiver must collect all the incoming beams at the same time, record the power distribution along the PIC waveguides line, find the positions of maximum power (peak), and the total emitted power.
The use of optical fibers is discarded immediately: the precision required in positioning increases the alignment time and makes the procedure difficult.
The linear optical power distribution along the waveguides direction is the only one significant, it is chosen a linear photo-detector array, together with collimated arrays of lens. Furthermore if the receiver is chosen with a sufficient sensor area, the alignments will require lower precision.

In order to control the synchronized emission of PIC and the acquisition of photo-detector, ad-hoc software ables to manage both PIC, and the receiver is made.
The main features to implement are following:

- real-time display of the optical power distribution, total power, peak power, and its position;
- automated saving of PDA patterns for further subsequent data processing;
- reduce the interaction between test-bed and operator;
- increase automation defining the PIC and PDA parameters through files, instead of operator input.

The program complexity requires the necessity of *Object Oriented Language* with support for graphical user interface

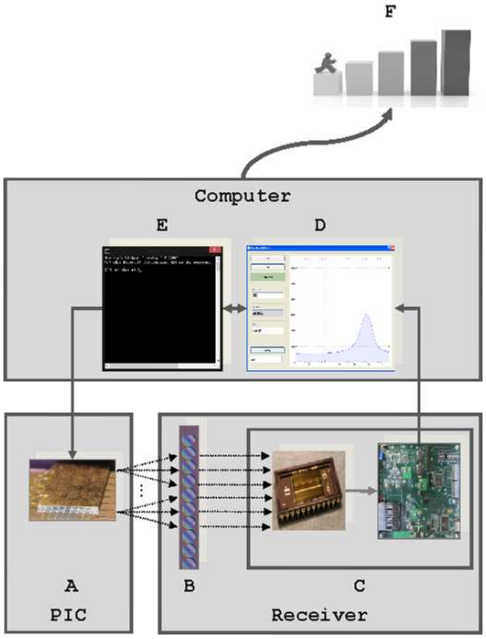


Fig. 1. Block diagram - A: PIC; B: microlens array [9]; C: PDA [10] and PDA-board; D: *Data displayer*; E: *Test controller*; F: data analysis.

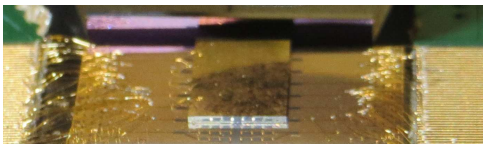


Fig. 2. Photonic integrated switch 8×8 used during the test.

libraries. The *C++* language is chosen [11].

III. Components

The assembly (Fig. 1) includes:

- the flip chip bounded PIC;
- the microlens array (MLA);
- the photo-detector array (PDA);
- software development for PIC control, real-time acquisition and fast screening.

A. Photonic integrated circuit

The test-bed is designed to evaluate any multiport photonic integrated circuit up to 32 ports, Fig. 2, following with the characterization:

- up to 32 divergent waveguides;
- $1600nm$ wavelength;
- numerical aperture (NA) equal to 0.5;
- output waveguides pitch (L_{wg}) equal to $250\mu m$;
- maximum estimated transmitted power $0dB_{mW}$.

The PIC structure and pad mapping, for the test circuit in this work, are shown in Fig. 3.
Each SOA is defined by an index, and a current value. There are 96 pads, divided in 12 groups, and each group has 8 tracks, the index is specified by matrix notation: $index_{group}.index_{track}$. Each SOA has, at least, 2 pads: some

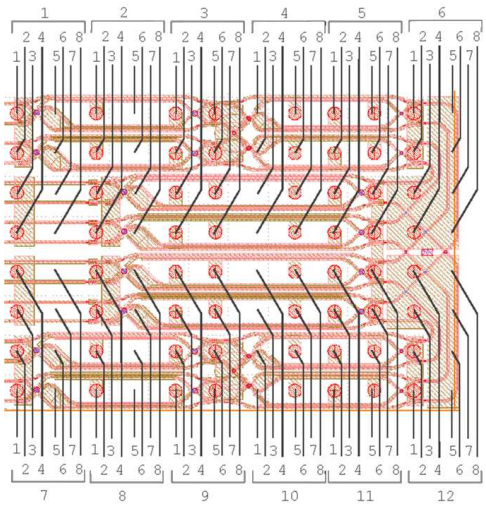


Fig. 3. Photonic integrated switch 8×8 layout and track indices.

TABLE I
MLA types.

	Fused Silica Lenses (18-0092)	Silicon Lenses (18-00284)
Type	circular	circular
Focal distance	$744.9\mu m$	$665.9\mu m$
Pitch	$250\mu m$	$250\mu m$
Num. Lenses	48	48
AR coating	$1.25 - 1.65\mu m$	$1.2 - 10\mu m$

of them are not connected: for instance, pad 1.1 and 1.2 are connected to the same SOA and 1.7 is not connected.
The values are provided to PIC by a current controller board [12]. The electrical connections between the PIC and the tile PCB have been already tested [6].

B. Microlens array

The PIC requirements impose to the lens array that its focal distance is as greatest as possible to simplify the placement procedure but, at the same time, lower than the distance at which the waveguide beams are overlapped (lens crosstalk): it comes clear the trade-off.

The lens crosstalk is now analysed.
For the lenses choice, the most important PIC parameter is the numerical aperture: it allows to calculate the maximum distance between PIC and MLA without crosstalk (D_{if}). This depends also on the distance between the turned on waveguides, it can be demonstrated. In the worst case scenario 3 adjacent waveguides [13] are turned on, at the same time, consequently, it can be calculate $D_{if} = 466.5\mu m$, as shown in Fig. 4.
The other constraints to take in account are following:

- lenses pitch equal to L_{wg};
- array of at least 32 lenses;
- linear array and circular lenses;
- AR coating to minimize the reflection loss;

The final choice is between 2 models by *SUSS MicroOptics* [14] shown in Table I. The model with the smallest focal

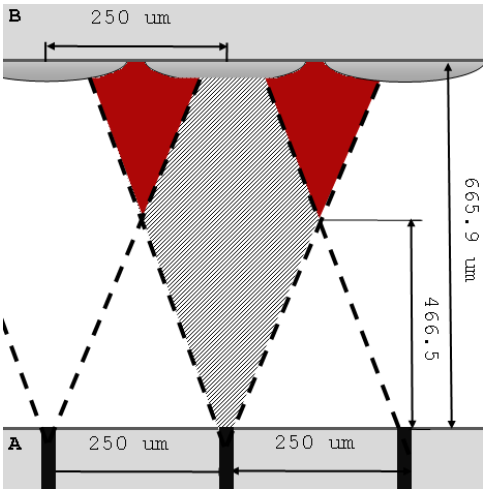


Fig. 4. Interference diagram- A: PIC; B: MLA. The crosstalk zones are shown in red.

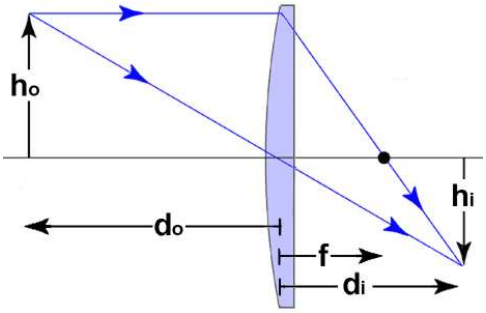


Fig. 5. Lens magnification on vertical plane, same scheme can be used for horizontal plane.

distance is the best option, in order to reduce the crosstalk between the lenses. The MLA Silicon Lenses, model 18-00284 is chosen.

Calibration: in order to study the MLA performance a test-bed is designed: an optical fiber is used as source, and IR camera as receiver [15]. The MLA collimation is made by IR camera, and microscope.
The magnification of the beam caused by mismatch of focus point is discovered and studied. The lens magnification is well known in optics. In this case, in first instance, the optical fiber beam can be represented as a spot on vertical plane, near the focal point, at distance d_0 (Fig. 5). The receiver is on the lens focal axis, behind it at distance d_i.
Defined h_0 the gap between the spot and the focal point. If $h_0 = 0$ the beam is collimated, and its image is at infinity. Otherwise the image is at finite and shifted from the focal axis. The distance h_i between the receiver and the image spot depends on d_i by $M_T \equiv -\frac{d_i}{d_0} = \frac{h_i}{h_0}$ [16]. Therefore, the beam is in a different position from the expected one. The magnification is more important when the receiver is far away from the lens and when it has a small width (for instance the PDA d_i is $190mm$).

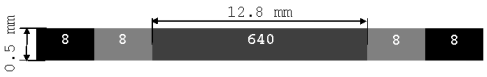


Fig. 6. The PDA pixel diagram.

C. Photo-diode array

The need of linear array, with sufficient surface area leads to chose the linear array 640 pixels *PDA-640 SFF InGaAs Photodetector Sensor* by *Princeton Lightwave Inc.* as receiver (Fig. 1).
The PDA provides, as shown in Fig. 6, a row of 640 active pixels, and 8 dark pixels and 8 disconnected pixels on each side. The dark pixels record the power provided by dark current.
The pixel array length is $12.8mm$, and is sufficient to acquire all PIC beams at the same time.

Via *integrate* trigger signal the exposure time is set and is equal to its duration (denoted as T_{int}) [17].
The readout circuit of PDA is an integrator operational amplifier followed by a sampler. The sampler input voltage (denoted as V_{out}) is defined in (1),

$$\begin{cases} V_{out} = V_{Ref} - \frac{1}{C_{INT}} \int_0^{T_{int}} i_p(t)dt \\ i_p(t) = R \cdot p_{opt}(t) + I_{dark} + I_{ng,opt} \end{cases} \quad (1)$$

in which C_{INT} is the capacitor used in the integrator, V_{Ref},R, I_{dark}, and $I_{ng,opt}$ are, respectively, the voltage reference, responsivity, dark current and negative-going current of pixel photo-detector [17].

PDA-board: the PDA has 8 inputs (6 signals, clock signal, and stabilized voltage), and 5 analogue outputs. Varied solutions are studied to interface it to the computer. The *640 Pixel Linear PD Array Demo Board* (PDA-board) by *Princeton Lightwave Inc.* is chosen.
The PDA-board communicates to the computer via USB interface. It also converts the input parameters into the proper PDA signal and performs the analogue-to-digital conversion providing the number of samples for each pixel. It is provided with a control software and DLL library for developers.

Photo-diode array test: the PDA performances are tested in order to establish which simulation and environmental parameters affect the measurements.

1) Maximum power: the maximum received power of PDA (denoted as $P_{rx,max}$) is calculated and it is equal to $11.67dB_{mW}$ [18]. During the experiment are used maximum $7.52dB_{mW}$ over a 150 pixels.

2) Measurement time versus saturation: the T_{int} variation effect on PDA output is studied both by (1) and measures.
As shown in Fig. 7 and already defined by the mathematical model: increasing T_{int} the received power rises up to the power level corresponding to the sampled voltage value $Count_{max} \simeq 50000\ samples$. Greater values of optical power are analogue to digital converted equal to $Count_{max}$,

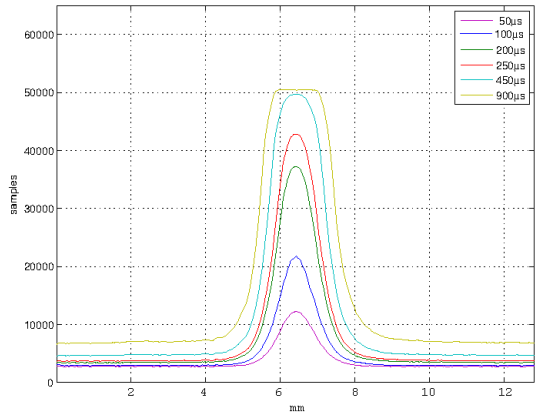


Fig. 7. Saturation effect versus T_{int}.

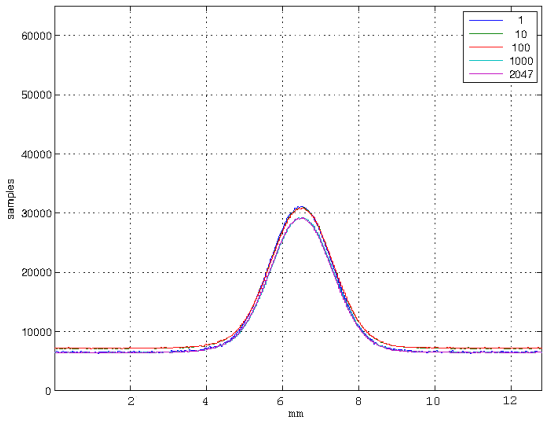


Fig. 8. The power distribution variation versus N_{Lines}.

this phenomenon is denoted as PDA saturation.

3) Number of measurements versus data reliability: during the test the variation of optical received power is discovered, for the same transmitted signal and test-bed conditions.
The number of measurements (denoted as N_{Lines}) influence the reliability of output data, as shown in Fig. 8: since, the relative error of maximum between $N_{Lines} = 1 - 2047$ is 6.574%, it decreases to 0.29% between $N_{Lines} = 1000-2047$. As consequence N_{Lines} determines the number of reliable digits in all the output data, and the possibility to reveal the minimum power change is not caused by random variation.

4) Electromagnetic interference: the possible interference by EM field at low and high frequencies are studied.
The electrical grid EM and the other devices did not affect the measurement of PDA. The environmental light (in particular the light used with the microscope) produces a flat interference pattern more important with the increase of T_{int}.
The interference did not affect the output values as the software can recognize the interference and can erase it before it saves the values.
The interference adds power to the optical beams received, reducing the number of samples available for the useful signal or, as well as, saturating the PDA.

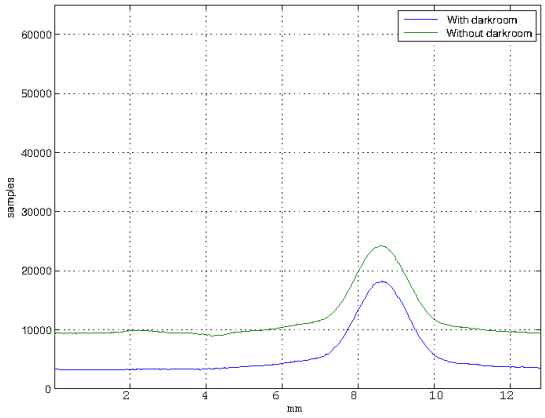


Fig. 9. The PDA optical power changing the environmental light ($T_{int} = 1.5ms$).

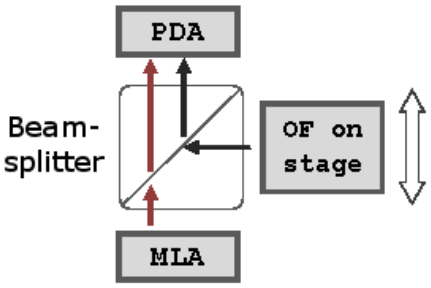


Fig. 10. Block diagram test-bed with 2 optical fiber, the second one moves along 1 axis.

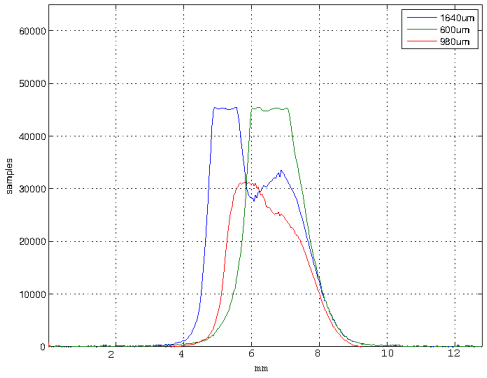
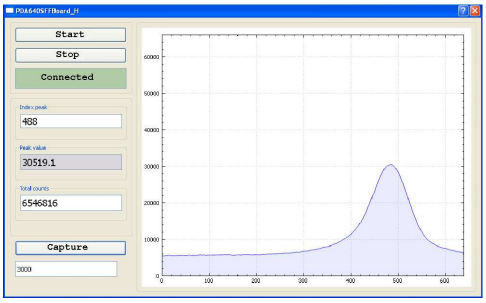


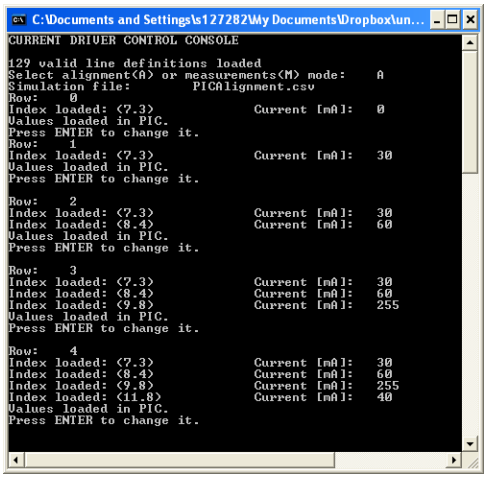
Fig. 11. Optical power changing the distance between the beams. The distances are reported at PDA photo-sensor, the beam provided by the second source is saturated in order to clearly display the MLA beam (the lowest peak of each curve).

The interference is sensible reduced using a darkroom for PDA (Fig. 9), therefore the environmental light interference, in this condition, is negligible.

5) Spatial resolution: the pixel array length, as written in section III-C, is sufficient to acquire all the PIC beams together. This simplifies the measurement but, more important, allows to recognize the position of each beam and distinguish each one. This feature introduces the possibility for new tests on PIC, for instance, optical crosstalk, measure erroneous waveguide routing, and SOA mapping.



(a)



(b)

Fig. 12. Screen-shoot of *Data displayer* (a), *Test controller* (b).

The position identification depends on the spatial resolution of PDA. It can be defined as the minimum distance between the maximum of 2 beams. The peak and its position are necessary to calculate the mean value and the variance of the theoretical gaussian curve.
The test-bed includes a beamsplitter [19], positioned between the MLA and PDA, and a second collimated optical fiber, as shown in Fig. 10. The minimum distance recognizable between 2 optical beams is $980\mu m$, as shown in Fig. 11.

Software suite

In order to achieve the goals required by the test-bed, 3 specific software are written. The interface is possible by DLL library provided by *Princteon Lightwave Inc.* [20].

The DLL library functions, provided with PDA-board, are able to interface it with any computer *Windows XP* based. They manage the communications with the board, and return the recorded pattern. This is displayed, for each measurement, as 1 dimensional array of 672 integer. Each array element is the number of samples used to convert the voltage signal [21]. The linear relationship between the received optical power, expressed in Watt, and the number of sample is demonstrated.

The software also performs the dark voltage power cancellation. Moreover in the first PDA testes show an unwanted ripple [22] produced by the PDA-board on the output value. It is checked that the cause is not in the test-bed set-up and is equalized by PDA function.

TABLE II
Data displayer INPUT, OUTPUT FILES: NAME AND DESCRIPTION.

File	Type
SimParameters1.csv	Input: define low sensitive PDA parameter
SimParameters2.csv	Input: high sensitive PDA parameter
Value.csv	Output (optional): generated by *capture()*
LogFile.txt	Output: logfile

D. Data displayer software

The first software is denoted *Data displayer* and is a graphical user interface program, as shown in Fig. 12a, for real-time display of recorded pattern, total power, maximum and peak position. The PDA in this configuration can be used as linear IR camera.
To write this program the language *C++* is used with *Qt*, and *QCustomPlot* [23] – [25] graphical user interface libraries. The class declaration is:

Listing 1. *Data displayer* class declaration of public functions.

```
class PDA−GUI : public QDialog {
 Q_OBJECT
 public:
 PDA640SFFBoard_H();
  virtual ~PDA640SFFBoard_H();
 public slots :
 // connect the board
 void start ();
 // disconnect the board
 void stop ();
 // display pattern
 void updateCurve();
 // save in .csv file the pattern
 void capture ();
};
```

The Fig. 12 shows 3 buttons: *start*, *stop* and *capture*. When, for the first time, *start* is clicked the function *start()* is called. It performs the PDA initialization procedure. If *start* is clicked meanwhile the measurement is stopped, it will start again the acquisition. The result of the procedure is written in the display below the buttons, it can be: “connected” (green background), or “error” (red background), more error information are written in the logfile. When the *stop* button is clicked, for the first time, *stop()* performs the disconnection procedure, and ”disconnected” on red background is displayed. When *capture* button is clicked the displayed pattern is saved in Value.csv file.
The typical procedure to use *Data displayer* is: start the program, click *start* button, and the graph displays the pattern. When a pattern needs to be saved: click *stop* button, the pattern remains in the graph, and press *capture* button to save it, to continue the measurements click, again, the *start* button. The real-time visualization is obtained by a timer: when the count is finished the curve is updated and displayed by *updateCurve()* then the timer re-starts to count.
Data displayer uses 34 different functions and 8 libraries. Despite its complexity the public interface is simple: 4 functions with no parameters, this is the main advantage to

use *C++*.

The dark power provided by dark pixels is cancelled: the program, after the acquisition, discards the values provided by the disconnected pixels, calculates the mean value of dark pixels in order to find the dark offset, and *Data displayer* subtracts the offset from the active pixel values. In this way the provided power values do not depend on dark current.

Some tests need to change frequently the measurement parameters. Simulation parameter automatic setting (autoset) is needed. Therefore a feature is programmed in order to recognize when the pattern is badly displayed, and change automatically the PDA parameters between 2 different configurations, to better display the pattern.
All the input, and output procedures are performed by file (Table II). SimParameters1.csv and SimParameters2.csv are the files used for the autoset feature. No output is generated at least that *capture()* is used. The logfile is generated to records all the software activities and failures.

E. Test controller software

The second, and main, software is denoted as *Test controller*, and its command line user interface is shown in Fig. 12b. It initializes and checks the status of PIC and PDA, sends the inputs from the first, records the values to the second, and saves the data.
The sequence of SOAs, their currents, as well as all the PDA parameters are specified by *Comma Separated Value* files. The output values, and the status flag are not shown on screen but saved in output and log files.
The program provides two modes: alignment and measurements.

Alignment mode is designed for the PIC positioning in order to find the focus points of MLA for each waveguide. The software provides the SOA current and index. Neither the PDA, nor the output recording are controlled, instead they are managed by *Data displayer* in order to send an immediate feedback to the operator.

Measurements mode manages both the PIC controller, and PDA-board. In particular: it initializes the PIC and PDA, loads the set of SOA from PICMeasureSequence.csv or PICAlignment.csv (Table III), and enables SOAs. Then the program performs the data acquisition, and saves the read values in OutputParameters.csv and patterns folder. After that, the next set of SOA is loaded and the same procedure is repeated. No operator control is required.
The program uses 2 classes. The first to manage PIC is called *Controller* [12]:

Listing 2. *Test controller* PIC class declaration of public functions.

```
class Controller {
 public:
 Controller ();
 ~Controller ();
 // initialization function
 string Init ();
void getSimData(int & NumCopiedEntry,
                string &InputFile);
 // set read input

 int SetOutput(int & SimIndexEntry,
               bool & ReturnedValue,
               bool & CalibrationMode);
};
```

When the program starts, *Init()* is called to initialize the PIC driver output.
When a mode is chosen, the *getSimData(int & NumCopiedEntry,string &InputFile)* loads the SOA sequence to turn on in PIC: *InputFile* specifies the name of the file to load (PICAlignment.csv or PICMeasureSequence.csv) and returns the number of row copied via *NumCopiedEntry*, the data are saved in a private array. Therefore, the software loads the data by *SetOutput(int & SimIndexEntry,bool & ReturnedValue, bool & CalibrationMode)*, which sequence it has to set is specified by the *SimIndexEntry*, all the specified SOA are enabled and the result is written in *ReturnedValue*, it will be true if the procedure returns correctly, false otherwise. The function also return *CalibrationMode=true* if the first SOA has current equal to zero, this is the flag communicating to the PDA that the pattern which is going to acquire is the interference pattern (to subtract to the other ones will be acquired, in order to perform the interference elimination). Usually the special entry is specified in the first row but can be written more times in the file in order to update the interference pattern, in this case the software recognizes each time the entry and update the interference array.

The PDA is controlled by *PDA640SFFBoard_H*:

Listing 3. *Test controller* PDA class declaration of public functions.

```
class PDA640SFFBoard_H {
public:
 PDA640SFFBoard_H();
 virtual ~PDA640SFFBoard_H();
 //connect the board
 void start ();
 // disconnect the board
 void stop ();
 // check temperature
 void checkStatus ();
 // save data
 void capture (bool &CalibrationMode);
};
```

When measurement mode is activated the *Test controller* also manages the PDA.
The constructor initializes the object and loads the default measurement parameters using SimParameters1.csv.
The connection and disconnection are performed, respectively by *start()* and *stop()*. In case of failure the functions write in LogFile.txt, and exit the program.
After the PIC class function *SetOutput()* is called, $10s$ are waited in order to be sure that the PIC output are stable and *checkStatus()* is called to check the temperature of PDA-board; if it is greater than $65°[C]$ the board is disconnected,

TABLE III
Test controller INPUT AND OUTPUT FILES AND FOLDER: NAME AND DESCRIPTION.

File	Type
SimParameters1.csv	Input: define low sensitive PDA parameter
SimParameters2.csv	Input: high sensitive PDA parameter
PICAlignment.csv	Input: SOA sequence
PICMeasureSequence.csv	Input: SOA sequence
OutputParameters.csv	Output: maximum and power
patterns\	Output: recorded patterns folder
LogFile.txt	Output: logfile

the logfile is updated and the program is terminated. After the temperature check, *capture(bool &CalibrationMode)* is called. If *CalibrationMode=true*, it sends the measurement parameters to the board, starts the acquisition, receives the pattern from PDA, performs the autoset and memorizes the distribution in a particular array as interference pattern, the entire pattern is saved in a *comma separated variable* and the title is the measure time.
If *CalibrationMode=false*, it performs the same operations, and for the received distribution the interference array is subtracted, and the maximum, its position, and the total power are calculated. Finally, before the function returns, it saves the output: this means the entire pattern is saved in a *comma separated variable* in patterns folder. It also saves in OutputParameters.csv: the SOA index, current, peak position and value, total power, measurement PDA file used, and time (Table III).

Despite the easy public interface, the 2 classes counts in total 64 different functions and 15 libraries, this is the main advantage to use *C++*.
The PDA class also performs the dark power cancellation in the same way provided by *Data displayer* software.

F. Data analysis

The curent versus power, full width at half maximum and current-spacial power distribution are displayed by scripts of *Matlab*.
The script, initially, copies patterns folder, OutputParameters.csv, LogFile.txt and SimParameters1.csv, and SimParameters2.csv in a specified target folder. All the paths are specified as strings in the first lines of code.

The program reads, in OutputParameters.csv, the currents, total power and maximum and memorizes them in 3 different arrays.
The software imports, also, each *comma separated variable* file in patterns folder and save them in 1 matrix ($640 \times NumberOfMeasurements$). This matrix is, in addition, saved in a .mat file in order to avoid another import if it will be necessary to use again the data.

The current versus power curve is obtained displaying the current and total power arrays with *plot()* function and the figure are saved in .fig, .eps, and .jpeg formats in the target folder.

The full width at half maximum is calculated: the theoretical half maximum power is calculated from the maximum power array, for each current value. The nearest value is searched in column of power distribution matrix and its positions are returned (they are two, one on the left and one on the right of the maximum), the width is calculated as difference of the 2 positions. The current and width arrays are displayed and saved in .fig, .eps, and .jpeg formats in target folder.

To display the color-bar graph: the power distribution matrix is normalized to 255 (maximum of RGB color scale), the normalization is on 50000 samples in order to have the same scale for each graph, the normalized matrix is displayed with *image()* and saved .fig, .eps, and .jpeg formats in the target folder.
Finally, the script deletes all the read data from the software folder, in order to make it ready for the next test.

TABLE IV
SOA 1.1 CURRENT (mA).

Software	PIC	Test board
0	16	16
10	11	11
30	30	31
45	44	43

IV. VALIDATION

The PIC tests has as main goal to demonstrate the effective validity of the test-bed described in this paper. It is achieved analysing the performances of SOAs at the edge of PIC as well as inside the PIC.

A. Waveguide characterization

This tests are going to characterize the SOA 1.1, 1.4, 7.3, and 7.1 (edge SOAs), Fig. 3. The PIC is controlled by a driver which takes the software output (index and current) and activates the proper outputs.

The driver outputs are checked, the provided current values are measured with a test board, before connecting the PIC. Also the driver power supply currents are measured during all the experiment. The current variation at the power supply, for the equal condition, are the same during the preliminary test and PIC trials.

The current absorption at the power supply makes possible to check the status of each connection per time as well as the real current at PIC during the test.
In Table IV are shown the input software currents, the ones measured with PIC connected and with the test board. There is, for both the cases, an initial offset that depends on the driver, all the other values are consistent.
In Table V are illustrated the current at SOA 1.4: in this case the test board measurements demonstrate the driver output correctness, the value provided during the PIC test gives the same offset but impossible value for the other cases. Moreover the same values are measured for disconnected output, therefore the connection can be supposed not working properly. The same test performed with the other SOA contact (1.3) gives consistent results.

The maximum current provided to each SOA is estimated in $70 - 80(mA)$.

TABLE V
SOA 1.4 CURRENT (mA).

Software	PIC	Test board
0	11	10
10	-7	9
30	-5	28
45	-3	41

TABLE VI
SOA TEST SEQUENCE FROM 7.3 TOWARD 12.4, IN ITALIC THE SOA FOR WHICH THE WORKING POINT IS NOT FOUND; THE MAXIMUM CURRENTS ARE RELATED TO THE CALCULATED LIMIT.

test	SOA				
	7.3	8.4	9.8	11.8	12.4
1	0				
2	30				
3	30	0-75			
4	30	60	0-300		
5	30	60	255	0-60	
6	30	60	255	40	0-255
7	30	60	255	40	*255*

All the alignment procedures are made with maximum $30(mA)$ for maximum $30min.$ of enabled time.

After checking the SOA status and positioning the PIC at the focal point of MLA, the distance between all the 4 beams is studied: the results are shown in Fig. 13. It is easily recognizable the different position of them, in particular, the spatial disposition is respected as the first beam is the 1.1, the second 1.3 and so on. The order is reversed, if it is compared with PIC layout, due to the PDA placement, this does not influence the measurements.
All these test are performed with *Test controller* in alignment mode and *Data displayer*.

The analysis of the edge SOAs is performed via *Test controller* in measurement mode.
Each SOA is enabled one per time with current $0-75(mA)$, and step $1(mA)$. The Fig. 14 shows that the SOA connected to 1.4 cannot work properly, confirming the validity of current absorption as valid method to text the connection. The same SOA, also with the other connector (1.3), is not working correctly: first tests, Fig. 13, gave different results, and after few starts its performance decreased, probably due to SOA deterioration.
The Fig. 14 and Fig. 15 demonstrate the better performances of 1.1 and 7.1 than 7.3. Fig. 15 shows very high slope of curve for low current, supposedly it is caused by the start of all the for waveguides of the SOA.

The full width at half maximum shows that the beam width remains almost constant for all the currents (Fig. 16). The spike for the lowest values are caused by post-processing mismatch: at those currents the pattern is flat, the error caused by mismatch of theoretical half maximum creates more important discrepancy.

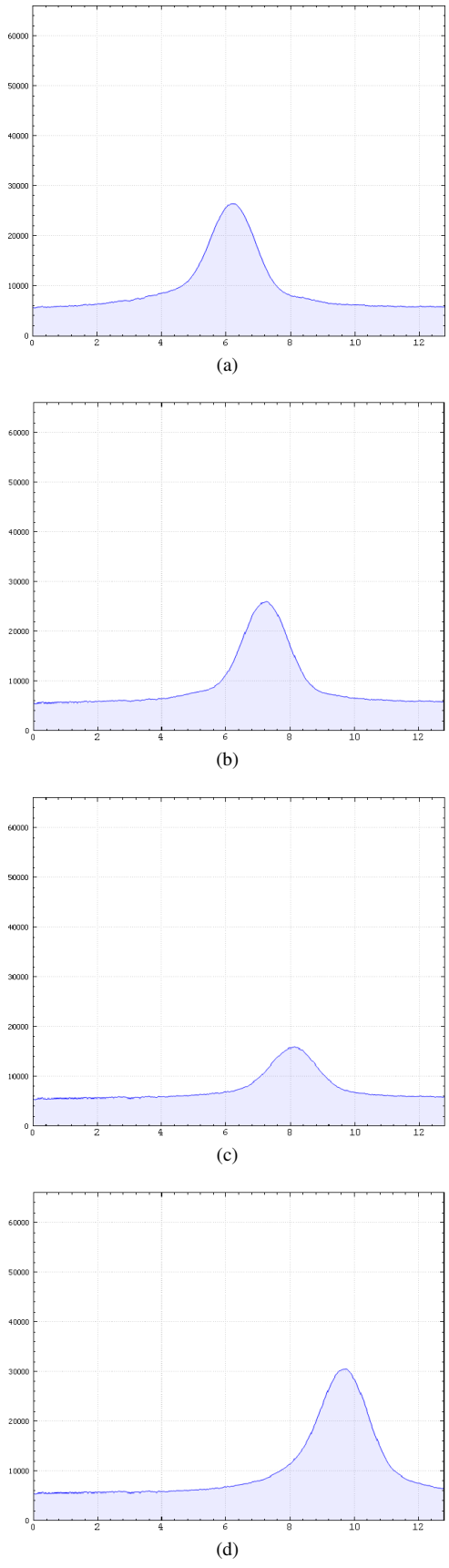


Fig. 13. SOA power distributions at $30mA$:1.1 (a), 1.3 (b), 7.3 (c), and 7.1 (d). Maximum position: 6.24, 6.8, 8.16, 9.76 mm, respectively.

B. Optical continuity

An optical path is defined as a path between 2 edge SOAs. A continue optical path is one in which the beam can propagate

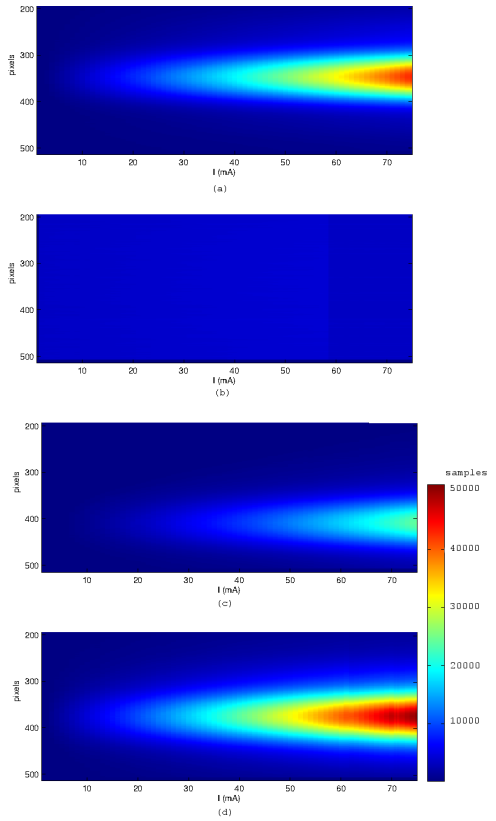


Fig. 14. Time-spatial power distribution SOA 1.1 (a), 1.3 (b), 7.3 (c), and 7.1 (d).

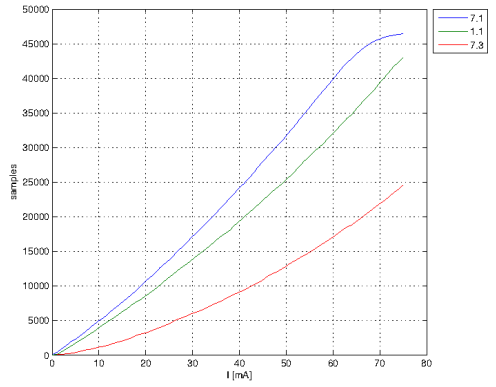


Fig. 15. Edge SOAs current versus power.

TABLE VII
SOA TEST SEQUENCE FROM 7.1 TOWARD 12.2, IN ITALIC THE SOA FOR WHICH THE WORKING POINT IS NOT FOUND; THE MAXIMUM CURRENTS ARE RELATED TO THE CALCULATED LIMIT.

test	SOA				
	7.1	8.2	9.6	11.6	12.2
8	0				
9	30				
10	30	0-140			
11	30	60	0-100		
12	30	60	40	0-71	
13	30	60	40	20	0-28
14	30	60	40	20	*28*

from one side to the other of the path.

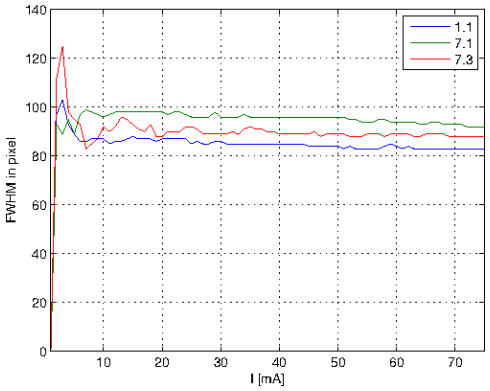


Fig. 16. Edge SOAs full width at half maximum (FWHM).

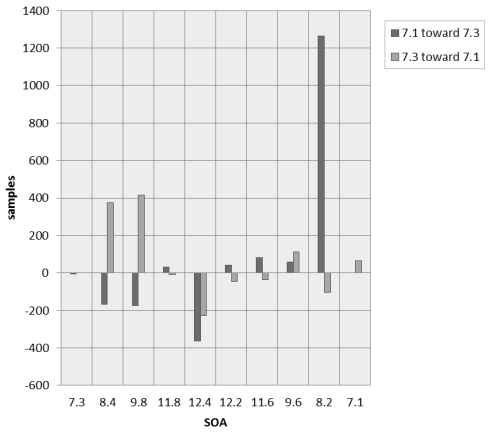


Fig. 17. Power changes versus SOA. Each bar shows the difference of power, made by the addition of that SOA to the path.

The best way to prove the continuity is verify if each SOA on the path is changing the output power: if the maximum power provided by 1 edge SOA is different from the power of the entire path turned on, in particular if it is greater or equal, the path can be said continuous.

This test is performed to study the performance of the test-bed in the optical continuity analysis. The path is defined by the SOAs in it. They must be specified by index and current. The indices are indicated in Fig. 3. The currents are unknown. Therefore the first step is to optimize them.

The maximum currents must be estimated in order not to damage the SOAs. The maximum current and the surface of the contacts are known for the edge SOAs then the maximum current density is calculated ($0.966 KA/cm^2$). Measuring the contact areas for each SOA in the path, the current is calculated by the product between current density and contact surface.
Therefore, for each SOA the working point must be found, it is defined as the current for which the SOA ASE balances the loss along the path. To do so the path is ”built” by steps: to find the 8.2 working point, for instance, the 7.1 is turned on with constant current and the current of 8.2 is changed from 0 to its maximum. The results are displayed in current versus power curves. The working point is the current for which the power starts to increase.
During this measurement, also, the electrical test is performed

recording the current absorption at PIC driver power supply, section IV-A. The same procedure, using the same example, is performed for the SOA 9.6, this time 7.1 and 8.2 are turned on with constant current equal to their working point, and so on.
The entire sequence is shown in Table VI and Table VII: the test is started from one side of the path and stopped in the middle, to continue to the other side in order to reduce the number of enabled SOAs, and in order to decrease the thermal stress, and the measurement time.

The role of the *Test controller* software in fundamental: the analysis of all working points is performed in few hours instead of months, this result can be achieved only through the automated procedure provided by *Test controller*.
In particular, after the working point estimation, the software is started in measurements mode specifying in the *comma separated variable* input file, an interval of current in which the working point is supposed to be. The output files are processed by *Matlab* script in order to display current versus power curve, the operator can analyse and finds the working point, if it is present the same procedure will be applied to the next SOA, otherwise the measure is repeated with a different interval. Each measurement takes less than $8min.$, in order to avoid the PIC overheating, for each SOA are, usually, necessary less than 4 measurements, in some cases up to 8.
The test of the entire path is totally automated, the input sequence is the same of Table VI and Table VII, the program, not the operator, adds the SOA to the path, the total measurement time is smaller than $8min.$.

The path is studied in both the ways. In Fig. 17 are shown the results: for each SOA is shown its contribution in power. If it is negative, the SOA current is not enough to balance the path losses. Vice versa if the contribution is positive. The test is done in both the directions due to the first test (7.1 toward 7.3) shows that every SOA from 12.4 is attenuating. The test in the opposite direction (7.3 toward 7.1) visualizes which every SOA from 12.4 is not amplifying. Due to the fact that the optimum working point for 12.4 was not found (it is caused by the current limitation of PIC driver), it is possible to conclude that every SOA, except 12.4, are working with the properly current.
The tests are also repeated breaking the optical path between PIC and PDA, in order to be sure that the values are provided by the optical beams and they are not caused by EM interference. In this case the optical distribution is equal to the noise pattern, therefore there is no pick-up effect.

In conclusion the optical continuity of the path is verified. Each SOA gives its contribute to the output power, in particular both side tests allows to verify that all the SOA are amplifying the beam, except the 12.4 that attenuate in both cases, probably, due to the PIC driver maximum current constraint.

V. Conclusion

A new automated optical test of photonic integrated chips with collimation of the beam, fast signal acquisition by photodetector linear array, test-bed management and data elaboration by software is assembled and verified. The most important test-bed concepts are analysed. Consequently, the components are selected, studied, and calibrated. Finally, the test-bed is validated by the characterization of 16 waveguides photonic integrated switch.

The high automation of the test-bed is reached by the *Test controller*, which proves the capability in order to perform an automated photonic integrated circuit test. The alignment precision relaxing is proved as well as the decreased alignment and measurement time: they are reduced from few weeks, of previous procedures, to few hours for the alignment and a couple of hour for the measurements.
Besides, the test flexibility, in terms of multiple ports assessment and chip layout independence, have been verified. The test can support up to 48 waveguides photonic integrated chip, and the chip change requires to redefine only one look-up table of the *Test controller* software. Moreover, the beam collimation increases, even more, the test flexibility allowing to add more components to the test (as verified during the spatial resolution analysis).

The test configuration results are very promising to support more complex procedures, for instance, the input of optical beams. The software suite also can support more complex data analysis algorithms, e.g., improved features for theoretical gaussian beam calculation and matching as well as multiple peak recognition.

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