Alma Mater Studiorum · Università di Bologna

SCUOLA DI SCIENZE
Corso di Laurea Magistrale in Fisica

Development and Testing of the ATLAS IBL ROD preproduction boards

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Sessione II
Anno Accademico 2012-2013

Abstract

Il lavoro di questa tesi riguarda principalmente la progettazione, simulazione e test di laboratorio di tre versioni successive di schede VME, chiamate Read Out Driver (ROD), che sono state fabbricate per l'upgrade del 2014 dell'esperimento ATLAS Insertable B-Layer (IBL) al CERN. IBL è un nuovo layer che diverrà parte del Pixel Detector di ATLAS. Questa tesi si compone di una panoramica descrittiva dell'esperimento ATLAS in generale per poi concentrarsi sulla descrizione del layer specifico IBL. Inoltre tratta in dettaglio aspetti fisici e tecnici: specifiche di progetto, percorso realizzativo delle schede e test conseguenti. Le schede sono state dapprima prodotte in due prototipi per testare le prestazioni del sistema. Queste sono state fabbricate al fine di valutare le caratteristiche e prestazioni complessive del sistema di readout. Un secondo lotto di produzione, composto di cinque schede, è stato orientato alla correzione fine delle criticità emerse dai test del primo lotto.

Un'indagine fine e approfondita del sistema ha messo a punto le schede per la fabbricazione di un terzo lotto di altre cinque schede. Attualmente la produzione è finita e complessivamente sono state realizzate 20 schede definitive che sono in fase di test. La produzione sarà validata prossimamente e le 20 schede verranno consegnate al CERN per essere inserite nel sistema di acquisizione dati del rivelatore. Al momento, il Dipartimento di Fisica ed Astronomia dell'Università di Bologna è coinvolto in un esperimento a pixel solamente attravers IBL descritto in questa tesi. In conclusione, il lavoro di tesi è stato prevalentemente focalizzato sui test delle schede e sul progetto del firmware necessario per la calibrazione e per la presa dati del rivelatore.

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Introduction

This thesis refers mainly to the work on designs, simulations and tests of several batches of VME boards, called ReadOut Drivers (ROD) that has been fabricated for the ATLAS Insertable B-Layer (IBL) experiment at CERN (see below). However, this work also introduces the ATLAS experiment and the Inner Detector, which includes Pixels and Insertable B-Layer. In particular, the IBL is an additional layer that will take part in the ATLAS Pixel Detector in 2014. In fact, until now the IBL has been a project developed and separately financed from the Pixel Detector of ATLAS but, starting from the beginning of 2013, IBL has joined the Pixel Detector as a new innermost layer of pixels. The intention is to keep IBL working along with the current three layers of pixels, namely Barrel Layer 0, 1 and 2, so that the entire system will be composed of four pixel layers. When the B0 Layer will show a severe degradation and a lack of performance due to the increasing luminosity of the collider, the Pixel Detector will still be composed of three layers.

This thesis first covers an overview of the system and involves a variety of physics and technical aspects, before going into details of Insertable B-Layer, how this was designed from specifications, how it was developed and constructed. As said, the VME boards are part of the innovative data readout chain that is going to be implemented along with the additional layers of pixels: IBL. The boards has been firstly produced into two batches of prototypes to test the system performance. In particular a first batch of two boards was designed and fabricated, showing some main bugs that were fixed in a second batch of five new cards.

After that a fine and in-depth investigation of the system has tuned the boards towards a third batch of other five as part of the final production. Now - December 2013 - the production is just finished, with an additional final adjustment of the specifications and altogether there are twenty VME 9U boards under tests.

Once the last fifteen boards will be validated by tests, they'll populate the data acquisition system of the ATLAS Pixel Detector. This work even if is mainly done in Bologna, it is considered on behalf of the ATLAS Pixel Collaboration. This stage is still on-going and I am the first student at the Physics and Astronomy Department of the University of Bologna involved into this project. In addition, the research in pixel experiments is also a frontier of research for its physics and technologic aspects, and this is a challenge for the Bologna Department.

In conclusion, my work has been mainly focused on the tests of the boards along with part of the development of the firmware that is necessary for the calibration and for the Data Taking of the ATLAS Pixel Detector. The work is ongoing within the ATLAS collaboration people at CERN and will continue after this thesis.

Chapter 1

Insertable B-Layer Upgrade

1.1 ATLAS Experiment overview

The Large Hadron Collider (LHC) is a proton-proton collider with 14 TeV centre of mass energy and design luminosity of $10^{34} cm^{-2} s^{-1}$. Beam crossings are 25 ns apart and at design luminosity there are 23 interactions per crossing.

1.1.1 Nomenclature

The beam direction defines the z-axis, and so the x-y plane. The positive x-axis is defined as a vector pointing from the vertex to Large Hadron Collider's Ring centre , and the positive y-axis is pointing upwards. The azimuthal angle ϕ is the one around beam axis on x-y plane, and the polar angle θ is the angle from positive beam axis direction (whose cosine projects on z). Pseudorapidity is defined as $\eta = -\ln \tan(\theta/2)$.

The transverse momentum p_T and energy E_T, as well as the missing transverse energy E_{Tmiss} and other variables, are defined in the x-y plane unless stated otherwise. The distance ΔR in the azimuthal angle space is defined as $\Delta R = \Delta 2\eta + \Delta 2\phi$. Trajectories of charged particles can be described by five parameters which draw an helix under the hypothesis of an ideal uniform magnetic field.

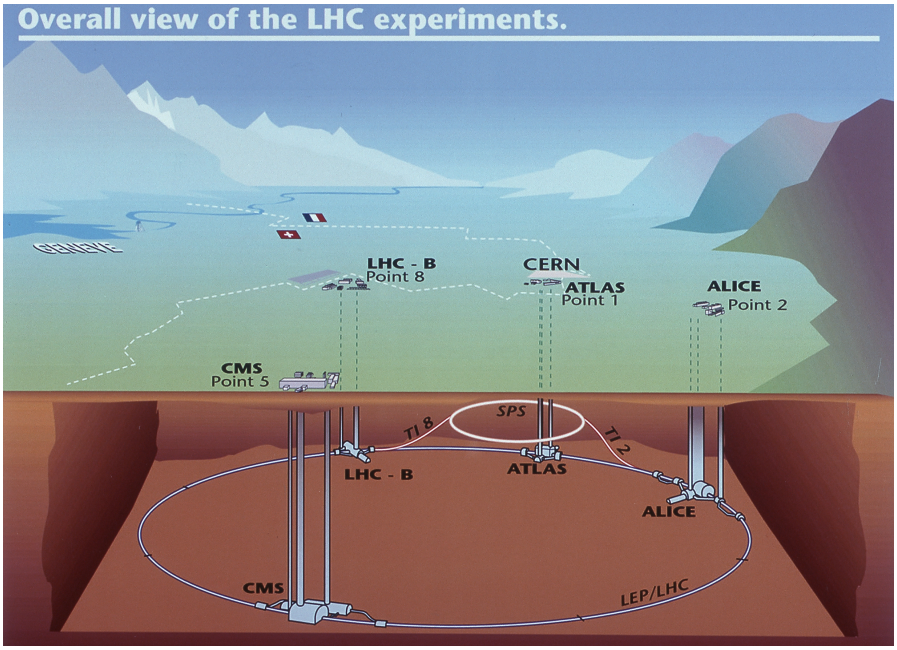


Figure 1.1: LHC overall view with all the main experiment locations indicated

The following helix parametrization is used in ATLAS, with all quantities measured at the point of closest approach to the nominal beam axis $x = 0$, $y = 0$.

Parameters in x-y plane are:

- $1/p_T$: Reciprocal of the transverse momentum.
- ϕ: Azimuthal angle, where $\tan\phi \equiv p_y/p_x$.
- d_0: Transverse impact parameter, is defined as the transverse distance to the beam axis at the point of closest approach; sign is given by the reconstructed angular momentum of the track.

Parameters in the R-z plane are:

- $\cot\theta$: Cotangent of the polar angle, where $\cot\theta \equiv p_z/p_T$;
- z_0: Longitudinal impact parameter, defined as the z position of the track at point of closest approach.

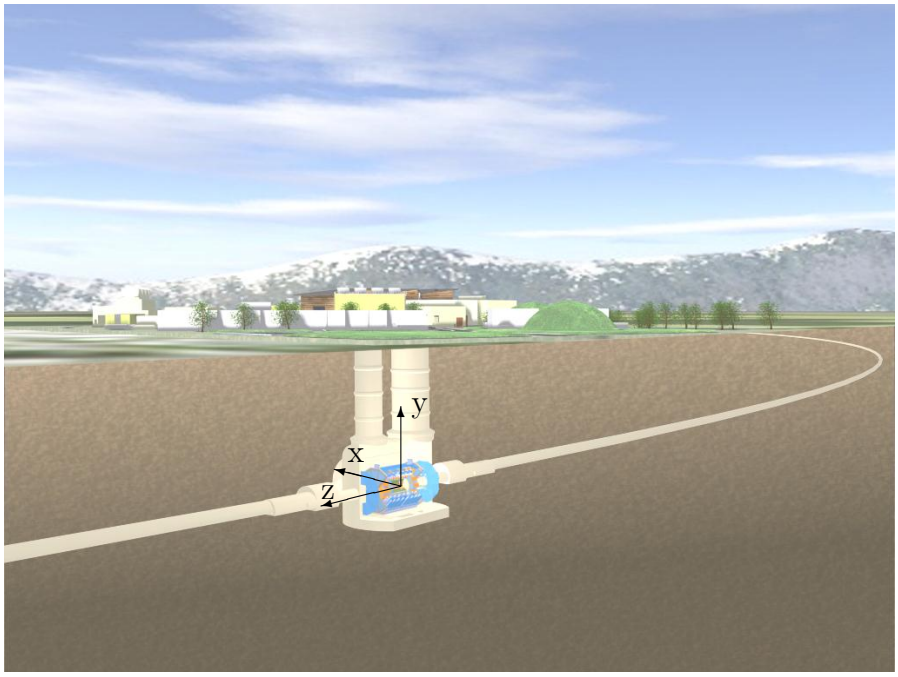


Figure 1.2: LHC's ATLAS well with nomenclature

The side A of the detector is defined as the side with positive z, and the side C is the side with $z < 0$. Side B is the plane where z equals zero.

1.1.2 Overall detector concept

The basic design criteria of the detector include the following points:

- Very good electromagnetic calorimetry for electrons and photons identification, complemented by full-coverage hadronic calorimetry for accurate jet and missing transverse energy (E_{Tmiss}) measurements;
- High-precision muon momentum measurements, with the capability to guarantee accurate measures at the highest luminosity using the external muon spectrometer alone;
- Efficient tracking at maximum luminosity for high p_t lepton-momentum measurements, electron, photon, τ-lepton and heavy-flavour identification, and

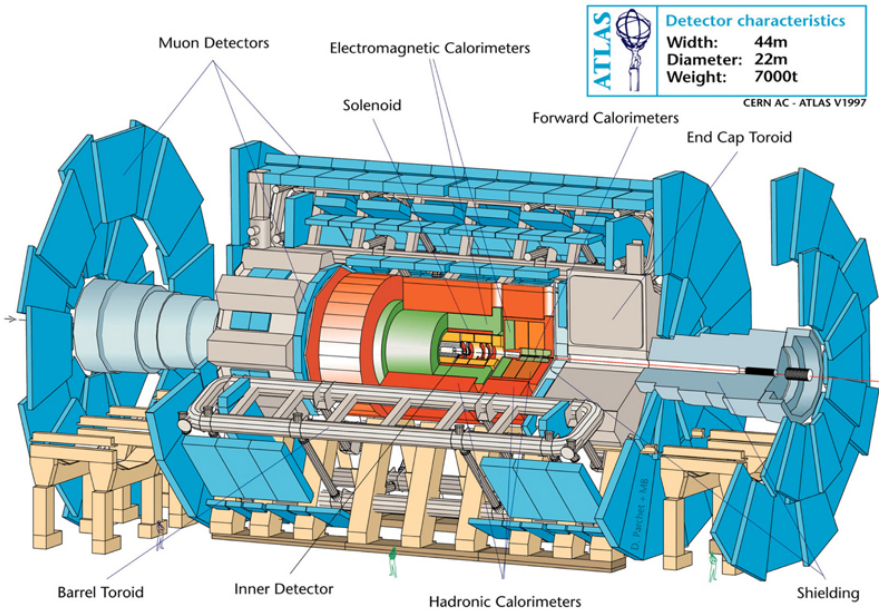


Figure 1.3: ATLAS detector overview

full event reconstruction capability at lower luminosity;

- Large acceptance in pseudorapidity (η) with almost full azimuthal angle (ϕ) coverage everywhere. The azimuthal angle is measured around the beam axis, whereas pseudorapidity relates to the polar angle (θ) where θ is the angle from the z direction.

- Triggering and measurements of particles at low-p_T thresholds, providing high efficiencies for most physics processes of interest at LHC.

The overall detector layout is shown in Figure 1.3.

The magnet configuration is based on an inner thin superconducting solenoid surrounding the inner detector cavity, and large air-core toroids consisting of independent coils arranged outside the calorimeters. This allows the hypothesis of constant magnetic field cited above. The Inner Detector (ID) is a cylinder closed by end-caps 7 meters long 1.5 of radius, in a solenoidal magnetic field of 2 Tesla.

Pattern recognition, momentum and vertex measurements, and electron identification are achieved with a combination of discrete high-resolution semiconductor pixel and strip detectors in the inner part of the tracking volume, and continuous straw-tube detectors with transition radiation capability in its outer part. This choice is a balance between tracking precision and costs of the apparatus because a single layer of pixels prices a lot more than a layer of straw tubes.

Highly granular liquid-argon (LAr) electromagnetic (EM) sampling calorimetry, with excellent performance in terms of energy and position resolution, covers the pseudorapidity range $|\eta| < 3.2$. Inside the end-caps LAr technology is also used for all hadronic calorimeters.

The cryostat also house the special LAr forward calorimeters which extend the pseudorapidity coverage to $|\eta| = 4.9$. The bulk of hadronic calorimetry is provided by a novel scintillator tile calorimeter, which is separated into a large barrel and two smaller extended barrels, one on each side of the barrel.

The overall calorimeter system provides a very good jet and E_{Tmiss} performance detector. The LAr calorimetry is contained in a cylinder with an outer radius of 2.25 m and length of more than 13 m along the beam axis. The outer radius of the scintillator-tile calorimeter is 4.25 m and its half length is 6.10 m.

The calorimeter is surrounded by the muon spectrometer. The air-core toroid system, with a long barrel and two inserted end-cap magnets, generates a large magnetic field volume with strong bending power within a light and open structure. Multiple-scattering effects are thereby minimised, and excellent muon momentum resolution is achieved with three stations of high- precision tracking chambers. The muon instrumentation also includes as a key component trigger chambers with very fast time response. The muon spectrometer defines the overall dimensions of the ATLAS detector. The outer chambers of the barrel are at a radius of about 11 m. The half-length of the barrel toroid coils is 12.5 m, and the third layer of the forward muon chambers, mounted on the cavern wall, is located about 23 m from the interaction point. The overall weight of the ATLAS detector is about

7 000 Tons. The primary goal of the experiment is to operate at high luminosity ($10^{34} cm^{-2} s^{-1}$) with a detector that provides as many signatures as possible. The variety of signatures is considered to be important in the harsh environment of the LHC in order to achieve robust and redundant physics measurements with the ability of internal cross-check. The measurement of the luminosity itself will be a challenge. Precision measurements employing the total and elastic cross-sections require specialised detectors. A measurement with a precision of 5% to 10% may be obtained from the machine parameters.

1.1.3 Magnet system

The ATLAS superconducting magnet system can be seen in Figure 1.4 and 1.5(a). It is an arrangement of a Central Solenoid (CS) providing the Inner Detector with magnetic field, surrounded by a system of three large air-core toroids generating the magnetic field for the muon spectrometer. The overall dimensions of the magnet system are 26 m in length and 20 m in diameter. The two End-Cap Toroids

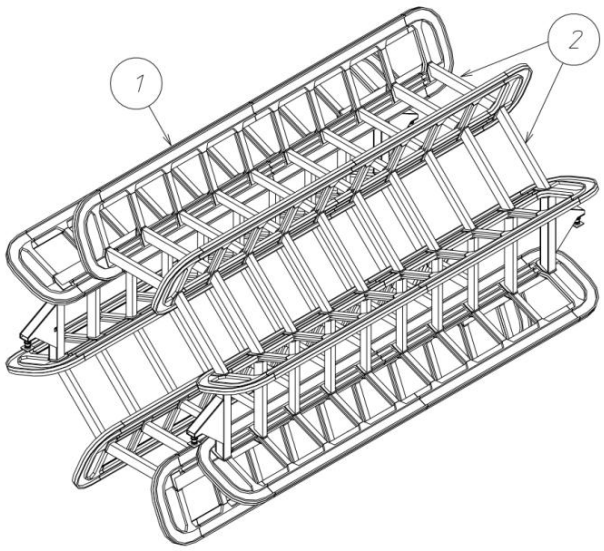
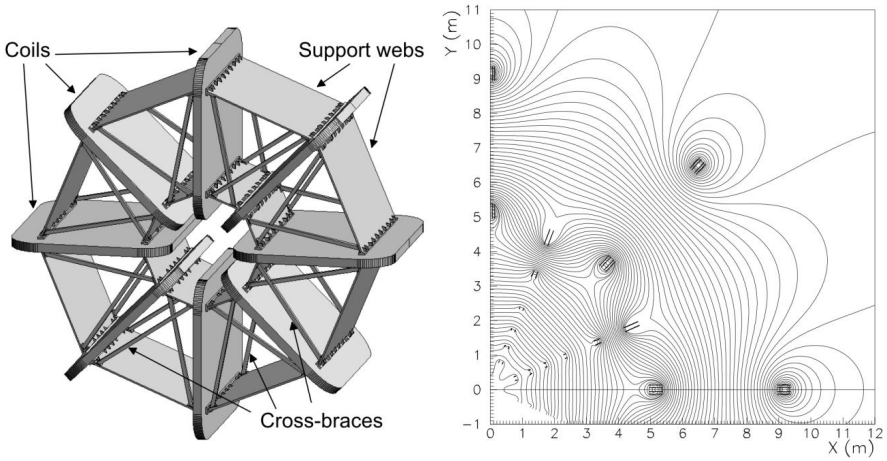


Figure 1.4: Magnets inside ATLAS detector



(a) End Cap Toroids (b) Magnetic field inside the detector

Figure 1.5: The magnetic field with the contribute of main magnets and ECT, as we see can, with some correction factor, be considered constant

(ECT Figure 1.5(a)) are inserted in the Barrel Toroid (BT Figure 1.4) at each end and line up with the CS. They have a length of 5 m, an outer diameter of 10.7 m and an inner bore of 1.65 m. The CS extends over a length of 5.3 m and has a bore of 2.4 m. The unusual configuration and large size make the magnet system a considerable challenge requiring careful engineering.

The CS provides a central field of 2 T with a peak magnetic field of 2.6 T at the superconductor itself. The peak magnetic fields on the superconductors in the BT and ECT are 3.9 and 4.1 T respectively. The performance in terms of bending power is characterised by the field integral $\int Bdl$, where B is the azimuthal field component and the integral is taken on a straight line trajectory between the inner and outer radius of the toroids.

The bending power is lower in the transition regions where the two magnets overlap ($1.3 < |\eta| < 1.6$). The position of the CS in front of the EM calorimeter demands a careful minimisation of the material in order to achieve the desired calorimeter performance. As a consequence, the CS and the LAr calorimeter share one common vacuum vessel, thereby eliminating two vacuum walls.

1.2 Inner Detector overview

Here the different layers that compose the Inner Detector are described sequentially starting from the external TRT up the the innermost IBL.

1.2.1 Transition Radiation Tracker

It's a layer of thin drift tubes in the outer part of inner detector, they can be used for high granularity is not needed at this distance from the vertex.

Transition radiation is a form of electromagnetic radiation emitted when a charged particle passes through inhomogeneous media, such as a boundary between two different media.

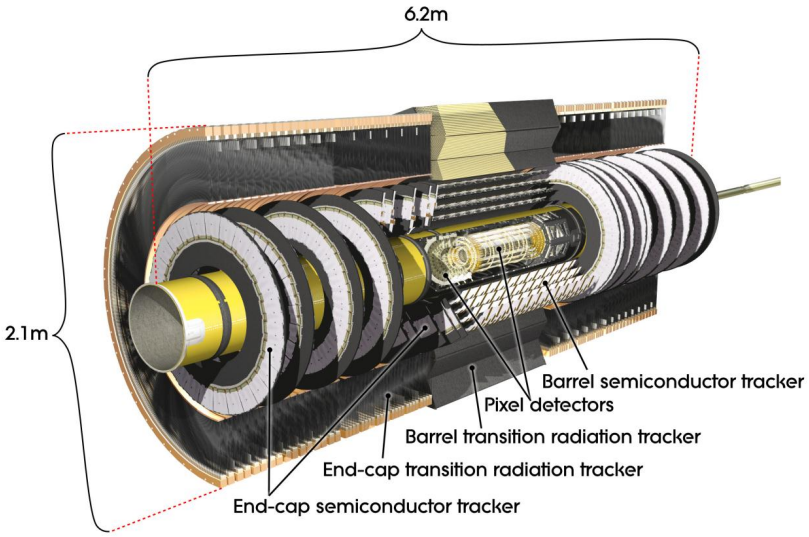
Using straw-tube technology this tube's outer walls are only $25\mu m$ placed at a potential of -1530 V. As mass is used a $31\mu m$ thin wire of gold plated tungsten put in centre of the cavity filled with a gas mix composed of Xenon (70 %), Carbon dioxide (27%), Oxygen (3%).

Tubes are placed along the pipe in barrel region and in a radial disposition on the end-caps, barrel's tube are 144 cm long and divided into two parts so to reduce the occupancy. Read-out is done on each side with the front end electronic described later.

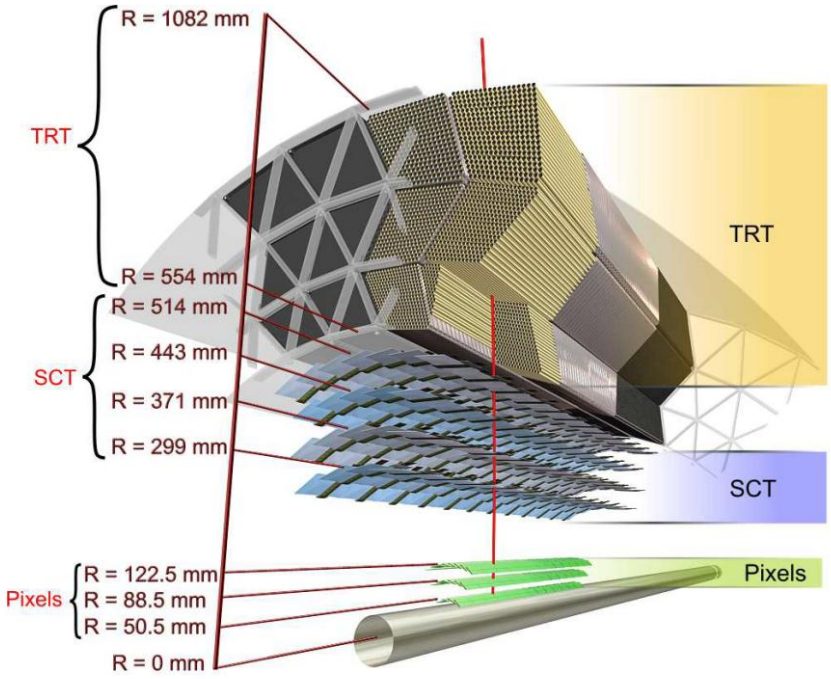
Drift time in the described conditions is $48ns$ maximum that permits a resolution of $130\mu m$.

Unlike all other active parts of inner detector drift tubes doesn't need refrigeration and are not subjected to radiation degrade, in fact the gas can simply be substituted. Another good point of this detector is that the angle at which photons are emitted, when an ultra relativistic particle passes through two different materials, goes with $1/\lambda$. In ATLAS case it's needed an high-Z gas,Xenon, to maximize the cross section of 5-15 KeV particles.

All those characteristics gives to TRT the ability to increase the precision of electromagnetic calorimeter's measures.



(a) Inner Detector



(b) ID layers

Figure 1.6: Inner detector overview

Front end electronics for this detector is basically implemented by two ASICs the first one called ASDBLR is responsible for amplification and shaping of the signal and has two discrimination thresholds, the 250 eV one is for minimum ionization particles while the 6 KeV one is for transition radiation signals. The second one is a radiation hard chip that measures drift time and buffers data waiting for trigger, it includes also a DAC to set the two thresholds mentioned above.

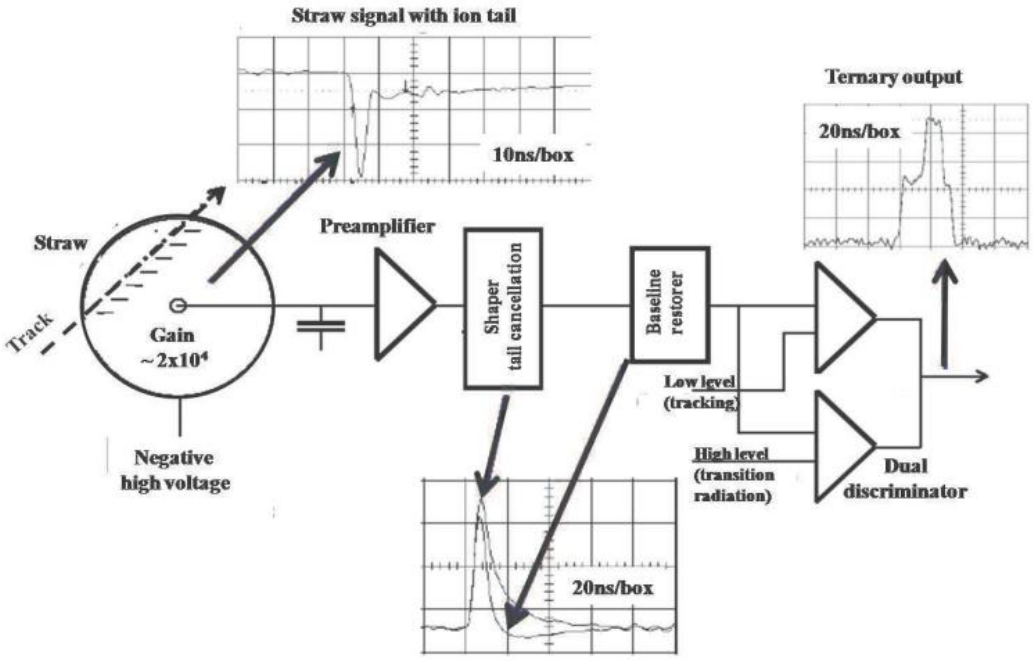


Figure 1.7: Front end electronic of a TRT

1.2.2 Semi Conductor Tracker

SCT is a lower cost silicon tracker made with a technology similar to that of a pixel detector. An n+ doped silicon strip within an n substrate and a p doping on the other side constitutes the semiconductor part of the tracker.

Layer (Ordered from the inner one)	Radius (mm)	Length (mm)	Angle (Deg)	Number of modules
3	299	1492	11°	384
4	371	1492	11°	480
5	443	1492	11.25°	576
6	514	1492	11.25°	672
Total				2112

Table 1.1: Semiconductor Tracker's characteristics.

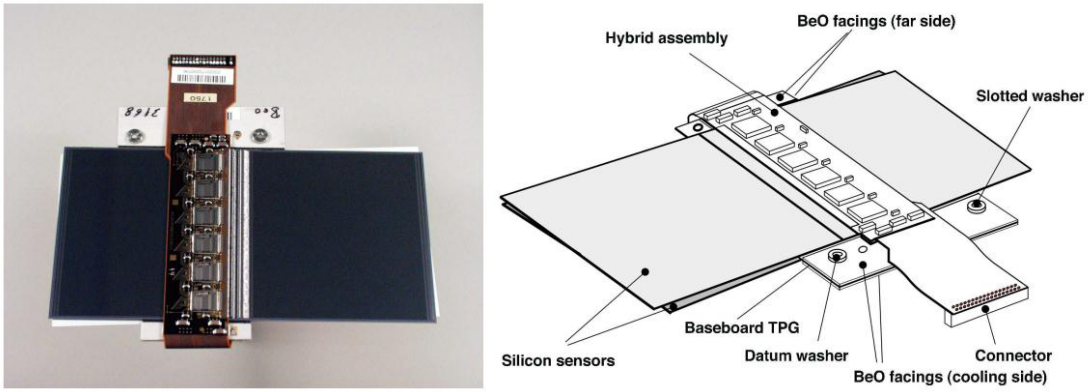


Figure 1.8: SCT module image and graphic with labels.

The reason for using semiconductor trackers instead of pixels are mainly economical for the barrel covers more than 30 times the pixel surface (63 m^2 versus 1.73 m^2).

The barrel part of the detector is made of 4 layers while 9 end-caps each side have been mounted. Each layer is made of many staves counting many modules each. Numbers and characteristics of every layer can be seen in Table 1.1. Each strip is 40 mrad tilted to be able to measure the second spatial coordinate, has a length of 6 cm and they are $80\mu m$ apart. This placement allows a resolution of $17\mu m$ on $x-y$ plane and a $580\mu m$ along z.

End caps SCT detector is slightly different for each layer has a ring shape, a

custom made trapezoidal shape of each module is allowed by low cost technology. In barrel's case read-out ASICs are placed in the middle of each module while end-caps are read out on the external circumference.

The external layer will receive an hundred times less radiation than B-layer, but considerations about radiation hardness in the project and construction phases of these staves are not to be spared.

The read-out ASIC is called ABCD3TA and holds interpreter of commands, buffer, threshold configuration, control and calibration functions within it.

As anticipated degrade will show up gradually in this detector in the form of an increasing inverse polarization need, also even if power consumption of each module is only 7.5W they need to be cooled down to -7° C during all run time to work properly.

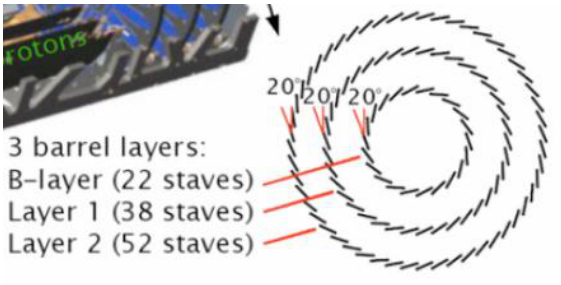
1.2.3 Pixel Detector

Pixels are the innermost sensitive layer and they are distributed on 3 barrels; their construction, in terms of radiation hardness and resolution, required the most advanced technology. All 801 mm long staves are made of 13 modules tilted

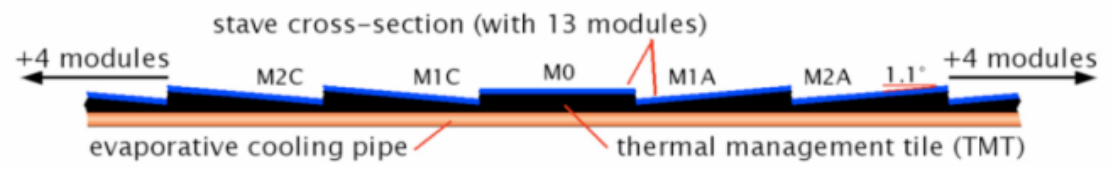
Layer Number	Mean Radius(mm)	Number of Staves	Number of Modules	Number of Channels	Active Area (m^2)
0(B)	50.5	22	286	13 178 880	0.28
1	88.5	38	494	22 763 520	0.49
2	122.5	52	676	31 150 080	0.67
Total		112	1456	67 092 480	1.45

Table 1.2: Pixel Layer characteristics.

on z axis by 1.1 degrees toward the interaction point as shown in Figure 1.9(b), also, to allow overlapping, the staves are tilted by 20 degrees on the x-y plane Figure 1.9(a).



(a)



(b)

Figure 1.9: Staves disposition around the beam pipe(a), and modules layout inside each stave(b).

Modules

Sensors, 16 Front End(FE-I3) chips, a flex-hybrid, a Module Controller Chip (MCC) and a pigtail together form what is called a module.

Leaving sensors to the next section, FE-I3 is responsible for reading the charge signal from the pixel. Each 195 μm thick and 1.09 by 0.74 cm large FE-I3 counts 3.5 millions of transistors in 250 nm CMOS technology.

They are bump bonded over the sensors like in Figure 1.10 and each one has an analog amplifier able to discriminate signals of 5 000 e^- with a noise threshold of 200 e^-. Analog signals are then digitized and buffered inside the End Of Columns electronic waiting for a trigger. EOC signals departs toward the MCC that has the following responsibilities:

- Distribute timing, trigger, reset and calibration signals.
- Order the 16 FE-I3 EoC data and produce an event for the ROD.

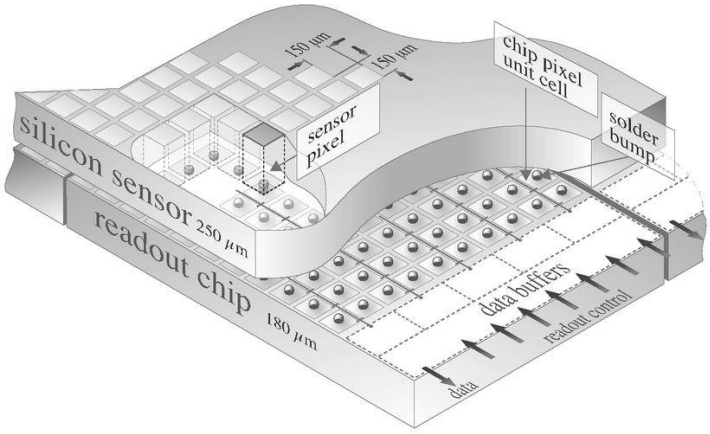


Figure 1.10: Silicon sensor and read out chip (FE-I3) bump bonded.

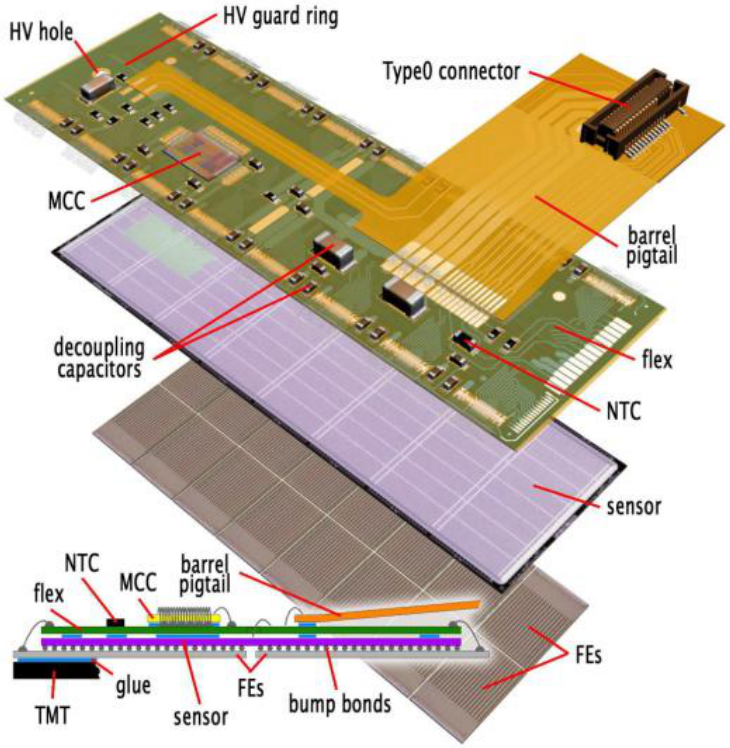


Figure 1.11: A figure representing all parts that forms a module.

Last but not least, the opto-board converts into optical signals the electric output from 6 MCC and send it out to the Back Of Crate board described later. Each opto-board is equipped with:

- PiN diode that converts optical to electrical.
- Digital Optical Receiver Integrated Circuit (DORIC) that adapt to LVDS standard the PiN signals.
- Vertical Cavity Surface Emitting Laser (VCSEL) does an great efficiency electrical to optical conversion.
- VDC interfaces MCC and VCSEL.

Sensors

A single pixel is composed of an n-doped crystalline semiconductor with a p-doped well, this "diode" is reverse polarized so the depletion region extends until a ionizing particle passes and frees some other electrons and holes. Before this charges can recombine the electric field separates and lead them on the metal contacts where a charge amplifier collect them as can be seen in Figure 1.12.

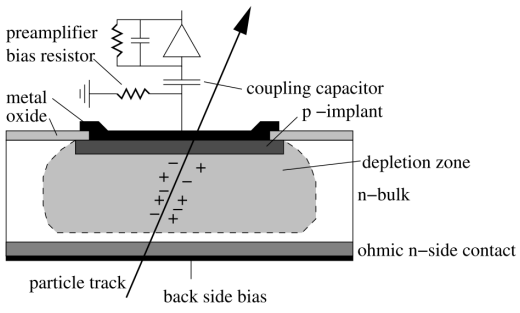


Figure 1.12: Single pixel layout with front end electronics connected.

Energy is proportional to the amount of charge collected by the contacts for that is the particle's track. Each module is made of a $256\mu m$ thick crystalline silicon layer and it is divided in 47 232 pixels of which 41 984 are 400 by $50\mu m$.

The others slightly bigger ($600\times50\mu m$) are located on the sides to minimize signal loss in the zone between two modules. The area of each pixel is bound to that of the read-out electronics, but the rate between length is not: the choice were made to have the maximum performance in x and y thus sacrificing z resolution.

Radiation affects pixels in two ways:

- Increasing the leakage current , requiring a better cooling system.
- Changing the n substrate type to p, thus moving the junction from the upper (Figure 1.12) to the lower face. The bias voltage will gradually increase from 150V to 600V until end of life as a result.

Two techniques were used to increase the radiation hardness and tests found them quite successful, leading to a doubled lifetime:

- Adding oxygen atoms into the crystalline structure.
- With a technique called *p-spray* creating p-doped dividing zones among the n-doped wells. Particularly *p-spray* creates a decreasing distribution near the edges of n wells.

Another mean to reduce the damages is to keep silicon at -20°C during all the data taking, in fact annealing consists of rising the amount of dopant absorbed by the substrates increasing its temperature.

1.3 IBL

The Insertable Barrel Layer (IBL) is a new pixel detector that will be inserted with a new shrunk beam-pipe inside the actual B-Layer, the main reasons for this upgrade are the following:

- The actual inner layer is suffering of a great mortality of pixels that will increase over time due to radiation exposure. This inefficiency causes a

serious loss of b-tagging capability. IBL restores this capability even in the case of B-Layer complete failure.

- Luminosity increase before the HL-LHC completion is too much for the current read-out system, the pile-up will lead to readout inefficiencies. The higher occupancy induced by luminosity will affect the present B-Layer more than other ones, leading to inefficiencies in the b-tagging. With IBL the b-tagging capability is restored and some redundancy added, also the high granularity leads to lower occupancy and higher precision.

- The tracking precision is strongly improved also with pixels closer to the interaction point. Improving the precision of impact parameter results in better sensitivity for signals in physics channels involving b jets

Being this close to the beam pipe forces some constraints that are not needed in other layers: electronics has to be a lot more radiation hard and sensible area need to cover more than 70% of the surface, as is in B-Layer, to achieve those objective the FE-I4 was developed leading to an active area of 90%.

1.3.1 Sensors and Modules

IBL's modules and sensors are different from ATLAS ones because of the technology chosen for the pixels. There were 3 candidates:

- planar

- 3-D

- diamond

Diamond ones, due to economic reasons, were left out, and the FE-I3 chip was upgraded to FE-I4 that is described below.

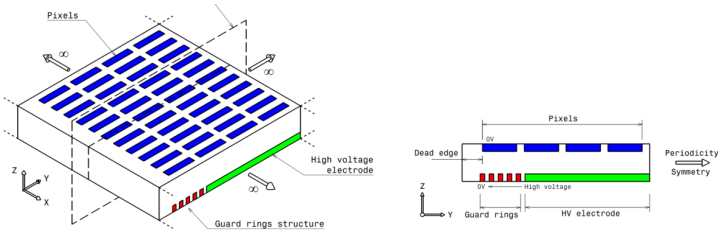


Figure 1.13: Planar Sensor graphic. The thin border ones.

Planar Sensors

Planar sensor were used within the B-Layer too, but the requests on IBL's one are much more strict, in fact the inactive border has to pass from 1mm of the old ones to $450\mu m$, and the acceptable effects on signal has to extend the actual NIEL dose of $2 \times 10^{15} n_{eq}/cm^2$ by at least 2 times.

Various studies were done since B-Layer pixels were produced and now it is known that an irradiated sensor is capable of double the collected charge if it is less thick.

Allowed configurations for planar sensors are 3:

- **Conservative:** Layout of the sensors would not change if this type of configuration were chosen. Length would be reduced to 250 μm to shrink the inactive border, and guard rings would be reduced from 16 to 13. This choice would produce characteristics pretty much equal to the old pixel's while responding IBL's constraints.

- **Thin border:** An n-type bulk with a conservative like structure with guard rings on the p-doped side instead of the n one are the characteristics of this layout. A $100\mu m$ inactive border and a non uniform electric field are the characteristics of this sensor, it seems that the non uniform field effect decrease with the irradiation.

- **Thin p-doped substrate:** These sensors are produced with a technology similar to the one of new ATLAS's strip detectors and a thinner wafer can be

used. During the tests, probably due to some polymer residue on the oxide layer, some discharge verified on FE-I3 chips.

3d

The geometry of 3-D sensors is completely different from planar one and the need of reading from two electrodes at once is risen by the low level of charge collected by this pixels. Unfortunately noise rises along with the number of electrodes and is even affected by their diameter. The difference between full 3-D and double sided

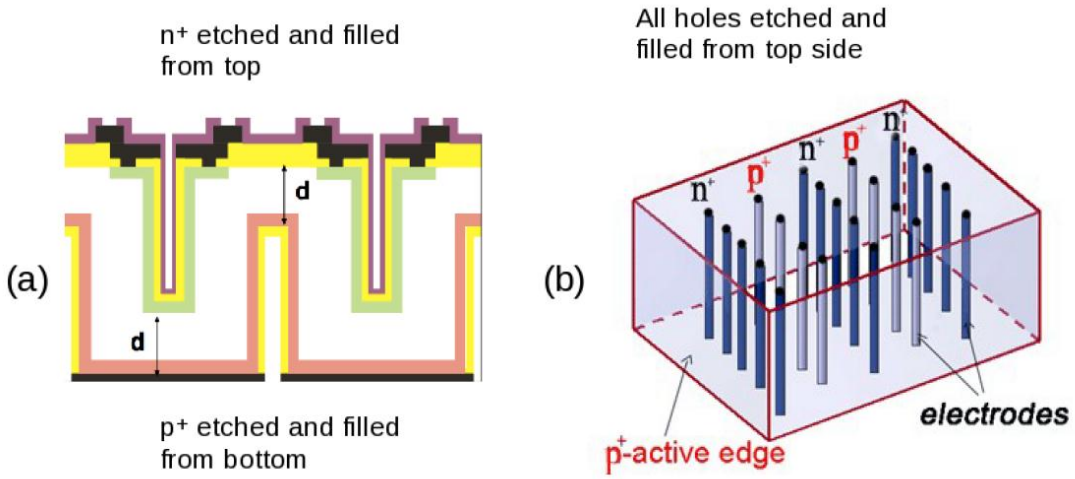


Figure 1.14: Two types of 3-D sensors, double sided(a) and full 3-D(b)

lies in etching, from one side or from each side of the wafer, during the productive process. Full 3-D sensors active area extends much closer to the surface reducing non sensible volume. The faces of 3-D sensors, independently from the type, are much closer one another ant that allows a much lower bias voltage (150V versus 1000V of a planar sensor). This leads to a lower leakage current an thus less cooling.

When a particle passes through the electrode area, efficiency results diminished by 3.3%. This effect affects only in perpendicular particles and thus will not affect

IBL for its sensors are tilted by 20°.

1.3.2 FE-I4

The main achievements of using a 130μm technology in FE-I4 is that the radiation hardness is better than the requested 250Mrad. Single Event Upset immunization is acquired by using a custom layout also three copies of memory and digital blocks are implemented. The new chip is 1.9 by 2 cm^2 and is 200μm thick, in this area are enclosed 26880 pixels.

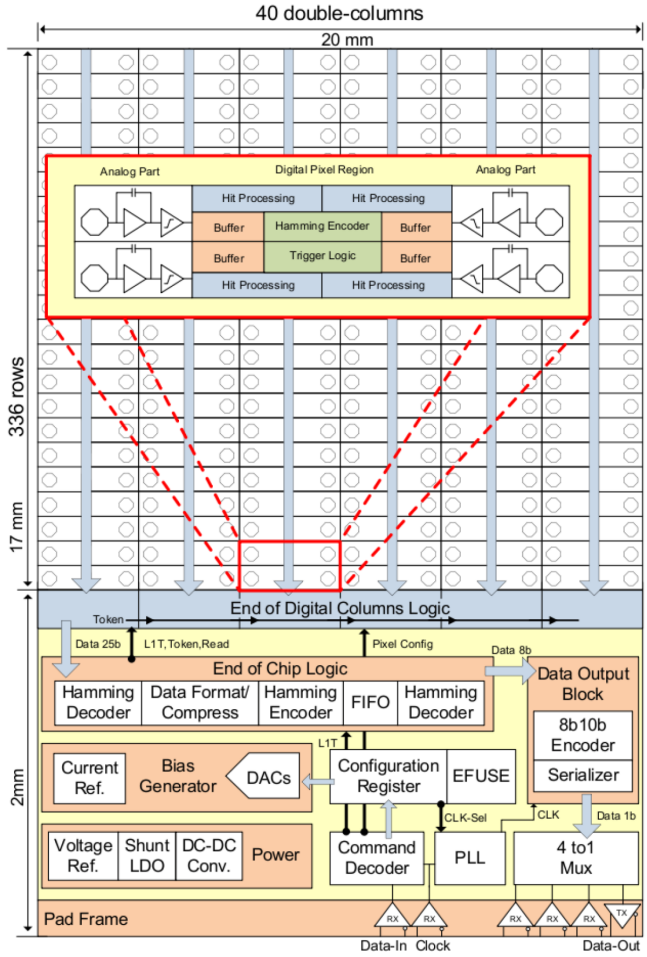


Figure 1.15: FE-I4 architecture layout.

A group of four cells forms a region and shares a big enough memory for 4 events. Time Over Threshold is, along the time of acquisition, the real data because of its proportionality with particle's energy. TOT is how many clock cycles the signal stayed over the threshold and it's computed in the digital part of the chip.

FEI4 power up and configuration

In Bologna the only working bonded FEI4s are one revision A and one B. In addition there is a Timing Interface Module that makes the data acquisition system vey similar to that in ATLAS cavern, actually that's not entirely true since front end is driven electrically instead of optically and this requires a little operational care.

Front end can communicate with the external world with two differential serial streams, one input at 40 MHz and one output 8b/10b encoded at 160MHz. It has also another differential line that brings the clock signal.

FEI4 has been made so there are different types of command to issue various operations. These types have been divided into Fast and Slow commands depending on the bit stream size needed. The chip has two functioning modes, configuration and run. When in configuration mode the chip accept only Slow commands while in run mode it accepts only Fast ones, the only command always accepted is RunMode (see Table 1.4)

When powered up, the global configuration register is completely unconfigured, the first set bit needed is the 8b/10b encoding for the BOC.

A lot of registers need to be set with a proper configuration before the data acquisition path can be filled up issuing a trigger. In Figure 1.16 is showed the full map of global register with all the meanings of addresses.

Name	Field 1	Field 2	Description
Size (bits:)	5	4	
LV1	11101	-	Level 1 Trigger
BCR	10110	0001	Bunch Counter Reset
ECR	10110	0010	Event Counter Reset
CAL	10110	0100	Calibration Pulse
Slow	10110	1000	Slow Command Header

Table 1.3: Fast commands, trigger and slow command header.

Name	Field 3	Field 4	Field 5	Field 4	Description
Size (bits:)	4	4	6		
RdRegister	0001	ChipID	Address	-	Read addressed global register
WrRegister	0010	ChipID	Address	Data	Write addressed global register
WrFrontEnd	0100	ChipID	000000	Data	Write Front end mask bits
GlobaReset	1000	ChipID	-	-	Puts the chip in its idle state
GlobalPulse	1001	ChipID	Width	-	Issue a pulse of Width on a specific line
RunMode	1010	ChipID	sssccc	-	Switch Run(s) and Conf(c) modes

Table 1.4: Slow commands.

Register Address	Bit Send F first in serial steam.....Send 0 last															
	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
0	spare															
1	-	-	-	-	-	-	-	SME	EventLimit: MSB							
2	MSB: Trig_Count				CAE	spare										
3	ErrorMask_0 for service records 15-0															
4	ErrorMask_1 for service records 31-16															
5	PrmpVbp_R: MSB								BufVgOpAmp and GADCVref: MSB							
6	spare								PrmpVbp: MSB							
7	TDACVbp: MSB								DisVbn: MSB							
8	Amp2Vbn: MSB								Amp2VbpFol: MSB							
9	spare								Amp2Vbp: MSB							
10	FDACVbn: MSB								Amp2Vbpff: MSB							
11	PrmpVbnFol: MSB								PrmpVbp_L: MSB							
12	PrmpVbpf: MSB								PrmpVbnLCC: MSB							
13	S1	S0	Pixel latch strobe 0 to Pixel latch strobe 12													-
14	LVDSDrvIref: MSB								GADCCompBias: MSB							
15	PllIbias: MSB								LVDSDrvVos: MSB							
16	TempSensIbias: MSB								PllIcp: MSB							
17	spare								PlsrIDACRamp: MSB							
18	VrefDigTune: MSB								PlsrVgOpAmp: MSB							
19	PlsrDACbias: MSB								VrefAnTune: MSB							
20	Vthin_Coarse (global threshold): MSB								Vthin_Fine (global threshold): MSB							
21	-	-	-	HLD	DJO	DHS	PlsrDAC (calibration voltage): MSB									
22	-	-	-	-	-	-	CP0	CP1	Colpr_Addr: MSB					-	-	
23	DisableColCnfg0 disable bits for digital double columns 15-0															
24	DisableColCnfg1 disable bits for digital double columns 31-16															
25	MSB: Trig_Lat (trigger latency)								DisableColCnfg2 disable bits for DDC 39-32							
26	MSB: CMDcnt12. Out of 14 bits of pulse settings these are bits 0-12. See M13													STC	HD1	HD0
27	PLL	EFS	STP	RER	-	ADC	SRR	-	-	-	HOR	CAL	SRC	LEN	SRK	M13
28	LV0	-	-	-	-	-	40M	80M	c10	c11	c12	c00	c01	c02	160	320
29	-	-	N8b	c2o	EmptyRecordCnfg: MSB								-	LVE	LV3	LV1
30	TM0	TM1	TMD	ILR												
31	PlsrRiseUpTau			PPW	PlsrDelay: MSB						XDC	XAC	-	MSB: GADCSel		
32	SELB(0:15) EFUSE bits to select B shift register for column pairs 15-0															
33	SELB(16-31) EFUSE bits to select B shift register for column pairs 31-16															
34	SELB(32-39) EFUSE SRB colpr 39-32								-	-	-	b7E	-	-	-	-
35	EFUSE Serial number user bits (no function inside chip)															

Figure 1.16: Global Register map.

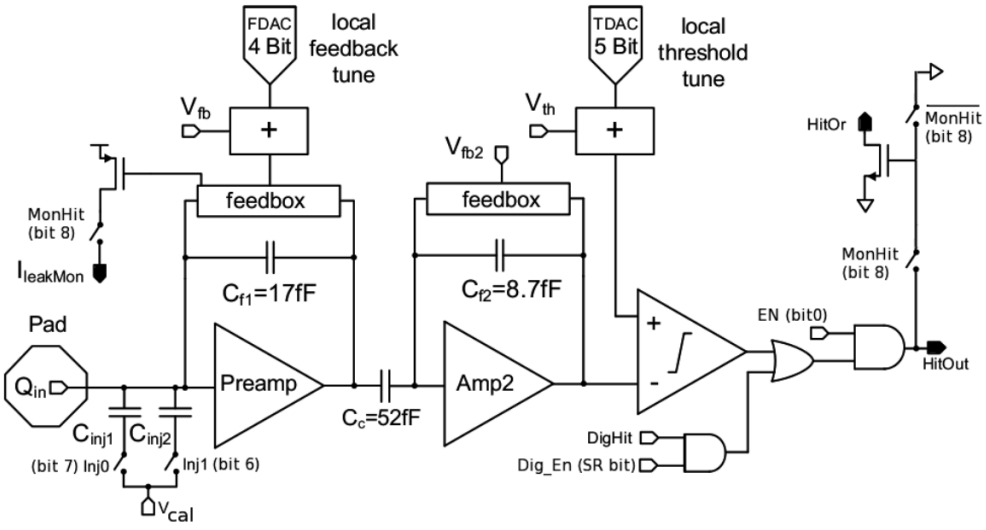


Figure 1.17: Front end analog circuit.

Analog FE-I4 architecture

Two stages of amplification is what has been decided for this part of the FE-I4. First stage or preamp is responsible for the signal shaping and has a gain of 60 while second stage has 6. Being the shaper on the first stage even if the second one saturate it doesn't affect the TOT measure.

FEI4 data encoding

When an LV1 is issued front end sends out some informations in addition to data so it's convenient to know how it communicates with the external world.

Normally after a Start Of Frame sequence (K28.5 8b/10b) should be sent out a Service Record built up this way

- 0xEF
- Code[5:0]
- Number[9:0]

followed by a Data Header

- 0xE9
- Flag
- LV1ID[4:0]
- BCID [9:0]

that precede some Data records that brings informations on the hits

- Column[6:0]
- Row[8:0]
- TOT[3:0] and TOT(2)[3:0] (every col and row is a double column)

then depending on a global register's bit it's sent out either another Service Record or directly an End Of Frame (0xBC).

Chapter 2

Off detector electronics for IBL

The data acquisition system of an experiment as complex as the ATLAS one deserves a large perspective that is outside the aim of this thesis. Figure 2.1 shows a brief graphic explanation of what our experimental setup is. Actually all the

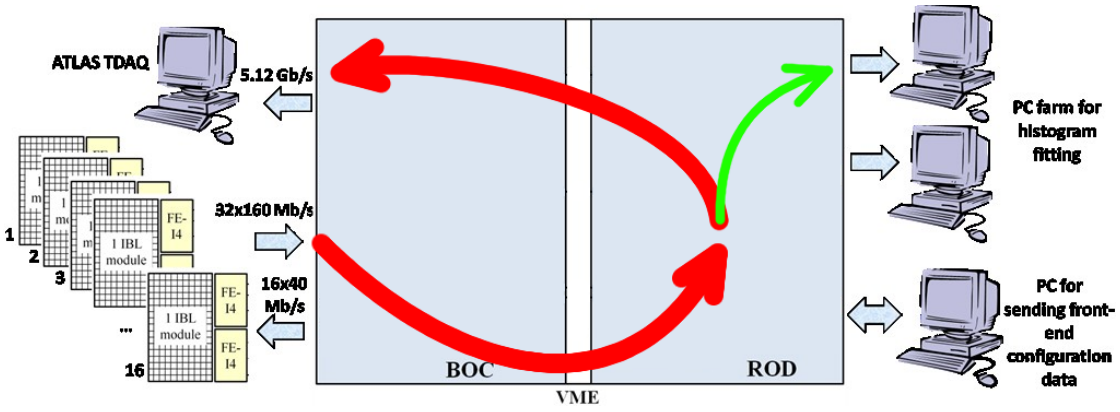


Figure 2.1: Complete visual layout of the data acquisition system. In red the normal data path, in green the Histogram data path.

hardware is implemented either in Bologna and at CERN but here the optical links are missing, mainly because of the transceivers cost. Therefore tests made here are not the real thing, but still quite accurate, as proved by the long list of bug-fix and features developed.

Data path is quite simple, from thirty-two FEI4 front-end chips depart 16 serial lines at 160 Mb/s toward the BOC board with an optical link, there the signal from each line is demultiplexed to eight 12 bits bus that proceeds toward the ROD through a connector named, ROD-side, J3. On the ROD starts up real data formatting to build up what is called a ROD data frame, that is sent towards the computer farm.

On this board data path follows two different ways. Along the first, the formatted data (data-taking events) are sent back to the BOC and then coverted to optical mean to be sent to the farm as seen above. The second path is used for calibration, when data extrapolated are collected and sent directly to a pc farm for histogram calibration purposes, without crossing back the BOC card.

2.1 TIM

TTC Interface Module is part of the ATLAS timing chain. It is the 13th slot occupier 9U VME board in the ROD crate; its tasks are basically the following:

- To propagate the TTC clock all over the experiment.
- To receive and propagate triggers, including LV1 ones.
- To keep updated with Bunch and Event Counters via Bunch Counter Reset(BCR) and Event Counter Reset(ECR) signals, with main TTC.
- To propagate the previous informations to the ROD.

TIM-ROD interface in the current version is exactly the same as it was in the previous, and shall not change.

2.2 SBC

Single Board Computer, as the name suggests, is actually a computer mounted on a 6U board with a VME interface chip. It is used to control all the VME

operations on the ROD, and it can actually program some of its components. Also it can be used to monitor the temperature on a particular ROD's component.

2.3 IBL BOC

Three Xilinx Spartan 6 FPGAs are responsible for controlling the card and processing the data from and to the detector as well as to the higher-level readout system. The BOC Control FPGA (BCF) is responsible for the ethernet and set-up bus communication with other devices. The two BOC Main FPGAs (BMF) receive 16 160 Mbit/s 8b/10b encoded serial links from front-end and, after decoding, send them out to the ROD in form of 8 12-bit buses. They also manage the output to 4 optical S-Links transceivers that carry out the data to ATLAS ROBIN boards equipped computers. The BOC card also distributes the global 40 MHz clock to the detector and to the ROD card. The two BMF also encode the configuration data coming from ROD into a 40 Mbit/s serial stream and then send it out to front-end, it can also generate this stream on his own for testing purposes. The deserialization of the incoming data from the front-end chip is part of the RX path. After the data collection and the word alignment the data are decoded and sent to the ROD card.

2.4 IBL ROD

The Read Out Driver is the off-detector board that interfaces the standard ATLAS Data Acquisition (DAQ) chain with the specific readout components inside the detector. In particular the device is designed:

- To propagate the timing and trigger signals, as BCR or ECR to the front-end electronics.
- To send an appropriate configuration to the connected front-end chips.

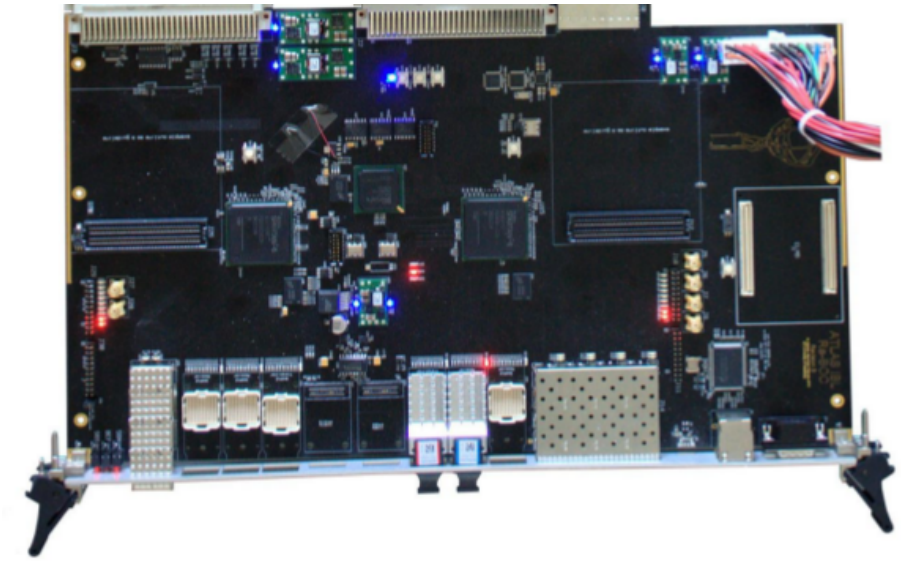
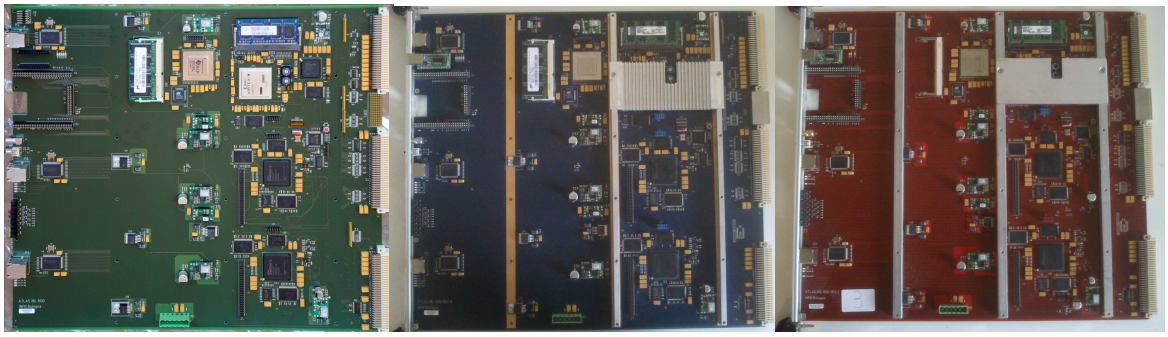


Figure 2.2: IBL BOC card with, from the left, the three FPGAs BMF BCF BMF

- To receive event fragments, from 32 FE-I4 and to compact them into a single ROD one, then send it back to Read Out Link connected to the BOC transceivers.

One of the decisions in the IBL project was to clarify if a new ROD board was required or the current SiROD card might have been adapted. Finally, it was clear that to overcome the data-rate expected increment and the new FEI4 chip to address, a new ROD card had to be designed. Consequently, a new BOC card was also to be designed. IBL's natural modularity is one stave, 32 FE-I4, but the old board can only handle 16 at a time. The upgrade should also be capable, with a dedicated firmware, to eventually substitute its ancestor dealing with Barrel Layer's FE-I3 chips.That is the reason why new ROD is still interfaced with the VME bus.

Backward compatibility is also important because IBL is going to be an extension of the existing detector. The VME's low data throughput is not a problem any more for we have two Gb ethernet connections to pass histograms through.



(a) ROD REV A (b) ROD REV B (c) ROD REV C

Figure 2.3: Rod versions compared

Calibration process is done by injecting a charge into each pixel of the front end chip and checking what comes out from the data chain; that is a fundamental process because, when it comes to real data, we must be able to tell what is a *"normal"* reaction for each pixel.

This process, called scan, generates a large number of events that are processed into the ROD; the relative histograms are sent to the Histogram Fit Farm via Ethenet.

The new board should be compatible with the old and the new BOC and, to do that, it has to feature the:

- Maximum compatibility with J3 custom backplane, in particular with the TIM part of the connector, while a new mapping could be arranged for BOC to ROD communication.

- Modularity correspondent to sixteen 160 Mb/s input channels and two 160 MB/s S-Link output, with the possibility to scale that down to eight and one, for backward compatibility with siROD.

Now the ROD is under production after being tested for at least one year and the current version, which is the final one inside this project, is the Rev C. This work is ongoing through the testing and firmware-software development, which I made personally.

2.4.1 Hardware

The 14-layers PCB is assembled with these components:

- 1 Digital Signal Processor (MDSP): 1 Texas Instruments TMS320C6201-GJC200, it is the same DSP device as in the SiROD board.
- 32 MByte SDRAM DDR
- 4 Mbit FLASH SST39VF040-70-4C-NH
- 3 types of FPGA devices:
  - 1 Xilinx Spartan6 XC6SLX45-FGG484: it is the new PRM device interfacing with the VME bus, the MDSP and the ROD Controller FPGA.
  - 1 Xilinx Virtex5 XC5VFX70T-FF1136: it is the new ROD Controller FPGA. It also hosts as an internal HW core a PowerPC device, whose performances will be compared to the MDSP.
  - 2 Xilinx Spartan6 XC6SLX150-FGG900: they implement the ROD data path (data gathering, event fragment building, histogramming). Each of these 2 Spartan6 devices features:
    - one 2-Gbit DDR2 chip (Mictor MT47H128M16RT-25E)
    - two 512Kx36 SSRAM chips (Cypress CY7C1370D-250AXC- ND).
- 2 GByte DDR2 SODIMM
- 64 Mbit FLASH Atmel AT45DB642D
- 3 Gbit Ethernet interfaces with PHY DP83865.

The ROD front panel features:

- 1 TTCrq mezzanine
- 1 USB mezzanine (UM232R USB)

- 1 JTAG connector (J9) for FPGA programming
- 1 LEMO trigger input (J4)
- 1 reset push button (SW1)
- 3 Gbit Ethernet interfaces
- 8 status LEDs

Power supply

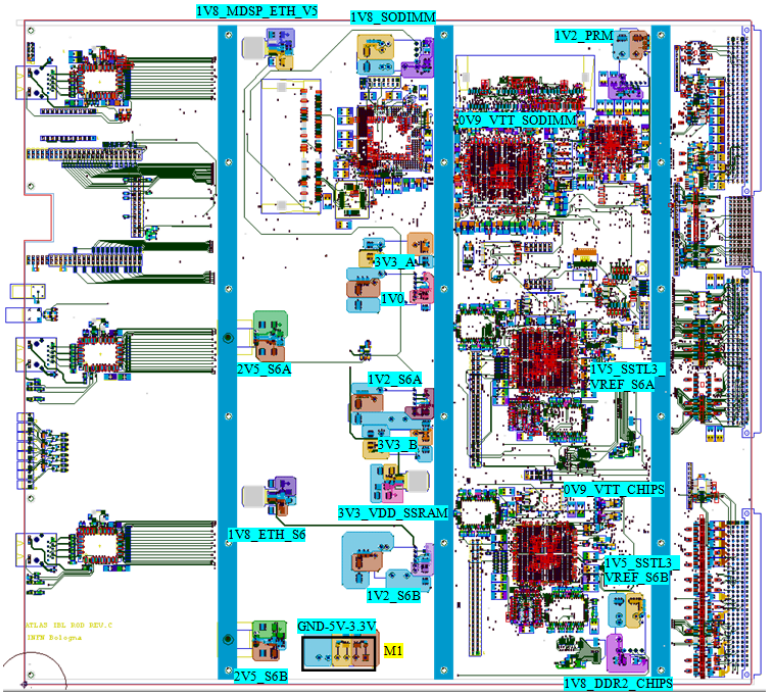


Figure 2.4: Power supply distribution on the board.

This complicated board requires a lot of different power supplies. Having different power suppliers is a reasonable approach for a board that is expected to run for a long time.

Clock distribution

There are two main clock sources for this board: an internal one, used when the board is in standalone mode, and an external one, coming from the BOC card via backplane as a Stub Series Terminated Logic (SSTL3). A Dip switch controls which of these clock sources drives the whole board. A Phase Locked Loop chip then multiplies and distributes the needed clock sources all over the board.

Also the BOC can be configured to lock on the TIM clock, with this set-up all the clocks inside the crate are perfectly in phase.

Two different clocks are needed by Virtex and Spartan FPGA, 100 and 40 MHz, while the PRM (Program Reset Manager) receives only the 100MHz and than produces by itself a 40MHz. PLL does not distribute the clock to Ethenet RAMs.

JTAG

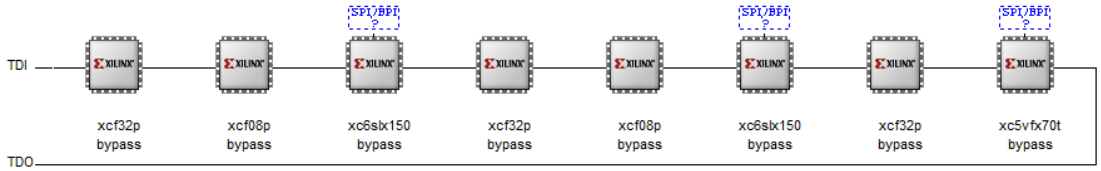


Figure 2.5: The main JTAG chain as seen by IMPACT (Xilinx)

The JTAG is a standard control and programming method for FPGA devices. On the board there are two different JTAG chains: one of them is used to program the PRM and its EEPROM (Electrically Erasable Programmable Read-Only Memory), the other one, that is fully connected inside the PRM firmware, can, if all jumpers are present, see the following devices:

- XCF32P (spartan 6A PROM)
- XCF08P (spartan 6A PROM)

- XC6SLX150 (spartan 6A FPGA)
- XCF32P (spartan 6B PROM)
- XCF08P (spartan 6B PROM)
- XC6SLX150 (spartan 6B)
- XCF33P (Virtex 5 PROM)
- XC5VFX70T (Virtex 5 FPGA)

BOC-ROD wires

There are 96 non-spare SSTL3 wires connecting BOC and ROD cards. They can be divided in groups of 12 each. One group is composed of 8 data bits, 1 control bit, 1 Write Enable bit and 2 Address bits. They handle the data from the Front End so they are a delicate part of the data path.

- Write Enable: Active low bit, asserts the validity of current data.
- Control: Active low bit, labels the current data as a control word.
- Address[1:0]: states which channel generated the current data.
- Data[7:0]: part of the FE-I4 output, 24 clock cycles are needed to pass down an entire frame.

The reason for Address being only two bits lies in the system modularity, each spartan 6, in fact, implements two separated data paths that do not interact. In conclusion we have 2 FE-I4 chips for each channel, by 4 channels, by 2 data paths for each Spartan 6. Altogether these make 32 FE-I4 chips interfaced with one only ROD, and this addresses one stave.

VME

Versa Module Eurocard is a standard protocol and specification that we followed for board dimensions and for buses. Each slot is characterized by the geographic position inside the crate. Every bus requires a controller that can be either of the boards or, as in the study case, the SBC. This bus was used, in previous version of data acquisition system, to download histograms. Now it's only used for updating and monitoring purposes since histograms, as said earlier, pass through the Gbit Ethernet.

Ethernet

Each FPGA has its own Ethernet connector corresponding to the front panel (Figure 2.6). Virtex5 Ethernet can be used to access registers of all the FPGA's processors and even to load the program to spartan6 embedded MicroBlazes.

Virtex 5

This is the Master of the Read Out Driver, which must interface with the front end chips, the triggers that comes from TTC Module and all the informations that refer to the Trigger itself. This task will be accomplished, depending if we are calibrating or data taking, by the PPC inside the Virtex 5 FPGA or by some other components also implemented inside the FPGA. The reasons behind this double control path are:

- allowing the possibility to use the ROD out of crate;
- the chance to make support for the TTC Module that communicates trough VME BUS;
- the alternative way to test the data path even without a TIM board, sending triggers via ethernet.

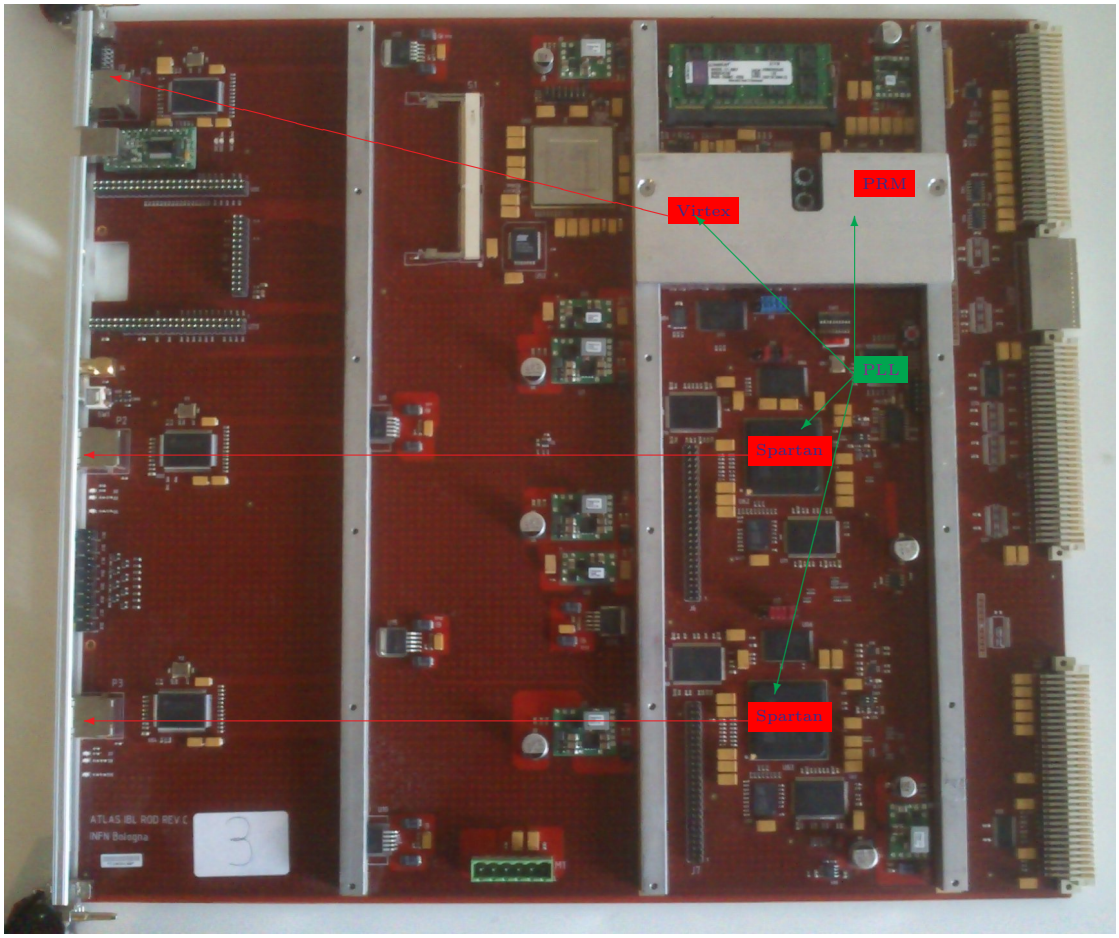


Figure 2.6: ROD REV C, Clock paths(in green) and Ethernet connection (in red)

Spartan 6

Spartans are smaller FPGAs that cope with all passing data during the data taking process. Also they collect histogram data inside an SSRAM and send them to an histogram server if required. To master all those tasks a MicroBlaze processor was implemented on each spartan running an application whose main concerns are the TCP/IP communication and the register block used to configure the data taking.

PRM

This is another Spartan 6 dedicated to the VME interface (HPI port).

2.4.2 Firmware

There are many versions of the firmware and each version has some branches to test a specific layout configuration. The main ones have the following general configuration.

The firmware of the Virtex5 has included an old MDSP code that is still used in the current SiROD board used in the pixel layers B0, 1 and 2.

Stable Firmware

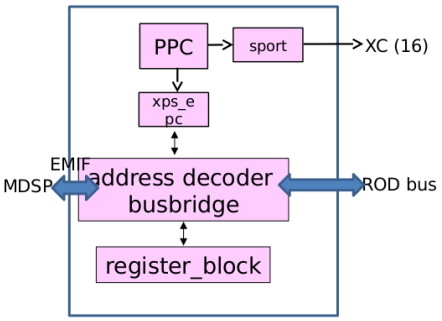


Figure 2.7: Rodmaster firmware logic blocks in the stable branch

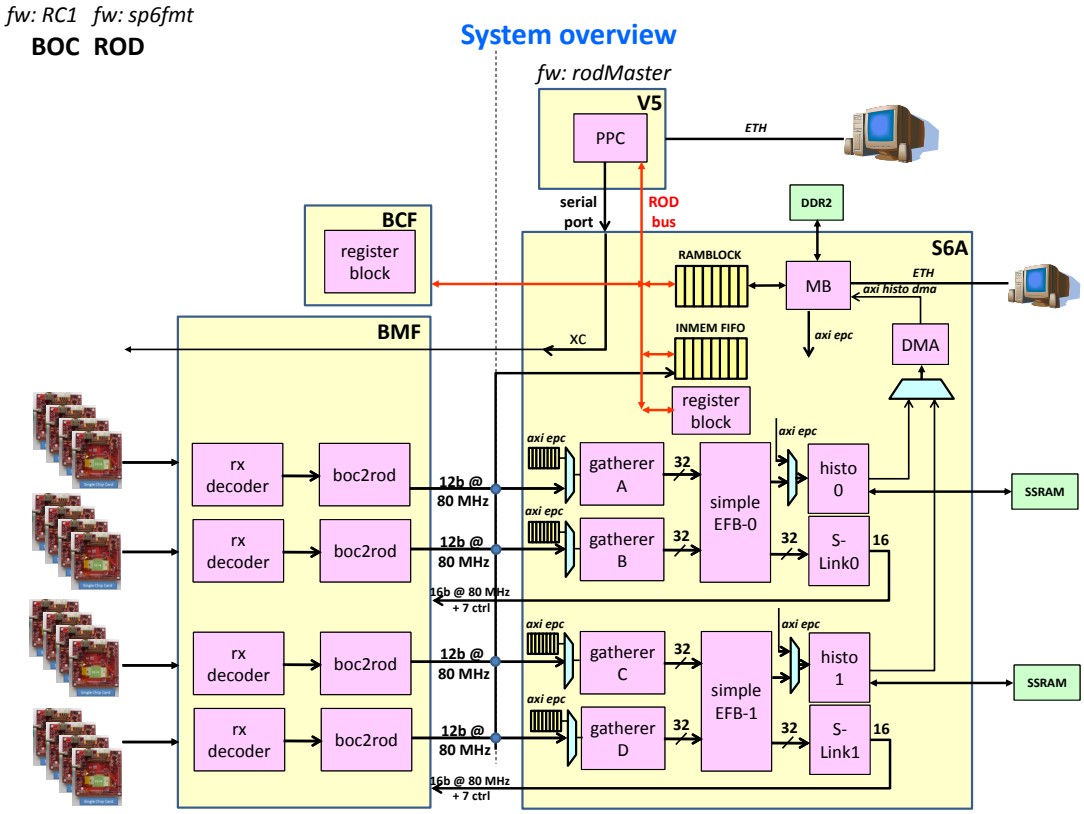


Figure 2.8: Overall view of the firmware seen as logic blocks, the Virtex part is expanded in Figure 2.7

Virtex 5 This FPGA's firmware has the duty to pass down configurations for the front-end and manage trigger commands and all configuraion registers of the board.

Set aside trigger's logic all operations with ethernet, ram, flash and so on are driven, or indirectly controlled trough registers, by PPC.

The main logic blocks that built up this code were originally only essential ones, and triggers were issued only via PPC, as we see in Figure 2.7.

PPC Power PC is a specific architecture of microprocessor embedded in the Virtex 5 FPGA. It is possible to modify the buses and peripherals of this component with Xilinx's program called EDK. Figure 2.7 shows in particular two important components: EPC(External Peripheral Controller) , use to read and write certain memory cells into FPGA code, and "sport" (Serial Port) that can access directly XC bus to write configurations on front end chips. EPC directly interfaces with a block called Address Decoder Busbridge that works as a demultiplexer.

Address Decoder Busbridge As said above it works as a demux, its duty is to route each read or write command to the right register. PPC can also write and read all registers on all main FPGAs (PRM is not one of them). As can be seen this component interacts with the Virtex 5 internal register block, with the ROD bus and with the now unused MDSP component.

Register Block

Spartan 6 The heart of data taking, from these component transits all data from sixteen front end chips.

As can be seen in Figure 2.8 the EFB is named "Simple EFB" that is because this firmware is only a version written in Bologna to emulate the entire data chain but misses certain software programmable features that shall be included in the Development Branch one.

Data path is routed trough sixteen FIFOs and grouped into quartets under one gatherer. This empties the FIFOs, one at a time. This logic shall change before runs because it can generate problems if triggers are too close.

Aafter this stage all data are passed down to four EFBs (Event Fragment Builder) that groups up all the data relative to a particular trigger in a ROD Frame labelled with the appropriate timing informations.

Now all that remains to do is sending out the raw data previously formed. The router sends appropriate informations either to S-link and Histogrammer.

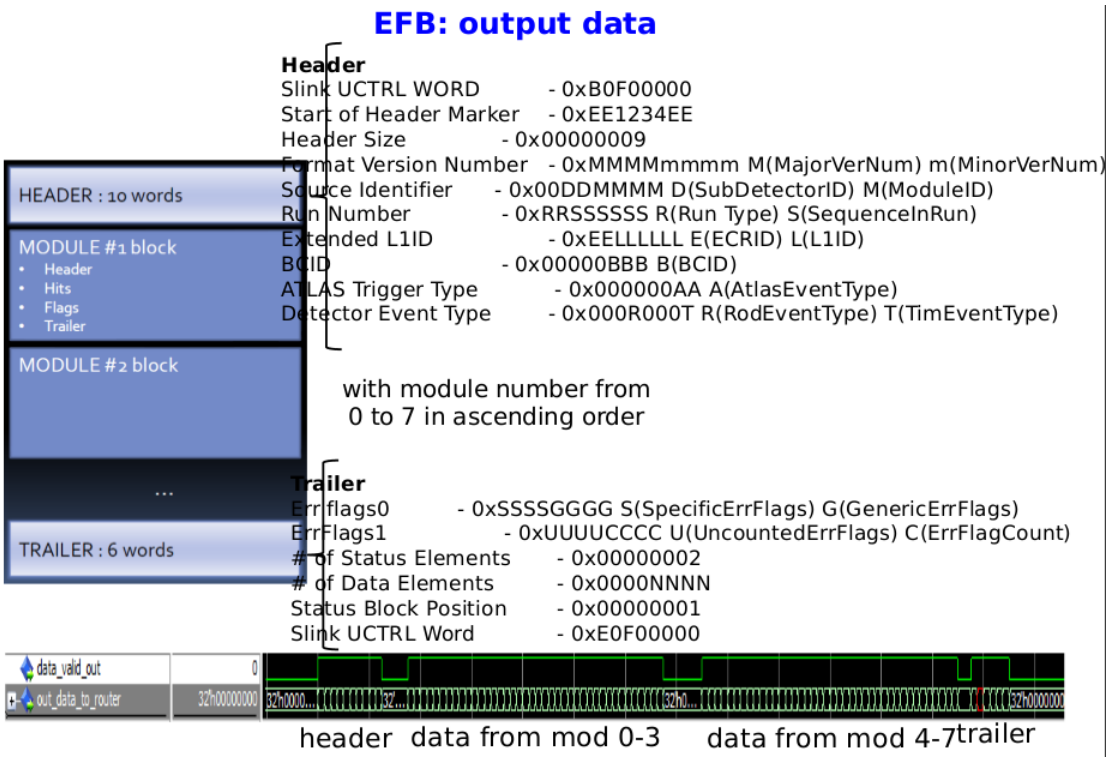


Figure 2.9: Data format of IBL ROD frame.

S-links optical transceivers are placed on the front panel of the BOC board so the informations have to transit on the ROD-BOC bus.

Histogrammer's final objective is to produce data for calibrating purposes and to write them on the DDR2 RAM waiting for the MicroBlaze to send them out via 100 Mb/s ethernet to a fit server.

Gatherer The gatherer, as the name suggests, is responsible for gathering data from all its input channels. The first component that needs a description is a dual clock FIFO that works as a connection between two clock domains: the 80MHz of the bus and the 40MHz for the FPGA. Four of these components are instantiated inside of the gatherer, one for each BOC-ROD link described previously. Along with this definitive data path there is a possible test data path that can inject data, with the epc peripheral, directly inside the component as shown in Figure 2.8.

Simple Event Fragment Builder Two gatherers are then connected to a single EFB that adds dummy, in this branch, header and trailer infos such as: trigger type, event id, bunch counter id. Between gatherer and EFB there is also a FIFO for "waiting to be processed" data.

Inmem FIFO This is mainly a debug feature: this FIFO collects all inputs from the BOC-ROD buses and can be accessed by the PPC via epc peripheral; data can then be verified even before entering the gatherer giving an insight of what should happen.

Historammer Histogrammer collects informations about calibration runs. As inputs it has the TOT and address coming directly from the FE-I4, it creates a map of pixels calibration responses inside a dedicated memory. An example of these maps can be seen below in the Test chapter.

MicroBlaze It is a software processor that must be included into the Spartan6. Conversely the PPC is a hardware component embedded into the Virtex5. There are other alternative components that can be used, for now it manages the Ethernet connection and sends out histogram read by the RAM through it.

S-Link Merely an interface that implements the S-Link chip connection its protocol il like the one needed to write on a FIFO. It sends out data toward the optical transceivers on the BOC.

Development Branch Firmware

Virtex Virtex firmware has been extended to include all the functionalities needed. In Figure 2.10 the yellow blocks are all newly developed to interface the external world without relying on the PPC. Some of them as the internal scan processor and diagnostic generator are far from being complete so they will not be described.

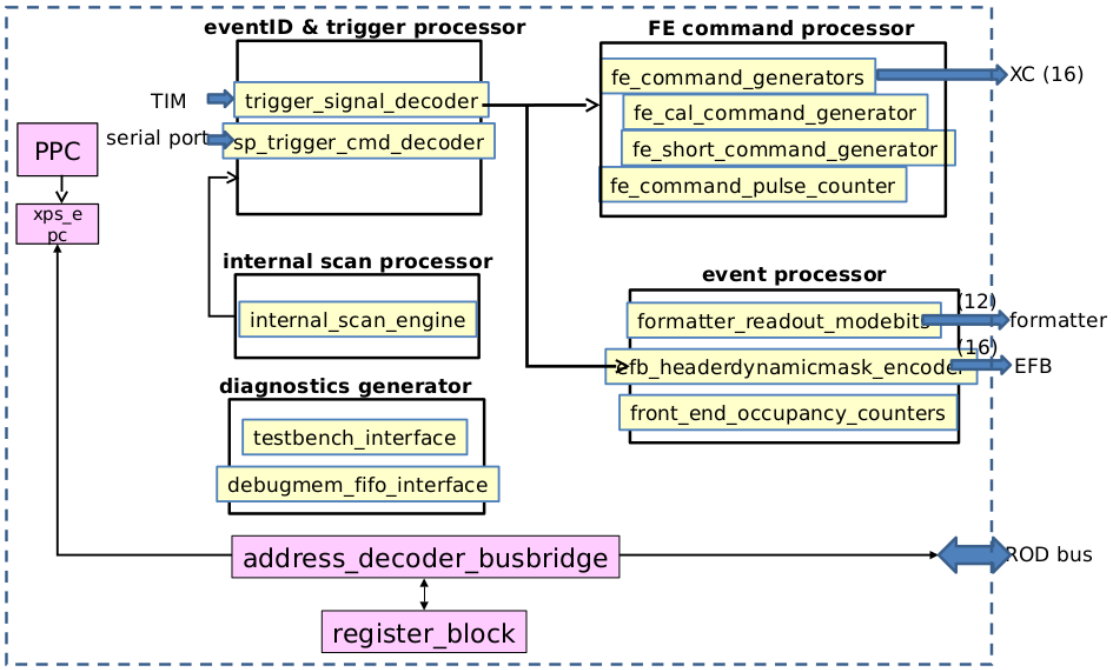


Figure 2.10: Rodmaster firmware logic blocks the under development ones

Event ID and Signal Processor As can be seen Event ID and Signal Processor can be driven either by PPC or by TIM signals. One of its duty is to process the trigger informations (like Event ID, Trigger Type and Bunch Counter

ID) and deliver them to the Spartan via Evet Processor. The other one is to tell the Front End Command Processor to generate and send the necessary commands, like LV1, to the front end.

FE Command Processor This block generates the proper commands for the front end, it can generate fast and slow commands so it is involved in the configuration process too. When a trigger is issued by the TIM it immediately generates an LV1 command, this is a much faster process than issuing an command via PPC.

Event Processor Event ID, Trigger Type and Bunch Crossing ID need to be sent Spartans EFB. They will be written inside the header of each ROD event as identifiers.

Spartan

Formatter This is the component that contains the gatherer, the EFB and the dual clock FIFOs. Formatter has undergone a bit upgrade mainly in the EFB part, but also in the gatherer.

Event Fragment Builder Now the EFB does not generate dummy IDs and Trigger types, they are received from the Virtex and incorporated in the ROD data frame.

Gatherer Gatherer has become smarter and now, instead of emptying the dual FIFOs in order, checks firstly the full ones. Still this behaviour has not been tested yet.

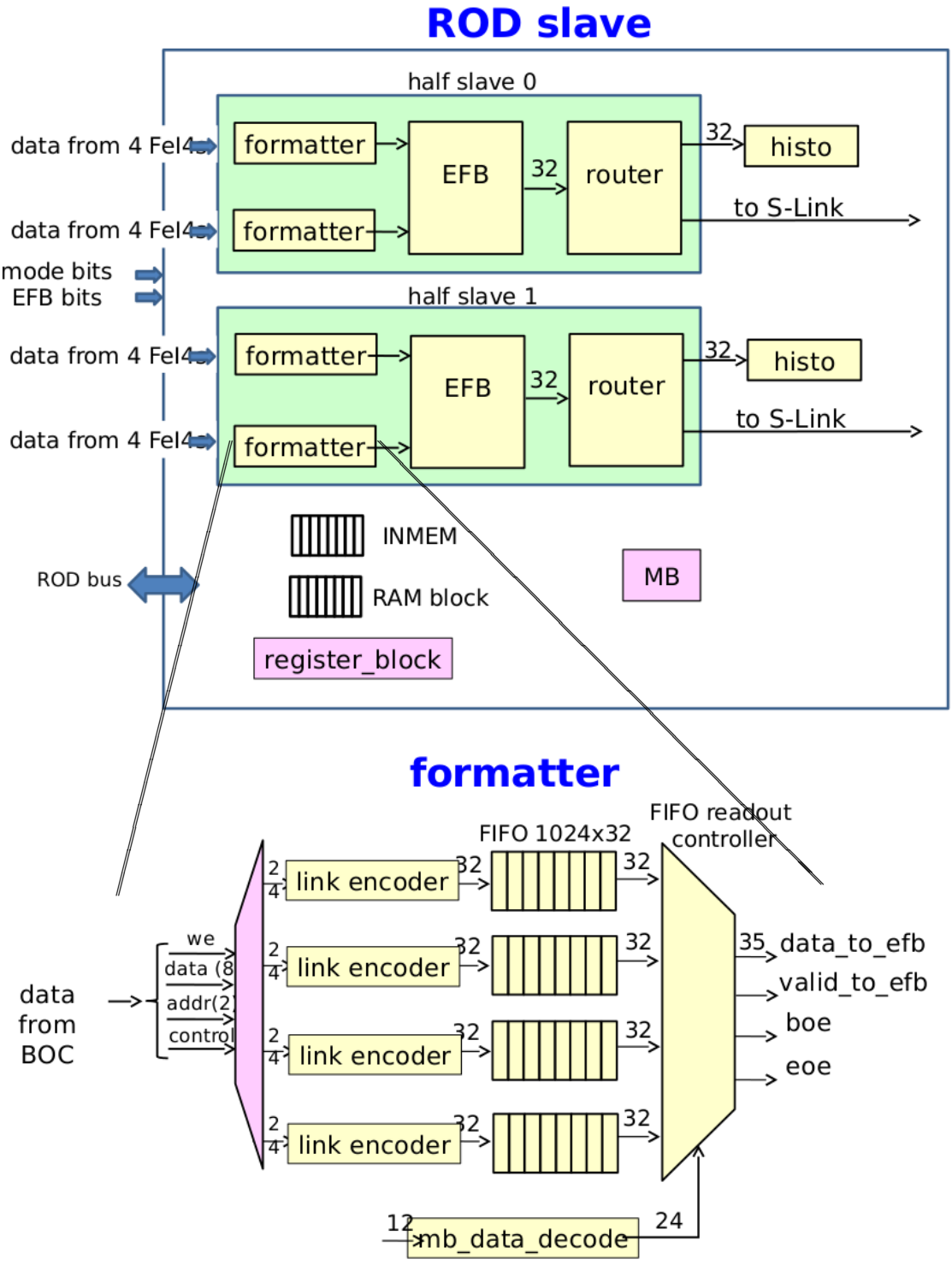


Figure 2.11: Slave firmware: the formatter in picture above is represented in tho one below.

Chapter 3

Tests

This chapter will explain in detail in which way preproduction and then production boards are tested. When a prototype PCB is produced and then assembled there are a lot of possible small errors that must be spotted and removed even before turning it on, especially wrong side mounted tantalum capacitors and accidental short circuits.

To explain some more advanced test a more detailed knowledge on the FPGA workflow is needed. Field Programmable Gate Arrays are pieces of hardware that can be programmed to execute some specific tasks, programming involves a change in the electrical behaviour of the component so in many ways it's different from a program that runs on a microprocessor. Writing firmware for testing purposes often does not require knowledge on what operations the electronic is going to perform. Sometimes the scope is only to test if there are hardware problems on buses or connectors. Once a problem has been found, however, the cause need to be identified and removed.

3.1 Power Supplies Tests

After a visual inspection checking if the components are correctly mounted and that there are not evident short circuits, the most basics of the tests can be started.

Once the board is powered up all the power supply are to be tested for the right output voltage, fairly easy with PCB in the Figure 2.4.

Absorption with the current firmware version should be around 25.7 W in total, 2.5A at 5 V plus 4 A at 3.3 V. SSRAM are not currently in use the full featured power consumption is expected to be around 32 W per board.

3.2 Temperature Tests

On power-up a thermal camera is the most useful tool to prevent component heat damages, which can be caused by soldering residues that creates electrical contacts between pads that should be isolated, or by components mounted the wrong way.

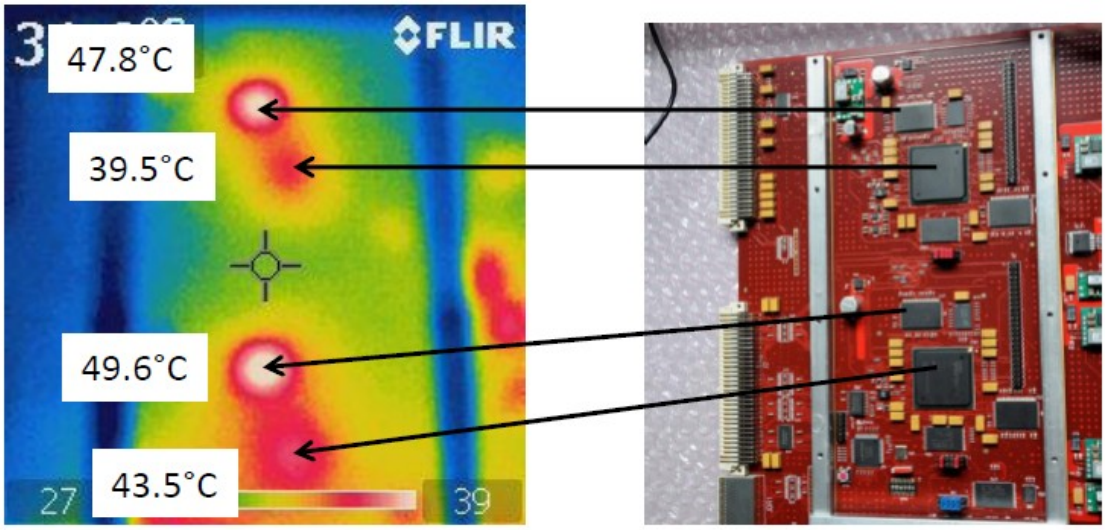


Figure 3.1: An image taken with the thermal camera of the board undergoing 200MHz RAM test.

3.3 Clock Distribution Tests

Clocks are usually Low Voltage Positive Emitter Coupled Logic (LVPECL) differential signals all over the ROD. On the BOC side these are PECL differential

signals and the conversion is done on the ROD right after J3 connector. Clock is then routed to a Lattice PLL which distributes it to all the needed components. PLL also multiplies it to match particular components needs, for example the PPC inside the Virtex needs a 100 MHz clock.

The preferred clock source is the one on from Timing Interface Module (TIM) and that's because it's the only interface with all the ATLAS experiment timing and thus it's the clock that must work when the data taking begins.

In fact there are other clock sources that can be used to work with the ROD:

- 40 MHz internal clock source. There's a quartz on ROD near the PLL that produces a 40 MHz clock source that is used when the board is stand alone.
- The BOC has a 40 MHz internal clock that has been received by ROD on J3 connector.
- Running a program called PLLInfo the BOC board can be configured to lock on the clock generated by the Timing Interface Module creating a chain of boards all with the same clock.

The clock is checked on the PLL output locked pin with an oscilloscope.

3.4 ROD Master Tests

3.4.1 TIM

The purpose of this test is to find out any communication problem with the Timing Interface Module.

Any failure in one of the signal listed in Table 3.1, apart from spares, leads to a certain data loss on the entire data acquisition chain, so a robust check is required and and also it takes a long run period.

Before running any test the ROD clock needs to lock on the TIM one, to do that PllInfo program is executed to change BOC clock source from internal to

external, so when the ROD locks, it does it on the global clock.

A dedicated firmware has been written in order to perform the following checks:

- Every trigger pulse shall be followed by event ID and Type.
- Every event ID shall increase by one the previous count.
- BCID shall be equal to the number of clocks cycles between two triggers.
- Event Type shall be always the same since it is saved on a TIM register.
- ECR and BCR frequency can be also programmed and so checked.
- When the busy is asserted ROD-side trigger generation shall stop.

The test was ran for at least 1 hour and during this time no error has been found.

TTC Bus signals	Description/Function	NOTES
TTC0	L1A - L1 Accept Trigger	Active Low, 25 ns pulse
TTC1	ECR - Event Counter Reset	Active Low, 25 ns Pulse
TTC2	BCR - Bunch Counter Reset	Active Low, 25 ns Pulse
TTC3	CAL - Calibration Strobe	Active Low, 25 ns Pulse
TTC4	Event ID - L1ID and BCID Values	Active Low, Serial Stream
TTC5	Event Type - ATLAS and TIM trigger type	Active Low, Serial Stream
TTC6	Not Used, Connected to the controller	Active low
TTC6	Not Used, Connected to the controller	Active low

Table 3.1: Meaning of the signals coming from the Timing Interface Module

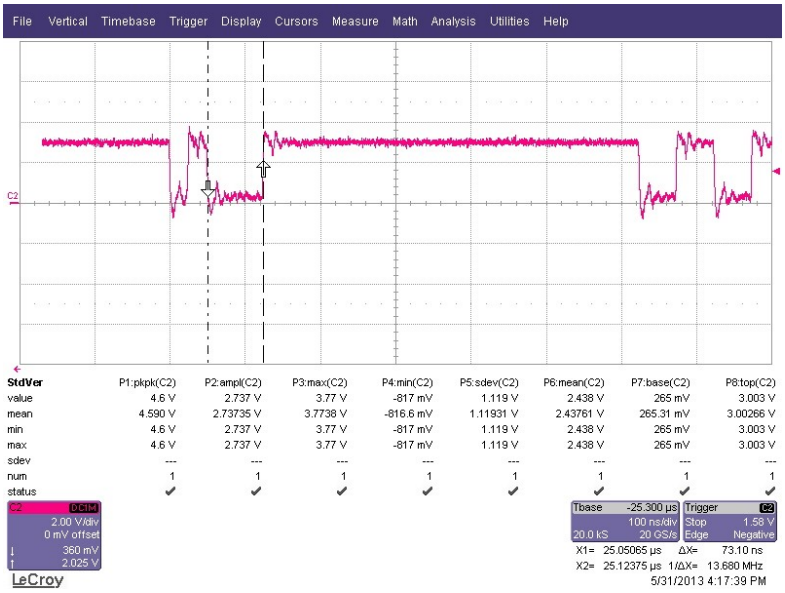


Figure 3.2: Signals have been checked even with a digital oscilloscope.

3.4.2 DDR2SODIMM

On the PPC implemented inside the rodmaster it has been run a program that reads and writes all the DDR addresses and reads them back, if a mismatch error occurs the process stops returning the failed address. This program found an address error that cannot be removed on one of the ROD rev B boards. Since this is not a production board the error is not critical but it cannot be used to take data.

3.4.3 Ethernet

There are three Gb ethernet each connected to one FPGA, the two linked with the slaves shall function at full speed to allow a fast histogram data output.

This one on the Virtex is usually just tested issuing commands to PPC and verifying their execution.

3.4.4 PRM-ROD Master Interface

The PRM – ROD master interface is mainly built upon the 77 lines shown in Figure 3.3.

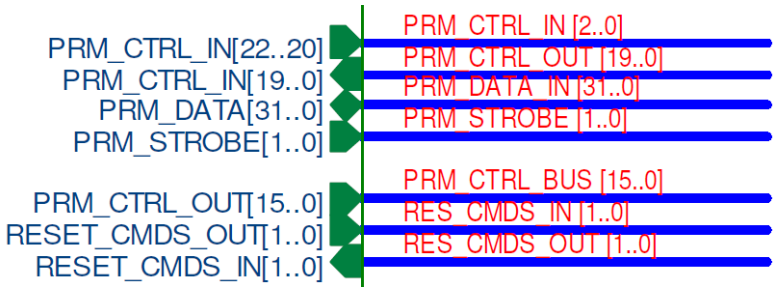


Figure 3.3: List of Buses that links PRM to Rodmaster

Some of them (40) are used to implement the HPI port, which is used to access the PPC address space via VME (for instance they are used to program and readback the ROD master FLASH device):

- prm_data (32 bits);
- prm_ctrl_in (3 bits);
- prm_ctrl_out (4 bits);
- prm_strobe0 (1 bit).

Four of them (reset_cmds_*) are used to exchange reset signals (and related acknowledge) between ROD master and PRM. The remaining 33 lines are not used by the current firmware version. The proper connection of these signals is evaluated sending known pattern from the ROD master and checking their value on the PRM at 80 MHz.

3.4.5 Master Slaves connection test

In order to check the proper connection and quality of the signals between the ROD master and the slaves, a data pattern at 80 MHz is sent from the master

to the slaves, where the data content is checked against the expected values. In particular the pattern can be decided by the user at the software level running the ELF file on the PPC, which fills a RAM block on the master, whose content is sent towards the slaves. Figure 3.4 shows the tested signals (the signals ending in A(or B) are going to slave A or slave B, while the others are going in parallel to both) the can be logically divided in the following groups:

- EFB event dynamic mask bit;
- formatter mode bits;
- XC;
- trailer informations;
- spares.

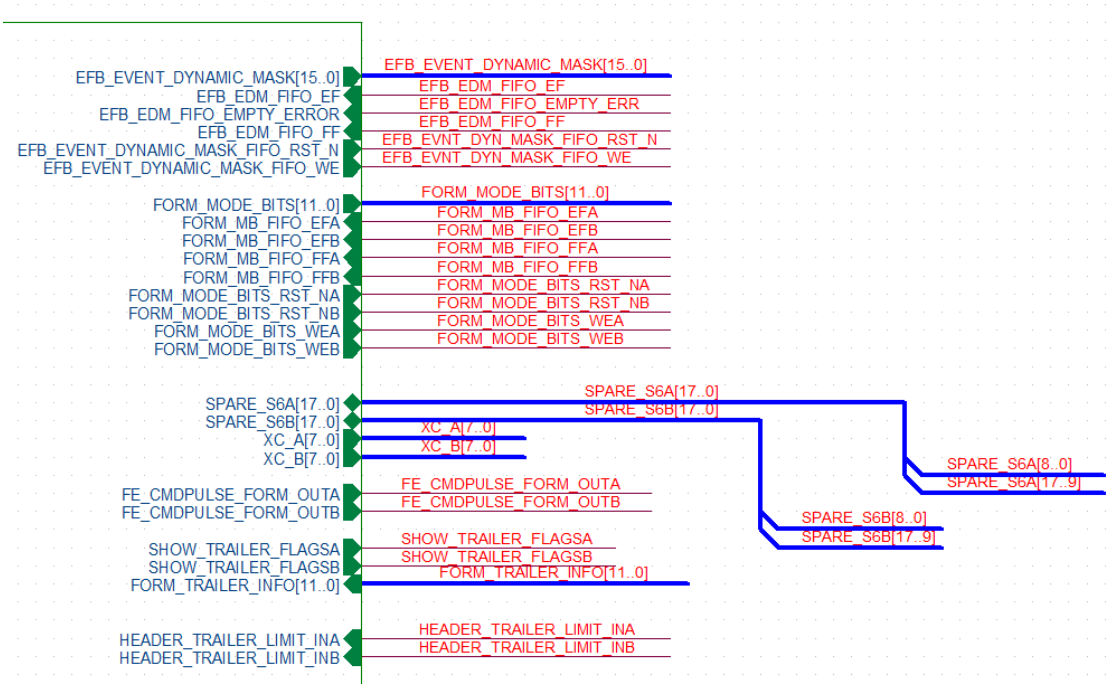


Figure 3.4: List of Master to slaves signals

Two types of error detection are performed as in Figure 3.5:

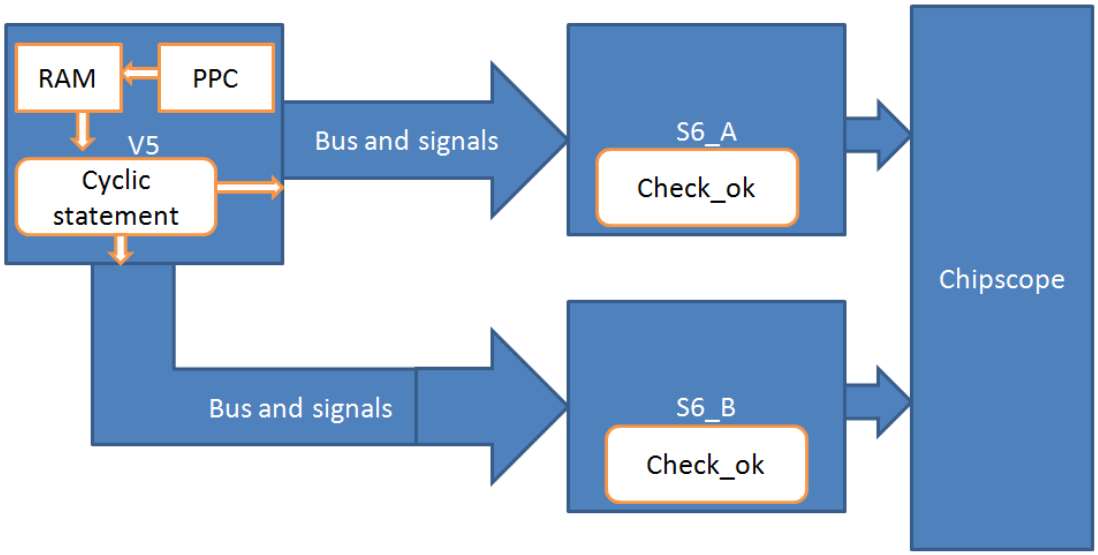


Figure 3.5: Performing the test of the bus in Figure 3.4

- with a known pattern: a word and then the complementary one are sent and the slave checks if the second one corresponds to the complemented original one.

- with a CRC algorithm: along with the 16-bit message a 16-bit checksum is generated with CRC. When the message is received, the S6 performs the check inside a pipeline, not to lose any patterns. The CRC is effective in detecting up to "length of the checksum" bit flips, in our case being 16 each for the message and the divisor, so that we can detect virtually any error.

A simple implementation of CRC algorithm can be explained this way: the message is padded with zeros by the length of the divisor. If the message bit above the leftmost divisor bit is 0, nothing is done, otherwise the divisor is XORed into the message, shifting it to the right one bit. The process is repeated until the divisor's MSB reaches the right-hand end of the input row. The message is now zero and the padded bits are forming a signature, now we send the original message along with our generated signature.

3.4.6 ROD-bus PPC Interface

The RODBus is driven by the PPC through an External Peripheral Controller (EPC) and it is used to access many registers on Microblazes and on the BOC. Another useful feature is to write a binary file directly into Microblazes memory to be executed. As can be seen in Figure 3.6, beside address and data there are many control signals inside this bus. The main reason behind having the PPC controlling directly the bus is to not have to write down a brand new communication protocol.

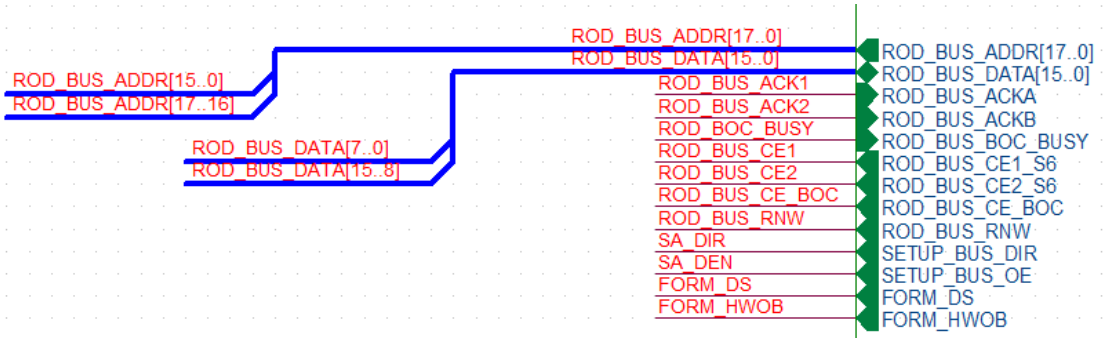


Figure 3.6: ROD bus signal list.

3.4.7 XC Test

The current version of the firmware implements one serial port driven by the PPC which can be forwarded in parallel to 16 XC lines (serial 40 MHz data used to program and send triggers to the FEI4B chips), depending on the value of a register that decides which links shall receive the serial data.

The 16 XC lines flow into the ROD slaves (8 each) and then are forwarded towards the BOC via the backplane. Only a few of these XC paths have been tested in conjunction with a BOC and a FeI4B chip, but eventually all of them need to be tested.

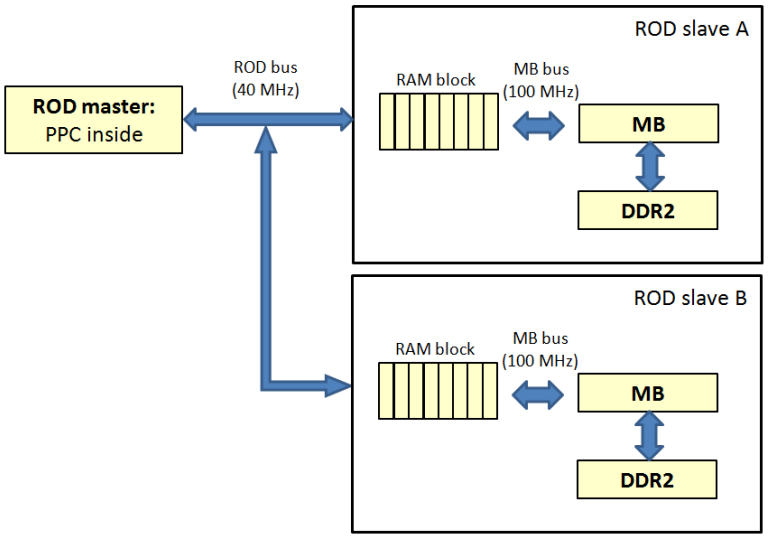


Figure 3.7: Programming the MicroBlazes from Virtex via ROD bus.

3.4.8 USB test

The USB line is tested with the Kermit program receiving the information of one of the embedded processors (PCC or MB) during the execution of a program.

3.4.9 JTAG

The ROD master FPGA can be accessed via JTAG from the IBL ROD front panel in a chain with 8 devices using the Xilinx USB JTAG programmer(Figure 2.5).

The order of JTAG chain devices is as follows:

- PROM1 S6A.
- PROM2 S6A.
- S6A.
- PROM1 S6B.
- PROM2 S6B.

- S6B.
- PROM V5.
- V5.

The JTAG port is also available via VME: the ROD master firmware can be loaded via VME using JAM player (and a STAPL file) in about 80 seconds. After switching-on the board, the ROD master gets automatically configured by reading the content of the PROM in a master-serial fashion. Also the PROM can be configured both via the JTAG programmer and via VME: in the former case the operation requires 3 minutes, in the latter about 15 minutes. An additional possibility is to write the flash via HPI port, when Virtex get programmed with a bit file containing a boot loader it loads the software directly from the flash device.

3.4.10 FLASH

A FLASH chip from Atmel (AT45DB642D, 64-megabit, Rapid Serial Interface: 66 MHz Maximum Clock Frequency, used with 1056 Bytes per page and 8192 pages) is connected to the ROD master via SPI. An EDK SPI interface with 8 bit SPI transfer and SPI/PLB clock ratio 1/8 (SPI clock = 15.625 MHz) has been implemented. A program ProgramVirtexFlash running on the SBC writes the FLASH chip via VME in about 1 minute. The FLASH chip can be written and read via VME by the SBC. After the FLASH is programmed, the PPC boots up by reading the SREC file from the FLASH (this process requires a few seconds).

3.5 ROD Slaves Tests

3.5.1 BOC-ROD Connection Test

Using the program BOC2ROD (from BOClib), a known pattern is sent from BOC to ROD on lines RD[95:0] at 80 MHz (96 bits @ 80 MHz = 7680 Mbits/s = 960

MBytes/s). ROD slaves checks the received pattern against the one previously saved in a memory block. The test lasts for a couple of hours, triggering with Chipscope on the error bit. Tests are performed using the pattern X"CC33" or a binary counter looking for hardware issues. The main goal of the test is to check if the termination resistors placed on ROD revC boards really improved the communication quality (with respect to revB in which the termination resistors were not used). The test shows that by placing the termination resistors on SSTL3 I lines, the quality of data from BOC to ROD improved (see Figures 3.8(a) 3.8(b) 3.9(a) 3.9(b) 3.10(a) 3.10(b)).

The board whose results are found in Figure 3.10(b) needed an X-Ray inspection to identify y and then remove a little excess of solder that touched a ground pin.

3.5.2 ROD-BOC communication test for four S-Link

In order to check the communication on the S-Link lines, an 8B/10B asynchronous transfer check has been implemented on each line. A synchronous data transfer check from ROD to BOC on S-Link lines has not been tested, nor implemented yet.

3.5.3 SSRAM 1 and 2

For each SSRAM has been implemented a dedicated firmware with different patterns in order to find out potential communication failures. A list of used patterns:

- Counter.
- Known pattern with its opposite (0x5555→ 0xAAAA).
- One high bit shifted in all positions (0x0001→ 0x0002→0x0004→0x0008...).

A first version with a single clock running at 100 MHz has been developed and successfully tested. For having the SSRAMs working at 200 MHz a special

Phase (degrees)	Device	Status	Problems
0	SP6A	FAIL	Multiple errors on every bus
	SP6B	FAIL	Multiple errors on every bus
90	SP6A	FAIL	Multiple errors on A bus
	SP6B	FAIL	Multiple errors on B bus
180	SP6A	FAIL	Sometimes read C8 instead of CC on A bus
	SP6B	OK	
270	SP6A	OK	
	SP6B	OK	

(a) Rod rev B number 4

Phase (degrees)	Device	Status	Problems
0	SP6A	FAIL	Multiple errors on every bus
	SP6B	FAIL	Multiple errors on every bus
90	SP6A	FAIL	Multiple errors on A bus
	SP6B	FAIL	Multiple errors on B bus
180	SP6A	FAIL	Sometimes read 08 instead of 0C on B bus
	SP6B	OK	
270	SP6A	OK	
	SP6B	OK	

(b) Rod rev B number 5

Figure 3.8: BOC to RODtest on Rev B boards

Phase (degrees)	Device	Status	Problems
0	SP6A	FAIL	Multiple errors on every bus
	SP6B	FAIL	Multiple errors on every bus
90	SP6A	FAIL	One error in 2 hours of test
	SP6B	OK	
180	SP6A	OK	
	SP6B	OK	
270	SP6A	OK	
	SP6B	OK	

(a) Rod rev C number 1

Phase (degrees)	Device	Status	Problems
0	SP6A	FAIL	Multiple errors on every bus
	SP6B	FAIL	Multiple errors on every bus
90	SP6A	OK	
	SP6B	OK	
180	SP6A	OK	
	SP6B	OK	
270	SP6A	OK	
	SP6B	OK	

(b) Rod rev C number 2

Figure 3.9: BOC to RODtest on Rev C boards

Phase (degrees)	Device	Status	Problems
0	SP6A	FAIL	Multiple errors on every bus
	SP6B	FAIL	Multiple errors on every bus
90	SP6A	OK	
	SP6B	OK	
180	SP6A	OK	
	SP6B	OK	
270	SP6A	OK	
	SP6B	OK	

(a) Rod rev C number 4

Phase (degrees)	Device	Status	Problems
0	SP6A	FAIL	Multiple errors on every bus
	SP6B	FAIL	Multiple errors on every bus
90	SP6A	OK	
	SP6B	FAIL	bit 4 of rx_rod_data_c (pin AG10, net BRD64) stuck at 0
180	SP6A	OK	
	SP6B	FAIL	bit 4 of rx_rod_data_c (pin AG10, net BRD64) stuck at 0
270	SP6A	OK	
	SP6B	FAIL	bit 4 of rx_rod_data_c (pin AG10, net BRD64) stuck at 0

(b) Rod rev C number 5

Figure 3.10: BOC to RODtest on Rev C boards

double-clock firmware version has been released with a particular care in the clock distribution and in the packing of logic elements inside IOBs (Input Ouput Buffers) in the FPGA. Two clocks are needed since overall timing delays are quite close to 5 ns or worse, so some work on phases of the clock is needed to overcome this issue.

In fact the output delay of the FPGA towards SSRAM is the sum of Output Logic Flip Flop (0.74 ns max), Output Buffer Delay (2.43 ns max), PCB Propagation time (0.35 ns typical) and SSRAM Setup Time (1.2 ns minimum) that leads to 4.72 ns at best.

We have the following estimated timings: Input from SSRAM up to 5.75 ns coming from SRAM Clock-to-output (2.6 ns max), PCB propagation time (0.35 ns typ), SP6 input buffer delay from pad (1.07 ns max) and SP6 ILOGIC2 setup (1.73 ns min). These values are calculated at the max propagation time in the worst operating conditions using FPGA XC6SLX150-2FGG900 (speed grade = -2). Even a better performing speed grade (-3) would require to use a double clock, even if timing closure would be easier.

The integration of the SSRAMs into the current complete version of the firmware is on-going starting with a 100 MHz frequency and then a study will be performed on how to get closer to the desired value of 200 MHz.

3.5.4 DDR2

The test is done running a small program on the MicroBlaze, which continuously accesses the DDR2 SODIMM first writing known patterns and then reading them back. Once a mismatch occurs, the program waits for input to allow debug through SDK.

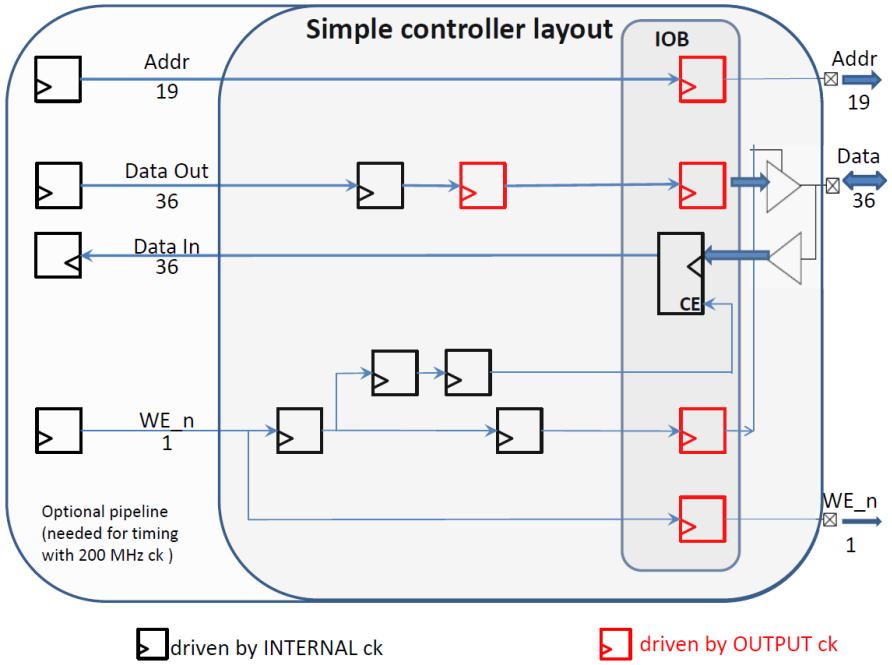


Figure 3.11: Clock distribution schematic, on the left there is the FPGA and on the right the RAM.

3.5.5 Ethernet

Only correct functioning has been tested since writing a program that works at full speed is quite complicated. The procedure followed this steps

- Echo server implemented with LWIP library on each MicroBlaze.
- Speed test increasing packet dimensions.

The process was repeated with each one of the two Ethernet connected to the Spartan 6, and the throughput reached was 140Mb/s with no errors in two hours. Also the rate reduced to 120Mb/s when the two interfaces was simultaneously connected to the switch, also in this case no error was found.

Also a firmware without embedded processor has been developed and run. It can reply to ARP requests and send out UDP packages with a software programmable number of data. The communication protocol in this case is custom made, and it needs constant feedbacks from the PC. As a feedback is accepted the reply at n-2 packet to speed up the process not having to wait every time for the last reply. In this configuration the throughput has reached 90Mbyte/s.

Current version of ROD's firmware employs a MicroBlaze that takes care of ethernet connection and histogrammer's RAM emptying towards fit server.

3.6 PRM tests

3.6.1 VME

A simple VME slave interface (taken from the Pixel ROD PRM) has been implemented. A stress test has been run for some hours writing and reading back registers with known values at incremental addresses using the vme_rcc_test tool. The VME interface is also tested when configuring the main FPGAs via VME, when using the HPI port for accessing the PPC address space and when writing/reading back registers from the SBC.

3.6.2 VME HPI bridge towards PPC

A bridge is used to access the PPC address space from VME, the HPI bit needs to be set with a dedicated software to enable this feature. Two of the possible applications in which it's useful are:

- programming Virtex 5 flash and boot the software from it;
- reading back internal ppc's registers, say, to read back ppc system monitor temperature and voltages via VME.

The latter one has been implemented, as all the software that needs VME bus, to run on the SBC (Single Board Computer) accessed via secure shell from a desktop. This program will monitor temperature runtime.

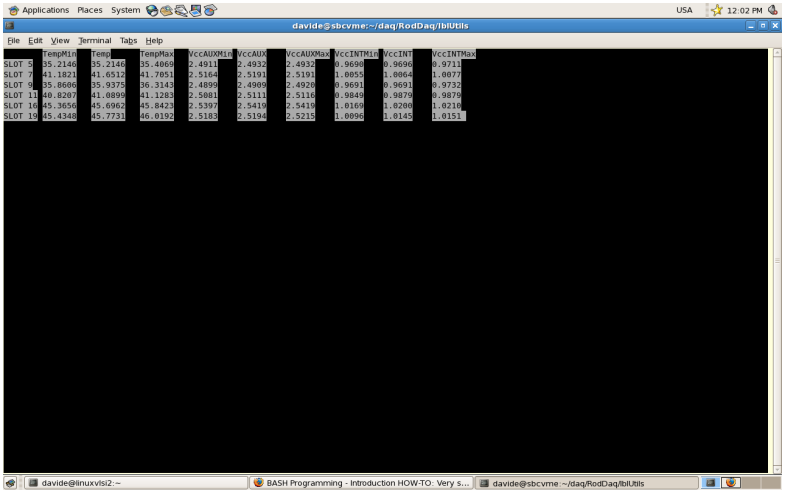


Figure 3.12: A screenshot of the temperature reading program.

3.6.3 JTAG-PROM

The PRM can be configured via JTAG from the front panel connector. JTAG chain only shows an XCF16P PROM and the Spartan6 device.

After the switch-on, PRM gets automatically programmed by reading its PROM via a master serial access. Both PROM and FPGA are not programmable via VME.

Chapter 4

Calibration Runs

Proceeding toward the full featured run, that won't be reached until full detector is mounted in the cavern, an important part is the one dedicated to the digital scans of a real FEI4 version B bonded on a SCC.

These chips are a challenge to configure the right way and until a full comprehension is reached unexpected behaviours are sometimes expected. To add more variables to the problem there were four chips out of six that behaved exceptionally bad and later it has been confirmed that they were broken from the start.

4.1 Issuing calibration runs

This sort of operations, that resemble a lot the data taking process, produces, although fake, realistic data far beyond the ones that comes out of any simulator and with a lot less effort.

To set up all the registers, a software has been written and run on a machine connected via ethernet to the PPC. This configuration will go down the XC bus of above described, and will reach the front end via BOC card.

First of all a "default" configuration, that is alike the definitive one, is sent and then the appropriate modifications are done in order to prepare the entire system for a calibration pulse that will act as a trigger.

In particular the runs done in Bologna were Digital Injection, but there are other types of tests that stress bigger parts of the chip. For example there's an Analog Injection, and each of these two procedures inject a charge into a different part of the circuit in Figure 1.17.

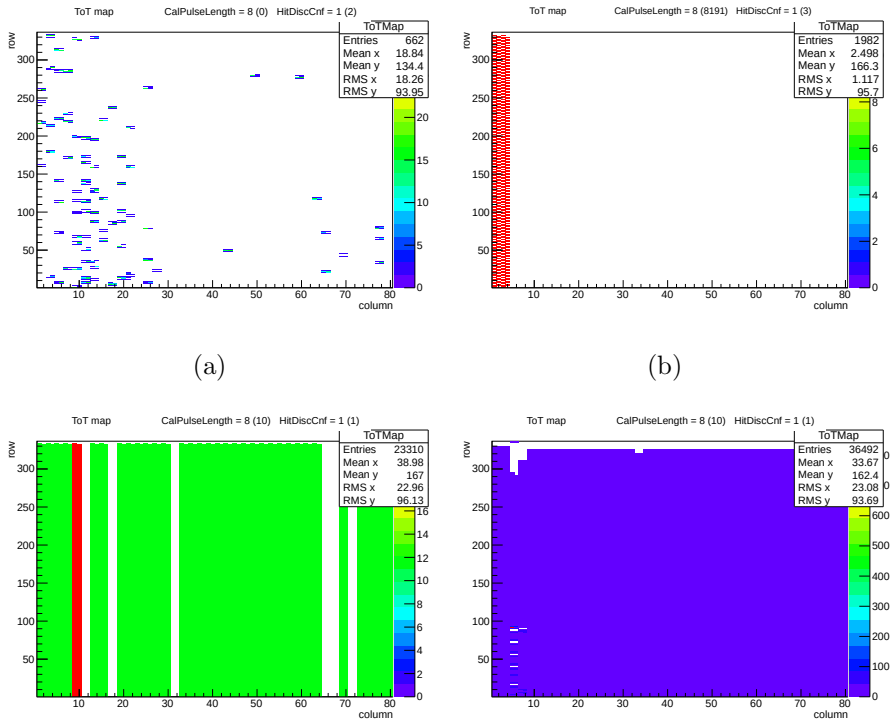
The Digital one injects a known charge on the DigHit pin (lower right of the picture) while Analog one stimulates Vcal pad (lower left of the picture).

It takes some time to inject a charge into all the pixels because it needs to be done one by one on all double columns and this task has no shortcuts, then informations need to be read from the RAM. In Geneva a great leap forward has been done since now a bunch of addresses can be read instead of one at a time.

However the results are often not well predictable in a setup not perfectly under control, since a 160 MHz line, even if differential, can lead to strange noises as well as a not shielded power cable. If a command is lost or misinterpreted the whole process can lead to results as in Figure 4.1(a) or 4.1(c). Along with the mentioned figure we see other runs that produced a good outcome even in the case of Figure 4.1(d) that shows some bad pixels, but those can be truly dead pixels.

Another way to get a similar map is to read the data via RodBus from the epc interface the INMEM FIFO, this process reads exactly the input data from BOC so it's useful to debug data chain problems. In fact the last problem was found like this and here's an image that summarizes the point (Figure 4.2).

The problem was trivial and showed up only when a multiple chip digital scan was run, now it's all better and a new problem, as always, popped up within the histogrammer memory map.



(a) (b)

(c) (d)

Figure 4.1: Various calibration runs done in Bologna. These are only a small set and the data are all read via PPC interface.

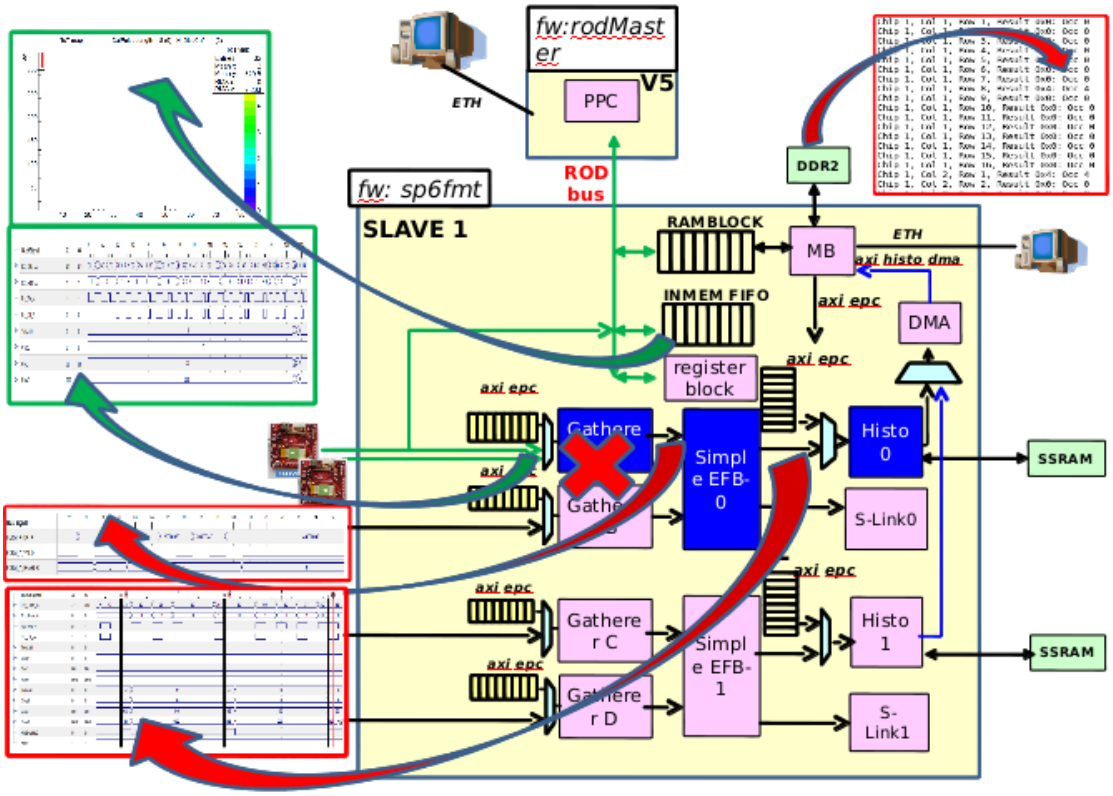


Figure 4.2: Last meeting data problem solved.

Conclusions and future developments

Eventually this work has helped the constructions of a set of VME 9U cards that will be part of the new data acquisition system of the ATLAS IBL experiment. The twenty boards will be delivered to CERN as soon as they will be tested as this is the deliverable of the Bologna commitment for the IBL experiment. The boards are under test now in the Bologna electronic laboratory of the INFN and Physics Department, then these boards will be tested again at CERN within a more complete system. In this way the entire data acquisition system will be able to prove the overall performance once connected to the real pixel detector. Moreover, the is particularly relevant for the National Institute of Nuclear Physics ("Istitiuto Nazionale di Fisica Nulceare, Sezione di Bologna") because it is now the unique involvement of the Bologna institute to a CERN pixel experiment. The experiment will continue in the future, beyond my thesis, with the development of the detector so that my work will be continued by the ATLAS collaboration. Until now, the Bologna commitment has been completed and the group is going to agree to continue the development of the system also for the other layers of pixels, starting from the Layer 2. In fact, Layer 2 is the first layer that is expected to fail upon a significant increment of luminosity. Hence, it is the planned updating the data acquisition system of the ATLAS pixel detector, very soon, also for the Layer 2, even if still maintaining the current physical detector.

For all described above it is crucial to save as much documentation as possible to make sure that other people will be able to understand and upgrade my work. This is why all the developed material is continuously updated and saved in a CERN repository that is continuously upgraded.

Appendix A

Specific developed features

As the work goes by some interesting new features were developed from scratch, some only to give more control over the ROD status, one of these is a system monitor, wrote in C++ with ncurses libraries, which can read some particular registers inside the PPC where can be found a treasure of infos about Virtex itself, in the figure below some RODs are being monitored to demonstrate that all RODs in the crate can be read at once. The code needs two things to work, the first one is that in ISE® the system monitor peripheral shall be implemented and the second is that the hpi bit shall be set.

Also to program all RODs at once for the tests a bash script that uses all the features to program the boards without JTAG programmer it has been written.

```
#!/bin/sh
for i
do
./jp_25 -X"$i" -v -aRUN_XILINX_PROC flashloader_rodmaster.stapl
done
for j
do
./ProgramVirtexFlash "$j" peripheral_tests_0.srec
```

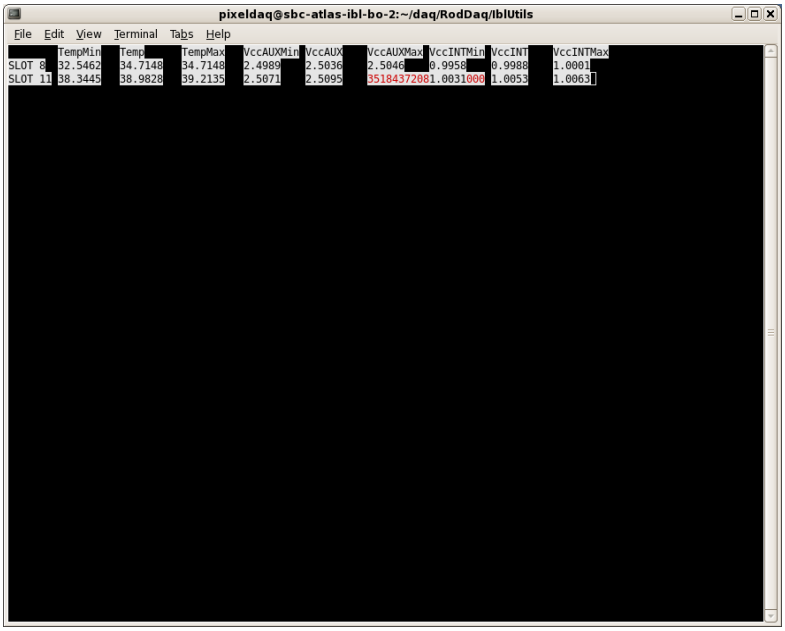


Figure A.1: A screenshot of SystemMonitor at work on two RODs, still some issues...

```
done
for l
do
./jp_25 -X"$l" -v -aRUN_XILINX_PROC buscheck.stapl
done
```

Fairly simple, launch it like this `.program <slot numbers>` and it begins looping over the slots and programming them obviously if an error is found it crashes.

Thanks

There are too many persons to thank for this result, and I mean my graduation along with personal achievements during all my academic career so I'll begin thanking my supervisors Davide, Enzo and Alessandro along with Gabriele, Mauro, Filippo and Riccardo.

CERN people especially the PixelLab: Marcello, Bing, Maria Elena, Yosuke, Laura, Karolos, Lynn, Timon...

Now starting another series of thanks to the people who studied with me, no exceptions, and the ones that brought coffee-breaks every time they showed up. Alessandra, Cristiano, Marco, Giulia, Giovanna, Federico, Laura, Valentina, Valeria, Enrico, Enrico, Luca, Mario, Stefano, Giulia, Marco, Mattia, Laura, Valentina, Francesca, Claudia, Lorenzo, Flavio, Andrea, Kristina, Emanuela and many others that i forgot to add.

Non academic friends that spared with me their time Sauro, Andrea, Gianluigi, Anna, Agnese, Arianna, Matteo, Dario... the list would be too long to write it all but would be very rude to leave out the one who taught me curiosity, Giorgio, one of my professors during High Schools.

Bibliography

[1] ATLAS Collaboration. Atlas detector and physics performance. 1999.

[2] ATLAS IBL Community. Atlas insertable b-layer tecnical design report. 2010.

[3] G.Balbi M.Bindi S.P.Chen D.Falchieri T.Flick A.Gabrielli S.Hauck S.C.Hsu A.Kugel L.Lama P.Morettini R.Travaglini M.Wensing. The read-out driver (rod) card for the atlas experiment: commissioning for the ibl detector and upgrade studies for the pixel layers 1 and 2. *Journal Of Instrumentation*, Yet to be published.

[4] FE-I4 Collaboration. The fe-i4b integrated circuit guide. 2012.

[5] Douglas P. Ferguson Andreas Korn Trevor Vickey John Joseph, Richard Jared. Atlas silicon readout driver (rod) user manual. 2008.