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Analysis of High-Level Injection in SCR-LDMOS for Enhanced ESD Protection of Smart Power Technology

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Abstract

The protection of Integrated Circuits (ICs) against Electrostatic Discharges (ESD) is becoming increasingly important due to the progressive reduction of robustness of these circuits against high current surges from ESD events, as a consequence of technology scaling.
A commonly implemented self-protected device is the Silicon Controlled Rectifier - Lateral Double-Diffused Metal-Oxide-Semiconductor (SCR-LDMOS), which combines the output driver capabilities of the LDMOS with the ESD robustness of the SCR. The introduction of Smart Power Technology in different application domains, such as automotive, poses an increase in the challenge of ESD protection, due to the higher power supply voltages characterizing this technology. Indeed, a high holding voltage in the protection devices is crucial to mitigate the risk of latch-up. In this thesis, different SCR-LDMOS structures based on Texas Instruments LBC9 technology have been simulated using Synopsys Sentaurus TCAD. In particular, the effect of high-level injection on the holding voltage and failure current has been investigated. A layout-only optimization for increased holding voltage has been proposed for effective protection of Smart Power Technology.

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Introduction

Over the past few decades, there has been a notable rise in the pervasiveness of electronic devices into our everyday lives. The necessity to integrate an increasing number of devices into confined spaces has obliged the electronics industry to develop progressively more compact devices each year. The combination of miniaturization and technological advancement has enabled the integration of a previously unfeasible level of complexity within integrated circuits (ICs).

Nevertheless, a consequence of miniaturization is the susceptibility of these devices to electrical phenomena that may ultimately result in the destruction of the device. The occurrence of high electric fields, which may be the result of phenomena such as electrostatic discharge (ESD), can result in the thermal failure of the device or other irreversible damage, such as dielectric breakdown. Even events that do not directly result in device failure can lead to the onset of permanent damage, which may subsequently affect device performance. Examples of such damage include increased leakage currents.

An ESD event occurs when two objects having different static charges come into contact, creating a high electric field and allowing a high current flow, potentially causing a voltage spike across the device. This can happen through contact between an external IC pin and a charged machine part or through human handling.

It is therefore of the utmost importance to develop ESD protection devices that can effectively protect the sensitive part of the circuit while occupying minimal space. Area occupation and ESD protection effectiveness are usually conflicting characteristics since a reduction in the size of the device typically results in a faster thermal failure or a lower breakdown voltage. Given the increasingly rapid development of technology, it is imperative to achieve a comprehensive understanding of the operational principles of protection devices. This will ensure the development of reliable devices that can be readily adapted and scaled in accordance with the advancements in technology.

The first chapter gives deeper insights on the cause of ESD events, and what specifically in technology scaling has affected the devices ESD robustness. The system level and TLP testing methods are presented, giving particular importance to the choice of the failure criteria in TLP testing.

The second chapter briefly introduces the general concepts of IC-level protection from ESD events, illustrating the most common architectures. Subsequently, the most significant semiconductor devices implemented in the protection networks are presented, with a detailed explanation of the underlying physics of their operation and its relationship with ESD protection. This includes one of the most promising candidates among self-protected devices, the SCR-LDMOS, which is the focus of the experimental work carried out in this thesis.

In the third chapter, different SCR-LDMOS structures have been simulated through 2D Technology Computer-Aided Design (TCAD) simulations to gain a deeper understanding of the principal parameters that affect the low holding voltage of these devices. Ultimately, a device structure optimization has been proposed for increased holding voltage.
Achieving a high holding voltage value is becoming an increasingly crucial prerequisite for the advancement of Smart Power Technology. The latter enables the integration of complex logic circuits with high-power devices that operate at high power supply voltages. It is therefore essential to have self-protected devices with holding voltages higher than the supply voltages in order to prevent the risk of latch-up.

In the fourth chapter, a preliminary study on the 3D effects using 3D TCAD simulations has been carried out. A further structure modification has been proposed to address the power-scalability problem of SCR-LDMOS and its effect on the holding voltage has been studied.

1. The ESD Problem

Electrostatic discharge (ESD) is a significant problem in today's microelectronics industry. The generation of ESD events is attributed to static electricity, often generated by a tribocharging mechanism. Contact of a charged object with a grounded IC pin can lead to a rapid high voltage and high current discharge through it, eventually leading to the damage or failure of the integrated circuit itself. This poses a significant risk to the reliability of the device. Even if the event does not lead to the complete failure of the device, it could result in performance degradation or latent damage that could manifest itself later during the normal system operation.

1.1. Technology scaling and ESD robustness

Modern technology nodes are increasingly susceptible to this kind of events due to the progressive scaling. Particularly, the main reasons being the reduction of junctions depth and oxide thickness.

It is well known how transistor scaling has many beneficial effects in both power consumption and performance. Smaller devices clearly enable higher switching frequencies due to the reduction of the parasitic capacitance. Historically, the voltage has been scaled accordingly to maintain a constant field through the device channel to achieve constant power density per area, following Dennard's scaling.[1] This allowed a reduction of the dissipated power P_{tot}:

$$P_{tot} = P_{dyn} + P_{stat} = \alpha C_L f V_{DD}^2 + I_{leak} V_{DD} \tag{1}$$

The constant field scaling reached its limits in the early 2000s, due to the originally unconsidered parasitic effects gaining an increasingly important role in smaller devices. Several paradigms, involving both architecture-level and device-level optimization, are currently being employed to continue to pursue miniaturization.

The end of Dennard's scaling has been reached due to the short channel effects (SCE) affecting very small devices. As the channel length decreases, SCE start to negatively affect the device and decrease the benefits of scaling.

One example of a relevant short channel effect is the threshold voltage roll-off. As the physical length of the channel is reduced, the depletion regions of the drain and source area move closer to each other influencing the channel. This causes a reduction of the gate control over the channel formation and thus a reduction of the threshold voltage. This is detrimental as it leads to an increase of the leakage current and thus an increased power consumption.

Two are the possible solution usually adopted to address this problem. First, an increase of the doping concentration helps by reducing the depletion region width hence postponing the prob-

[1] Robert H Dennard et al. "Design of ion-implanted MOSFET's with very small physical dimensions". In: *IEEE Journal of solid-state circuits* 9.5 (1974), pp. 256–268.

lem. Similarly, a reduction of the junction depth can be adopted.

These solutions, although helping V_{th} roll-off, severely affect the ESD robustness of the device. As it will be further clarified in Sect. 2.3.2, the reduction of the depletion region width causes a reduction of the junction breakdown voltage. As ESD events are related to voltage spikes across the device terminals, a reduction of the breakdown voltage (BV) is obviously detrimental.

Altogether technology scaling, an increase of the gate capacitance is necessary in order to obtain a high drive current with a lower gate voltage. Indeed, as V_{GS} is scaled to reduce power consumption, and as I_{ON} is proportional to both C_{ox} and V_{GS}, an equal increase of C_{ox} to maintain an acceptable I_{ON} is necessary as well. Therefore gate oxide scaling is usually employed in device scaling.
Needless to say that thinner oxides experience a higher electric field for the same applied voltage, thereby leading to a lower dielectric breakdown voltage.
Silicon oxide (SiO2) has now been replaced in the gate stack by high-k materials that allow for greater gate capacitance with the added advantages of an increased thickness. In fact, a thicker oxide allows a reduction of the tunneling leakage current through the gate by increasing the tunneling distance. Nevertheless, it has been shown experimentally that high-k materials have comparably lower critical electric field values[2] thus not solving the issue.

Damage of the oxide layer due to non-destructive ESD pulses are equally important, as it leads to a loss of performance. This can be due to charge trapping and defect creation in the oxide, resulting in a detrimental effect on both performance, such as threshold voltage modification or incremented leakage current, and deteriorated reliability as well.[3] Furthermore, it has been shown that thicker oxides (>2.5nm) are more affected by charge trapping, since carrier detrapping by direct tunneling positively affects thinner oxides.[4]

Due to its intrinsic limits, the planar MOSFET is no longer used in digital ICs in which aggressive integration and miniaturization is needed. Novel devices, such as the FinFET, are now the industry standard in very large scale integration circuits. These devices rely on a three dimensional structure to enable a better electrostatic control over the channel by surrounding the latter on three sides rather than just one side as in planar bulk MOSFETs.
However, the increase in performance comes at the cost of a further deterioration of ESD robustness. The reduction of silicon volume is trivially related to a reduction of the failure current due to a degradation of power dissipation, furthermore a pronounced localized heating related

[2] J.W. McPherson et al. "Trends in the ultimate breakdown strength of high dielectric-constant materials". In: *IEEE Transactions on Electron Devices* 50.8 (2003), pp. 1771–1778. DOI: 10.1109/TED.2003.815141.

[3] Tibor Grasser. "Stochastic charge trapping in oxides: From random telegraph noise to bias temperature instabilities". In: *Microelectronics Reliability* 52.1 (2012), pp. 39–70.

[4] Adrien Ille et al. "Reliability aspects of gate oxide under ESD pulse stress". In: *2007 29th Electrical Overstress/Electrostatic Discharge Symposium (EOS/ESD)*. IEEE. 2007, 6A–1.

to current crowding contributes to the problem as well.[5]

1.2. ESD causes

The triboelectric effect, as it can generate static electricity, is a major cause of ESD events. Electric charges can be transferred from one object to another when they touch and if no redistribution of the charges happens, this gives rise to static electricity. This effect is due to the difference of electron affinity between the two materials: the material with higher electron affinity attracts an electron from the material with lower electron affinity, leading to a separation of charges and thus a potential difference.
Although electron transfer is a common simplified explanation of the triboelectric effect, the real cause is still debated and different approaches have been proposed, such as ion transfer[6] and material transfer[7] depending on the materials that come into contact.

Electrostatic induction is another phenomena which might cause static electricity. As a charged object is placed near a metallic one, the electrons of the metallic object are either attracted or repulsed from the charged one, creating once again a charge separation.

ESD affects semiconductor devices both during manufacturing processes and after they are placed on the market. During wafer fabrication, due to the abundant use of synthetic materials in tools and containers, charge generation during fabrication processes is a common problem.[8] Beside the obvious zap risk, wafer being carried in charged insulating containers significantly raises the risk to attract airborne particles, which could stick to the wafer surface altering the sensible fabrication processes.[9] This can lead to an expensive reduction of the fabrication yield.

The risks don't stop once the device leaves the manufacturing facilities. The assembly processes and the handling itself of the device still poses a significant risk of ESD events. It is common to see electronic components and circuits stored in anti-static bags. These are usually made from anti-static polyethylene terephthalate plastic which, having a higher conductivity per area, helps in redistributing the charges through the material in order to avoid charge accumulation during handling or transportation.

[5] Dimitri Linten et al. "ESD in FinFET technologies: Past learning and emerging challenges". In: *2013 IEEE International Reliability Physics Symposium (IRPS)*. IEEE. 2013, 2B–5.

[6] Meurig W Williams. "Triboelectric charging of insulators—evidence for electrons versus ions". In: *ieee transactions on industry applications* 47.3 (2011), pp. 1093–1099.

[7] HT Baytekin et al. "The mosaic of surface charge in contact electrification". In: *Science* 333.6040 (2011), pp. 308–312.

[8] Sang U Kim. "ESD induced gate oxide damage during wafer fabrication process". In: *Journal of electrostatics* 31.2-3 (1993), pp. 323–337.

[9] Niels Jonassen. *Electrostatics*. Springer Science & Business Media, 2013.

Classification (HBM)	Voltage Range [V]
0Z	<50
0A	50 to 125
0B	125 to 250
1A	250 to 500
1B	500 to 1000
1C	1000 to 2000
2	2000 to 4000
3A	4000 to 8000
3B	>8000

Classification (CDM)	Voltage Range [V]
C0A	<125
C0B	125 to 250
C1	250 to 500
C2A	500 to 750
C2B	750 to 1000
C3	>1000

Table 1.1: HBM ESD Component Classification Levels from ANSI/ESDA/JEDEC JS-001 (left) and CDM ESD Component Classification Levels from ANSI/ESDA/JEDEC JS-002 (right).

1.3. System level testing methods

Due to the highly aleatory nature of these events, it is necessary to model their effect on devices so as to obtain repeatable results suitable for standard testing. It is essential to find an equivalent circuit for different ESD events which can be conveniently used for testing. Two models, briefly discussed in the next sections, are usually adopted in industry following the IEC 61000-4-2 standard. Tab. 1.1 shows the ESD component classification leves for the two models.

1.3.1. Human Body Model

The human body could become electrically charged, as explained, by triboelectric effect. A contact between the charged human body and a grounded object can lead to an ESD event. The ANSI/ESDA/JEDEC JS-001 human body model (HBM) standard characterizes this situation.

In order to do so, an average human body to ground capacity and series resistance is considered. The human body charging is modeled as the charging of an equivalent capacitance through a high value resistor. As the capacitor gets fully charged, a switch connects it to the device under test (DUT) through the equivalent series resistance. A high current discharge flows through the DUT. The equivalent circuit for testing is shown in Fig. 1.1.

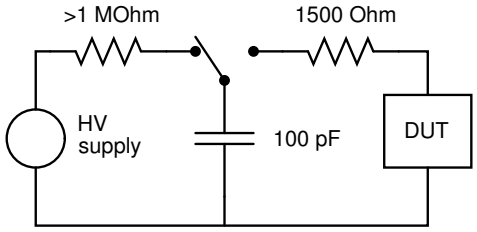

Figure 1.1: Human Body Model equivalent circuit.

1.3.2. Charged Device Model

Another mechanism by which an ESD event can occur, is if the device itself gets electrostatically charged, by triboelectric effect or electrostatic induction, and comes into contact with a grounded metal object. ANSI/ESDA/JEDEC JS-002 charged device model (CDM) standard characterizes the method to test this condition. The equivalent circuit is depicted in Fig. 1.2. The DUT gets charged through a series resistor by a high voltage generator, and a discharge to ground occurs.

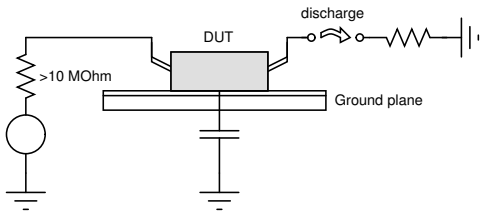

Figure 1.2: Charged Device Model equivalent circuit.

Compared to HBM, the current discharge resulting from CDM has a faster rise time, shorter duration and higher peak value, due to the low series resistance given by the contact of two conductors.
Waveforms correlated to CDM discharges usually present a typical oscillatory behavior. The typical waveforms of HBM and CDM are represented in Fig. 1.3.

A third standard, called Machine Model (MM), usually can be found in literature. Nevertheless, all major standard bodies don't recommend it anymore as a suitable testing method (e.g. JEDEC JESD47) due to the higher sensitivity to parasitic effects in the tester circuitry and redundancy with respect to the HBM and CDM tests.[10]

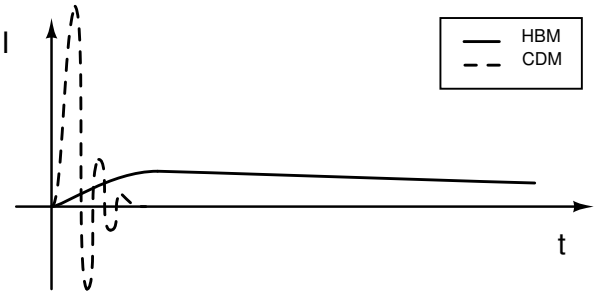

Figure 1.3: HBM (solid line) and CDM (dashed line) typical waveforms.

[10]Charvaka Duvvury et al. "Discontinuing use of the machine model for device ESD qualification". In: *Compliance Magazine* 7 (2012), pp. 56–63.

1.4. TLP testing method

While the above methods are suitable to emulate an ESD event affecting a system and usually report a simple pass/fail result, a different testing method must be adopted to characterize individual protection devices in order to optimize their design.

Transmission Line Pulse (TLP) as a characterization technique for ESD devices was firstly proposed in 1985 by Maloney[11] and makes it possible to get the I-V characteristic of the tested device. TLP firstly trace back to 1968 as a pulse characterization technique for power devices.[12]

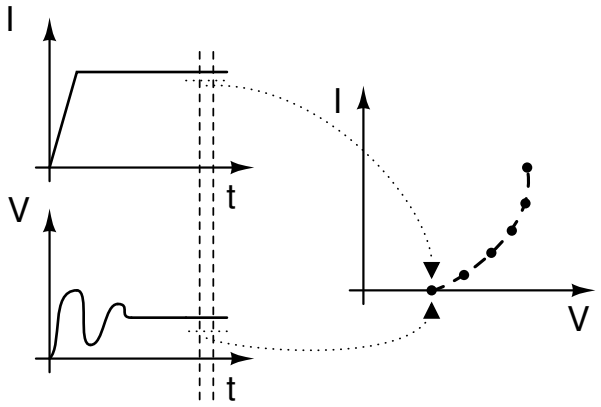

Figure 1.4: Construction of the quasi-static I-V characteristic.

In order to obtain the I-V characteristic of the tested device, pulses with increasing current values are applied until failure. For each pulse, an averaging window at the end of the pulse duration is considered in order to measure the voltage of the DUT and construct a single point in the so-called quasi-static I-V characteristic. This operation is schematically represented in Fig. 1.4.

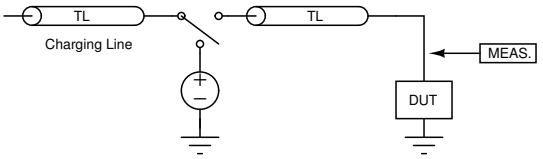

Figure 1.5: Pulse generation.

In Fig. 1.5 a simplified schematic for the pulse generation is shown. The charging line, which is usually a coaxial cable, is precharged to a voltage through a high voltage generator. As the relay connects the charging line to the second transmission line connected to the DUT, a square current pulse with a duration equal two times the propagation length of the cable is applied to the DUT. By changing the length of the charging line, the width of the pulse can be

[11] Timothy J Maloney. "Transmission line pulsing techniques for circuit modeling of ESD phenomena". In: *Proc. EOS/ESD Symp., 1985*. 1985.

[12] DC Wunsch and RR Bell. "Determination of threshold failure levels of semiconductor diodes and transistors due to pulse voltages". In: *IEEE Transactions on Nuclear Science* 15.6 (1968), pp. 244–259.

controlled. A length of approximately 10 meters generates a pulse width of 100 ns which is generally considered as equivalent to a HBM stress.[13]
The simplistic schematic depicted in Fig. 1.5 does not take into consideration the impedance mismatch between the transmission lines and the DUT. The mismatch has the well-known effect of generating reflections which might last several times the pulse duration, leading to a premature failure of the device and hence an incorrect characterization. To solve this problem, Time Domain Reflection TLP (TDR TLP) system is utilized, shown in Fig. 1.6.

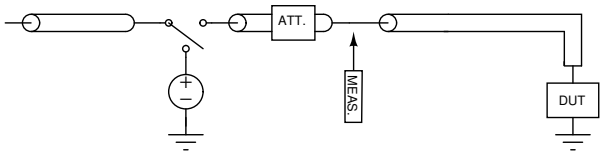

Figure 1.6: Time Domain Reflection TLP.

The system is equivalent to the previous one, but an attenuator is added. As the reflected wave from the DUT interface goes back to the charging line, its value is attenuated and when it is going back to the DUT after being reflected once again at the charging line, another attenuation takes place. In this way, as it reaches again the DUT, the wave has been attenuated twice, thus decreasing its effect on the tested device.

Another utilized standard is the Very Fast TLP (VF-TLP), in which a faster rise time and shorter pulse width, of approximately 10 ns, is used to resemble the stress induced by CDM.[14] Further system modifications, besides the charging line length, are needed to correctly apply the fast pulses of the VF-TLP.

1.4.1. Failure criteria

During an electrical stress, the device temperature increases due to self-heating. Failures often arise when the temperature increase leads to thermal runaway and the subsequent irreversible damage of the device. Furthermore, oxide degradation due to high electric fields adds up to the inflicted damage.

Thermal runaway is the phenomenon whereby an increase of the temperature leads to an increase of the current, which in turn increases the temperature again, causing a chain reaction until the destruction of the device. This can be due to devices with a negative temperature coefficient.

[13] Ajith Amerasekera and Charvaka Duvvury. "The impact of technology scaling on ESD robustness and protection circuit design". In: *IEEE Transactions on components, packaging, and manufacturing technology: Part A* 18.2 (1995), pp. 314–320.

[14] Horst Gieser and Markus Haunschild. "Very fast transmission line pulsing of integrated structures and the charged device model". In: *IEEE Transactions on Components, Packaging, and Manufacturing Technology: Part C* 21.4 (1998), pp. 278–285.

Experimentally, the failure point of the device is determined by measuring the device leakage current after each increase of the current pulse until it is higher than a certain threshold value. Nevertheless, this technique can't be reproduced by TCAD simulations due to difficulty to model defect creation and thus a different approach must be taken.

The simulation tool, given the correct thermal boundaries, is able to solve the heat diffusion equation altogether the carrier dynamics. This permits to use the maximum lattice temperature of the device as the parameter that needs to be monitored to predict the correct failure point. To evaluate the failure point of a device, it is therefore necessary to find the current value, usually called in literature I_{T2}, at which the maximum temperature of the device exceeds a determined point. It is common to assume that device failure arises when the maximum temperature reaches the melting point of silicon, $\sim$ 1700K, nevertheless experimental work has shown that a much lower failure temperature must be considered for ESD-induced thermal failure.[15] In this work, coherently to previous studies,[16] a temperature of 1200K is considered as the onset of thermal runaway.

It is worth noting that in literature another failure criteria is used as well. As it has been proposed by different authors[17],[18] the point at which a second breakdown occurs, i.e. where the device experience a second major voltage drop, is considered as the failure point.

[15] Meng Miao et al. "A new method to estimate failure temperatures of semiconductor devices under electrostatic discharge stresses". In: *IEEE Electron Device Letters* 37.11 (2016), pp. 1477–1480.

[16] Laura Zunarelli et al. "TCAD study of the Holding-Voltage Modulation in Irradiated SCR-LDMOS for HV ESD Protection". In: *2023 IEEE International Reliability Physics Symposium (IRPS)*. IEEE. 2023, pp. 1–6.

[17] Kai Esmark. "Device simulation of ESD protection elements". PhD thesis. ETH Zurich, 2001.

[18] Ajith Amerasekera and Jerold A Seitchik. "Electrothermal behavior of deep submicron nMOS transistors under high current snapback (ESD/EOS) conditions". In: *Proceedings of 1994 IEEE International Electron Devices Meeting*. IEEE. 1994, pp. 455–458.

2. Protection From ESD and Devices

In the following chapter, a brief overview of the most important concepts of ESD protection are given. The most commonly used devices are presented, along with the essential physics concepts required to understand their operation and how they enable protection from ESD events.

2.1. General concepts

The preceding considerations on technology scaling clarify why optimization of transistors for incremented ESD robustness are difficult to implement in digital circuits, since the majority of the necessary modifications go against modern scaling trends. Therefore, protection networks must be implemented at IC level in order to prevent electrostatic discharges from reaching the sensible logic circuitry.
Fig. 2.1 depicts a generic I/O protection network. Two main blocks are recognizable: the primary ESD protection part, here represented by two diodes, and a power clamp. As a positive surge reaches the I/O pad, when the voltage difference exceeds the threshold voltage of the diode, the top diode conducts the overvoltage to the positive power rail. In order to avoid that the surge reaches the core circuit, the power clamp is needed to offer a conductive path to the negative rail for the ESD current. Same operation applies for a negative surge involving the bottom diode.

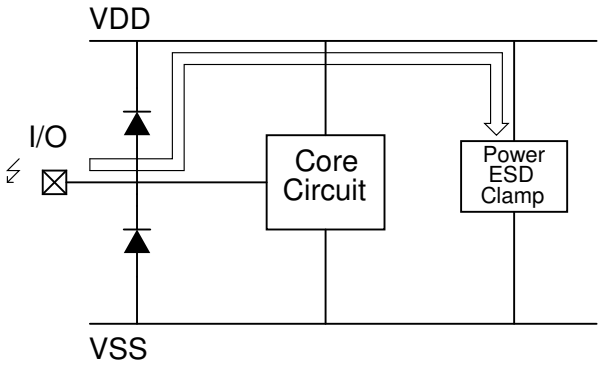

Figure 2.1: Generic I/O ESD protection network.

Different devices can be implemented in place of diodes. It is possible for example to implement one dual directional device instead of two one directional devices.
An example where the use of simple diodes might not work, is when the I/O pad might have to tolerate input voltage values higher than the sum of VDD and the diode threshold voltage. This is a common scenario in, e.g. 3.3V-5V tolerant I/O interfaces. One possible solution is to implement a string of diodes to sum each threshold voltage to avoid the premature triggering of the protection, nevertheless, as further explored in Sect. 2.4, this solution might give raise to parasitic structures that have to be taken into consideration.

Another issue that is worth mentioning is the case in which a multi-domain power supply is present. As modern ICs implement different blocks on the same chip, such as analog, digital and RF, it is often common practice to have different power supply voltages. This must be taken into consideration when designing a ESD protection network. Fig. 2.2 depicts a possible solution.[19]

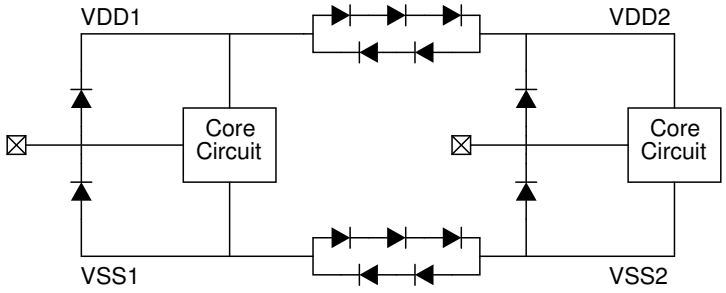

Figure 2.2: Coupling between two power supply domains.

The diode string networks in the center of the proposed scheme are designed in order to separate and block the noise between the two different power supplies, and to conduct the ESD current under an ESD stress. As the ESD voltage at the first power supply overcomes the blocking voltage of the diode string, the current is conducted through the second power supply and can be discharged through the second I/O pin.
Once again the use of diode strings might be problematic due to the already mentioned parasitic structure.
Different architectures implementing a separate VDD ESD Bus have been proposed,[20] based on a dedicated power supply bus connected to each single power supply through bidirectional devices and protected through a power clamp.

2.2. Snapback vs. non-snapback devices

Among the different existing devices for ESD protection, there is a distinction based on their I-V characteristic. Non-snapback devices have the characteristic response of a diode. There exists a triggering voltage, equivalent to the threshold voltage for a diode, after which the voltage is kept approximately constant. The other kind of devices are snapback devices. After reaching the triggering voltage, a positive feedback mechanism leads to negative differential resistance and thus a voltage drop till the reaching of the holding voltage. Typical examples of devices exhibiting this behavior are SCRs, the operation of which will be described in Sect. 2.6. The typical I-V characteristic of snapback and non-snapback devices is illustrated in Fig. 2.3.

[19]Ming-Dou Ker and Hun-Hsien Chang. "Whole-chip ESD protection strategy for CMOS IC's with multiple mixed-voltage power pins". In: *1999 International Symposium on VLSI Technology, Systems, and Applications. Proceedings of Technical Papers.(Cat. No. 99TH8453)*. IEEE. 1999, pp. 298–301.

[20]Ming-Dou Ker, Hun-Hsien Chang, and Tung-Yang Chen. "ESD buses for whole-chip ESD protection". In: *1999 IEEE International Symposium on Circuits and Systems (ISCAS)*. vol. 1. IEEE. 1999, pp. 545–548.

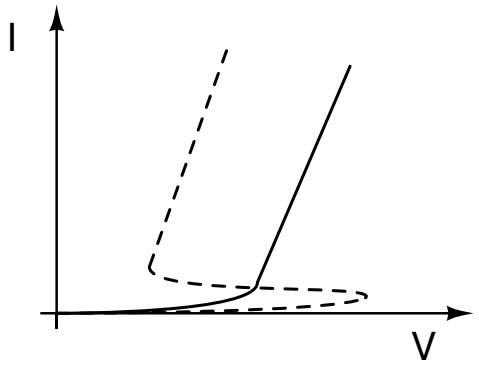

Figure 2.3: Snapback (dashed line) and non-snapback (solid line) typical I-V characteristics.

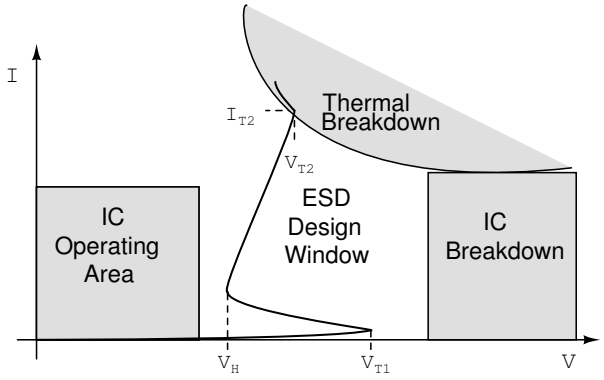

Figure 2.4: ESD design window.

In Fig. 2.4, the generic I-V characteristic of a snapback ESD protection device and its parameters is shown.

The first important parameter of a protection device is the triggering voltage (V_{T1}), representing the point at which the protection comes into operation. It is important to ensure that V_{T1} is lower than the breakdown voltage of the IC to avoid the failure of the device before the start of protection. It is good practice to maintain a good distance from the breakdown limit to assure that no near-breakdown effects such as oxide degradation affects the IC reliability. Needless to say that V_{T1} must be higher than the operation voltage of the IC to prevent the activation of the protection device during the normal functioning of the circuit.

The second parameter, which plays a key role in the proposed experimental work, is the holding voltage (V_H). The holding voltage is the voltage that the protection device maintains during the ESD event after snapback. The effort in research is oriented toward the increase of its value, since, as discussed in the following sections, different protection device architectures suffer from low holding voltages. Although a low V_H might look appealing due to reduced joule heating, it is instead essential to guarantee an holding voltage value higher than the IC operating voltage. Failing to do so leads to the risk of latch-up i.e., when the ESD event ends, the IC operating voltage is high enough to keep sustaining the operation of the protection device thus making it impossible to return to normal operation.

As Smart Power Technology becomes increasingly important due to the rising need of combining power semiconductor devices and highly complex logic circuitry on the same IC, the necessity of designing effective ESD protection networks with high holding voltage to protect power devices is reflected in the visible effort of current literature to optimize protection devices for incremented V_H.

Lastly, as already mentioned, I_{T2} is the failure current of the device. A high value ensures that the protection network can tolerate the ESD event without failing.

2.3. Diode

To better understand how protection work, it is useful to start from the simplest device, the diode. Different implementations in CMOS technology are reported in Fig. 2.5.

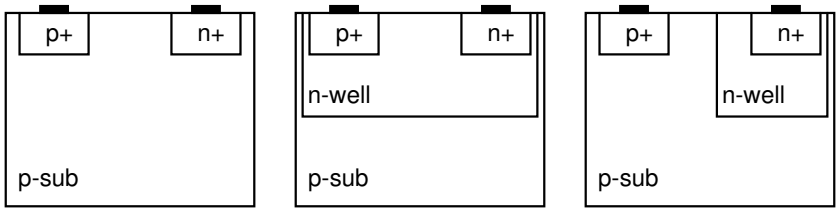

Figure 2.5: Different implementation of diodes in CMOS technology. N^+ diode (left), P^+ diode (center), N-well diode (right).

Considering an abrupt PN junction, the current can be expressed using the well known equation:

$$I_D = I_S \left[\exp\left(\frac{V_D}{V_t} \right) - 1 \right] \tag{2}$$

where $V_t = k_B T / q$ is the thermal voltage and I_S is the saturation current which can be expressed as:

$$I_S = qAn_i^2 \left[\frac{1}{N_D} \sqrt{\frac{D_p}{\tau_p}} + \frac{1}{N_A} \sqrt{\frac{D_n}{\tau_n}} \right] \tag{3}$$

where $D_{p,n}$ are the diffusion coefficients and $\tau_{p,n}$ the hole and electron carrier lifetimes, respectively.

2.3.1. High-level and ultra high-level injection

Since ESD stresses usually cause high currents, it is necessary to take into consideration the high-level injection regime.

High-level injection is defined as when the excess minority carrier density exceeds the doping concentration in the considered region. Since the derivation of Eq. (2) is based on the hypothesis that the excesses minority carriers are negligible with respect to the doping concentration, it is

clear that it is not valid in high-injection conditions and another formulation must be adopted. It can be found that the current density in high-injection has the form:

$$J_D \propto e^{\frac{V_D}{2V_T}} \tag{4}$$

While the potential drop in low-level regime is usually concentrated at the junction, when considering high currents it is necessary to take into account the resistive drop through the entire diode region that further deteriorates the slope of the characteristic.

As the injected current furthermore increases, it may give raise to a different high-level injection regime.

Considering a diode in which a low doped region is interposed between the P^+ and N^+ regions, it can be shown analytically that, for very high currents, the current density of the diode can be expressed as:[21]

$$J_D \propto (V_D - V_{bi})^2 \tag{5}$$

where V_{bi} is the built-in voltage of the diode, which reads for an abrupt junction, as:

$$V_{bi} = \frac{kT}{q} \ln\left(\frac{N_D N_A}{n_i^2}\right) \tag{6}$$

The dependence in Eq. (5) has been attributed to the contribution of the recombination currents at the highly doped ends regions of the device which become no longer negligible for higher injection levels. As the current furthermore increases, another different behavior can be observed which has been called "ultra high-level injection".[22] The latter variation of the behavior has been experimentally verified for P^+-N^--N^+ substrate diodes with a linear dependence on V_D:[23]

$$J_D \propto V_D \tag{7}$$

thus showing a resistor-like behavior.
To model the behavior of the diode through the overall different high-level injection regimes during ESD stresses, the following expression has been proposed:[24]

$$J_D = (\ln V_D)^2 \tag{8}$$

[21] Adolf Herlet. "The forward characteristic of silicon power rectifiers at high current densities". In: *Solid-State Electronics* 11.8 (1968), pp. 717–742.

[22] Ibid.

[23] Gianluca Boselli et al. "Modeling substrate diodes under ultra high ESD injection conditions". In: *2001 Electrical Overstress/Electrostatic Discharge Symposium*. IEEE. 2001, pp. 70–80.

[24] Ibid.

2.3.2. Junction breakdown

In the previous section, the forward bias condition was explored. Here, the details of the reverse bias condition are given in order to better understand the breakdown mechanisms governing the PN junction.

The first illustrated phenomenon causing junction breakdown is thermal instability.
Thermal instability is caused by an intrinsic positive feedback embedded in the PN junction. Considering a high reverse voltage condition, the non-negligible reverse current flowing through a junction gives rise to an increase in temperature. Recalling Eq. (3), it is visible how, since the quantities n_i, $D_{p,n}$ are temperature dependent, I_s is temperature dependent as well. If the ratio D_p/τ_p is proportional to T^γ, where γ is a constant, it can be proved that the temperature dependence of I_S is equal to:[25]

$$I_S \propto T^{(3+\gamma/2)} \exp\left(\frac{-E_g}{k_B T}\right) \tag{9}$$

Hence the positive temperature coefficient leads to an increase of the reverse current with temperature, which in turn will increase the reverse current leading to a positive feedback mechanism till the eventual thermal failure of the junction.
The same mechanism applies to the forward bias condition, in which the increase of the temperature leads to an increase of the forward current and a reduction of the built-in voltage eventually leading once again to thermal failure.

The Zener effect is another phenomenon causing electrical breakdown. Considering a reverse biased junction, a high electric field may cause the creation of a thinner potential barrier at the junction due to the increased band bending. This is particularly accentuated in highly doped junctions due to the reduction of the depletion region width. It is a well known result of quantum mechanics the possibility of a carrier to tunnel through a potential barrier. Approximating the potential barrier as triangular, it is possible to find the band-to-band tunneling current flowing through the junction as:[26]

$$J_t = \frac{\sqrt{2m^*}q^3\mathscr{E}V_R}{4\pi^2\hbar^2\sqrt{E_g}} \exp\left(-\frac{4\sqrt{2m^*}E_g^{3/2}}{3q\mathscr{E}\hbar}\right) \tag{10}$$

where $\hbar$ is the reduced Planck constant, m^* the carrier effective mass, q the carrier charge, E_g the bandgap energy, V_R the reverse voltage, and $\mathscr{E}$ the electric field at the junction. In silicon, an electric field $>10^6$ V/cm can lead to a significant tunneling current.[27] The situation is depicted

[25] Simon M Sze, Yiming Li, and Kwok K Ng. *Physics of semiconductor devices*. John wiley & sons, 2021.
[26] Ibid.
[27] Kauschick Roy, Saibal Mukhopadhyay, and Hamid Mahmoodi-Meimand. "Leakage current mechanisms and leakage reduction techniques in deep-submicrometer CMOS circuits". In: *Proceedings of the IEEE* 91.2 (2003),

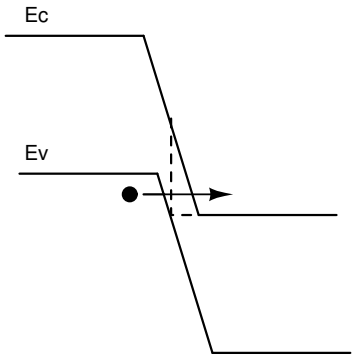

Figure 2.6: Band diagram representation of the Zener effect.

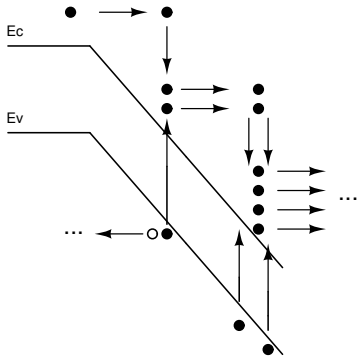

Figure 2.7: Band diagram representation of avalanche multiplication.

in Fig. 2.6.

Another significant phenomenon is avalanche breakdown, which occurs due to avalanche multiplication.
Avalanche multiplication is a carrier generation mechanism that happens when high electric fields are applied to a semiconductor. If the electric field is sufficiently high, a free charge can be accelerated to the point that impact with a charge in the valence band brings promotion of the latter into the conduction band thus generating a new free electron-hole pair, effect known as impact ionization. This mechanism is repeated, thus generating an avalanche effect that leads to rapidly increasing current through the semiconductor. This situation is shown in Fig. 2.7
Let's consider the current $I_n(0)$ entering the space charge region, represented in Fig. 2.8. Due to the high electric field in reverse bias conditions, avalanche multiplication happens and the current at end of the space charge region can be expressed as:

$$I_n = M_n I_n(0) \tag{11}$$

where M_n is defined as the multiplication factor.

pp. 305–327.

It is possible to express the current increment as:

$$I_n(x) = I_n(x)\alpha_n dx + I_p(x)\alpha_p dx \tag{12}$$

where I_p is the hole current and α_n,α_p respectively the ionization coefficients for electrons and holes. The generation rate due to impact ionization can be formulated as:

$$G_{\text{II}} = \alpha_n n v_n + \alpha_p p v_p \tag{13}$$

where n, p are the electron and hole concentration and v_n, v_p the electron and hole drift velocity, respectively.
Eq. (12) can be expressed in the differential form:

$$\frac{dI_n(x)}{dx} = I_n(x)\alpha_n + I_p(x)\alpha_p \tag{14}$$

Considering that $I = I_n(x) + I_p(x)$ and making the assumption that $\alpha_n = \alpha_p = \alpha$, it is possible to integrate Eq. (14) along the depletion region width:

$$I_n(W) - I_n(0) = I \int_0^W \alpha \, dx \tag{15}$$

and recalling the definition of the multiplication factor, it is finally possible obtain the so-called ionization integral:

$$Y_n = 1 - \frac{1}{M_n} = \int_0^W \alpha \, dx \tag{16}$$

The avalanche breakdown condition is given by imposing:

$$\int_0^W \alpha \, dx = 1 \tag{17}$$

which is simply equivalent to $M_n \to \infty$.
The analytical solution of Eq. (17) is not trivial due to the dependence of the ionization rates on the electric field which in turn is not constant through the space region. Miller proposed the following empirical approximation of the ionization integral for a diode:[28]

$$1 - \frac{1}{M} = \left(\frac{V}{V_{BD}}\right)^n \tag{18}$$

where V_{BD} is the breakdown voltage and n a fitting factor.
Let's now consider the depletion region width W_d of an abrupt PN junction:

$$W_d = \sqrt{\frac{2\varepsilon_s}{q} V_R \left(\frac{1}{N_A} + \frac{1}{N_D}\right)} \tag{19}$$

[28] SL Miller. "Ionization rates for holes and electrons in silicon". In: *Physical Review* 105.4 (1957), p. 1246.

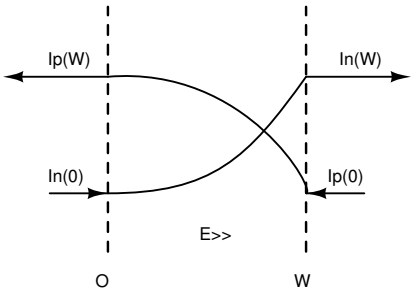

Figure 2.8: Multiplication of the electron and hole currents in the space charge region.

in which V_R is the applied reverse voltage and the built in potential ψ_{bi} has been neglected. Considering now a one-sided abrupt junction, i.e. an asymmetrical junction in which N is the lower doping concentration, the total depletion width can be assumed to be due to the low doping side:

$$W_d \simeq \sqrt{\frac{2\varepsilon_s}{q} V_R \frac{1}{N}} \tag{20}$$

The maximum electric field in the aforementioned one-sided abrupt junction is equal to:

$$\mathscr{E}_m = \frac{qNW_d}{\varepsilon_s} \tag{21}$$

therefore, by combining Eq. (21) and Eq. (20) and assuming V_R to be equal to the breakdown voltage V_{BD}, we finally obtain:

$$V_{BD} = \frac{\varepsilon_s \mathscr{E}_m^2}{2qN} \tag{22}$$

The obtained expression points out an important result: the higher the doping concentration, the lower will be the breakdown voltage.
This explains why in power semiconductor devices, as mentioned in the previous section, lighter doping is preferred due to the higher voltages that needs to be sustained.

In the preceding discussion, no importance was given to the ionization coefficients α_n,α_p, nevertheless their dependencies are equally important to correctly model avalanche multiplication.
In this work, the University of Bologna impact ionization model has been used in the simulations carried out in the next chapter.[29] This model is validated to temperatures up to nearly 800K which is essential for correctly predicting ESD related failures. The latter reads:

$$\alpha(\mathscr{E}, T) = \frac{\mathscr{E}}{a(T) + b(T) \exp\left[\frac{d(T)}{\mathscr{E} + c(T)}\right]} \tag{23}$$

[29] Susanna Reggiani et al. "Experimental extraction of the electron impact-ionization coefficient at large operating temperatures". In: *IEDM Technical Digest. IEEE International Electron Devices Meeting, 2004.* IEEE. 2004, pp. 407–410.

where $\mathscr{E}$ is the electric field, T the lattice temperature and $a(T), b(T), c(T), d(T)$ are temperature dependent fitting parameters.
This model is already implemented in the simulation tool.[30]

Avalanche breakdown is an important phenomenon exploited in both on-chip and component level ESD protection (e.g. TVS diodes). The abrupt current conduction after a voltage threshold is exceeded makes it a good mechanism to exploit in a variety of different devices.

Nevertheless, a delay in the onset of avalanche breakdown and a consequent voltage overshoot has been observed in different works.[31][32] The reason of the delay is attributed to the low number of free carriers present in the depleted region that can initiate the avalanche mechanism. The source of the seed free carriers are SRH recombination, tunneling and emission from traps. As the SRH contribution in BCD technologies is usually not sufficient to initiate avalanche breakdown due to the low concentration of defects, electron tunneling and trap emission are found to be the major contributors.[33]
In highly doped junctions, the width of the depleted region shrinks, leading to a reduction of the probability of avalanche breakdown and therefore a tunneling-dominant breakdown will be present in junctions with low breakdown voltages. For intermediate breakdown voltages, both phenomena will be present, and the presence of tunneling generated carriers will enhance the onset of avalanche multiplication thus not presenting the mentioned delay. For junctions with higher breakdown voltages, due to the absence of tunneling, the scarcity of free carriers will slow down the avalanche breakdown thus reducing the ESD robustness from fast stresses.[34]
As mentioned above, carrier emission from trap states is another mechanism that aids the onset of avalanche multiplication. It has been found that if a bias voltage is applied to the junction prior to the ESD pulse the emptying of deep trap states causes the onset of avalanche breakdown to be once again delayed.[35]

2.4. Diode strings

A diode has usually a threshold voltage of about 0.7 V. This low value might be problematic in 3.3V-5V tolerant I/O interfaces in which a greater voltage than the VDD can be expected and must be tolerated without triggering the protection element. Since a forward biased diode

[30] Synopsys. *Sentaurus Device User Guide*. 2022.

[31] Dimitri Linten et al. "Extreme voltage and current overshoots in HV snapback devices during HBM ESD stress". In: *EOS/ESD 2008-2008 30th Electrical Overstress/Electrostatic Discharge Symposium*. IEEE. 2008, pp. 204–210.

[32] J Willemen et al. "Characterization and modeling of transient device behavior under CDM ESD stress". In: *Journal of electrostatics* 62.2-3 (2004), pp. 133–153.

[33] David Johnsson et al. "Avalanche breakdown delay in ESD protection diodes". In: *IEEE transactions on electron devices* 57.10 (2010), pp. 2470–2476.

[34] Ibid.

[35] David Johnsson et al. "Avalanche breakdown delay in high-voltage pn junctions caused by pre-pulse voltage from IEC 61000-4-2 ESD generators". In: *IEEE Transactions on Device and Materials Reliability* 9.3 (2009), pp. 412–418.

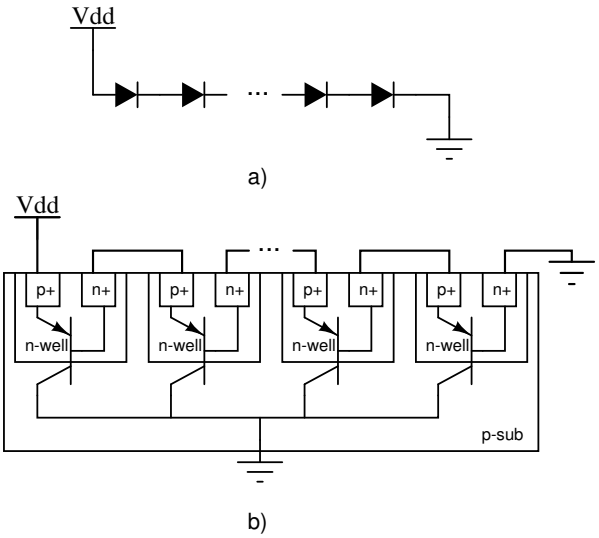

Figure 2.9: (a) Diode string schematic and (b) typical CMOS implementation with parasitic PNP transistors highlighted.

can sustain a higher current with respect to the reverse bias condition, instead of exploiting breakdown mechanisms it is possible to implement a higher triggering voltage using a diode string.[36] In Fig. 2.9 the schematic and typical CMOS implementation is depicted. As it is highlighted in the figure, the implementation of the diode string in CMOS technology leads to the creation of parasitic vertical PNP transistors.
When this solution is implemented as a VDD to VSS ESD clamp, it clearly causes a significant increase of the leakage current, attributed to the embedded multistage Darlington β gain.
Furthermore, the expected linear increment of the triggering voltage with the number of diodes is degraded by the parasitic transistors. It can be found that the expression for it is:[37]

$$V_{\text{trig}} = mV_D - nV_t \cdot \left[\frac{m(m-1)}{2}\right] \cdot \ln(\beta + 1) \tag{24}$$

where V_D is the forward turn on voltage of a single diode, m is the number of diodes, n the ideality factor and β the PNPs gain.
Different architectures using additional MOSFETs have been proposed in order to reduce the leakage current.[38]

[36] Steven H Voldman et al. "Analysis of snubber-clamped diode-string mixed voltage interface ESD protection network for advanced microprocessors". In: *Journal of electrostatics* 38.1-2 (1996), pp. 3–31.

[37] Ming-Dou Ker, Wen-Yu Lo, and Hun-Hsien Chang. *Low-leakage diode string for use in the power-rail ESD clamp circuits*. US Patent 6,671,153. 2003.

[38] Timothy J Maloney and Sanjay Dabral. "Novel clamp circuits for IC power supply protection". In: *IEEE Transactions on Components, Packaging, and Manufacturing Technology: Part C* 19.3 (1996), pp. 150–161.

2.5. GGMOSFET

The Grounded-Gate MOSFET (GGMOSFET) is a common ESD protection device obtained by connecting the drain contact to the protected I/O pad and by tying together both gate and source to ground.

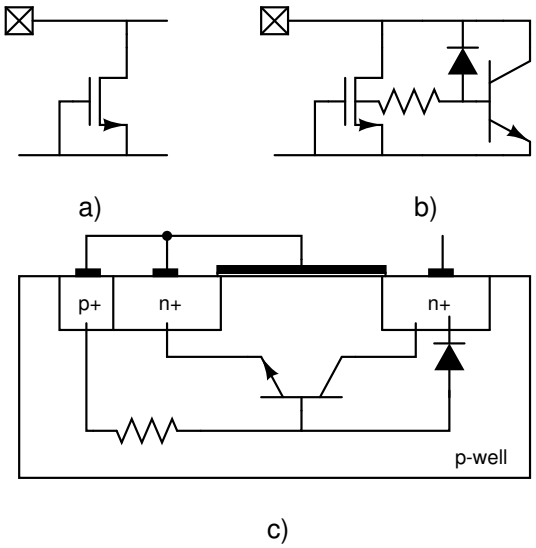

Figure 2.10: (a) GGNMOS symbol, (b) GGNMOS schematic with parasitic structures highlighted and (c) planar CMOS implementation.

Fig. 2.10 shows the implementation of a GGNMOS highlighting the parasitic structures. The N^+ drain contact and the P-well make up a parasitic reverse biased PN junction, while the N^+ drain, P-well and N^+ source a parasitic lateral NPN bipolar transistor.
During normal operation the NMOS is in its off state, thus no current, but the leakage current, flows through its terminals.
During an ESD stress, the drain voltage raises till avalanche breakdown is reached for the N^+ drain P-well junction, as extensively explained in Sect. 2.3.2. The hole current drifts to the P^+ substrate contact. The current originates a voltage drop in the substrate that biases the base-emitter junction of the parasitic NPN BJT. As this voltage drop reaches the threshold voltage of the junction, the transistor turns on activating an additional current path. Since the electric field required to maintain this current flow is lower than the one required to maintain the breakdown condition, a reduction of the voltage at device terminals happens. This originates the snapback behavior, therefore creating a typical snapback I-V characteristic as previously illustrated. The role of the avalanche current is represented in the equivalent circuit of Fig. 2.11.

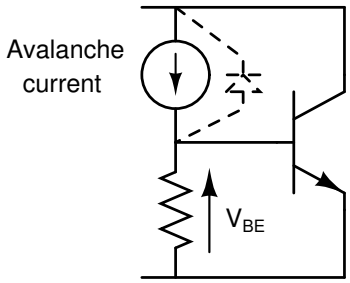

Figure 2.11: Triggering mechanism of the parasitic BJT in the GGNMOS.

The breakdown voltage is trivially correlated to the N^+ drain P-well junction characteristics. The Miller formula can be used to find empirically the avalanche multiplication factor M in MOS operation:[39]

$$M = \frac{1}{1 - [(V_{DB} - V_{Dsat})/BV_{DB}]^n} \tag{25}$$

where V_{DB} is the drain-bulk voltage (collector-base of the parasitic BJT), BV_{DB} the avalanche breakdown voltage of the drain-bulk junction at open source and n an empirical power factor. The holding voltage instead is found to be highly correlated to the current gain of the parasitic transistor:[40]

$$V_h \simeq \frac{BV_{\mathrm{CB0}}}{(k\beta)^{1/n}} \simeq \frac{BV_{\mathrm{CB0}}}{k2^{1/n}} \left(\frac{L_{\mathrm{eff}}}{L_n} \right)^{2/n} \tag{26}$$

where BV_{CB0} is the breakdown voltage of the collector-base junction, L_{eff} the effective channel length, L_n the electron diffusion length in the P-well and k,n empirical constants.

Different implementations from the one depicted in Fig. 2.10(c) can be obviously utilized depending on the IC technology. This can lead to variations of the device behavior.
Different works have reported the presence of a double snapback behavior in HV GGNMOS correlated to Kirk effect leading to a degradation of ESD robustness.[41][42]
Due to the extensive use of FinFET in modern ICs, several investigations on the difference between planar and FinFET GGNMOS have been performed as well. A heavy degradation of I_{T2} is expected due to the significant loss of silicon volume and worse thermal dissipation.[43] Furthermore, a reduction of the breakdown voltage has been observed caused by the higher fin

[39] Ajith Amerasekera et al. "Modeling MOS snapback and parasitic bipolar action for circuit-level ESD and high current simulations". In: *Proceedings of International Reliability Physics Symposium*. IEEE. 1996, pp. 318–326.

[40] Y Fong and C Hu. "High-current snapback characteristics of MOSFETs". In: *IEEE transactions on electron devices* 37.9 (1990), pp. 2101–2103.

[41] Prantik Mahajan et al. "Optimization of GGNMOS Devices for High-Voltage ESD Protection in BCDLite Technology". In: *2020 International EOS/ESD Symposium on Design and System (IEDS)*. IEEE. 2021, pp. 1–6.

[42] Ming-Dou Ker and Kun-Hsien Lin. "Double snapback characteristics in high-voltage nMOSFETs and the impact to on-chip ESD protection design". In: *IEEE Electron Device Letters* 25.9 (2004), pp. 640–642.

[43] Junjun Li et al. "ESD device performance analysis in a 14nm FinFET SOI CMOS technology: Fin-based versus planar-based". In: *Electrical Overstress/Electrostatic Discharge Symposium Proceedings 2014*. IEEE. 2014, pp. 1–6.

resistance and therefore a lower substrate current needed to turn on the parasitic transistor.[44] The optimization of ESD related parameters in FinFET devices is a current research topic.

A variation of the GGNMOS is the Gate-Coupled NMOS (GCNMOS) shown in Fig. 2.12.

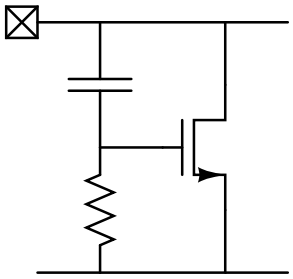

Figure 2.12: Gate-Coupled NMOS.

It has been observed that by applying a small voltage bias to the gate contact, it is possible to lower the first breakdown voltage. The current generated in the channel by the normal MOS operation helps biasing the substrate-source junction therefore reducing the breakdown voltage.[45] However, an excessive gate bias can lead to a reduction of the failure current I_{T2}.[46]

2.6. SCR

Another important component in ESD protection devices is the Silicon Controlled Rectifier (SCR).
It consists of a PNPN junction and it can be implemented in standard CMOS technology as depicted in Fig. 2.13(a). The two parasitic BJT transistors present in the device are represented in Fig. 2.13(a).
The operation of the SCR vaguely resembles that of the GGNMOS. As an ESD stress reaches the anode contact, the reverse biased N-well P-sub junction may reach the breakdown condition hence determining the trigger voltage. This causes a current flow that forward biases the emitter-base junction of the PNP transistor thus injecting a current in P-sub.
Due to the voltage drop in the P-sub region along the resistive path, the base-emitter junction becomes forward biased and the parasitic NPN BJT turns on as well. The current injected in the N-well by the NPN transistor supplies the base of the PNP transistor, therefore the anode does not need to supply all the base current for the PNP and a voltage drop occurs. This positive

[44] Jian-Hsing Lee et al. "Methodology to achieve planar technology-like ESD performance in FINFET process". In: *2015 IEEE International Reliability Physics Symposium*. IEEE. 2015, 3F–3.

[45] Ming-Dou Ker et al. "On-chip ESD protection using capacitor-couple technique in 0.5-/spl mu/m 3-V CMOS technology". In: *Proceedings of Eighth International Application Specific Integrated Circuits Conference*. IEEE. 1995, pp. 135–138.

[46] Julian Zhiliang Chen, Ajith Amerasekera, and Charvaka Duvvury. "Design methodology for optimizing gate driven ESD protection circuits in submicron CMOS processes". In: *Proceedings Electrical Overstress/Electrostatic Discharge Symposium*. IEEE. 1997, pp. 230–239.

feedback mechanism then originates the snapback behaviour of this device.
After the snapback, the device reaches the minimum voltage, V_H, and can be then modeled as a $P-i-N$ diode.[47]

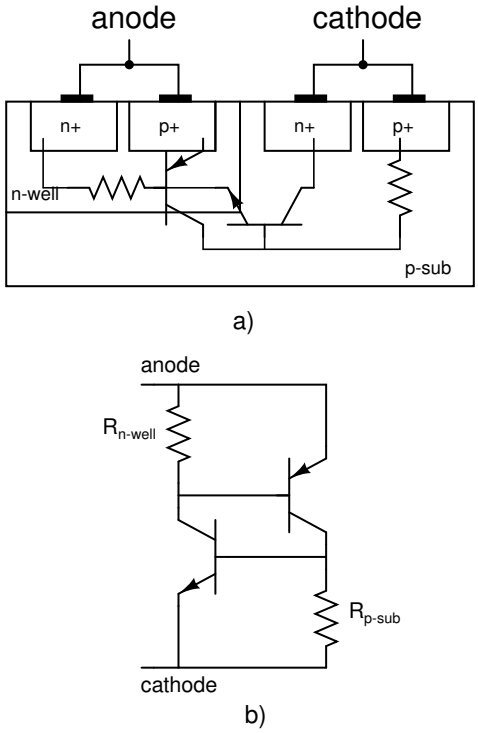

Figure 2.13: (a) Cross section of a CMOS SCR and (b) SCR equivalent circuit.

Due to the strong positive feedback mechanism, SCRs usually show very low holding voltages in the range of 1-2 V,[48] which makes them susceptible to the risk of latch-up when used as ESD protection devices.
Furthermore, when compared to the GGNMOS, SCRs present a higher triggering voltage. This is due to the intrinsic difference of the two structures: while the GGNMOS relies on the N^+ drain P-sub junction breakdown thus achieving a low triggering voltage thanks to the highly doped N^+ drain region, the SCR exploits the breakdown of the N-well P-sub junction therefore obtaining higher triggering voltages due to the lower doping concentrations.
This problem has been address in the Low-Voltage Triggering SCR (LVTSCR), briefly introduced in the next section.

To improve the holding voltage, one adopted technique is to decrease the effective area of the N^+, P^+ regions so that the emitter injection efficiencies are lowered to reduce the closed-loop gain of the device.[49]

[47] AMITAVA Chatterjee et al. "Direct evidence supporting the premises of a two-dimensional diode model for the parasitic thyristor in CMOS circuits built on thin epi". In: *IEEE electron device letters* 9.10 (1988), pp. 509–511.

[48] Vladislav A Vashchenko et al. "High holding voltage cascoded LVTSCR structures for 5.5-V tolerant ESD protection clamps". In: *IEEE Transactions on Device and Materials Reliability* 4.2 (2004), pp. 273–280.

[49] Zhiwei Liu, Juin J Liou, and Jim Vinson. "Novel silicon-controlled rectifier (SCR) for high-voltage electro-

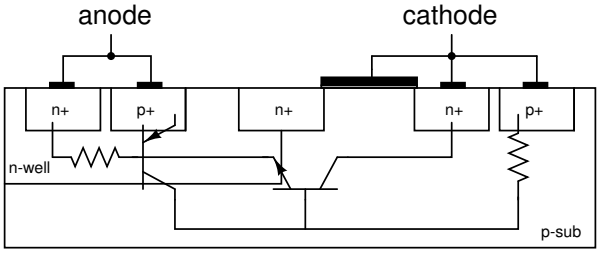

Figure 2.14: Cross section of a LVTSCR.

FinFET technology instead lacks a planar-equivalent ESD robustness due to the difficulty of implementing a FinFET SCR. In conventional FinFETs the absence of a SCR triggering mechanism, i.e., no snapback, is found due to a weaker bipolar action.[50]

2.6.1. LVTSCR

The structure of the Low-Voltage Triggering SCR (LVTSCR) is shown in Fig. 2.14.
The first modification in order to reduce the triggering voltage of an SCR is adding a N^+ region at the edge of the N-well region, thus creating the so-called Modified Lateral SCR (MLSCR).[51]
The reduction of the triggering voltage happens thanks to the shifting of the breakdown junction from the N-well P-sub to the new highly doped N^+ region and P-sub.
To further reduce V_{T1}, the additional N^+ region at the drain contact of the NMOS transistor embedded in the structure is used.[52] Its triggering voltage is reported to be the same of the short channel NMOS.
The operation of the LVTSCR is as follows. Once breakdown occurs at the N^+ P-sub junction, an impact-ionization-generated current contributes to the substrate current. This current flows from the drain to the bulk of the NMOS and, respectively, from the emitter to the base of its parasitic NPN BJT through the $R_{p\text{-}sub}$ resistor. Once the voltage drop of the base emitter junction reaches a sufficiently high value, the NPN transistor turns on, triggering the PNP transistor as well and thus leading to a snapback behavior as fr the standard SCR.

Similarly to the conventional SCR, the holding voltage can be increased by incrementing the NMOS gate length thus reducing the closed-loop gain and incrementing the resistance.[53]

static discharge (ESD) applications". In: *IEEE electron device letters* 29.7 (2008), pp. 753–755.

[50] Milova Paul et al. "FinFET SCR: Design challenges and novel fin SCR approaches for on-chip ESD protection". In: *2017 39th Electrical Overstress/Electrostatic Discharge Symposium (EOS/ESD)*. IEEE. 2017, pp. 1–6.

[51] Charvaka Duvvury and Robert Rountree. "A synthesis of ESD input protection scheme". In: *Journal of electrostatics* 29.1 (1992), pp. 1–19.

[52] Amitava Chatterjee and Thomas Polgreen. "A low-voltage triggering SCR for on-chip ESD protection at output and input pads". In: *Digest of Technical Papers. 1990 Symposium on VLSI Technology*. IEEE. 1990, pp. 75–76.

[53] S Dong et al. "Analysis of 65 nm technology grounded-gate NMOS for on-chip ESD protection applications". In: *Electronics Letters* 44.19 (2008), pp. 1129–1130.

However the increase of thin gate oxide area leads to an increase of the leakage current.[54] Recently, an increase of the drain contact length has been proposed to rise V_H without increasing the thin gate oxide length.[55]

2.6.2. DDSCR

The devices investigated so far, present the snapback characteristic only in the positive direction. If a I/O pad needs to be operated with both positive and negative voltages an ESD protection device with snapback on both directions is necessary.[56]
Regarding this problem, the Dual Direction SCR (DDSCR), depicted in Fig. 2.15, has been proposed.

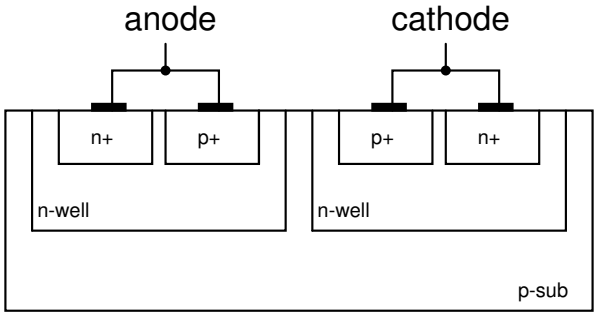

Figure 2.15: Dual Direction SCR.

The symmetric structures allows to use this device as a protection ESD stresses of both polarities.
Once again, analogously to the conventional SCR, a N^+ region can be added at the edges of the two N-wells to decrease the triggering voltage, and variations of the contact distance can improve the holding voltage.

2.7. LDMOS

In the previous sections, it has been investigated how and why the heavy scaling in digital circuits has made modern devices particularly sensible to ESD stresses. As ESD robustness usually requires features contrary to the miniaturization trend, it is an hard task to achieve both small area, high-performance and protection from ESD.

[54] Chang-Tzu Wang and Ming-Dou Ker. "Design of 2× VDD-Tolerant Power-Rail ESD Clamp Circuit With Consideration of Gate Leakage Current in 65-nm CMOS Technology". In: *IEEE Transactions on Electron Devices* 57.6 (2010), pp. 1460–1465.

[55] Kyoung-Il Do and Yong-Seo Koo. "A new SCR structure with high holding voltage and low ON-resistance for 5-V applications". In: *IEEE Transactions on Electron Devices* 67.3 (2020), pp. 1052–1058.

[56] Juin J Liou, Javier A Salcedo, and Zhiwei Liu. "Robust ESD protection solutions in CMOS/BiCMOS technologies". In: *2007 International Workshop on Electron Devices and Semiconductor Technology (EDST)*. IEEE. 2007, pp. 41–45.

That's why, as illustrated at the beginning of this chapter, protection devices are usually implemented.
However, a different scenario must be taken into consideration as well. While the sensible digital devices usually fill the majority of the IC area, there is still the need to interface the logic part with the outside of the chip. Here different devices able to sustain higher currents and voltages must be employed to drive the I/O ports. Unlike digital devices, which need to be replicated millions of time and in which the slightest area increase gets enormously amplified, a limited number of power devices needs to be implemented thus allowing to exploit a bigger area to deliver the higher current needed.
This opens up the possibility to use power devices as protection devices, therefore giving rise to the category of so-called self-protected devices.

The Lateral Double-Diffused Metal Oxide Semiconductor (LDMOS) is a common power device used in Smart Power Technologies thanks to its compatibility with CMOS processes.[57] The need of lateral diffusion stems from the challenge of raising the breakdown voltage of conventional MOSFETs to use them at higher drain voltages. The structure is depicted in Fig. 2.16.

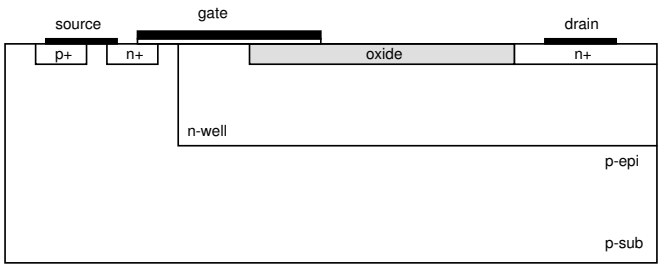

Figure 2.16: LDMOS cross-section.

A new lightly doped region, called drift region, is interposed between the drain contact of the device and the channel region. This allows to support high drain voltages in the low doping regions avoiding premature breakdown in the channel region. Clearly, the length of the drift region has a strong dependence on the breakdown voltage, as a longer drift allows greater spread of the electric field for a given drain voltage.

2.7.1. RESURF effect

The Reduced Surface Field (RESURF) effect is commonly utilized to improve the breakdown voltage of LDMOS transistors.
To support high drain voltages in vertical devices, thick and lightly doped drift regions are usually needed. However, it was reported that for thinner epi layers, an increase of the breakdown

[57] Ming Li, Jeoung-Mo Koo, and Raj Verma Purakh. "0.18 μm BCD technology platform with performance and cost optimized fully isolated LDMOS". in: *2015 IEEE International Conference on Electron Devices and Solid-State Circuits (EDSSC)*. IEEE. 2015, pp. 820–822.

voltage is experienced, due to the RESURF effect.[58]
To better explain the operation of the RESURF effect, a simple diode is considered in Fig. 2.17

A lightly doped N^- epitaxial layer over a P^- sub layer is interposed between the P^+ and N^+ diffusion regions. In Fig. 2.17(a), a thick epitaxial layer is considered.
Two different junctions are visible: the first one is given by the lateral diode and composed by the N^--P^+ vertical junction, while the second one is given by the vertical diode and the N^--P^- horizontal junction. When a voltage V_{BD1} is applied to the first to the device with the thicker epitaxial layer, a narrow depletion region forms, and two electric field peaks establish at the mentioned junctions. The surface P^+-N^- junction, having the highly doped P^+ region, reaches breakdown before the horizontal N^--P^- bulk junction. Therefore a premature anode breakdown is experienced. This situation is depicted in Fig. 2.17(a). It is now possible to consider the situation shown in Fig. 2.17(b) in which, applying the same V_{BD1}, a thinner epitaxial layer is used.
While in the first case the depletion region of the N^--epi and P^+-sub junction was neglected, due to the fact that its width was much smaller than the epitaxial layer thickness, in this case it must be taken into account. This leads to a spread of the electric field of the surface junction, thus reducing the peak value. The device does not undergo anode breakdown, while the vertical bulk junction electric field remains untouched and lower than the critical value for the bulk $E_{crit,B}$.
Finally, the same structure with a voltage $V_{BD2} > V_{BD1}$ applied is considered in Fig. 2.17(c). Now the depletion region fills entirely the epitaxial layer. Two electric field peaks, lower than the breakdown value $E_{crit,S}$ are present at the anode and cathode junction. Now the electric field at the N^--P^- finally reaches the breakdown value $E_{crit,B}$.
Summarizing, the RESURF effect allows to shift the electric field peak from the surface junction, which has a much lower breakdown voltage due to the higher doping concentration, to the lowly doped bulk junction, by considering the 2D effect of the depletion region.
However, care must be taken in the RESURF design, i.e., the correct epitaxial layer thickness and doping must be selected, otherwise premature anode breakdown could still occur or even be displaced into premature cathode breakdown.

The same concept can be applied to LDMOS transistors to improve their breakdown voltage (BV) by lowering the electric field peak at the gate edge that usually leads to breakdown. RESURF LDMOS allow to optimize the trade-off between a low on resistance and a high BV.[59] Different structures have been proposed and implemented based on the same concept, such as

[58] JA Appels and HMJ Vaes. "High voltage thin layer devices (RESURF devices)". In: *1979 international electron devices meeting*. IEEE. 1979, pp. 238–241.

[59] HMJ Vaes and JA Appels. "High voltage, high current lateral devices". In: *1980 International Electron Devices Meeting*. IEEE. 1980, pp. 87–90.

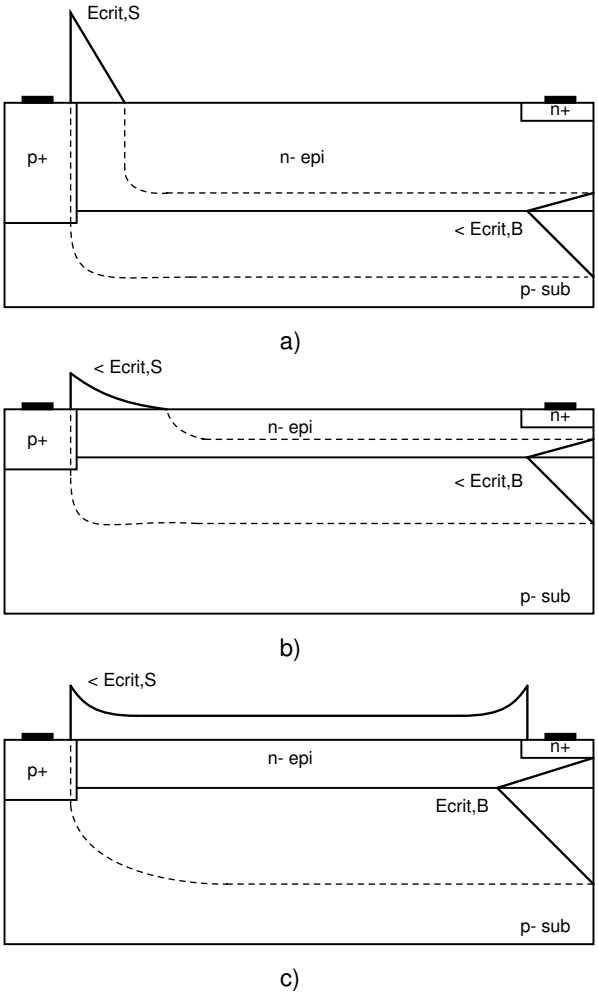

Figure 2.17: Depletion region and electric field highlighted in a diode with a thick epitaxial layer during breakdown at the voltage V_{BD1} (a), at the same V_{BD1} with a thinner epitaxial layer (b), and at the breakdown voltage $V_{BD2} > V_{BD1}$ (c).

double RESURF,[60] and triple RESURF.[61]

2.7.2. LDMOS under ESD stress

After briefly reviewing the reasons why LDMOS transistors are an optimal choice in HV ICs, an analysis of their behaviour under ESD conditions is needed.
LDMOS devices usually have a weak ESD robustness due to localized current crowding effects and non uniform triggering of the parasitic BJT.[62]
By reviewing the structure in Fig. 2.16, a parasitic bipolar transistor can be observed at the N^+ source, P-epi, N-well junctions. While in conventional MOSFETs the snapback caused by the triggering of the parasitic bipolar does not lead to failure until reaching I_{T2}, in most LDMOS devices it causes current filamentation and crowding culminating in thermal failure before reaching the holding regime.
An empirical expression for the holding voltage was proposed by Mergens et al.:[63]

$$V_H \propto \frac{V_{BD}}{\sqrt[n]{1+\beta/k}} \tag{27}$$

where $k = \beta \cdot (M-1) \geq 1$, $M = 1/(1-(V_{DS}/V_{BD}))$ and n is a fitting factor.
Eq. (27) thus relates the breakdown and the holding voltage.

The mentioned failure during snapback, is usually attributed to an electric field peak at the N^+-N^- junction which might give rise to a hotspot and subsequent thermal failure. The mechanism behind the electric field peak is space-charge modulation (SCM): as the N^+ injects carriers inside the lightly doped N^- drift, the carriers grow in number and a point is reached in which the total charge injected is greater than the background doping concentration of the region. This leads to the shift of the electric field peak from under the gate to the N^+-N^- drain junction.
This mechanism is correlated to the Kirk effect in bipolar transistors:[64] under high injection conditions the carrier injected relocate the field peak from the P-base - N^--collector junction to the N^--collector - N^+-contact junction effectively widening the base region and thus reducing the bipolar gain. In Fig. 2.18 the shift of the electric field peak with increasing current is depicted. Recalling once again the LDMOS structure in Fig. 2.16 and its parasitic NPN bipolar, it is trivial to see how the Kirk effect might affect these devices causing premature failure during snapback.

[60] Shikang Cheng et al. "A novel 700V deep trench isolated double RESURF LDMOS with P-sink layer". In: *2017 29th International Symposium on Power Semiconductor Devices and IC's (ISPSD)*. IEEE. 2017, pp. 323–326.

[61] Ming Qiao et al. "A Novel Ultralow R ON, sp Triple RESURF LDMOS With Sandwich npn Layer". In: *IEEE Transactions on Electron Devices* 67.12 (2020), pp. 5605–5612.

[62] Markus PJ Mergens et al. "Analysis of lateral DMOS power devices under ESD stress conditions". In: *IEEE transactions on electron devices* 47.11 (2000), pp. 2128–2137.

[63] Ibid.

[64] CT Kirk. "A theory of transistor cutoff frequency (f T) falloff at high current densities". In: *IRE Transactions on Electron Devices* 9.2 (1962), pp. 164–174.

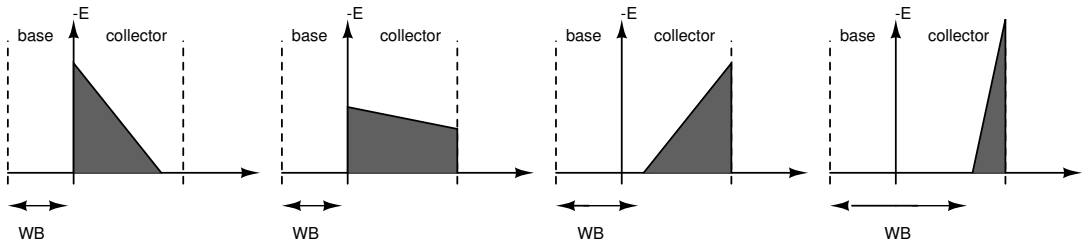

Figure 2.18: Electric field evolution at the base-collector junction at increasing currents.

Lastly, filament formation is the other failure mechanism that undermines LDMOS ESD robustness. The operation behind filament formation is based on the high field mobility degradation correlated to the Kirk effect.

As the electric field increases, the electrons velocity does not vary proportionally with the electric field due to the reaching of the saturation velocity v_{sat}. After space-charge modulation happens and a high electric field peak forms at the N^+-N^- junction, the carriers mobility drops. To overcome the decrease of mobility and increase of resistance, the system forms a filament, i.e., a region of very high carrier density, which screens the electric field and thus improves the carrier mobility.[65] As the root cause of this mechanism is the high electric field peak, smoothing of the drain diffusion has been demonstrated to help in increasing I_{T2} by reducing the electric field peak and discouraging filament formation.[66]

The spatial motion of the thermally generated filaments has been observed, as a result of self-heating and the correlated decrease of the impact ionization rates with increasing temperatures.[67] It is found that the filament motion can mitigate the early local failure induced by static filaments.[68] The motion is triggered by the temperature gradient inside the filament, which is dependent from the parasitic NPN gain and heat dissipation inside the device.[69]

2.8. SCR-LDMOS

Having analyzed and understood the main weaknesses of LDMOS as a self-protected device, it is now possible to describe one of the most promising devices and focus of this work, the SCR-

[65]Mayank Shrivastava et al. "ESD robust DeMOS devices in advanced CMOS technologies". In: *EOS/ESD Symposium Proceedings*. IEEE. 2011, pp. 1–10.

[66]Vijay Parthasarathy et al. "A double RESURF LDMOS with drain profile engineering for improved ESD robustness". In: *IEEE Electron Device Letters* 23.4 (2002), pp. 212–214.

[67]Dionyz Pogány et al. "Moving current filaments in ESD protection devices and their relation to electrical characteristics". In: *2003 IEEE International Reliability Physics Symposium Proceedings, 2003. 41st Annual.* IEEE. 2003, pp. 241–248.

[68]Robert M Steinhoff et al. "2A. 5 Current Filament Movement and Silicon Melting in an ESD-Robust DENMOS Transistor". In: *ELECTRICAL OVERSTRESS ELECTROSTATIC DISCHARGE SYMPOSIUM PROCEEDINGS*. 25. 2003, pp. 98–107.

[69]NK Kranthi, Gianluca Boselli, and Mayank Shrivastava. "HV-LDMOS device engineering insights for moving current filament to enhance ESD robustness". In: *IEEE Transactions on Electron Devices* 69.3 (2022), pp. 1242–1250.

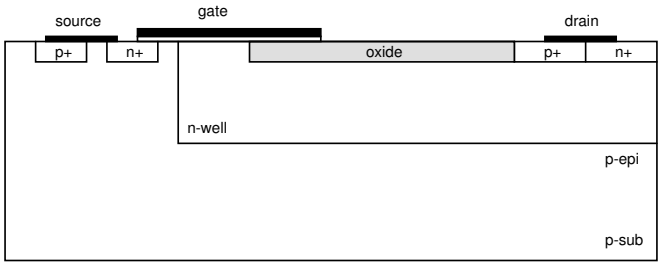

Figure 2.19: SCR-LDMOS cross-section.

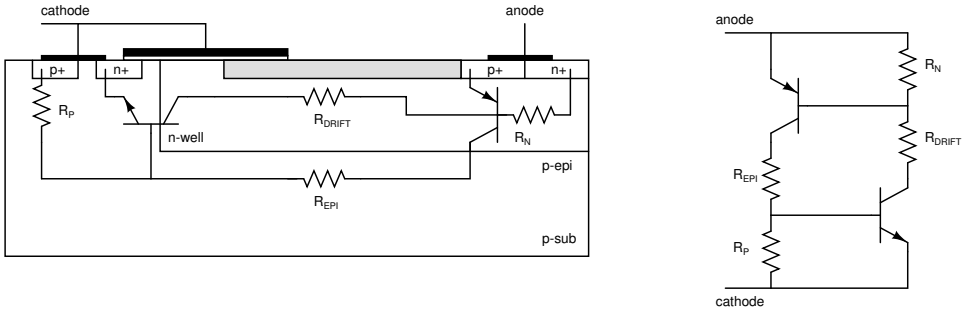

Figure 2.20: (a) SCR-LDMOS structure in which the parasitic components are highlighted and (b) SCR-LDMOS equivalent circuit.

LDMOS. The conventional device structure is presented in Fig. 2.19. This device was proposed by Pendharkar et al.[70] and differs from the LDMOS by the addition of a P^+ diffusion in the drain side. This enables the implementation of a parasitic SCR structure inside the LDMOS. Fig. 2.20 shows the equivalent circuit of the device.
This device allows to combine the high current capability and good ESD robustness of the SCR and the enhanced triggering voltage of the LDMOS given by the drift region.
Most of the consideration made for the LDMOS also apply to the SCR-LDMOS.

The behavior under ESD stress is now studied. As the anode voltage increases, the N-well - P-epi junction becomes increasingly reverse biased until the breakdown voltage is reached. A sudden current flows from the N^+ drain region to the P^+ region through the junction determining the triggering voltage (V_{T1}) of the device. R_P represents the intrinsic resistance that is crossed by the breakdown current, therefore a voltage drop forms through it. As the voltage V_{Rp} reaches approximately the base-emitter junction voltage of the NPN transistor, the latter turns on. Once again, a voltage drop through R_N is created, till it reaches the emitter-base junction voltage of the PNP transistor. When both transistors are on, the typical self-sustaining double injection conduction of the SCR drives the device. The described mode of operation is depicted in Fig. 2.21.

[70] Sameer Pendharkar et al. "SCR-LDMOS. A novel LDMOS device with ESD robustness". In: *12th International Symposium on Power Semiconductor Devices & ICs. Proceedings (Cat. No. 00CH37094)*. IEEE. 2000, pp. 341–344.

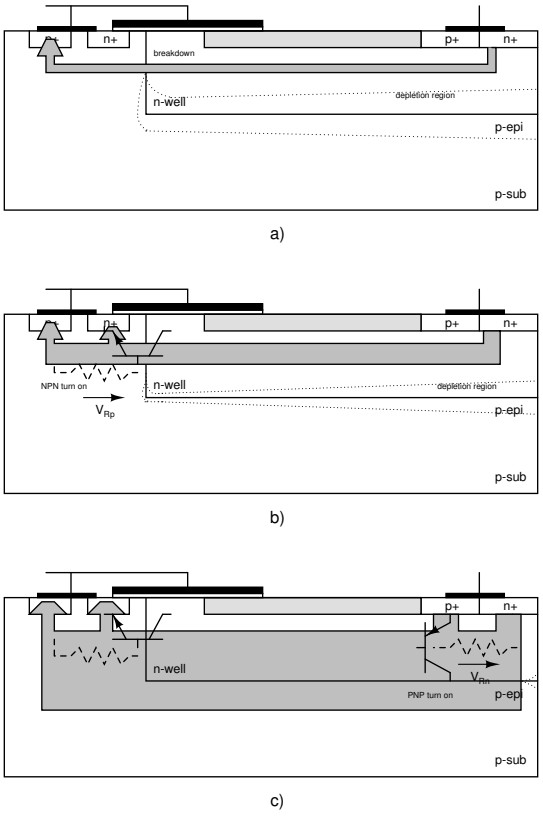

Figure 2.21: (a) Representation of the current flow through: breakdown of the N-well P-epi junction, (b) activation of the NPN transistor and (c) activation of the PNP transistor.

Thus, analogously to the SCR, the feedback injection mechanism between the NPN and PNP transistor creates a quasi-neutral region in the device that severally reduces the holding voltage.[71] Once again, an effective solution to increase V_H is to mitigate the feedback mechanism.

2.8.1. P^+ and N^+ implantation layers

In order to optimize the holding voltage, Liu et al. proposed the addition of a P^+ implantation layer (PIL) under the source side and a N^+ implantation layer (NIL) under the drain side, as seen in Fig. 2.22, in SOI technology.[72]

The main idea behind this proposed modification is that a part of the injected holes from the PNP transistor on the drain side will be neutralized by recombination by the NIL layer hence reducing the feedback mechanism. Similarly, the PIL layer will reduce the electrons injected by the source side NPN transistor.

The reduced double injection conduction leads to a higher holding voltage hence increase latch-

[71] Vashchenko et al., "High holding voltage cascoded LVTSCR structures for 5.5-V tolerant ESD protection clamps".

[72] Si-Yang Liu et al. "A novel latch-up free SCR-LDMOS for power-rail ESD clamp in half-bridge driver IC". in: *2012 IEEE 11th International Conference on Solid-State and Integrated Circuit Technology*. IEEE. 2012, pp. 1–3.

up immunity.

An increase of the holding voltage from 7 V to 17 V has been shown with the implementation of the NIL layer only with minimal I_{T2} degradation. A further increase of V_H has been found by adding the PIL layer as well, however this corresponds to a much bigger I_{T2} degradation.[73]

As a PIL layer is present in the device object of this work, further investigations about the nature of the failure current degradation will be carried out in the next chapter.

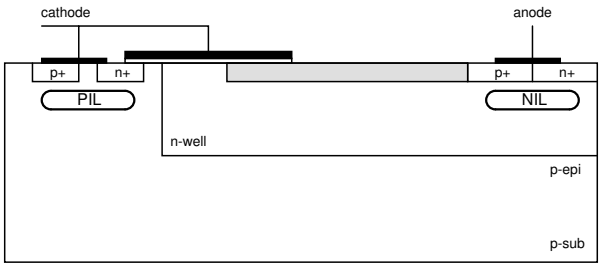

Figure 2.22: Addition of PIL and NIL layers to SCR-LDMOS for improved V_H.

[73] Liu et al., "A novel latch-up free SCR-LDMOS for power-rail ESD clamp in half-bridge driver IC".

3. Study on the Effects of Device Structure Modifications on the Holding Voltage in SCR-LDMOS Devices via 2D TCAD Simulations and Proposed Drift Length Optimization

In this chapter, a description is first given of the physical models used in the simulations. Next, the devices under study are shown, and the effects on V_H of various structure modifications analyzed. In the end, the effects of the length of the drift region on V_H and I_{T2} are deeply investigated.

3.1. Technology Computer-Aided Design

Research and development on semiconductor devices is a difficult task because of the complex physics equations governing these devices, which often make it impossible to find analytical solutions to simple problems.
In addition, the economic investment and long production times make the development of cost- and time-effective optimized devices problematic.

Technology Computer-Aided Design (TCAD) is a powerful tool that models semiconductor fabrication and device operation by solving numerically the complex equations required. This allows a faster development time, and thus an improved time to market.

In this work, Synopsys Sentaurus TCAD is used to perform the simulations.[74]
The tool Sentaurus Structure Editor allows to create and modify semiconductor structures by defining the geometry, the different materials and their properties i.e., doping profiles, defect distributions, intrinsic polarization, anisotropic crystal structure. Successively, Sentaurus Device can be used to simulate the electrical behavior of the device by considering different physical and mathematical models and using numerical solvers.

3.1.1. Physical models

Choosing the correct physical models to consider during simulations is of critical importance. In fact, this is necessary not only to achieve consistent results, but also to reach solutions convergence in a sufficiently short time.
The main considered models will be briefly described.

The transport model utilized in this work is the thermodynamic model which couples the carrier drift-diffusion with an additional driving term given by temperature gradient. Drift-diffusion takes into account both the drift component of the current density given by an electric

[74] Synopsys Sentaurus TCAD. *Synopsys, Inc., Mountain View, CA, USA*.

field and the diffusion component given by the concentration gradient of carriers, and can be expressed as:[75]

$$\begin{aligned} J_p &= q\mu_p p\mathscr{E} - qD_p\nabla p \\ J_n &= q\mu_n n\mathscr{E} + qD_n\nabla n \end{aligned} \tag{28}$$

The additional temperature gradient term is expressed as:

$$\begin{aligned} J_p &= P_p\nabla T \\ J_n &= P_n\nabla T \end{aligned} \tag{29}$$

where $P_{p,n}$ are the absolute thermoelectric powers.

In a semiconductor, the bandgap is defined as the difference between the highest energy level of the valence band and the lowest one of the conduction band and can be expressed by the Varshni's equation:[76]

$$E_g(T) = E_g(0) - \frac{\alpha T^2}{T+\beta} \tag{30}$$

where $E_g(0)$ is the bandgap energy at 0 K and α, β are material parameters. It has been shown experimentally that a high doping level leads to a narrowing of the bandgap. This effect is known as bandgap narrowing (BGN) and can be expressed as:

$$E_{g,eff}(T) = E_g(T) - E_{\text{bgn}} \tag{31}$$

Sentaurus Device handles bandgap narrowing by considering:[77]

$$E_{\text{bgn}} = \Delta E_g(0) + \Delta E_g^{\text{Fermi}} \tag{32}$$

where $\Delta E_g(0)$ depends on the chosen model, and $\Delta E_g^{\text{Fermi}}$ is a correction to account for carrier statistics.
In this work, the Bennett-Wilson model is considered, which reads:[78]

$$\Delta E_g(0) = \begin{cases} E_{\text{ref}}\left[\ln\left(\frac{N_{\text{tot}}}{N_{\text{ref}}}\right)\right]^2 & \text{if } N_{\text{tot}} \geq N_{\text{ref}} \\ 0 & \text{otherwise} \end{cases} \tag{33}$$

[75] Sze, Li, and Ng, *Physics of semiconductor devices*.

[76] Yatendra Pal Varshni. "Temperature dependence of the energy gap in semiconductors". In: *physica* 34.1 (1967), pp. 149–154.

[77] Synopsys, *Sentaurus Device User Guide*.

[78] Herbert S Bennett and Charles L Wilson. "Statistical comparisons of data on band-gap narrowing in heavily doped silicon: Electrical and optical measurements". In: *Journal of applied physics* 55.10 (1984), pp. 3582–3587.

where E_{ref} and N_{ref} are material-dependent parameters.

Doped semiconductor presents charged impurity ions that might cause scattering with the free carriers. This leads to a doping dependent degradation of mobility which must be taken into account.
The selected model is the University of Bologna bulk mobility model, developed for a temperature range between 25 °C and 973 °C, which reads:[79]

$$\mu_{\text{dop}}(T) = \mu_0(T) + \frac{\mu_L(T) - \mu_0(T)}{1 + \left(\frac{N_{D,0}}{C_{r1}(T)}\right)^{\alpha} + \left(\frac{N_{A,0}}{C_{r2}(T)}\right)^{\beta}} - \frac{\mu_1(N_{D,0}, N_{A,0}, T)}{1 + \left(\frac{N_{D,0}}{C_{s1}(T)} + \frac{N_{A,0}}{C_{s2}(T)}\right)^{-2}} \tag{34}$$

where $\mu_L(T)$ is the lattice mobility, expressed as:

$$\mu_L(T) = \mu_{\max}\left(\frac{T}{300K}\right)^{-\gamma + c\left(\frac{T}{300K}\right)} \tag{35}$$

where μ_{max} is the lattice mobility at room temperature and c is a correction factor for higher temperatures.
The parameters μ_0 and μ_1 are expressed as weighted averages of the limiting values for pure acceptor-doping and pure donor-doping densities.

In addition to the bulk mobility model, a surface mobility model is necessary as well. Considering the surface of a semiconductor, a field normal to the interface between the semiconductor and the insulator can be present, decreasing the mobility. One common example being the interface of the channel and gate oxide in a MOSFET. Different mechanisms might degrade the surface mobility, such as Coulomb scattering at low normal fields, or surface phonons and surface roughness scattering at high normal fields.
The University of Bologna surface mobility model combines these different mechanisms by using the Matthiessen's rule:[80]

$$\frac{1}{\mu} = \frac{1}{\mu_{bsc}} + \frac{D}{\mu_{ac}} + \frac{D}{\mu_{sr}} \tag{36}$$

where $\frac{1}{\mu_{bsc}}, \frac{1}{\mu_{ac}}, \frac{1}{\mu_{sr}}$ are respectively the contribution of Coulomb scattering, surface phonons and surface roughness scattering. Lastly, $D = \exp(-x/l_{crit})$ is a damping factor that attenuates the terms as the distance x from the surface increases, using a fitting parameter l_{crit}.

As mentioned in Sect. 2.3.2, the University of Bologna impact ionization model has been selected to model avalanche breakdown in a wide range of temperatures.

[79] Susanna Reggiani et al. "Electron and hole mobility in silicon at large operating temperatures. I. Bulk mobility". In: *IEEE Transactions on Electron devices* 49.3 (2002), pp. 490–499.

[80] S. Reggiani et al. "A Unified Analytical Model for Bulk and Surface Mobility in Si n- and p-Channel MOSFET's". In: *29th European Solid-State Device Research Conference*. Vol. 1. 1999, pp. 240–243.

3.2. Devices under study

3.2.1. Reference device

In order to deeply understand the behavior of complex structures, it is fundamental to start from the the basic structure of the reference device, depicted in Fig. 3.1.

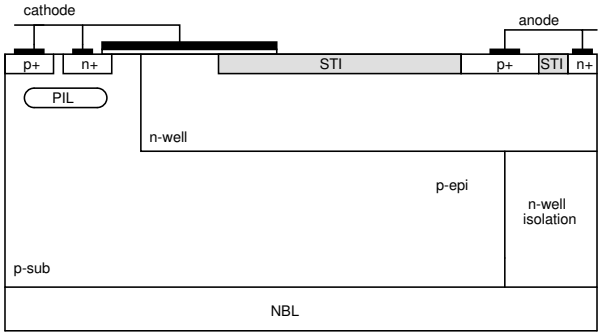

Figure 3.1: Structure of the reference device.

This device presents the typical structure of a SCR-LDMOS. A shallow trench isolation (STI) is used over the N-drift region. An additional STI region is present between the P^+ and N^+ diffusions in the anode region. A PIL layer is present under the source region.
Furthermore, in the bulk of the device, a N^+ Buried Layer (NBL) is implemented alongside a N-Well isolation region.

This device has been simulated by means of TLP simulations, thus a rise time of 100 ps and a pulse length of 100 ns have been utilized. The obtained I-V characteristic is reported in Fig. 3.2.

The extracted values of V_{T1}, V_H and I_{T2} are visible in Tab. 3.1. The obtained holding voltage value is extremely low, thus placing the device at severe risk of latch-up.
The main objective of this work is to understand the intrinsic reason behind the very low V_H value in this kind of structure, and the possible optimization strategies to improve it.

In Fig. 3.3 (left), the distribution of total current density at a current level corresponding to 0.4 mA/µm is shown. This point is located at the onset of the breakdown ($V = V_{T1}$).
A different operation with respect to the one describe in Sect. 2.8 appears due to the presence of the N-well isolation and NBL regions.

	V_{T1}	V_H	I_{T2}
Reference	155 V	3.1 V	30 mA/µm

Table 3.1: Extracted V_{T1}, V_H and I_{T2} of the reference device.

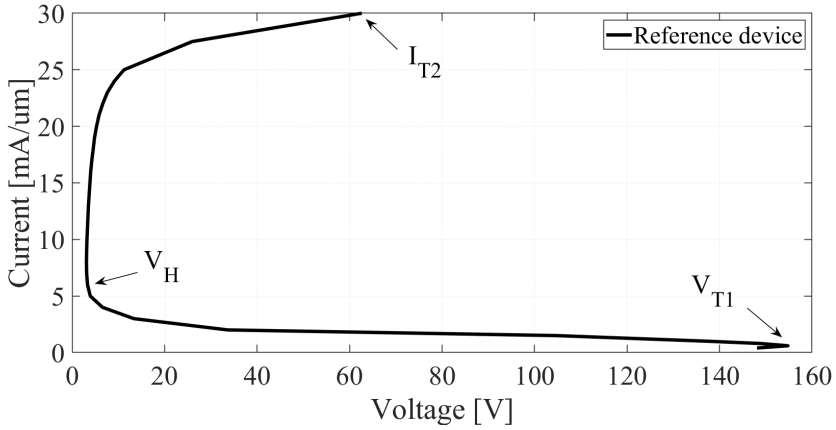

Figure 3.2: I-V characteristic in TLP regime of the reference device.

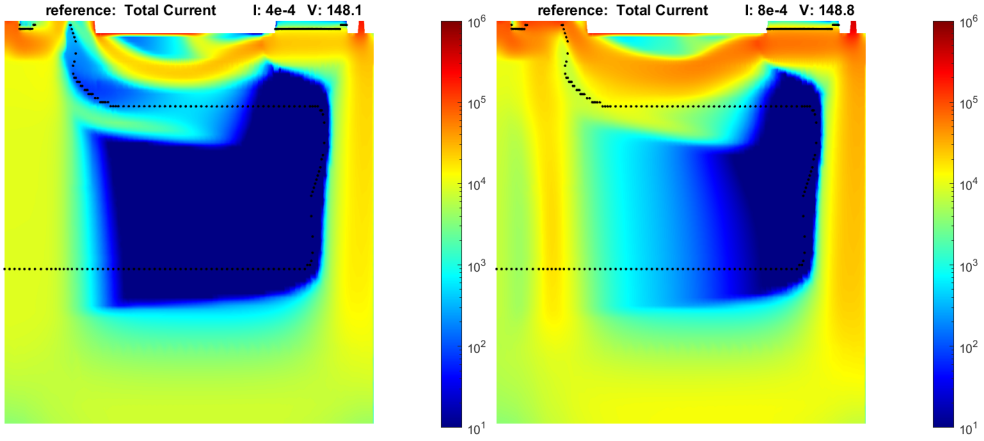

Figure 3.3: Reference device total current density at (left) 0.4 mA/µm, junctions breakdown and (right) 0.8 mA/µm, turn-on of the parasitic NPN.

In the typical SCR-LDMOS structure the breakdown is expected to happen at the P-epi - N-drift junction. In this structure it is visible how, instead, a deeper current conduction is present as well. This is due to the impact-ionization generation of the NBL - P-sub junction: as the NBL presents a high doping concentration, the BV of this junction can be lower than the P-epi - N-drift junction. Therefore, both a superficial and a deep conduction path are distinguishable. In Fig. 3.3 (right), the distribution of total current density is reported for a current level corresponding to 0.8 mA/µm. The next step of the triggering mechanism is clearly visible: the activation of the parasitic NPN transistor leads to an increase of the total current and injection of carriers inside the N^+ diffusion in the source side. The device voltage is of approximately 148.8 V.

So far, the P^+ diffusion on the drain side has played no role in the operation. However, as the current increases, the voltage drop on the drain side reaches the built-in voltage of the emitter-base junction of the parasitic PNP BJT, therefore turning it on.
This situation is clearly visible in Fig. 3.4 (left), in which the total current-density distribution

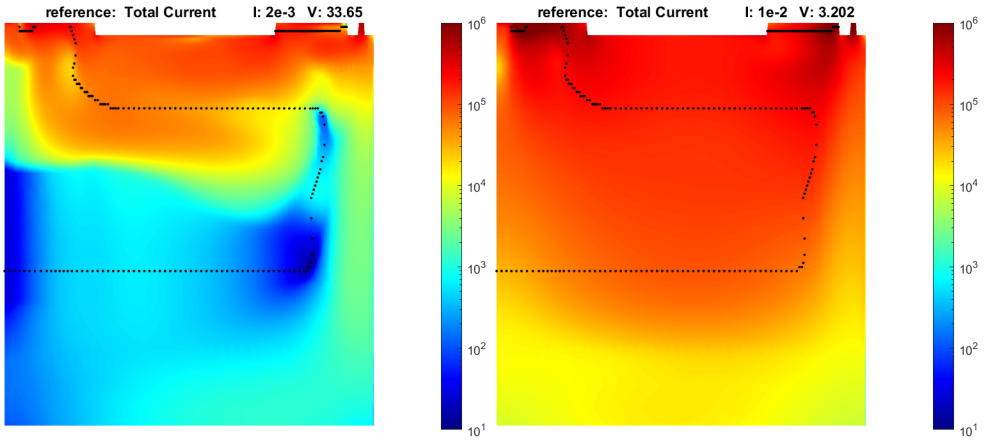

Figure 3.4: Reference device total current density at (left) 2 mA/µm, turn-on of the parasitic PNP and SCR structure and (right) 10 mA/µm, holding regime.

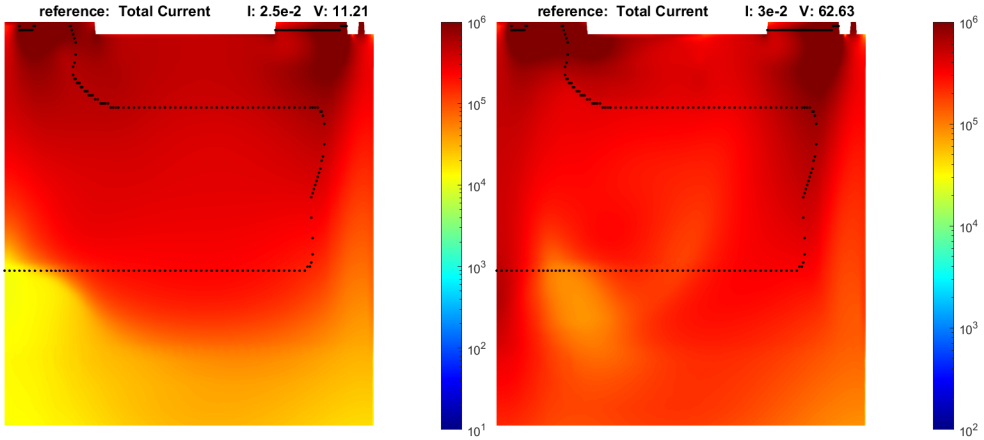

Figure 3.5: Reference device total current density at (left) 25 mA/µm, self-heating and (right) 30 mA/µm, failure.

is shown at 2 mA/µm. The parasitic PNP transistor turns on thus initiating the typical double injection conductivity of the SCR device and lowering the voltage to V_H.

When the current continues to increase, the number of injected carriers far exceeds the doping concentration in the N-drift and P-epi regions, and thus the device reaches the high-level injection regime. Fig. 3.4 (right) depicts the total current-density distribution at 10 mA/µm, in the full holding regime. It is visible how the current distribution is uniform along the whole volume of the device.

In Fig. 3.5 (left) the current density at 25 mA/µm is shown. A variation of the behavior at high currents level is evident in the I-V characteristic. An increase of the device resistance is experienced due to self-heating and thermal carrier generation. As result, the voltage increases as well, reaching approximately 11 V at 25 mA/µm. Finally, the current density at failure is reported in Fig. 3.5 (right). As the maximum temperature reaches the failure value, the high thermal carrier generates raises even more the device voltage up to approximately 60 V.

3.2.2. PNP-E-PIL device

A new device structure based on the same technology of the reference device is proposed in Fig. 3.6, derived from previous work.[81]

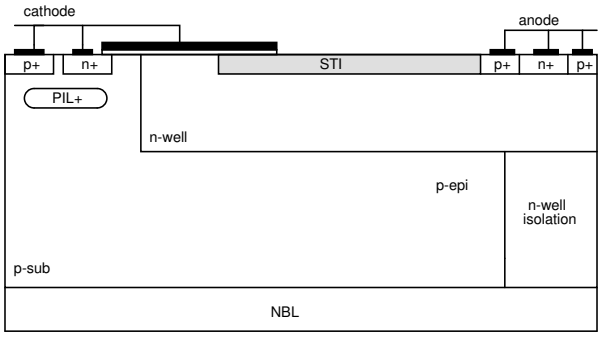

Figure 3.6: PNP-E-PIL device structure.

With respect to the reference device, the drain side configuration has been greatly modified. On the drain side: the STI isolation has been removed, the length of the P^+ diffusion region has been decreased and a second P^+ diffusion region has been added. This give rise to a second parasitic PNP transistor on the drain side. This drain-side configuration has already been proposed in a SCR-LDMOS with buried-oxide isolation for improved I_{T2} and V_H,[82] and has been applied to the conventional SCR-LDMOS with N buried bulk isolation and 150 V off-state breakdown under study. The alignment of the junction of the P+ diffusion and the N^+ diffusion with the N-well isolation is important, and is explored more in detail in the next section.
Furthermore, on the source side, the doping concentration of the PIL layer has been incremented.
Differently from the mentioned previous work, the length of the N^+ diffusion has been incremented, maintaining the rest of the geometry unvaried, thus incrementing the total device length of 0.6 μm.
This device is referred to as "PNP-E-PIL" to highlight the drain side configuration, the extension of the source region and the increased PIL doping concentration.
The obtained TLP I-V characteristic is depicted in Fig. 3.7 and the extracted parameters reported in Tab. 3.2. The value of the holding voltage has been determined as the minimum voltage reached by the device.

[81] Laura Zunarelli et al. "Optimization of the drain-side configuration in ESD-protection SCR-LDMOS for high holding-voltage applications". In: *Proc. of the 35 European Symposium on Reliability of Electron Devices, Failure Physics and Analysis (ESREF)*. IEEE. 2024.

[82] Hung-Wei Chen et al. "ESD improvements on power n-channel LDMOS devices by the composite structure of super junctions integrated with SCRs in the drain side". In: *IEEE Journal of the Electron Devices Society* 8 (2020), pp. 864–872.

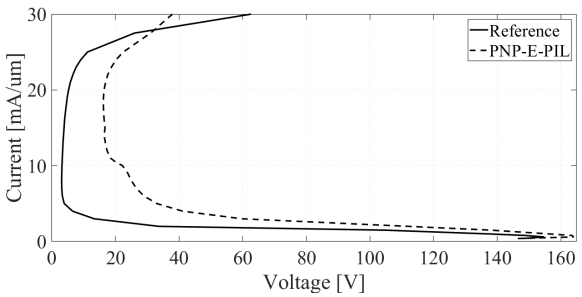

Figure 3.7: I-V characteristic of the PNP-E-PIL device.

	V_{T1}	V_H	I_{T2}
Reference	155 V	3.1 V	30 mA/µm
PNP-E-PIL	164 V	16.2 V	30 mA/µm

Table 3.2: Extracted V_{T1}, V_H and I_{T2} of the PNP-E-PIL device.

The holding voltage has increased from 3 V to 16 V without any failure current degradation. The triggering voltage, instead, experienced an increase of 9 V.
Fig. 3.8 (left) and Fig. 3.8 (right), which depict the total current density respectively at 0.4 mA/µm and 0.8 mA/µm, show a behavior analogous to the reference device.

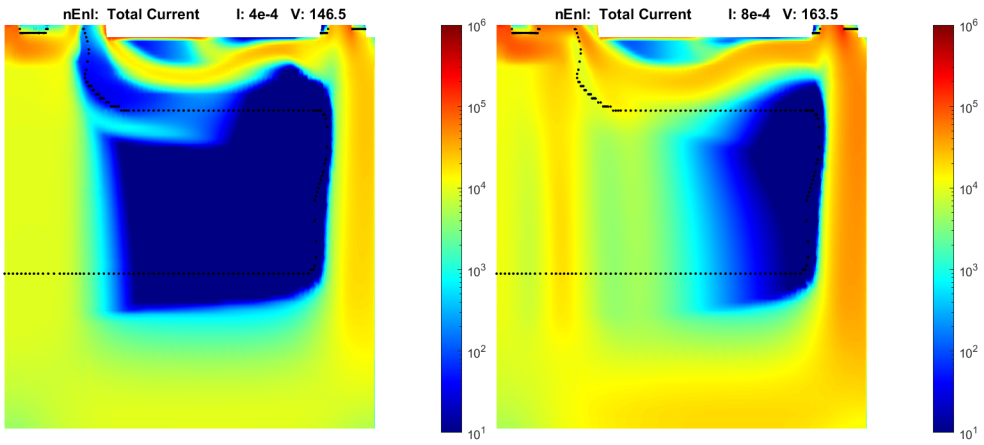

Figure 3.8: (left) PNP-E-PIL device total current density at 0.4 mA/µm, breakdown and (right) at 0.8 mA/µm, turn-on of the parasitic NPN

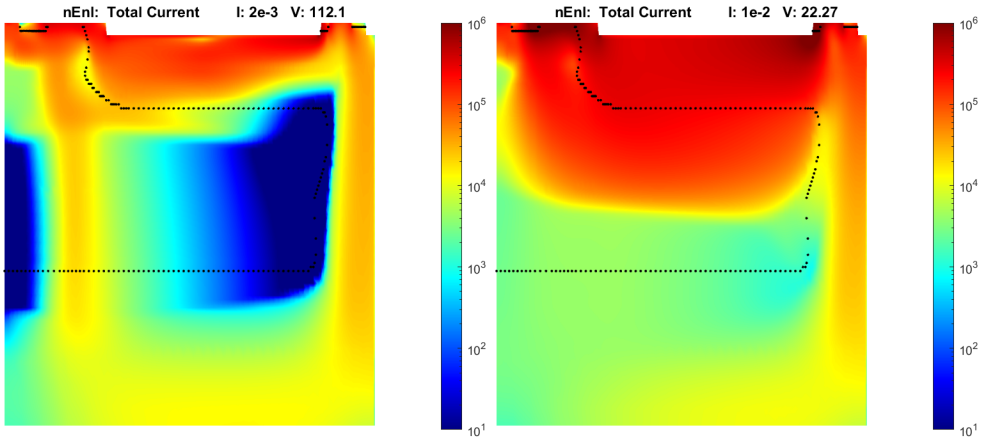

Figure 3.9: (left) Total current density at 2 mA/µm, turn-on of the first PNP and (right) at 10 mA/µm, turn-on of the second PNP.

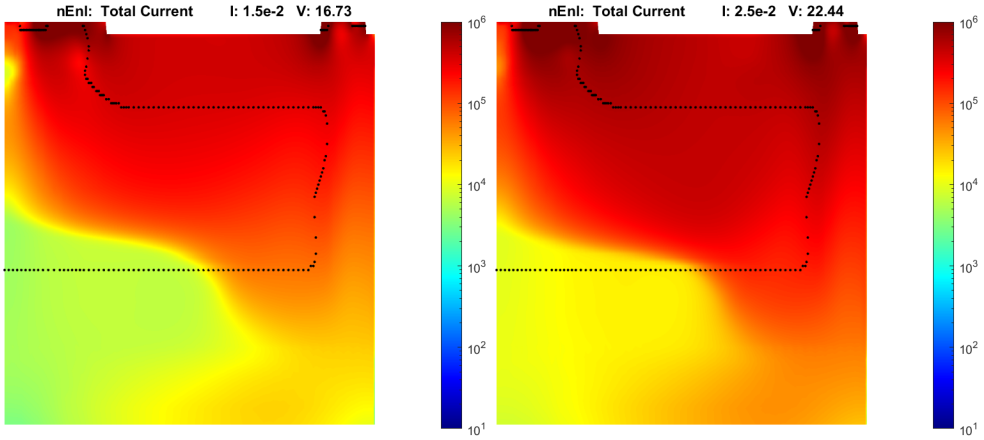

Figure 3.10: (left) Total current density at 15 mA/µm, holding regime and (right) at 25 mA/µm, self-heating.

The same two conduction paths, the superficial and the deep one, are visible during junction breakdown and turn-on of the parasitic NPN BJT.
In Fig. 3.9 (left), the turn-on of the first PNP transistor is visible. Since the length of the P^+ diffusion has been reduced with respect to the reference device, a narrower current path can be seen.

In Fig. 3.9 (right), the turn-on of the second PNP transistor is visible as well. The main visible difference between the holding regime of the reference device and the PNP-E-PIL device is the narrower current path along the depth of the PNP-E-PIL device. In Fig. 3.10 (left) the total current density is shown at 15 mA/µm, in the full holding regime with a voltage of approximately 16 V. In Fig. 3.10 (right), the device voltage rises due to the onset of self-heating, showing an increase of the resistance in the I-V characteristic similar to the reference device. Nevertheless, the current distribution is more confined with respect to the latter.

3.3. Analysis of different structure modifications

3.3.1. Comparison between PNP-E-PIL and reference device

The above brief analysis, is not sufficient to understand why the PNP-E-PIL device shows such a higher V_H than the reference device. Therefore, a more in-depth study has been carried out. The hole density and the electric field plots at various current values are reported below in order to clarify the different behavior of the two devices.

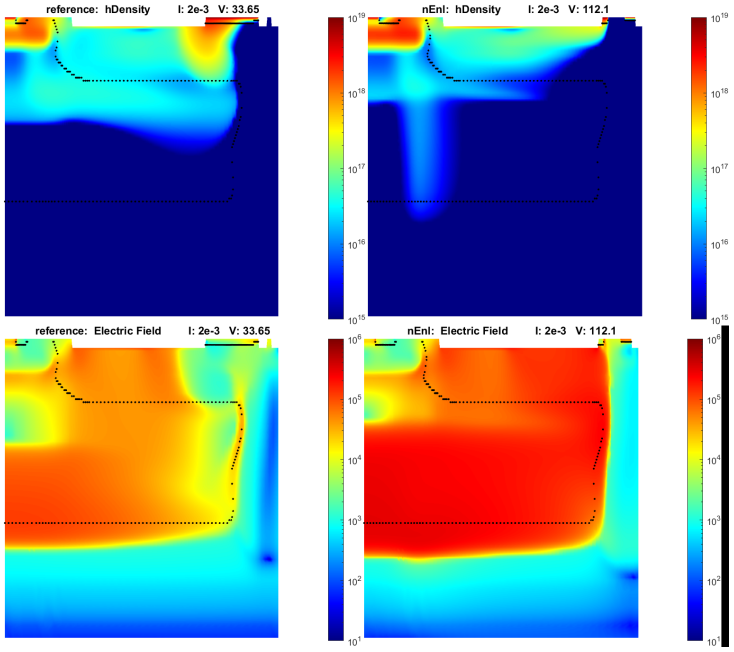

Figure 3.11: (top) Hole density and (bottom) electric field at 2 mA/µm of (left) reference device and (right) PNP-E-PIL device.

Fig. 3.11 shows the hole density and electric field in the reference device (left) and in the PNP-E-PIL device (right) at 2 mA/µm. In both devices, the turning on of the PNP transistor is visible from the holes injected from the P^+ diffusion. As the reference device has a much longer P^+ diffusion, i.e., an increased emitter length, the gain of the bipolar is higher with respect to the PNP-E-PIL device. This is reflected by the greater injection of carriers in the drift region. Looking at the electric field plot, it is possible to observe, along the length of the device, a high electric field region. In the reference device, the latter is obviously impacted by the carriers injected from the PNP transistor, while due to the reduced emitter length of the PNP-E-PIL device, its high field region fully extends up to the N-well isolation.

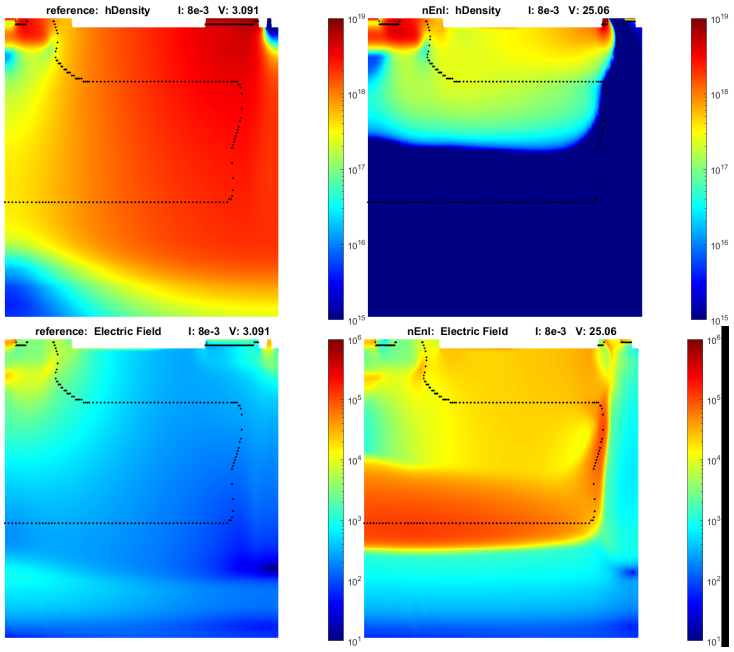

Figure 3.13: Hole density and electric field at 8 mA/µm.

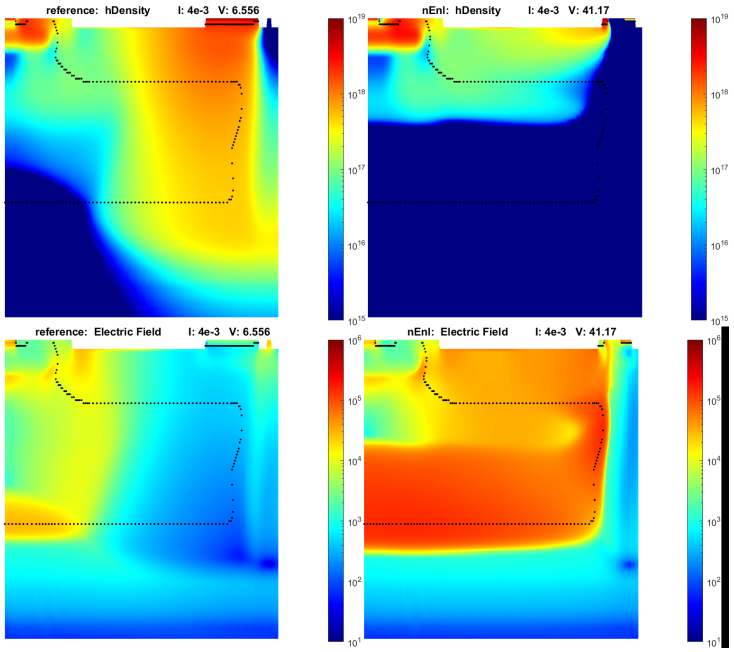

Figure 3.12: Hole density and electric field at 4 mA/µm

This is mostly visible in Fig. 3.12 (bottom). The possible explanation behind this behavior is the following. This device, analogously to most power devices, present low doping concentration regions to allow for higher breakdown voltages, as explained in the previous chapter. Therefore, a very low carrier density is enough to reach the high-level injection regime. As the carriers from the P^+ diffusion are injected, the corresponding regions start to behave as a resistive region due to the very high carrier density. This causes a drop of the electric field. In Fig. 3.13, the two devices at 8 mA/µm are depicted. The reference device, due to the longer emitter,

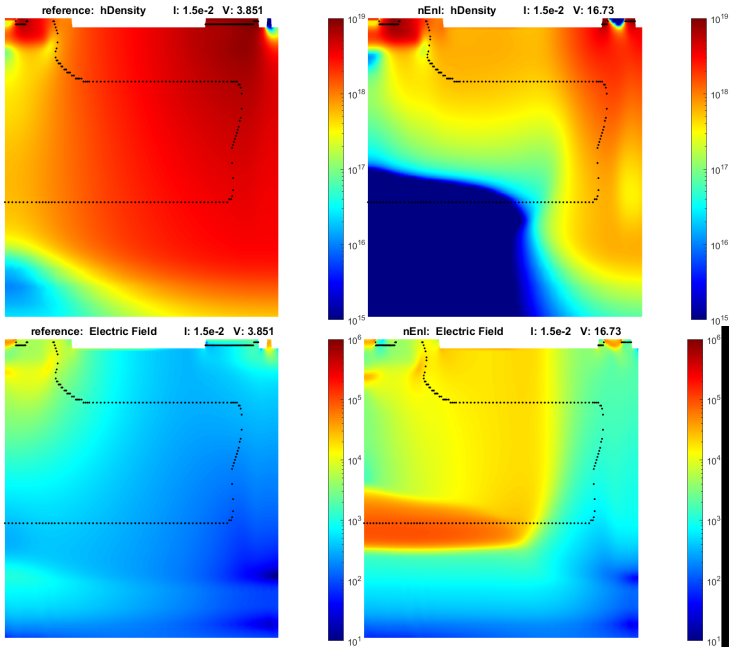

Figure 3.15: Hole density and electric field at 15 mA/µm.

is already in the holding regime ($V_H \simeq 3V$). The carriers are spread along most of the device length, and the high field region is mostly suppressed. Meanwhile, the PNP-E-PIL device is still in snapback. A considerable voltage difference is present between the two devices.

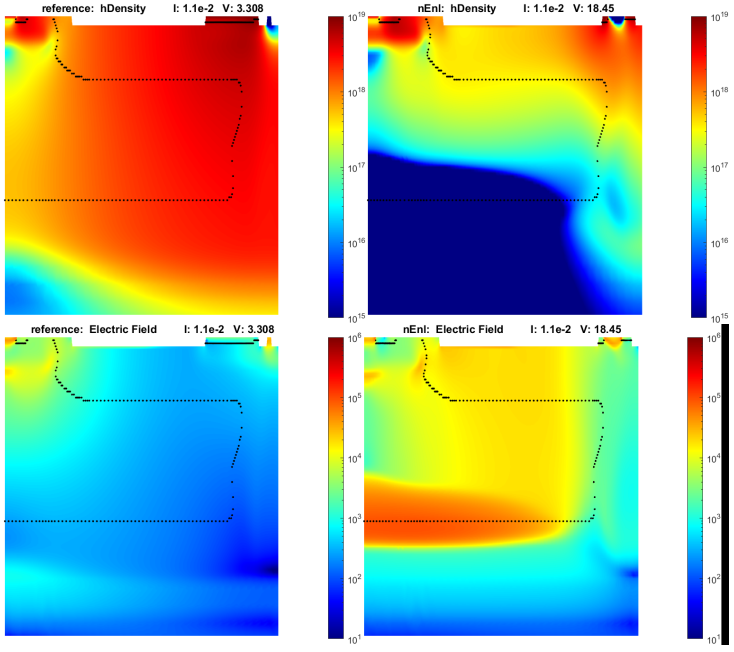

Figure 3.14: Hole density and electric field at 10 mA/µm.

In Fig. 3.14, the turn-on of the second PNP transistor can be noticed in the PNP-E-PIL device at 11 mA/µm. The high field region starts to retract due to the increase of injected carriers.

Finally, in Fig. 3.15 the PNP-E-PIL device reaches the holding regime as well, at 15 mA/µm. The second PNP has fully turned on providing a deeper carrier injection through the N-well isolation, while the high field region settles approximately in the middle of the device.

From the above analysis it has been found that the carrier injection from the drain plays an important role in determining the device voltage.
To further investigate the nature of this relation, the hole density and electric field have been plotted in the drift region along the length of the device, as shown in Fig. 3.16.

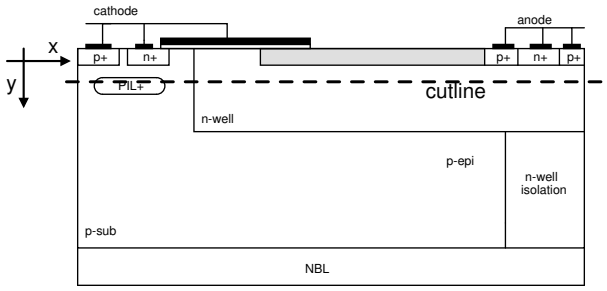

Figure 3.16: Considered cutline for the following 2D plots.

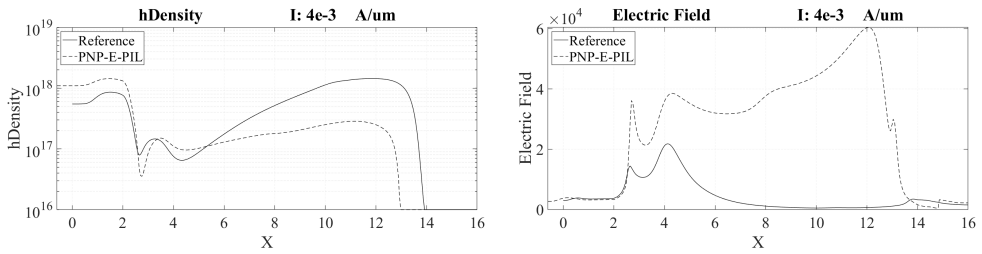

Figure 3.17: (left) Hole density and (right) electric field cutline plots along the drift region at 4 mA/µm.

As it is visible in Fig. 3.17, the reference device shows a greater hole density near the drain side at 4 mA/µm, which can be attributed to its longer emitter region. It is worth noting the hole density numeric value: despite the relatively low input current, the carrier concentration already exceeds 10^{18} cm^{-3}, thus exceeding the drift region doping concentration as well. This is reflected in the electric field plot as the reaching of the high-level injection regime leads to a drop of the electric field.
The PNP-E-PIL device instead, thanks to the reduced PNP gain, has a lower injected hole density thereby keeping a higher electric field along the length of the device.
The hole density and electric field are once again plotted along the length of the device at 15 mA/µm in Fig. 3.18. Both devices are in the holding regime, where the reference device has a voltage of 3 V and the PNP-E-PIL device of 16 V.

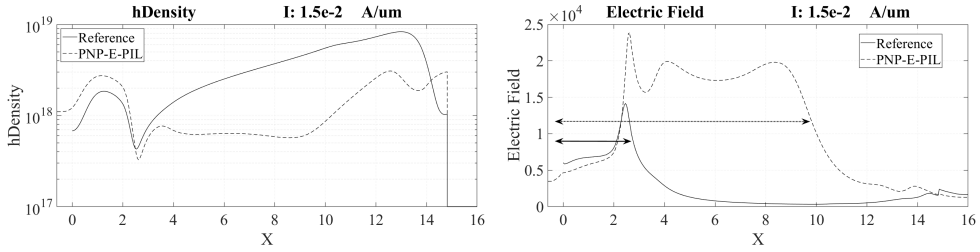

Figure 3.18: (left) Hole density and (right) electric field cutline plot along the drift region at 15 mA/µm.

The same considerations made above apply here. The reference device still shows a higher carriers concentration, now reaching 10^{19} cm^{-3}. The PNP-E-PIL device instead shows not only a lower concentration, but also a characteristic double peak near the drain region. This is attributed to the presence of two PNP transistors injecting carriers. Furthermore, the carriers seems to be less spread along the drift region but more confined near the drain region. This contributes in maximizing the length of the high field region.
This can be assumed as the main reason behind the substantial difference in the holding voltage of the two devices. Recalling the expression of the electrostatic potential:

$$V = -\int_{x_0}^{x_1} \mathscr{E}(x)\, dx \tag{37}$$

where $\mathscr{E}$ is the electric field, it is to be expected that maximizing the length of the region in which $\mathscr{E}$ is high helps in maximizing the voltage.

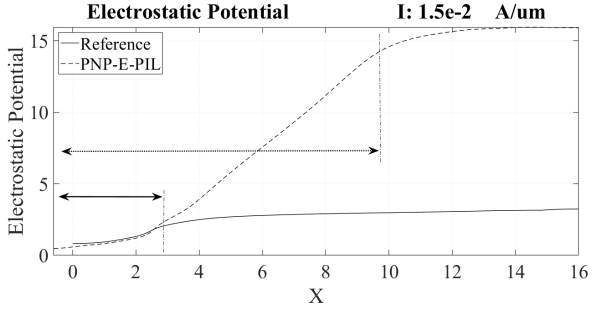

Figure 3.19: Electrostatic potential cutline plot along the drift region at 15 mA/µm.

This is reflected in the electrostatic potential, plotted in Fig. 3.19. The two arrows serve to highlight the correspondence between the high electric field region and the growth of the electrostatic potential in the two devices. The PNP-E-PIL device, thanks to the less spread carrier injection and wider high field region allows a greater increase of the electrostatic potential eventually reaching the holding voltage value of 16 V. On the other hand the reference device shows little to no high field region. The growth of the electrostatic potential is stopped before even reaching the drift region. The total voltage can be thus attributed mostly to the P-epi N-drift junction voltage drop, as the drift region undergoes conductivity modulation given by the

higher carrier injection.

3.3.2. Specific study of the role of the second P^+ diffusion

The previous analysis has proved that a reduction of the parasitic PNP gain is beneficial to the holding voltage thanks to reduction of the injected carriers and resulting maximization of the electric field along the length of the device.
Nevertheless, this can be achieved by simply decreasing the P^+ diffusion length on the drain region. No further explanation of the usefulness of the second P^+ diffusion has yet been given. In order to further investigate its role, the following device, here referred to as 'PNN', has been simulated.

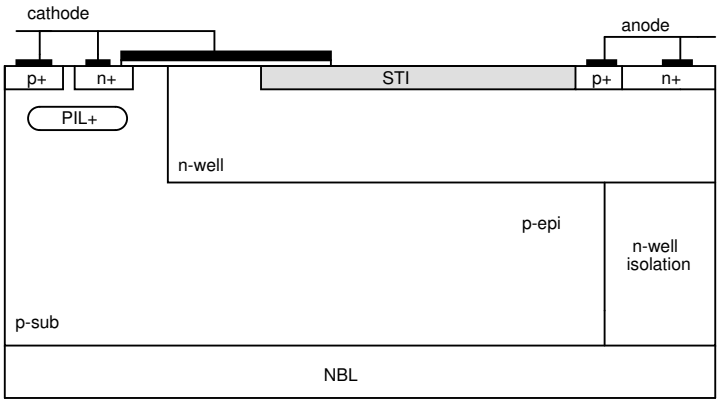

Figure 3.20: PNN device.

The drain side configuration has been modified by removing the second P^+ diffusion and replacing it with an extension of the N+ diffusion. The rest of the device has been left unchanged. The structure is depicted in Fig. 3.20.

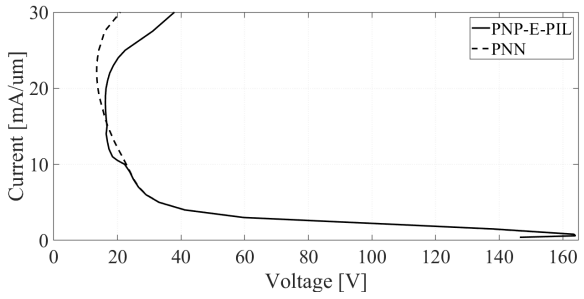

Figure 3.21: I-V characteristic of the PNN device.

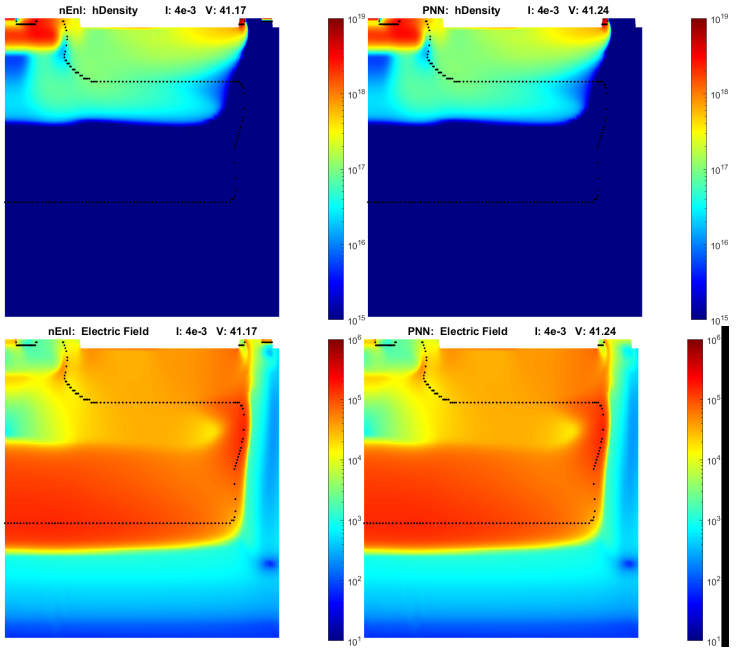

Figure 3.22: (top) Hole density and (bottom) electric field plots of the (left) PNP-E-PIL device and (right) PNN device at 4 mA/µm.

	V_{T1}	V_H	I_{T2}
Reference	155 V	3.1 V	30 mA/µm
PNP-E-PIL	164 V	16.2 V	30 mA/µm
PNN	164 V	13.5 V	27.5 mA/µm

Table 3.3: Extracted V_{T1}, V_H and I_{T2} of the PNN device.

From the I-V characteristic in Fig. 3.21 it is visible how both devices, as expected, present the same behavior during snapback since the second P^+ diffusion does not affect neither the junction breakdown or the NPN turn-on.
The PNN device does not show the change of slope evident in the PNP-E-PIL device in the holding regime, which can then be attributed to the turn-on of its second PNP transistor. This leads to the lower V_H value of the PNN device, as reported in Tab. 3.3, due to the continuing decrease of the voltage.

The turn-on of the first PNP transistor is the same for both devices as well, as shown in Fig. 3.22, proving that the modification of the N^+ diffusion length doesn't influence the parasitic resistor involved in the turn-on. In Fig. 3.23 the turn-on of the second PNP in the PNP-E-PIL device is depicted, at 10 mA/µm. At this point, the PNN device shows a higher voltage (21.55 V) with respect to the PNP-E-PIL device (18.45 V). The reason behind this can be easily understood from the above figure. As the second transistor turns on, more carriers are injected inside the device thereby reducing the high field region. The PNN device instead maintains a higher voltage thanks to the reduced injection.

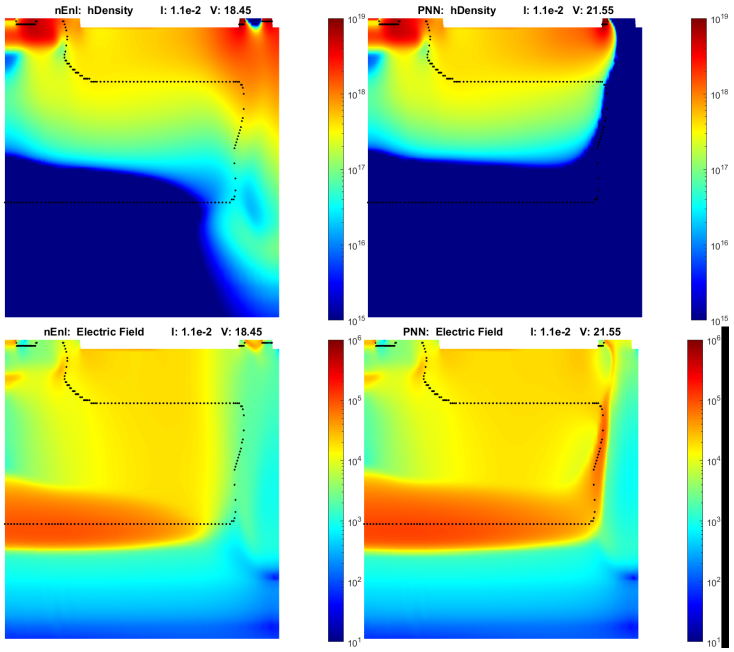

Figure 3.23: Hole density and electric field plots at 11 mA/µm.

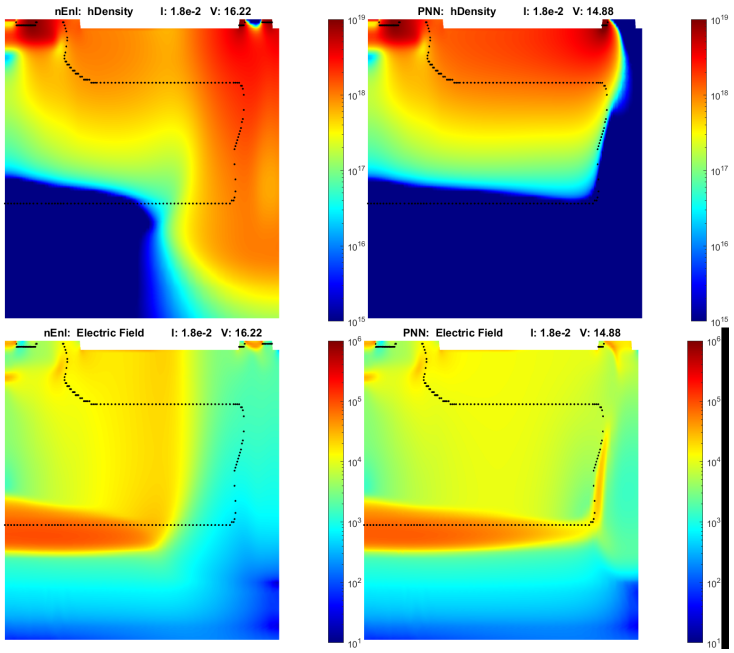

Figure 3.24: Hole density and electric field plots at 18 mA/µm.

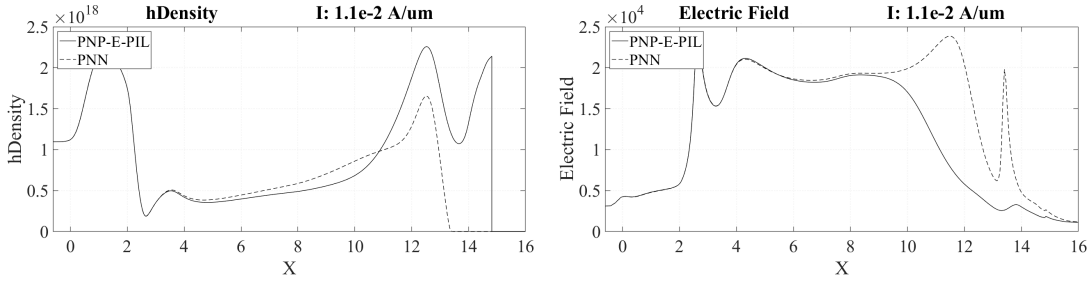

Figure 3.25: (left) Hole density and (right) electric field cutline plots at 11 mA/µm.

In Fig. 3.24, at 18 mA/µm the PNN device shows a lower voltage value (14.88 V) with respect to the PNP-E-PIL device (16.22 V). It is clearly visible how in the PNP-E-PIL device the carriers are injected deeper through the N-well isolation to the NBL layer, while the PNN device maintains a more superficial conduction.

In order to better understand the behavior of these two devices, the hole density and electric field are once again plotted along the length of the device through the drift region.

In Fig. 3.25 the cutline plots at 11 mA/µm are reported. This is the point in which the PNN device shows a higher voltage with respect to the PNP-E-PIL device.

The PNP-E-PIL device once again shows the peculiar hole density double peak caused by the two PNP transistors. This augmented injection is reflected in the electric field, which drops near the drain region. This difference leads to the reduction of the voltage of the PNP-E-PIL device with respect to PNN.

The singular electric field peak in the PNN device can be attributed to the depletion region of the P^+ diffusion N-drift junction, which due to high-injection has shifted from the metallurgic junction down into the N-drift.

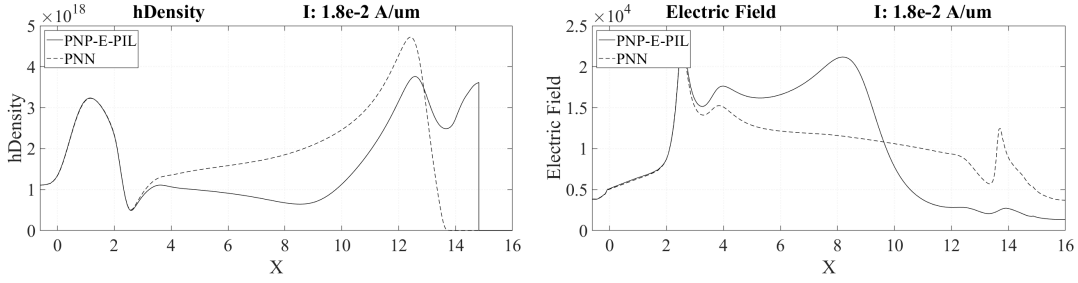

Figure 3.26: (left) density and (right) electric field cutline plots at 18 mA/µm.

In Fig. 3.26 the hole density and electric field are plotted at 18 mA/µm, where the PNP-E-PIL device has a greater voltage than the PNN.

The role of the second P^+ diffusion is now clear: the second PNP transistor serves the role of injecting carriers into the N-well isolation. This helps in containing the spread of the carriers

along the length of the device, thus maximizing the high field region. The PNN device due to the superficial-only conduction path shows a reduced electric field value along the drift, resulting, as visible in the electrostatic potential plotted in Fig. 3.27, a softer electrostatic potential increase. The PNP-E-PIL device instead shows a wider injection near the drain region, due to the vertical path, and a much lower hole density along the drift, resulting in a higher electric field value and thereby increased slope of the electrostatic potential growth.

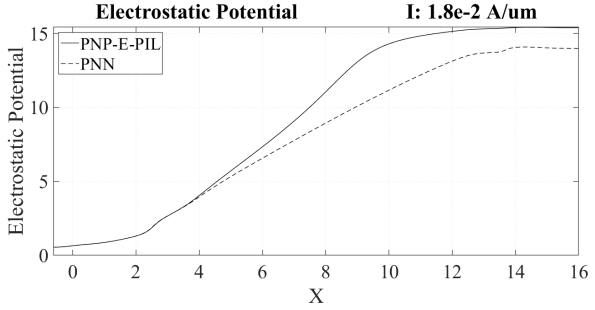

Figure 3.27: Electrostatic potential cutline plot along the drift region at 18 mA/µm.

3.3.3. Variation of the second PNP emitter length

Since the role of the second P^+ diffusion has been clarified, the effect of the variation of its length are discussed. Two different devices are simulated and compared to the PNP-E-PIL device. In the first one, named "Long P2", the second P^+ diffusion has been extended by 0.2 um, while in the second one, "Short P2", it has been reduced by 0.2 um. The devices are represented in Fig. 3.28.

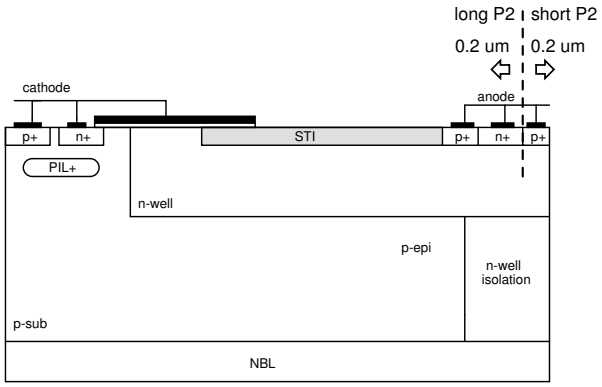

Figure 3.28: Long P2 and Short P2 devices structure.

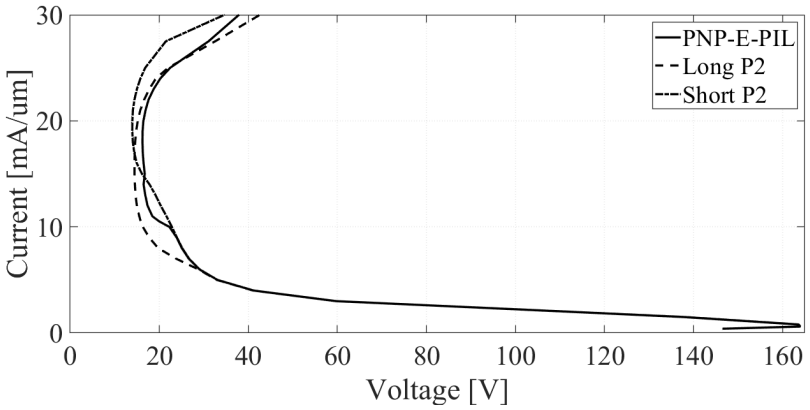

Figure 3.29: I-V characteristics of the long P2 and short P2 devices.

	V_{T1}	V_H	I_{T2}
Reference	155 V	3.1 V	30 mA/µm
PNP-E-PIL	164 V	16.2 V	30 mA/µm
Long P2	164 V	14.5 V	30 mA/µm
Short P2	164 V	13.9 V	30 mA/µm

Table 3.4: Extracted V_{T1}, V_H and I_{T2} of the Long P2 and Short P2 device.

It is worth noting that these configurations lead to a variation of the N^+ diffusion as well, nevertheless, as validated by the previous analysis, it is expected that its length variation is not particularly relevant to the characteristic of the device.

Fig. 3.29 depicts the I-V characteristics of the two devices and Tab. 3.4 the extracted parameters. Once again, both devices present a lower holding voltage. Upon a better analysis of the I-V characteristics, it is possible to see the second PNP transistor turn-on at different input current values in the three devices, as highlighted in Fig. 3.30.

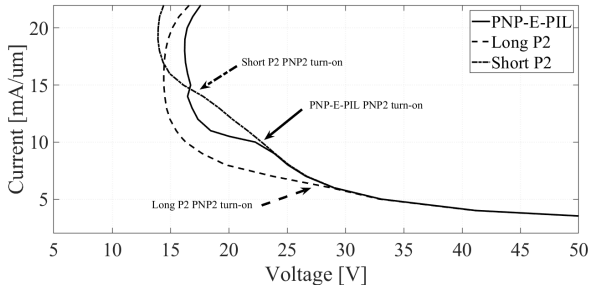

Figure 3.30: Enlargement of the I-V characteristic.

Clearly, due to the variation of the gain of the parasitic transistors caused by the incremented emitter area, different turn-on currents are expected. Nevertheless, this does not still explain the

origin of the different holding voltage.
In Fig. 3.31 the hole density and electric field are plotted. In all three devices, differently to the previous PNN device, the deep carrier injection into the N-well isolation is present. However, the device with the shorter P^+ diffusion (left) shows an incremented superficial injection and a reduced deep one, caused by the decreased second PNP gain. On the contrary, the device with the longer P^+ diffusion (right) has an enhanced deep injection but, surprisingly, still presents a lower voltage with respect to the original PNP-E-PIL device. The reason is investigated through the cutline plots along the length of the device.

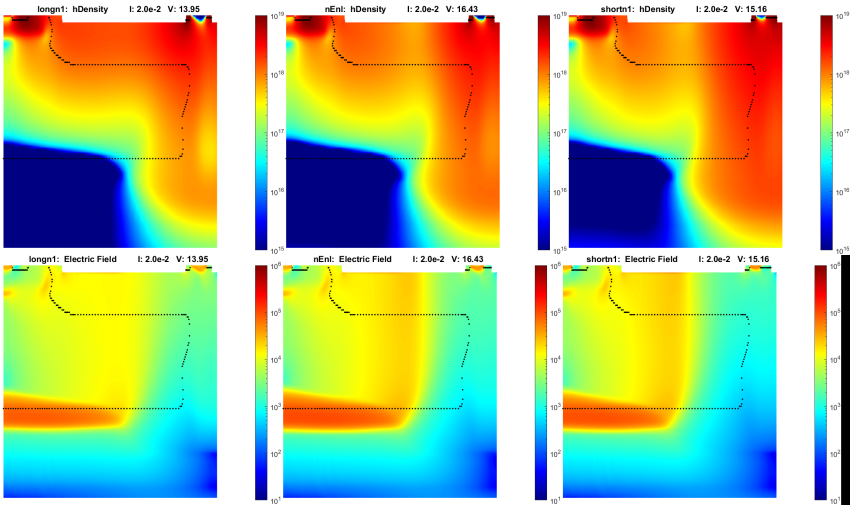

Figure 3.31: Hole density and electric field plots at 20 mA/µm for (left) Short P2, (center) PNP-E-PIL and (right) Long P2 devices.

Considering the Short N2 device hole density (dash-dotted line), a behavior similar to the PNN device is evident: only a smaller part of the carriers are injected into the N-well isolation region due to the reduced gain, thereby showing a higher density along the drift and thus reducing the electric field value.
The Long P2 device, instead, presents a much higher second peak in the carrier density, however, the first peak has incremented as well. The region with high carrier density near the drain becomes wider while the density far from the drain is lower with respect to the PNP-E-PIL device. This can be attributed to the following reason: the incremented emitter area leads to a greater deep injection, nevertheless, this in turn leads to a widening of the conductivity modulated region towards the drift. This is particularly evident in the electric field plot, where the Long P2 device shows a higher electric field value, thanks to the reduced carrier injection into the drift, but a decrease in width due to the aforementioned widening of the region affected by high-level injection. This can be clearly seen in Fig. 3.32

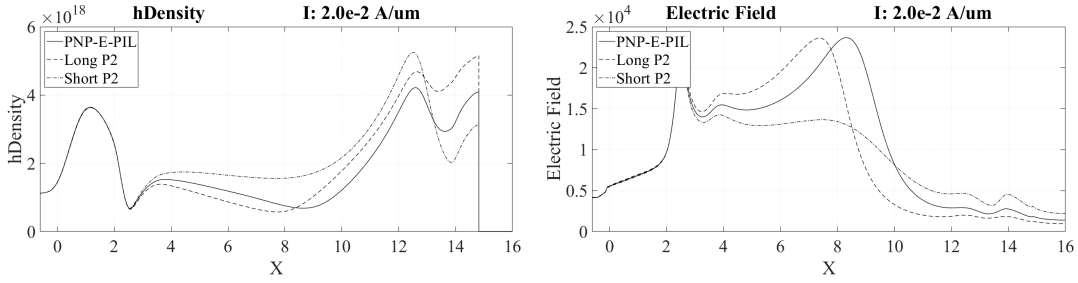

Figure 3.32: (left) Hole density and (right) electric field cutline plots at 20 mA/µm.

The above behavior is obviously reflected on the electrostatic potential, as visible in Fig. 3.33. The Short P2 device shows a flatter potential growth along the drift due to the lower electric field value. The Long P2 instead has a steep growth, which however stops too early to achieve a sufficiently high voltage value.

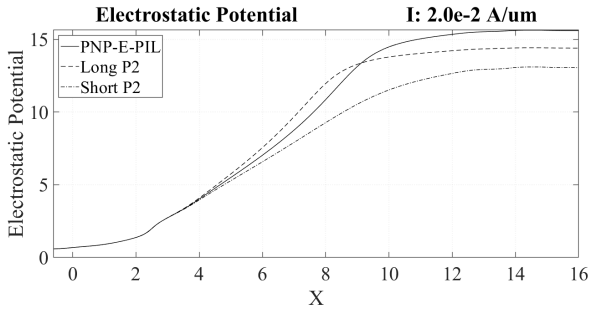

Figure 3.33: Electrostatic potential plot at 20 mA/µm.

The obtained result from this investigation is that while the role of the second P^+ diffusion is to redirect carrier inside the N-well isolation to contain the spreading of the high-level injection regime region, a careful choice of its alignment is necessary in order to optimize the resulting holding voltage.

3.3.4. Role of the PIL layer: a novel structure-specific deep conduction mechanism

Recalling the introduction of the PNP-E-PIL device in Sect. 3.2.2, with respect to the reference device, three were the main modifications made:

- PNP configuration on the drain side.
- Increase of the PIL doping concentration.
- Extension of the N^+ diffusion on the source side.

While the advantages of the PNP configuration on the drain side have been extensively studied in the previous sections, the purpose of the increased PIL doping concentration and extension of the source have yet to be clarified.

In order to do so, two devices have been simulated: the device named ”PNP” presents the PNP configuration on the drain side without the increased PIL doping and without the source extension, while the device ”PNP-PIL” presents the increased PIL doping and no source extension. The I-V characteristics of the two devices are compared to the PNP-E-PIL device in Fig. 3.34 and the resulting parameters in Tab 3.5.

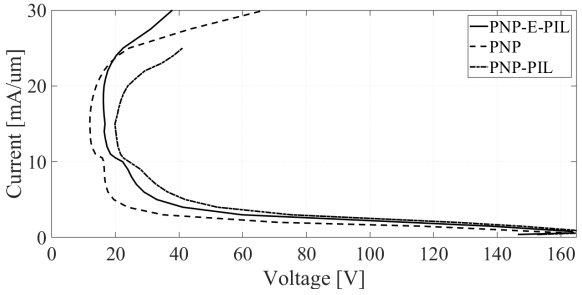

Figure 3.34: I-V characteristics of the PNP and PNP-PIL devices.

	V_{T1}	V_H	I_{T2}
Reference	155 V	3.1 V	30 mA/µm
PNP-E-PIL	164 V	16.2 V	30 mA/µm
PNP	166 V	12 V	30 mA/µm
PNP-PIL	162 V	20 V	25 mA/µm

Table 3.5: Extracted V_{T1}, V_H and I_{T2} of the PNP and PNP-PIL device.

Beside the negligible variation of the trigger voltage, the modifications are mostly reflected in the holding voltage and failure current. The PNP device shows an important reduction of V_H, while maintaining $I_{T2} = 30$ mA/µm. On the other hand, increasing only the PIL doping concentration without extending the source side leads to an increase of V_H but an important degradation of I_{T2}. The PNP-E-PIL device once again shows the optimal trade-off between a high holding voltage and failure current.

The hole density plots at 6 mA/µm are reported in Fig. 3.35. The most visible difference between the three devices is the spreading of the carriers along the depth of the devices.

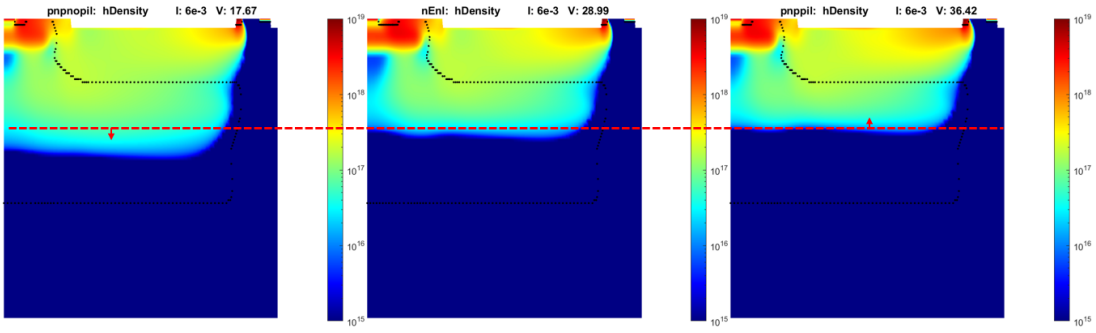

Figure 3.35: Hole density plot at 6 mA/µm of (left) PNP, (center) PNP-E-PIL, (right) PNP-PIL.

This is an expected result recalling the considerations on the implantation layer in the previous chapter: the role of the PIL is to reduce the NPN gain by enhancing recombination in the base. This leads to a reduction of the double injection SCR mechanism and thus an increase of the voltage.
However, this simple analysis of the situation still doesn't fully explain the behavior visible at 13 mA/µm in Fig. 3.36, where the second PNP transistor is active.
The PNP device shows an important enhancement of the carrier injection in the N-well isolation, which is on the other hand widely reduced in the PNP-PIL device. The above explanation of the effect of the PIL layer lacks the justification for this increased deep injection.

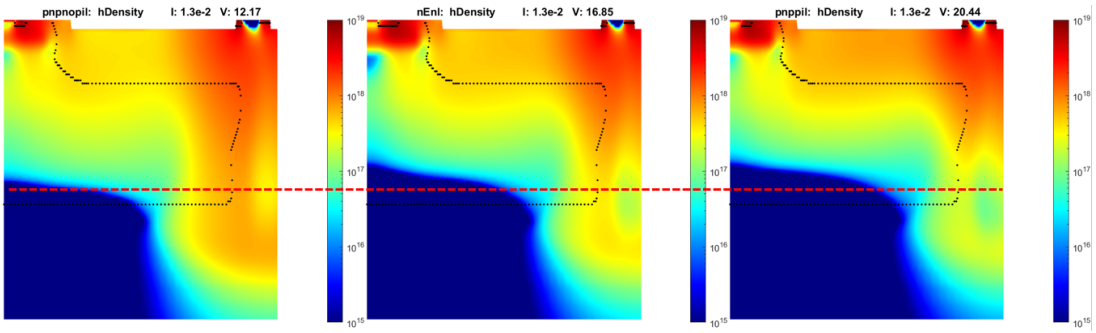

Figure 3.36: (left) Hole density plot at 13 mA/µm of PNP, (center) PNP-E-PIL, (right) PNP-PIL.

Differently from the previous sections, in Fig. 3.37 the cutline hole density along the depth of the device is reported near the source side.

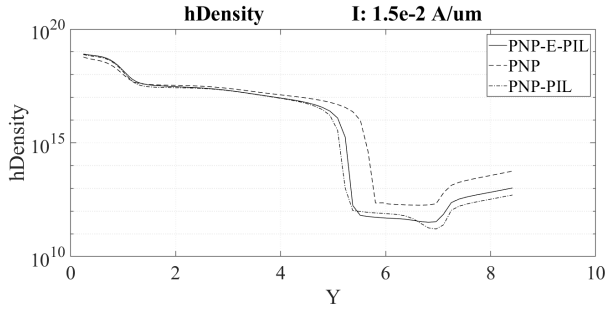

Figure 3.37: Hole density cutline plots along the depth at 15 mA/µm near the source region.

The plot once again highlights the deeper carrier density in the PNP device. In Fig. 3.38, the hole density along the depth of the device is plotted in the drift region. The PNP device shows an enhanced deep injection, which is instead reduced near the surface, while the PNP-PIL device likewise has a more superficial conduction which quickly decays along the depth. The PNP-E-PIL device shows an intermediate behavior.

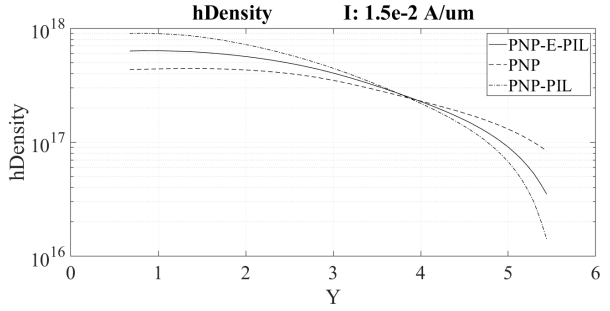

Figure 3.38: Hole density cutline plots along the depth at 15 mA/µm in the drift region.

In Fig. 3.39, the vertical component of the hole current density is shown. Interestingly, the PNP device presents an important increase of the vertical component with respect to the two other devices.

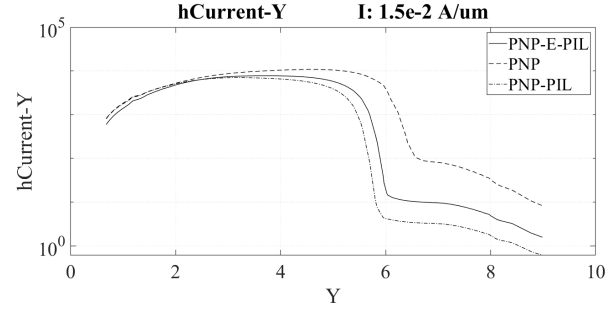

Figure 3.39: Vertical component of the hole current cutline plots along the depth at 15 mA/µm in the drift region.

These results cannot be explained by the given simplistic interpretation of the operation of the SCR-LDMOS.

It is now clear that the added regions with respect to the conventional device, i.e., the N-well isolation region and the buried layer, must be taken into account in the analysis.
Therefore, by reviewing the device structure, it possible to notice the presence of another additional parasitic structure. In fact, the combination of the source side N^+ diffusion, P-epi and NBL, forms another parasitic vertical NPN transistor. This differs from the already mentioned conventional lateral NPN transistor, formed from the N^+ diffusion, P-epi and N-drift regions.

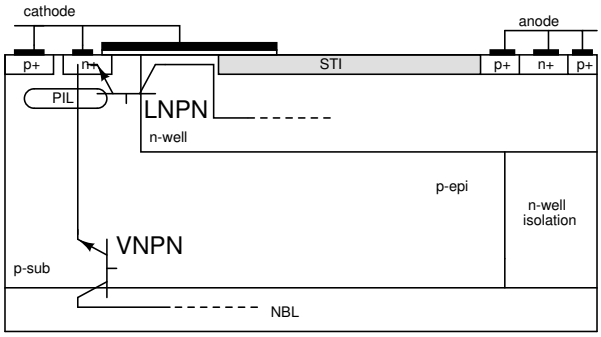

Figure 3.40: Structure of the device with the vertical NPN highlighted.

The presence of this additional component, shown in Fig. 3.40, can partially explain the behavior seen above. The increase of the PIL doping concentration not only has the effect of reducing the lateral NPN gain, but reducing the vertical NPN gain as well. Therefore, the devices with increased PIL doping concentration presents a lower vertical component of the current.

Nevertheless, despite taking into consideration this new parasitic structure, the increased deep carrier injection from the N-well isolation visible in the low PIL concentration device is yet unclear.
The reason attributed to this behavior is the presence of a new deep conduction mechanism involving the above mentioned vertical NPN. By considering the drain P^+ diffusions, and the VNPN, as shown in Fig. 3.41, it is possible to see a different parasitic SCR structure, here named ”Deep SCR”.

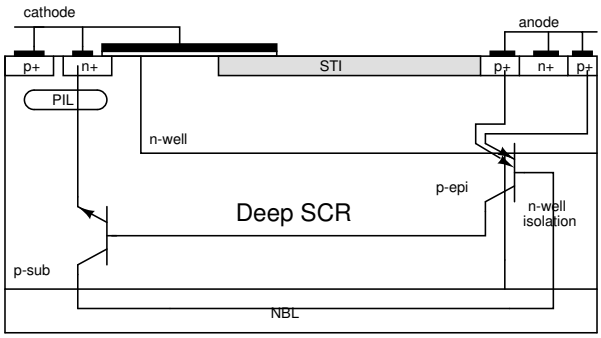

Figure 3.41: Deep SCR structure composed by the parasitic PNP transistors and the vertical NPN.

This novel structure is responsible for the deep conduction mechanism visible in the low PIL device. Indeed, with respect to the high PIL device, the reduced PIL doping concentration enhance the operation of the vertical NPN, thereby enhancing the operation of the deep SCR as well, finally explaining the incremented carrier injection in P-epi from the N-well isolation.
Recalling the above considerations about the importance of limiting the injection of carriers due to high-level injection reducing the electric field across the device, this ultimately clarifies why the increase of the PIL doping concentration increases the holding voltage of the device.

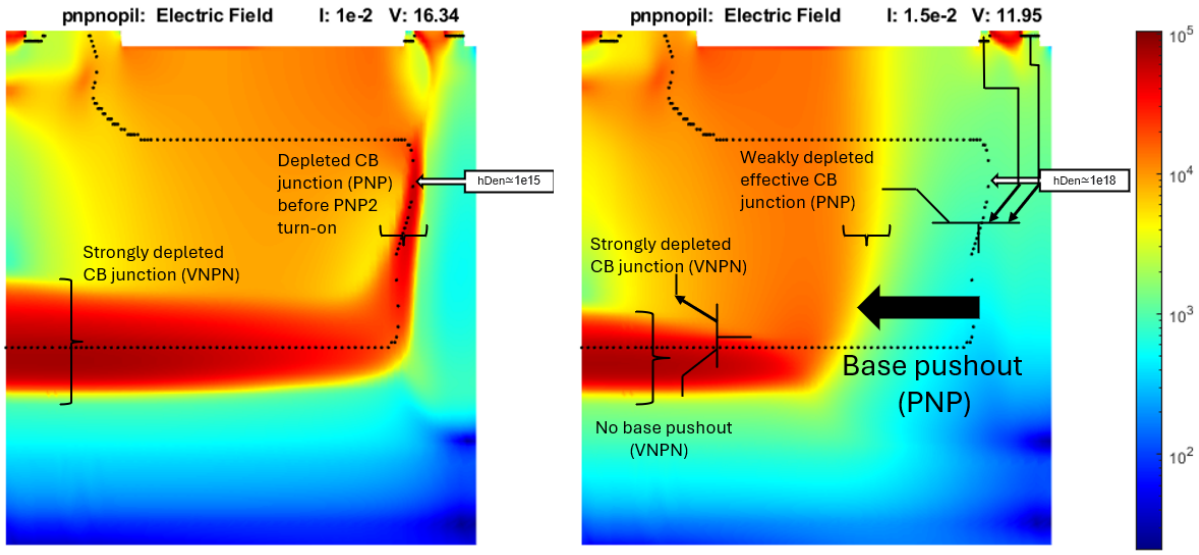

Figure 3.42: Electric field plot at (left) 10 mA/µm and (right) 15 mA/µm .

In Fig. 3.42 the above described mode of operation is clearly visible. The electric field in the PNP device is plotted at 10 mA/µm and 15 mA/µm. At 10 mA/µm, the second PNP transistor is still off. It is possible to see a high field peak along the NBL - P-sub and N-well isolation - P-epi junctions, attributed to the depleted collector base junction of respectively the VNPN and PNP BJTs.
At 15 mA/µm, the second PNP is active, and a strong injection of carriers occurs. Due to the lower PIL doping concentration, the deep SCR operation is enhanced. The high injection causes the onset of base pushout due to Kirk effect, as visible from the evident shift of the electric field peak inside the P region. The VNPN is not affected from base pushout due to the higher doping concentration in the NBL layer and lower injected carriers.

Summarizing, increasing the PIL doping concentration inhibits the operation of the deep SCR structure thanks to the reduced VNPN gain, thus limiting the injection of carriers and thereby mitigating the electric field reduction caused by high-level injection. This finally results in the desired V_H increase.

Lastly, it is now possible to address the need of the source extension used in the PNP-E-PIL device with respect to the PNP-PIL device. As visible in Tab. 3.5, the PNP-PIL device

reports the highest holding voltage, nevertheless a drop of the failure current from 30 mA/µm to 25 mA/µm occurs. As graphically shown in Fig. 3.43, this is attributed to a current crowding effect: by inhibiting the operation of the deep SCR, an increased superficial current is present in the device. This leads to the onset of current crowding near the STI edge, eventually leading to a localized hotspot and consequent premature failure.
The adopted solution to this problem is to increase the length of the source side N^+ diffusion, to relax the crowding effect near the STI. This comes at the cost of increased device footprint area, but allows to maintain the original I_{T2} value.

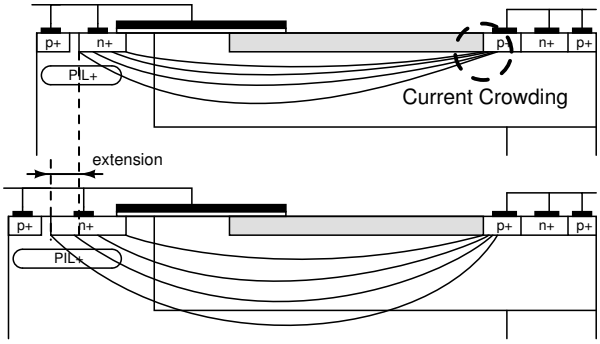

Figure 3.43: Schematic representation of the effect of source extension on current crowding.

However, this extension has clearly the side effect of enhancing the operation of the deep SCR by increasing the emitter area of the VNPN, therefore, a reduction of the holding voltage is experienced.

3.3.5. Summary of key findings

A summary of the most important results obtained in this comparative study is now given.

- The high injection of carrier was found to be detrimental to achieve a high holding voltage due to the reduction of the electric field along the length of the device caused by conductivity modulation. Therefore, a reduction of the drain P^+ diffusion area is beneficial.
- The role of second PNP transistor, given by the additional P^+ diffusion, is to redirect the injected carriers through the N-well isolation region thus minimizing the carriers injected in the drift region. The diffusion alignment proved to be crucial in order to efficiently do so.
- Increasing the PIL doping concentration has the effect of suppressing the operation of the deep SCR structure by reducing the vertical NPN transistor gain. This allows a more superficial current flow and a reduction of carrier injection.

3.4. Drift length variations for scalable V_H

In the previous chapter, it was possible to understand the importance of the carrier spread along the length of the device. Due to the onset of high-level injection, the spread of the carrier results in a substantial reduction of the electric field along the device which is fundamental to achieve a high holding voltage.
The proposed modification to address this problem is the increase of the drift length: as the voltage across the device is mainly given by the width of the high field region, by increasing the drift length it is possible to increase the width of the high field region as well. The proposed modification is depicted in Fig. 3.44.

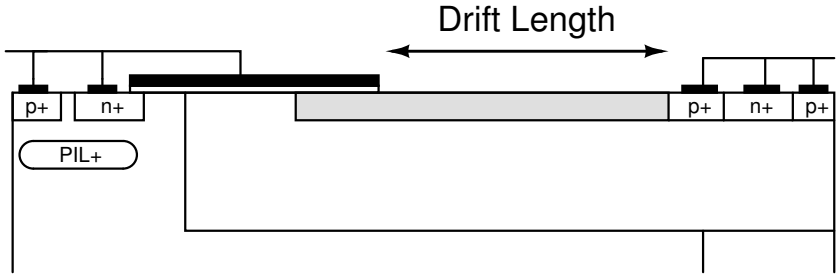

Figure 3.44: Proposed increase of the drift length.

Different drift lengths have been simulated. The results are illustrated in Fig. 3.45 and Tab. 3.6.

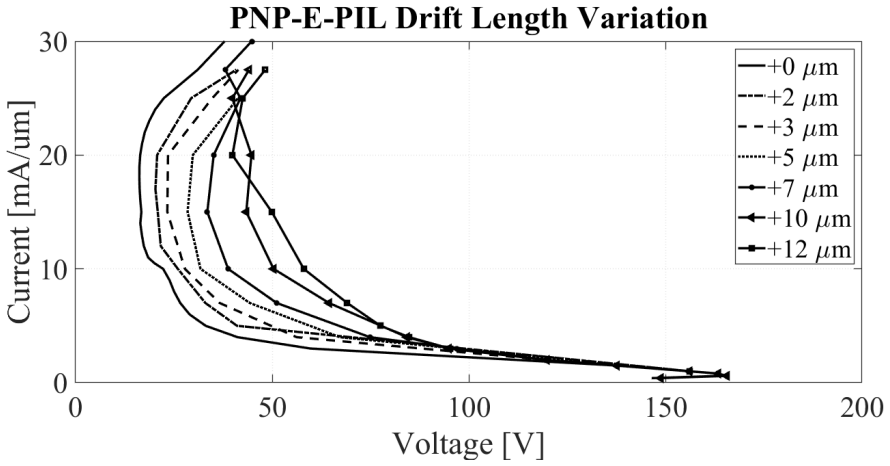

Figure 3.45: I-V characteristics for different drift lengths.

The trigger voltage V_{T1} remained practically constant, proving that the breakdown in this device is not related to the horizontal N-drift P-epi junction, which would have a dependence on the drift length, but to the vertical NBL- P-sub junction, which has a very weak dependence on the drift length, only related to the low increase of the resistive drop across the highly doped NBL layer.

Drift length	V_{T1}	V_H	I_{T2}
Original	164 V	16.2 V	30 mA/µm
+2 µm	164.9 V	20.3 V	27.5 mA/µm
+3 µm	165.1 V	23.5 V	27.5 mA/µm
+5 µm	165.3 V	28.5 V	25 mA/µm
+7 µm	165.5 V	33.5 V	30 mA/µm
+10 µm	165.6 V	43.4 V	27.5 mA/µm
+12 µm	165.8 V	39.3 V	27.5 mA/µm

Table 3.6: Extracted V_{T1}, V_H and I_{T2} for different drift lengths.

3.4.1. Holding voltage increase

As expected, a quasi-linear increment of the holding voltage is experienced. This is due to the extension of the high field region, as depicted at 15 mA/µm in Fig. 3.46, corresponding to an increase of the electrostatic potential, as visible in Fig. 3.47.

Nevertheless, the device with a drift length increase of +12 µm shows a V_H value lower than the device with a drift length increase of +10 µm.
The reason behind this variation in behavior can be understood from the plot of the hole density in at 20 mA/µm in Fig. 3.48.

It is possible to see the difference between the two devices: the +10 µm device behaves similarly to the original device, while the +12 µm device shows a important increase of the deep carriers injected from the N-well isolation region. This is due to an enhanced operation of the deep SCR structure, also visible from the boosted carrier injection from the VNPN on the source side.
As extensively explained in the previous sections, this corresponds to a drop of the voltage across the device.
To confirm the involvement of the NBL in the degradation of the holding voltage with respect to the drift length increase, a test device, shown in Fig. 3.49, in which both the N-well isolation and the NBL layer have been removed has been simulated. The second P^+ diffusion has been removed as well since it serves no purpose without the N-well isolation region and NBL.

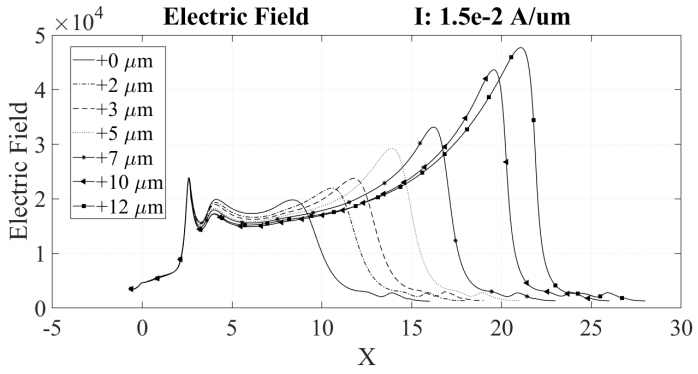

Figure 3.46: Electric field cutline plot at 15 mA/µm.

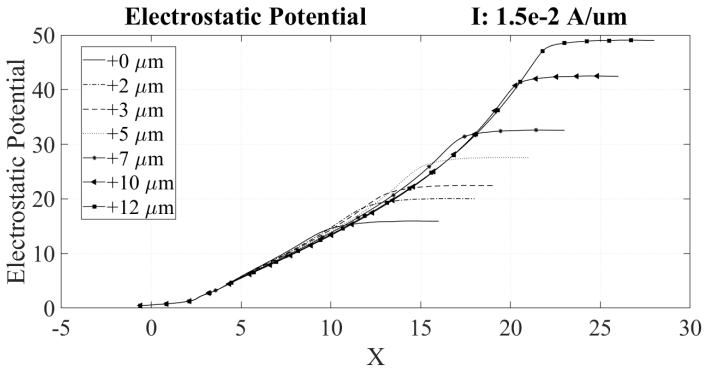

Figure 3.47: Electrostatic potential cutline plot at 15 mA/µm.

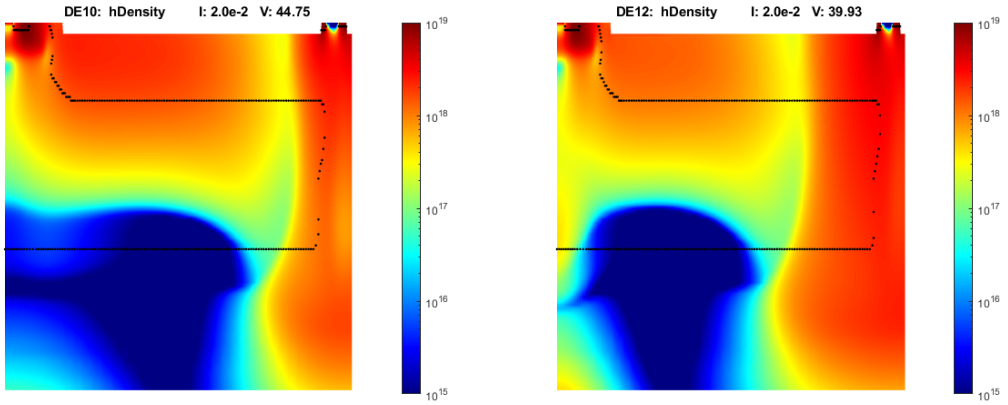

Figure 3.48: Hole density of the (left) +10 µm device and (right) +12 µm device at 20 mA/µm.

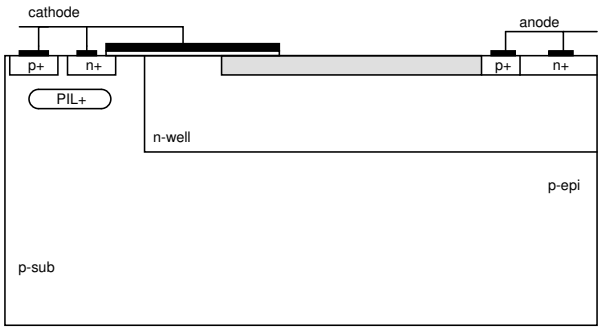

Figure 3.49: Structure of the PNP-E-PIL device without the NBL and N-well isolation regions.

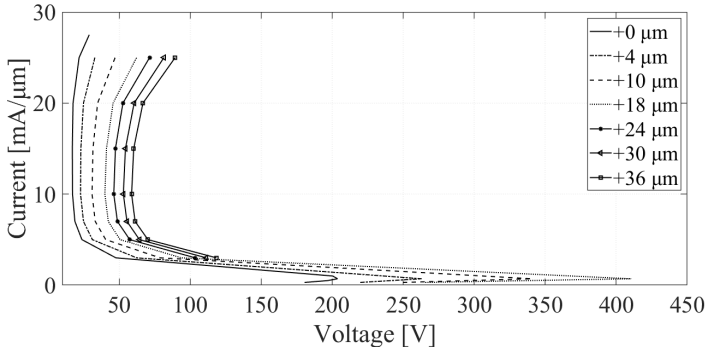

Figure 3.50: I-V characteristics for different drift lengths with no NBL and no N-well isolation regions.

The results are illustrated in Fig. 3.50. It is visible how the I-V characteristic of the device with the original drift length gets shifted by increasing the drift length, without any apparent distortion. This confirms the NBL layer, and thus the VNPN, as the source of degradation of V_H. However, Fig. 3.50 shows as well the reason why it is necessary to implement the NBL layer in the device: without the latter, the trigger voltage not only is higher than the original device, but also displays a strong dependence on the drift length. Without the vertical breakdown clipping the trigger voltage value, the device can reach V_{T1} values up to 400 V with a drift length increase of +18 µm.

3.4.2. Failure current

After analyzing the holding voltage variation, it is now possible to address how the failure current varies with respect to the drift length.
Indeed, Tab. 3.6 highlights how, from the device with the original drift length up to +5 µm, there is a decreases of the failure current. Successively, the +7 µm device exhibits instead an increase of I_{T2}, while +10 µm and +12 µm show once again a decrease.
The different behavior can be better analyzed by observing the plot of the maximum temperature for the different devices, depicted in Fig. 3.51.

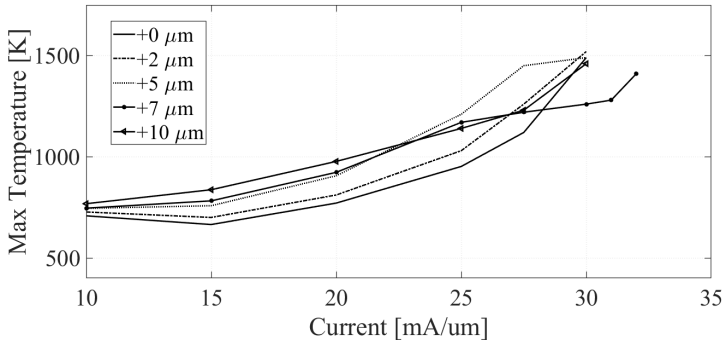

Figure 3.51: Maximum temperature for different drift lengths.

The maximum temperature trend demonstrates an initial steady increase, followed by a more pronounced rise, indicating the potential onset of thermal runaway. Analyzing the temperature trend from +0 µm to +5 µm reveals a consistent increase in maximum temperature across different current values. This can be attributed to the rise in joule heating, which results from the greater voltage across the device as the drift length increases.
Notably, the +7 µm device exhibits a change in slope at 25 mA/µm, which delays the onset of thermal runaway; however, this behavior is not observed in the +10 µm device.
Further understanding of this particular mechanism can be gained from analysis of the I-V characteristics, a magnification of which is shown in Fig. 3.52.

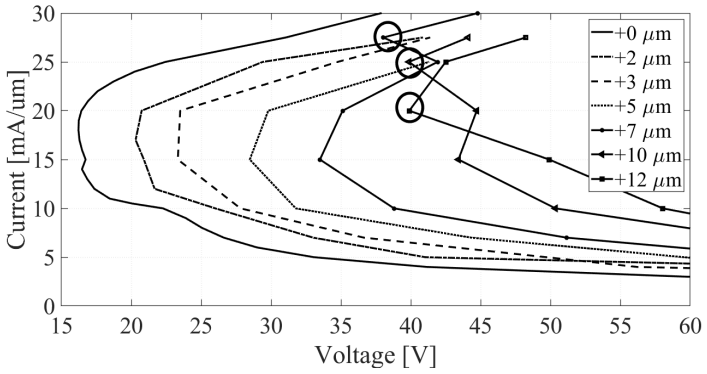

Figure 3.52: Enlargement of the I-V characteristics: highlight of the VNPN turn on.

The sudden change in slope evidenced by the circles can be attributed to the turning on of the VNPN which, as illustrated above, leads to a drop of the voltage.
From +0 µm to +5 µm there is no variation of the device behavior, thereby the failure current maintains the same trend. At +7 µm, the turn on of the VNPN enhance the deep conduction through the device, thus reducing the current flowing at the surface and hence postponing the failure point. The same happens to the +10 µm device, nevertheless a premature failure due to a localized hotspot in the NBL layer is experienced. In Fig. 3.53 the plot of the temperature at 25 mA/µm is shown. The +5 µm device fails due to overheating in the drift region, analogously to the original length device. The +10 µm device instead, displays the cited localized hotspot in the NBL which causes the premature failure.
The nature of this hotspot might be attributed to the electric field peak at the NBL - P-sub junction and the base pushout effect, which now affects this junction as well due to the strong activation of the VNPN .

Summarizing the results found in this section, this particular architecture allows to achieve a scalable holding voltage by changing the device drift length. Furthermore, this can lead to an increase of the failure current due to enhanced VNPN and deep SCR activation. Nevertheless, the NBL layer sets the limit to the holding voltage increase since an overly premature triggering of the deep SCR results in a holding voltage drop due to enhanced injection of carriers in the

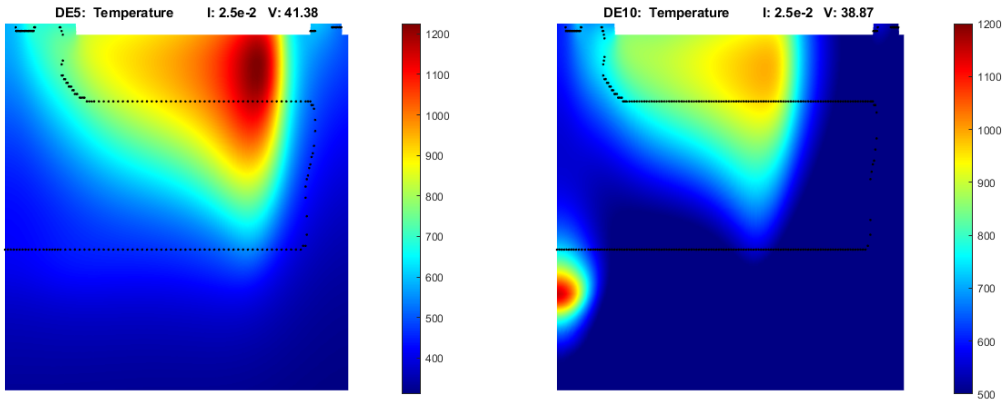

Figure 3.53: Temperature plot for the (left) +5 µm and (right) +10 µm.

depth of the device. The increase of the failure current with the drift length seems to have a limit as well due to the onset of base pushout at the NBL junction.

4. Evaluation of 3D Effects on SCR-LDMOS Devices

The last chapter focused on the 2D device optimization in order to achieve a high holding voltage. In this chapter, a further investigation of the three-dimensional effects on the device has been carried out.

The PNP-E-PIL device, with the original drift length as detailed in Sect. 3.4, has been uniformly extruded along the third direction, i.e., no modification of the structure along the width of the device has been performed. The device is depicted in Fig. 4.1.

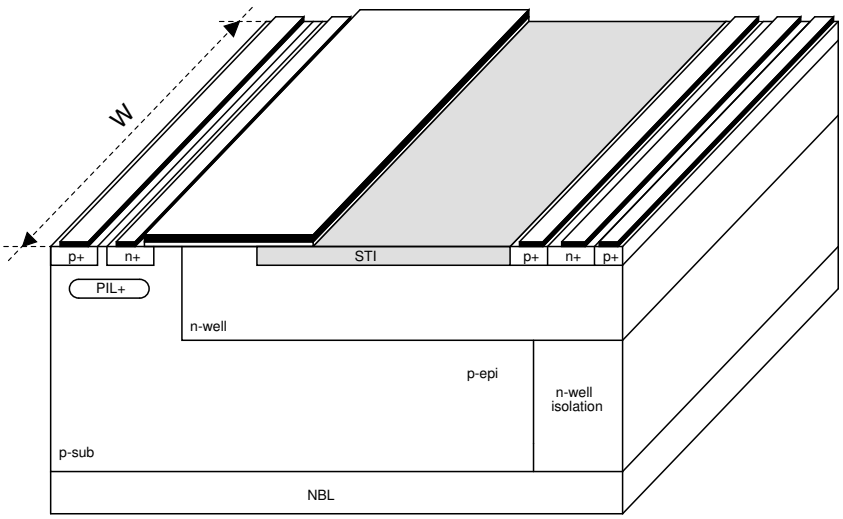

Figure 4.1: 3D structure of the PNP-E-PIL device.

The width (W) of the device has been varied. The obtained I-V characteristics are reported in Fig. 4.2.

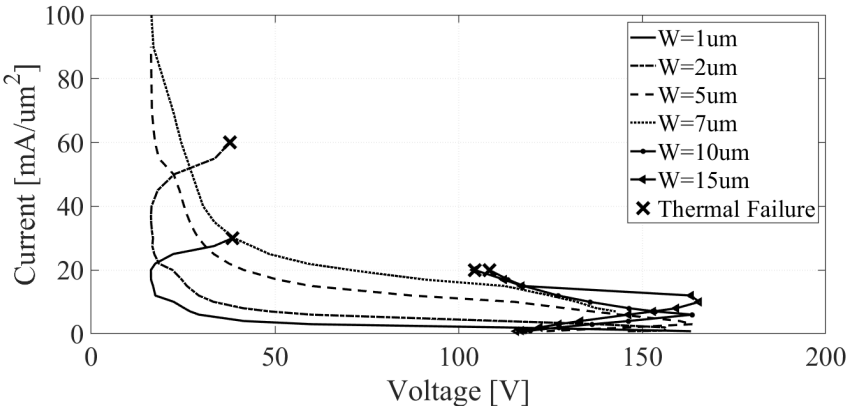

Figure 4.2: I-V characteristics for different width values.

In Fig. 4.3 the current has been normalized with respect to the width of the device.

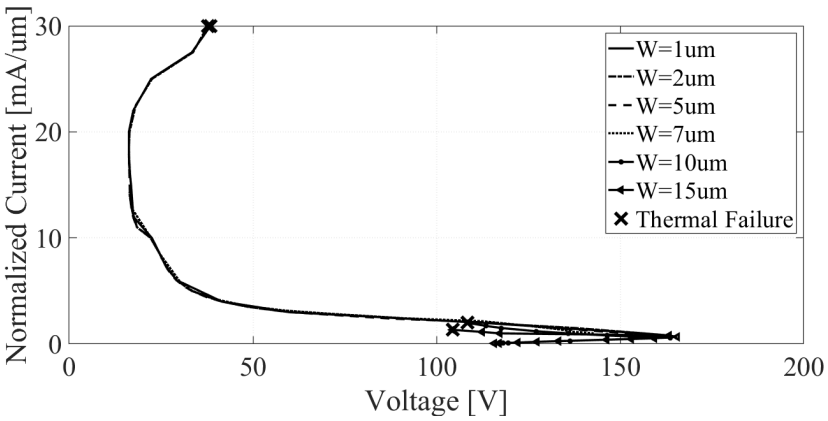

Figure 4.3: Normalized I-V characteristics for different width values.

4.1. Current filamentation

Up to 7 µm, the device shows no variation of the I-V characteristic, as visible from the normalized current plot. The same holding voltage is reached, and the same normalized failure current is experienced.

However, the devices with W = 10 µm and W = 15 µm present a premature failure during snapback.

The temperature plot is reported in Fig. 4.4.

Both devices present a hotspot near the NBL - P-sub junction on the source side. This is attributed to current filamentation, as already discussed in Sect. 2.7.2, which affects LDMOS devices.

The current filament can be seen in Fig. 4.5, in which it is evident how not all the width of the device is uniformly crossed by the anode current.

Some considerations are now given regarding the problem of current filamentation.

As already discussed, current filamentation is a limiting factor in LDMOS devices. It has been correlated to the high electric field peak given by the Kirk effect at the anode region. The smoothing of the doping profile of the N^+ diffusion on the anode has already been proposed to address this problem by suppressing the electric field at the junction. However, this solution can not be applied to this device. In fact, it can be applied only to a conventional SCR-LDMOS structure, i.e., with no NBL and N-well isolation regions. It has been already proved in the previous chapter that the device under study triggers through the breakdown of the NBL - P-sub region, which allows V_{T1} independent of the drift length. Therefore, the problematic junction for current filamentation is the above mentioned NBL - P-sub.

While modifications of the doping on the surface of the device can usually be done, the deeper regions, such as the NBL, require a much more careful approach. Indeed, the latter is optimized for Smart Power Technology and can't be modified unless an additional mask is used in the photolithography process, which is too expensive a solution to improve ESD performance alone.

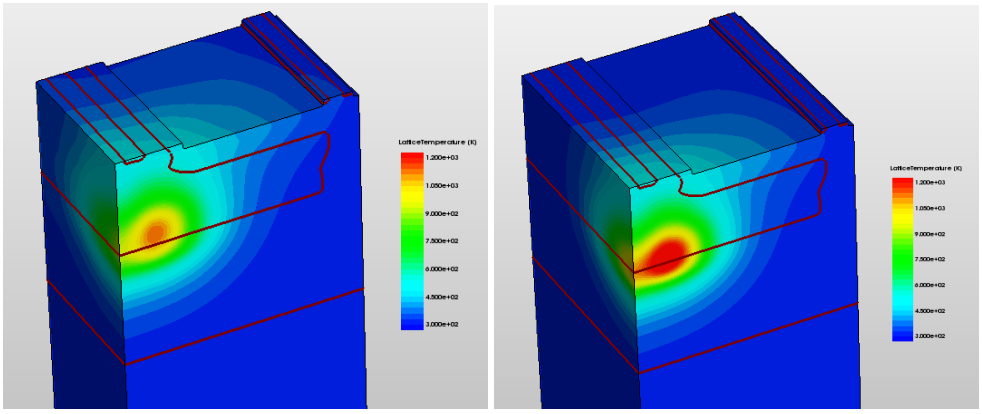

Figure 4.4: Temperature at failure for (left) W = 10 µm and (right) W = 15 µm.

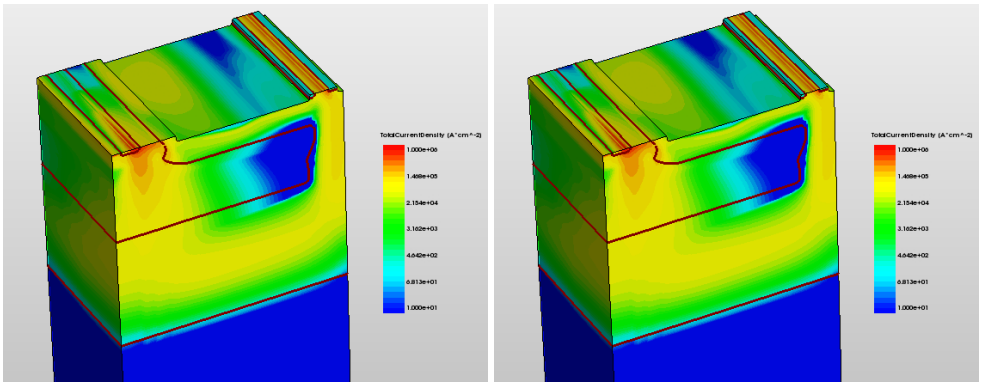

Figure 4.5: Total current density at failure for (left) W = 10 µm and (right) W = 15 µm.

The above considerations allows to understand why the modification of the doping profile of the NBL is not a suitable approach.
As a result, the onset of current filamentation of the embedded LDMOS in this particular device is of difficult solution.

4.2. Variation of the first P^+ diffusion length for increased robustness from current filamentation

Similarly to the LDMOS, SCR-LDMOS are susceptible to current filamentation, as these devices are inherently LDMOS prior to the activation of the parasitic SCR, and thus suffer from premature failure.
This effect in SCR-LDMOS can be avoided if the parasitic PNP BJT turns on before the onset of current filamentation in the embedded LDMOS structure.[83]
Therefore, a possible solution is to increase the length of the first P^+ diffusion, as shown in Fig.

[83] Nagothu Karmel Kranthi et al. "Physical insights into the low current ESD failure of LDMOS-SCR and its implication on power scalability". In: *2019 IEEE International Reliability Physics Symposium (IRPS)*. IEEE. 2019, pp. 1–5.

4.6, to increase the transistor gain.

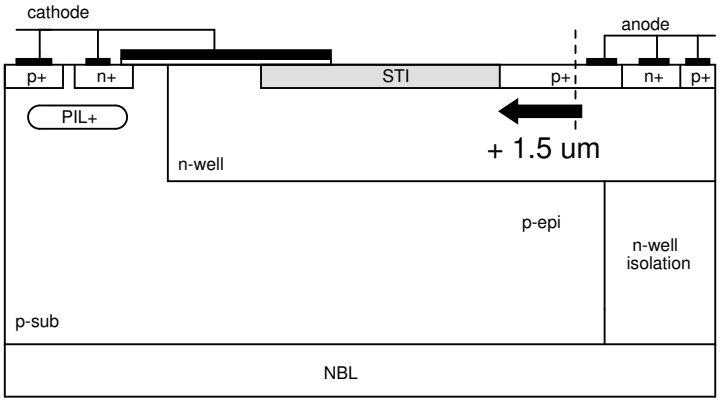

Figure 4.6: Modification of the first P^+ diffusion.

This leads to an enhanced gain of the parasitic PNP transistor due to the increased emitter area, therefore a earlier activation of the latter is expected.
The obtained normalized I-V characteristics for W = 1,10,15 µm are reported in Fig. 4.7.

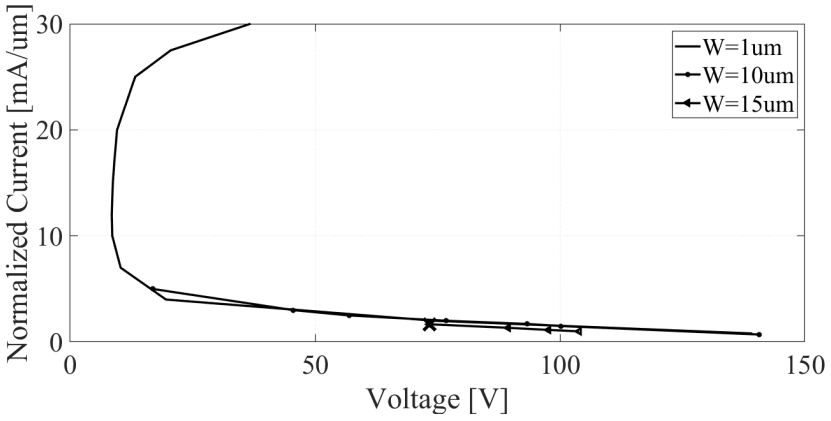

Figure 4.7: Normalized I-V characteristics.

As visible, the device now survives snapback at W = 10 µm, and the premature failure related to current filamentation has been postponed to W = 15 µm.

However, while this solution helps addressing the current filamentation problem, it also leads to a degradation of the holding voltage. The variation of the P^+ diffusion length has changed the holding voltage from 16 V to 8 V. This is obviously given by the increased carrier injection due to the enhanced PNP BJT gain.
Nevertheless, the reduction of the holding voltage can be addressed, as proposed in the last chapter, by increasing the drift length. However, this obviously has the side effect of increasing the area consumption of the device.

Conclusions

In the first part of this thesis, the reasons why SCR-LDMOS is a promising device for ESD protection despite its low holding voltage value were presented.
The experimental study carried out, showed that in the considered technology, the onset of high-level injection is the limiting factor to achieve a high holding voltage. Furthermore, it was shown how it is possible to exploit the NBL region as an additional current path to maintain a high failure current. Nevertheless, this particular architecture presents an additional parasitic SCR that deteriorates the holding voltage by increasing the injection of carriers into the device. In fact, the high-level injection regime leads to conductivity modulation that lowers the electric field, and thereby the electrostatic potential, along the device.
It is possible to suppress the gain of this structure and thus increase the holding voltage by increasing the doping concentration of the PIL layer, but this leads to a reduction in the failure current due to current crowding effects, which can be suppressed, however, by increasing the length of the N^+ diffusion in the source side. Nonetheless, this leads to a slight deterioration of the holding voltage due to the re-increased gain of the vertical NPN BJT forming the parasitic SCR.

Next, the increase of the drift region length was proposed to achieve a scalable holding voltage. Although this leads to an expected initial reduction of the failure current due to the increased joule heating, it was shown that for a certain value of drift length it is possible to exploit the breakdown of the vertical NPN BJT to increase the failure current again, providing a stronger deep conduction.
However, this mechanism has limitations: the increase in holding voltage is limited by the premature breakdown of the vertical NPN BJT, and similarly, the increase in failure current is limited by the overheating of the NBL- P-sub junction given by the high electric field.

Nevertheless, it was shown that it is possible to obtain a device with holding voltage up to 40 V with minimal degradation of the failure current.

Finally, 3D simulations have shown how this device is affected by premature failure due to onset of current filamentation at high width values. It was proved that increasing the gain of the parasitic PNP BJT can delay the onset of this effect at higher width values, this, nevertheless, leads to an important reduction of the holding voltage.

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