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Corso di Laurea Magistrale in
Ingegneria Elettronica

DESIGN OF A LOAD MODULATED BALANCED AMPLIFIER FOR SUB-6GHz 5G COMMUNICATIONS

Elaborato in

Lab of High Frequency Circuit Design M

Relatore

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Presentata da

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Abstract

L'oggetto della presente tesi consiste nell'analisi teorica, la progettazione e la verifica sperimentale di un Load Modulated Balanced Amplifier (LMBA). Si tratta di un amplificatore a radio frequenza il cui obiettivo è mantenere dei livelli di efficienza elevati anche quando la potenza di uscita assume valori più bassi del picco di 6-8 dB. Questo si ottiene attraverso l'introduzione di un segnale di controllo esterno nella porta normalmente isolata del coupler di uscita di un Balanced Amplifier.

Dopo una prima spiegazione teorica del funzionamento di un LMBA, la progettazione di tale amplificatore verrà affrontata in tre fasi: verrà illustrato il progetto di un semplice amplificatore costituito da un singolo transistor, successivamente sarà sviluppato in Balanced Amplifier (BA) e infine si otterrà un LMBA attraverso l'utilizzo di un segnale di controllo. Ciascun amplificatore è stato simulato attraverso il software ADS prima di essere realizzato sul substrato ROGERS RO4350.

L'intero studio presentato nel seguito è stato condotto presso la sede olandese della Gallium Semiconductor utilizzando i transistor GT010D progettati dalla azienda in tecnologia GaN on SiC.

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Introduction

RF Power Amplifiers (PA) are fundamental blocks for compensating the losses which overcome throughout the transmission in communication systems. Linearity and efficiency are highly required properties nowadays because of the distortion generated during the transmission and the high Peak-to-Average Power Ratio (PAPR) used for modulated signals in modern wireless systems. This value is defined as $PAPR = \frac{|x_{peak}|^2}{x_{rms}^2}$, for a given signal $x(t)$. Having an high PAPR means that the signal will be more likely to assume lower values than the peak, and this allows to avoid the distortion given by signal peaks compression and to improve the spectrum usage, but it leads to a bigger problem concerning PAs. Since the efficiency drops when the output power backs off, the efficiency will be low most of the time. One of the possible techniques to maximize efficiency is the dynamic load modulation, which is adopted by the recently introduced architecture of the Load Modulated Balanced Amplifier (LMBA) [3]. This new PA is based on a Balanced Amplifier's (BA) architecture, where a control signal is injected into the normally isolated port of the output coupler. The load impedances of the transistors can be modulated by changing the amplitude and the phase of the control signal in order to optimize the value when the amplifier goes into back off. This dinamic modulation allows to operate on a larger bandwidth than the one achievable when exploiting conventional passive networks such as in the Doherty PA.

The purpose of this thesis is to design an LMBA working on a 3.3 - 3.8 GHz bandwidth exploiting the 0.5um GaN on SiC GT010D transistor by Gallium Semiconductor. The theory of operation of LMBAs is presented in Chapter 1, then the design and the measurments' analysis are discussed in Chapters 2 and 3.

Chapter 1

Load Modulated Balanced Amplifier (LMBA)'s theory of operation

In this section the LMBA's working theory is analytically presented. After having briefly explained how the BA works, that is the basis to realise the LMBA, then the load modulation mechanism will be presented. A proof of concept simulation using simple networks and ideal components is displayed at the end of this chapter.

1.1 Balanced Amplifier (BA)

The Balanced Amplifier (Figure 1.1) is composed by a 3dB input quadrature hybrid coupler, two equal single-ended amplifiers working ninety degrees apart and a 3dB output quadrature combiner.

A quadrature coupler is a passive device with four ports: the input port (port 1), the output port (port 2), the coupled port (port 3) and the isolated port (port 4)[1]. It can be used both to divide or to combine the incident power. The term "3dB" refers to the ability of splitting in two equal parts the input signal at port 1.
When the coupler is used as a divider (input), an input signal is injected into the port one and it splits in two equal signals: one is in phase with the input signal (at port 2)[1] and it's called transmitted signal, and the other one is 90 degrees phase shifted (at port 3)[1], which is the coupled signal.
The output combiner is a reversed coupler, where the two signals to combine are injected

[1] the port numbers refer to Figure 1.1

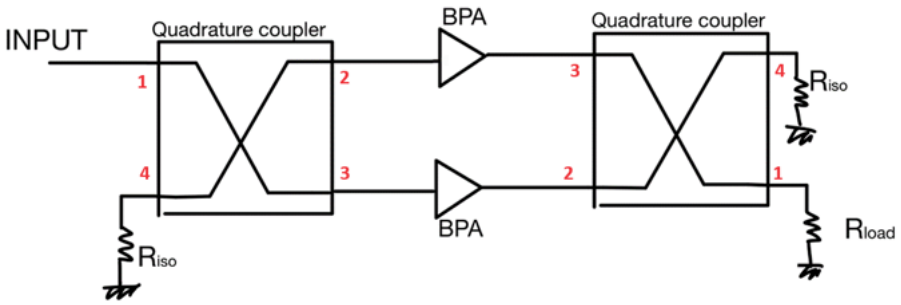


Figure 1.1: Balanced Amplifier's scheme

into the output port and the coupled port. Precisely, the signal which was previously phase shifted by 90 degrees is now injected into port 2 and the other signal, which was in phase with the primary input signal, is injected in port 3. The overall output signal can be measured at the port 1 of the output coupler used as a combiner, whereas the isolated port (4) is connected to a 50 Ω resistance R_{iso}. In the end, the signal entering in port 2 doesn't get further phase shifted at port 1, so it appears with a 90 degrees phase shift with respect to the primary input signal. The signal entering in port 3 gets phase shifted by 90 degrees at port 1 instead, so the two signals have the same phase and are summed together. The signal entering in port 2 is phase shifted again by 90 degrees when showing at port 4, for a total of 180 degrees shift, whereas the signal entering in port 3 is kept to 0 degrees phase. The two signal are canceled at port 4, as a result.

As described above, the input quadrature coupler allows to equally split the signal in two parts with a ninety degrees phase shift. Each half of the input signal is injected into one of the two amplifiers located in the two branches. These amplifiers are identical, so they will have the same reflection coefficient. The reflected signals will recombine at the input and the isolated ports with ninety degrees rotation. As a result, the two signals are subtracted at the input port and summed at the isolated port of the input coupler, in a similar way to what happens on R_{iso} and R_{load} at the output. Since the reflection coefficients are equal, the two signals cancel each other at the input port of the amplifier, whereas the resulting signal is doubled at the isolated port. The isolated port is normally terminated with a load that matches the input impedance of the coupler, meaning 50 Ω, so that the resulting signal at the isolated port isn't reflected back towards the coupler. This is the reason why couplers are often used to protect circuits against reflected waves.

The output quadrature coupler allows to recombine the output signals coming from the two amplifiers. Thanks to the ninety degrees phase shift, the two signals are canceled

at the isolated port and added at the output port.

The Balanced Amplifier is able to sum the output powers of two equal single transistor amplifiers with the same gain and efficiency of the single branches, so the maximum output power is doubled if it is compared with the single branch's saturated power. Also the input power corresponding to saturation needs to be doubled; each amplifier receives half of the input power due to the input quadrature coupler which divides the input power in two equal parts.

1.2 Load Modulation

Starting from the BA architecture, the LMBA can be obtained by introducing a control signal allowing the load modulation: the load seen by each transistor can be modulated thanks to the injection of a control signal into the normally isolated port of the output coupler (Figure 1.2, where CSP is the Control Signal Power amplifier), as explained next [3].

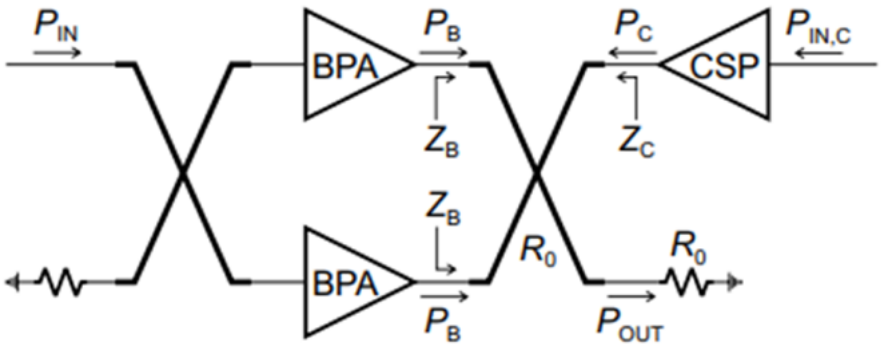


Figure 1.2: LMBA's scheme

Let's consider the output currents coming from each of the BPA amplifiers as $I_1 = I_b$ and $I_2 = -jI_b$, the control signal's current as $I_3 = jI_c e^{j\phi}$, and the voltage at the output port as $V_4 = -R_0 I_4$.

The Z - matrix of the output coupler is the following [5]:

$$\begin{bmatrix} V_1 \\ V_2 \\ V_3 \\ V_4 \end{bmatrix} = Z_0 \begin{bmatrix} 0 & j & -j\sqrt{2} & 0 \\ j & 0 & 0 & -j\sqrt{2} \\ -j\sqrt{2} & 0 & 0 & j \\ 0 & -j\sqrt{2} & j & 0 \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \\ I_3 \\ I_4 \end{bmatrix} \tag{1.1}$$

Solving the consequent system of equation 1.2, the impedance's value seen by the two main amplifiers constituting the BA's scheme can be calculated.

$$\begin{cases} V_1 = (jI_2 - j\sqrt{2}I_3)Z_0 \\ V_2 = (jI_1 - j\sqrt{2}I_4)Z_0 \\ V_3 = (jI_4 - j\sqrt{2}I_1)Z_0 \\ V_4 = (jI_3 - j\sqrt{2}I_2)Z_0 \end{cases} . \tag{1.2}$$

The following equations are obtained:

$$Z_1 = \frac{V_1}{I_1} = Z_0 \frac{jI_2 - j\sqrt{2}I_3}{I_b} = Z_0 \frac{I_b + \sqrt{2}I_c e^{j\phi}}{I_b} = Z_0 \left(1 + \frac{\sqrt{2}I_c e^{j\phi}}{I_b}\right) \tag{1.3}$$

Analogously:

$$Z_2 = \frac{V_2}{I_2} = Z_0 \left(1 + \frac{\sqrt{2}I_c e^{j\phi}}{I_b}\right) \tag{1.4}$$

Equations 1.3 and 1.4 show how the control signal $jI_c e^{j\phi}$ manages to change the load seen by each BPA, that is the load seen by the transistors constituting those main amplifiers [8]. Notice that the modulation is the same for both the transistors' load [6]. By tuning the amplitude and the phase of the control signal, it is possible to make the transistors see the optimum load maximizing efficiency for every power level and every frequency.

Precisely, the obtained load modulation depends on the ratio between the control signal and the output signal coming from one of the two main transistors, as expressed in 1.3 and 1.4; it doesn't depend on the absolute value of the control signal. It is hence convenient to define the P_{rel} quantity as the ratio between the control signal power and the main amplifier BPA's output power [3].

$$P_{rel} = \frac{P_{ControlSignal}}{P_{main}} = \frac{\frac{1}{2}Z_0|I_c|^2}{\frac{1}{2}Z_1|I_1|^2} = \frac{Z_0}{Z_1}\frac{|I_c|^2}{|I_b|^2} \tag{1.5}$$

$$\begin{aligned}
&\frac{Z_1}{Z_0} = \frac{Z_0\left(1+\frac{\sqrt{2}I_c e^{j\phi}}{I_b}\right)}{Z_0} = 1 + \frac{\sqrt{2}I_c e^{j\phi}}{I_b} \\
&\frac{1}{\sqrt{2}}\left(\frac{Z_1}{Z_0} - 1\right) = \frac{I_c e^{j\phi}}{I_b} \\
&\left|\frac{I_c}{I_b}e^{j\phi}\right|^2 = \left|\frac{I_c}{I_b}\right|^2 = \left|\frac{1}{\sqrt{2}}\left(\frac{Z_1}{Z_0} - 1\right)\right|^2 = \frac{1}{2}\left|\frac{Z_1}{Z_0} - 1\right|^2
\end{aligned} \tag{1.6}$$

$$P_{rel} = \frac{Z_0}{Z_1}\frac{1}{2}\left|\frac{Z_1}{Z_0} - 1\right|^2 = \frac{\left|\frac{Z_1}{Z_0} - 1\right|^2}{2Re\{\frac{Z_1}{Z_0}\}} \tag{1.7}$$

The reflection coefficient seen by each main transistors can be expressed in terms of P_{rel} (equations 1.10 and 1.11):

$$\Gamma_1 = \frac{\frac{Z_1}{Z_0} - 1}{\frac{Z_1}{Z_0} + 1} \tag{1.8}$$

$$\begin{aligned}
&|\Gamma_1|^2 = \frac{\left|\frac{Z_1}{Z_0} - 1\right|^2}{\left|\frac{Z_1}{Z_0} + 1\right|^2} = \frac{2P_{rel}Re\{\frac{Z_1}{Z_0}\}}{\left|\frac{Z_1}{Z_0} + 1\right|^2} \\
&\left|\frac{Z_1}{Z_0} + 1\right|^2 = \left|\frac{Z_1}{Z_0} - 1 + 2\right|^2 = \left|\frac{Z_1}{Z_0} - 1\right|^2 + 4 + 4\left|\frac{Z_1}{Z_0} - 1\right|
\end{aligned} \tag{1.9}$$

$$|\Gamma_1|^2 = \frac{P_{rel}}{\frac{\left|\frac{Z_1}{Z_0}-1\right|^2}{2Re\{\frac{Z_1}{Z_0}\}} + \frac{4\left(1+\left|\frac{Z_1}{Z_0}-1\right|\right)}{2Re\{\frac{Z_1}{Z_0}\}}} = \frac{P_{rel}}{P_{rel} + \frac{4Re\{\frac{Z_1}{Z_0}\}}{2Re\{\frac{Z_1}{Z_0}\}}}$$

$$|\Gamma_1|^2 = \frac{P_{rel}}{P_{rel} + 2} \tag{1.10}$$

Analogously:

$$|\Gamma_2|^2 = \frac{\frac{Z_2}{Z_0} - 1}{\frac{Z_2}{Z_0} + 1} = \frac{P_{rel}}{P_{rel} + 2} \tag{1.11}$$

When changing the amplitude of the control signal, and P_{rel} as a consequence, and the phase, the reflection coefficient corresponding to the load impedance seen by each main

amplifier, creates circular contours on the Smith Chart, as expressed by equations 1.10 and 1.11 and depicted in Figure 1.3. The center of those contours is the reflection coefficient seen when no control signal is applied, corresponding to the Balanced Amplifier case. The radius of the contours depends on the amplitude of the control signal, whereas the phase makes the reflection coefficient rotate by following the circular trajectory. A significant portion of the Smith Chart can be covered by using this technique.

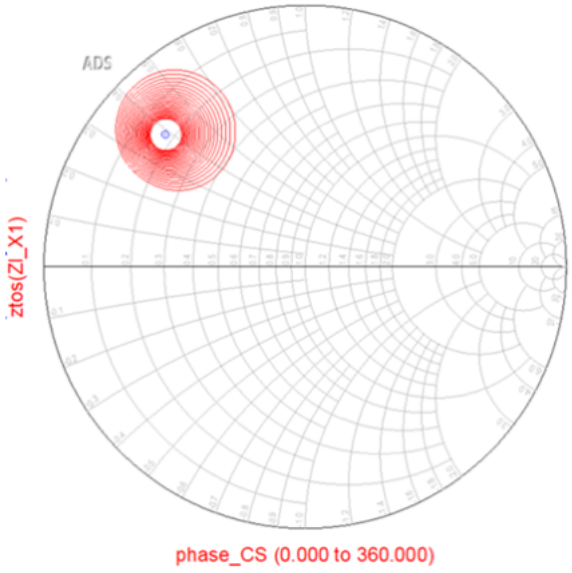


Figure 1.3: Load reflection coefficient's circular contours

Another important characteristic of LMBAs is that the control signal power is always completely recovered at the output port of the amplifier [3] if the couplers are lossless, as showed below by exploiting 1.2 and 1.3.
Power at the output port of the LMBA:

$$P_4 = \frac{1}{2}Re\{I_4^* V_4\} = Z_0 \left(|I_b|^2 + \frac{1}{2}|I_c|^2 + \sqrt{2}|I_b||I_c| sen\phi \right) \tag{1.12}$$

Output power of one of the main amplifiers in the two main branches of the LMBA:

$$P_{main} = \frac{1}{2}|I_1|^2 Re\{Z_1\} = \frac{1}{2}Z_0 \left(|I_b|^2 + \sqrt{2}|I_c||I_b| sen\phi \right) \tag{1.13}$$

The control signal power is

$$P_{ControlSignal} = \frac{1}{2}Z_0|I_c|^2 \tag{1.14}$$

By considering 1.13 and 1.14, the output power equation 1.12 can be re-written as

$$P_4 = 2P_{main} + P_{ControlSignal} \tag{1.15}$$

The additional power needed to generate the control signal hence isn't lost, but it's always added to the output power and it contributes positively; then the LMBA's total output power will be greater than the Balanced Amplifier's one.

1.3 Proof of concept

In order to verify the theoretical mechanism explained in the previous section, some simple and ideal schematics have been simulated, by starting with a Single Transistor Amplifier, then a Balanced Amplifier and the LMBA in the end.

1.3.1 Single Transistor Amplifier

The schematic in Figure 1.4 depicts a Power Amplifier composed by one transistor biased in class AB with a 16 mA drain quiescent current, the stabilization network, input and output matching networks and ideal DC blocks and DC feeds for biasing. This represents the basic block needed for realizing the BA and the LMBA.
The 16 mA quiescent current is obtained by biasing the transistor with 2.5 V at the gate and 28 V at the drain.

The stabilization network is composed by a 73 Ω resistor and a 2.5 pF capacitor in order to stabilize the amplifier at the lower frequencies and obtain an unconditionally stable circuit. Figures 1.5 and 1.6 show some stability indexes such as the Stability Factor, μ and μ', together with Max Gain, before and after having added the stabilization network respectively. After having stabilized the transistor, the gain has been reduced in order to have a Stability Factor always greater than one, especially at lower frequencies where the initial circuit was unstable.

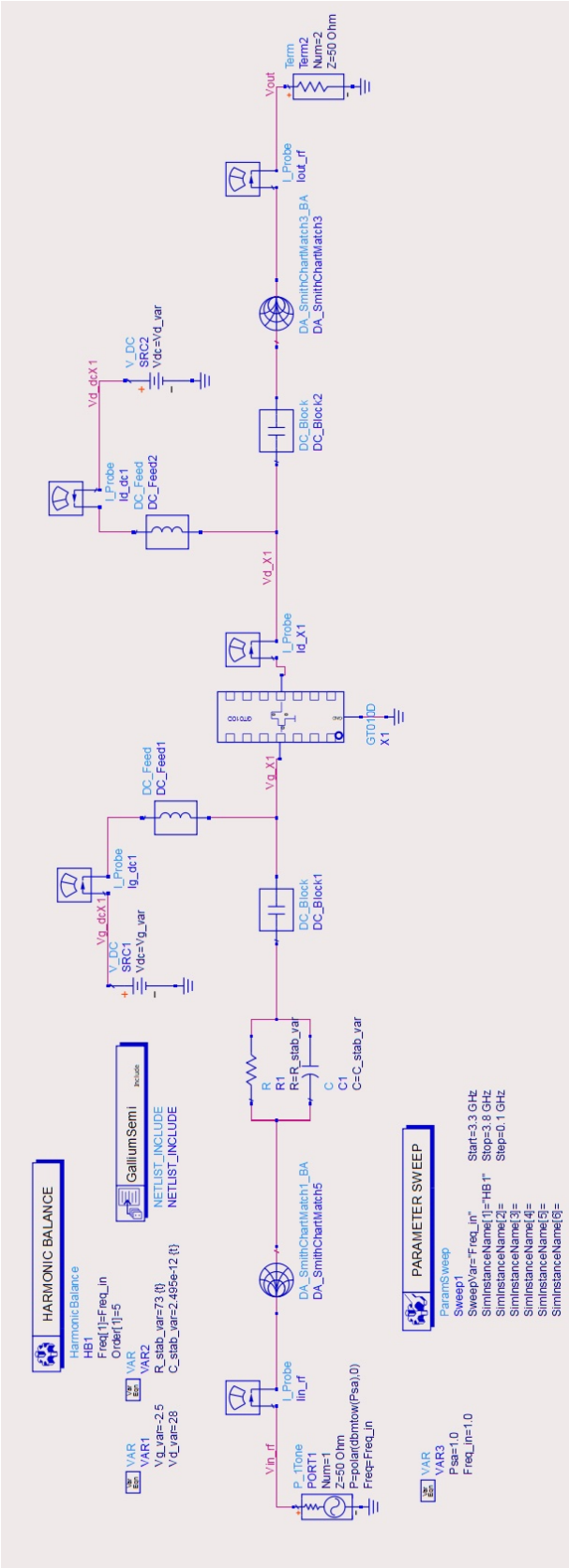


Figure 1.4: Simple single transistor schematic for a proof of concept simulation

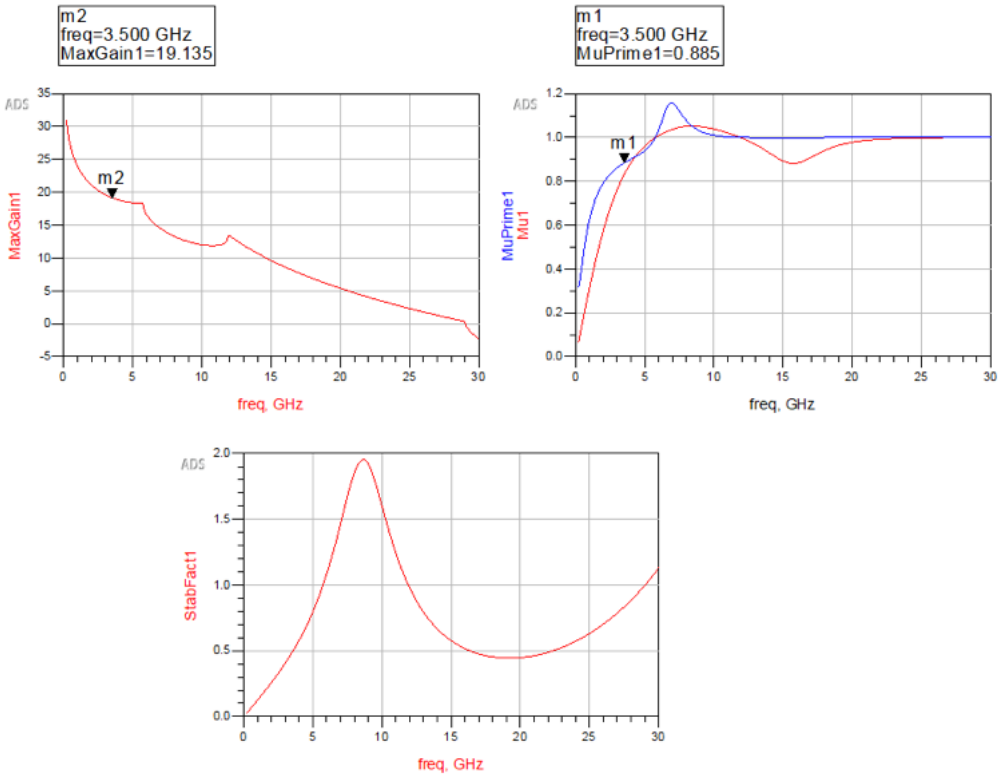


Figure 1.5: Stability analysis without stabilization network

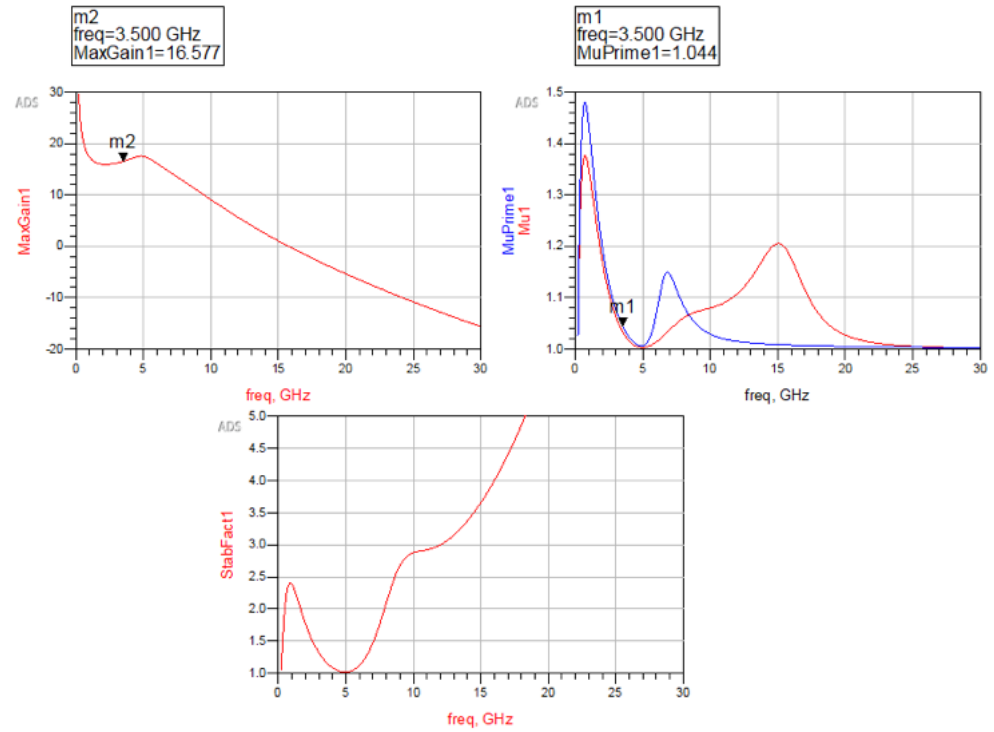


Figure 1.6: Stability analysis with stabilization network

The Output Matching Network (OMN) of this single transistor amplifier has been created for transforming the load 50 Ω impedance into $8.7 + j18.9$, which maximizes the efficiency when the output power is saturated. This value can be found through a Load Pull simulation, whose results are shown in Figure 1.7.

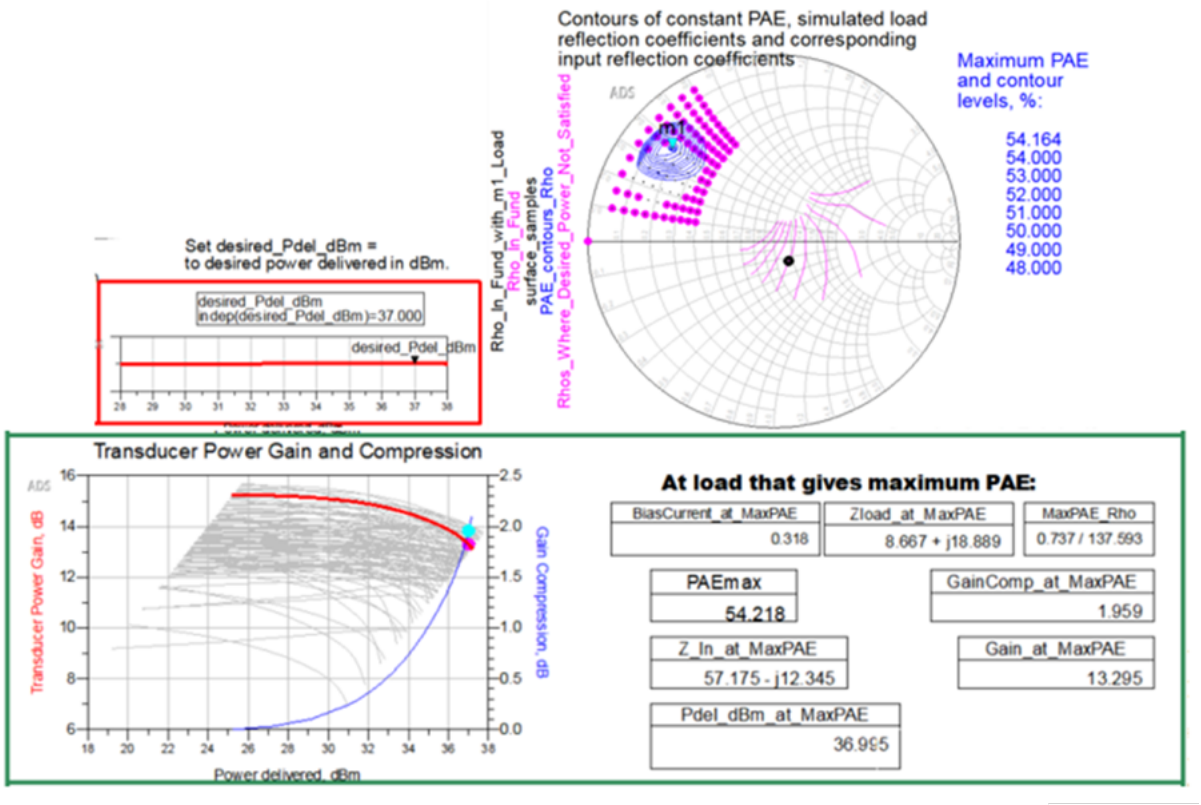


Figure 1.7: Load Pull simulation results for the single transistor

The Load Pull simulation consists on sweeping the load impedance presented to the transistor (i.e. GT010D by Gallium Semiconductor) and measuring the performances for each value. Contours are then created on the Smith Chart pointing out the impedance's values corresponding to different levels of efficiency: the center of the contours corresponds to the one providing maximum efficiency and each contour corresponds to a different efficiency value. The further the contour is from the center, the less is the efficiency. The same contours are created by referring to the output power and the gain. The blue contours in Figure 1.7 corresponds to the efficiency ones.

The Smith Chart Utility tool in ADS has been used for this simple proof of concept to realize the Output Matching Network in order to better monitor how each component acts. Figure 1.8 shows the ADS tool window, where the impedances at each section of the network have been highlighted. The magnitude of the S_{11} S-Paramenter of the OMN is

also shown at the top right of Figure 1.8. Its very low value in the bandwidth of interest suggests good matching, especially at the central frequency (3.55 GHz).

The resulting network is represented in Figure 1.9

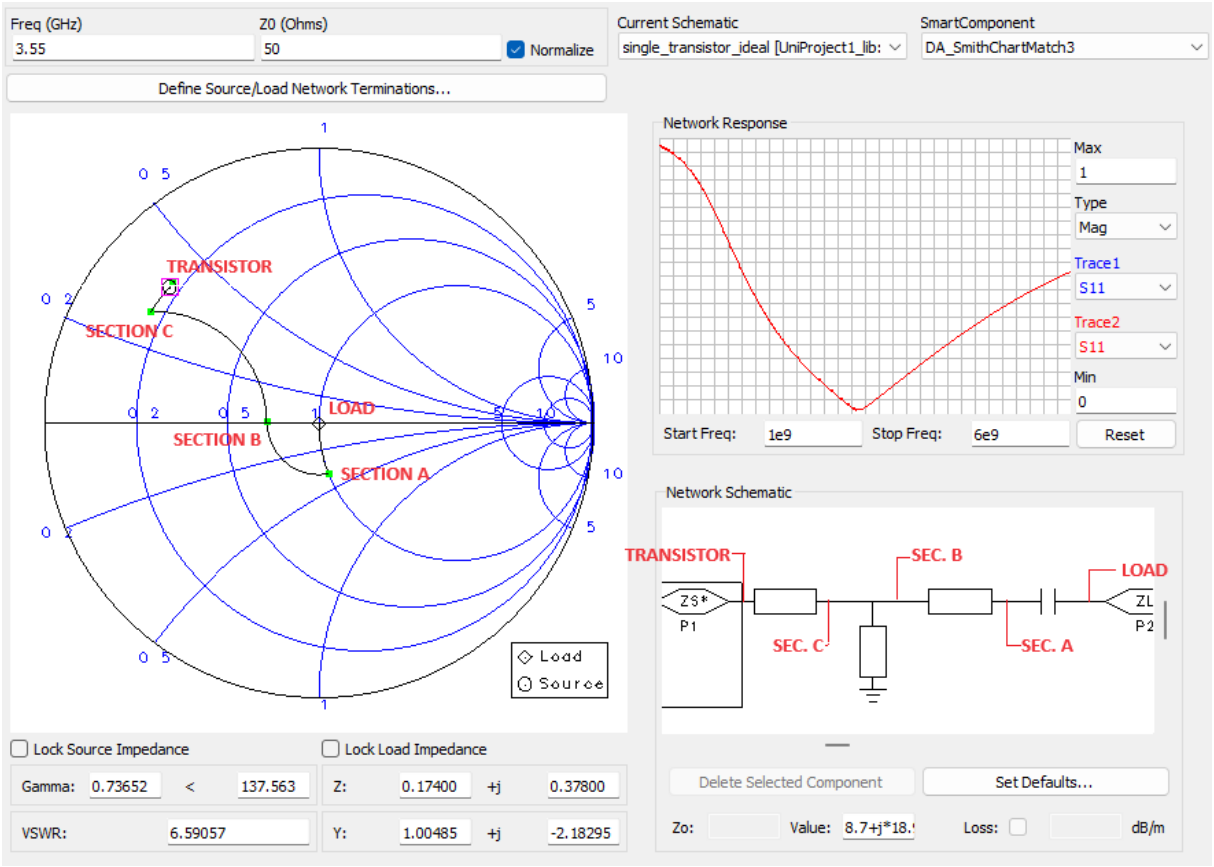


Figure 1.8: Ideal Output Matching Network action

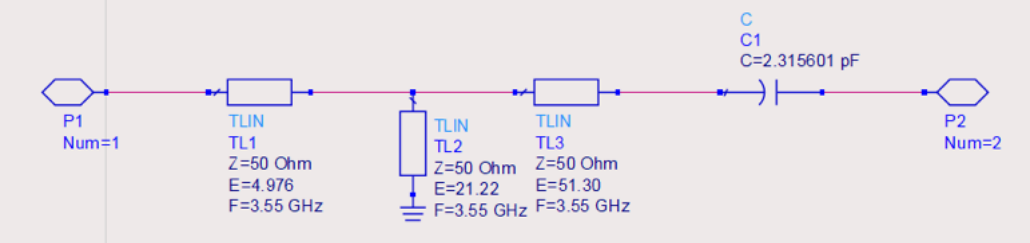


Figure 1.9: Ideal Output Matching Network - Proof of concept version

A simple version of the Input Matching Network (IMN) is designed by exploiting the same ADS tool used for the OMN. The IMN has to transform the 50 Ω impedance of the signal source into the impedance by providing conjugate impedance matching at the gate port of the transistor, in order to optimize the power transfer at the input of the amplifier. An S-Parameters simulation of the amplifier schematic without any IMN has

been performed in order to find the proper value for the conjugate matching. Figure 1.10 shows the resulting input reflection coefficient and the corresponding impedance value, that is $6.24 - j8.044$ at 3.55 GHz. The IMN has to show to the transistor an $6.24 + j8.044$ impedance in order to obtain the conjugate impedance matching.

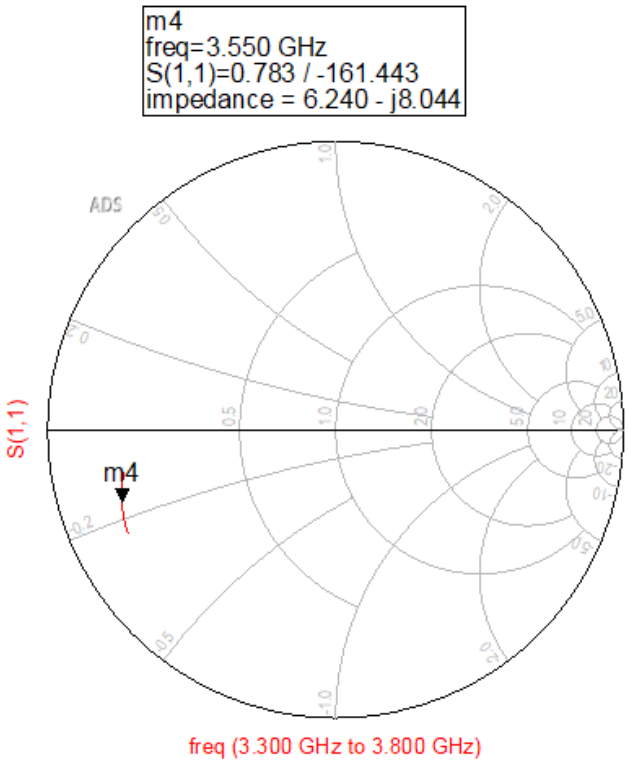


Figure 1.10: S_{11} of the single transistor amplifier missing the Input Matching Network

Figure 1.11 shows the creation of the Input Matching Network and Figure 1.12 the result.

By performing an S-Parameters simulation of the same schematic represented in Figure 1.4, the impedance transformations can be verified: Figure 1.13 shows the magnitude of the gain S(2,1) and the input reflection coefficient S(1,1). S(1,1) has a very low value, which means that the input matches the 50 Ω resistance of the signal source. S(2,1) value is between 14.9 dB and 15.9 dB in the band, which is close to the maximum value achievable of 16.6 dB determined during the stability analysis (Figure 1.6).

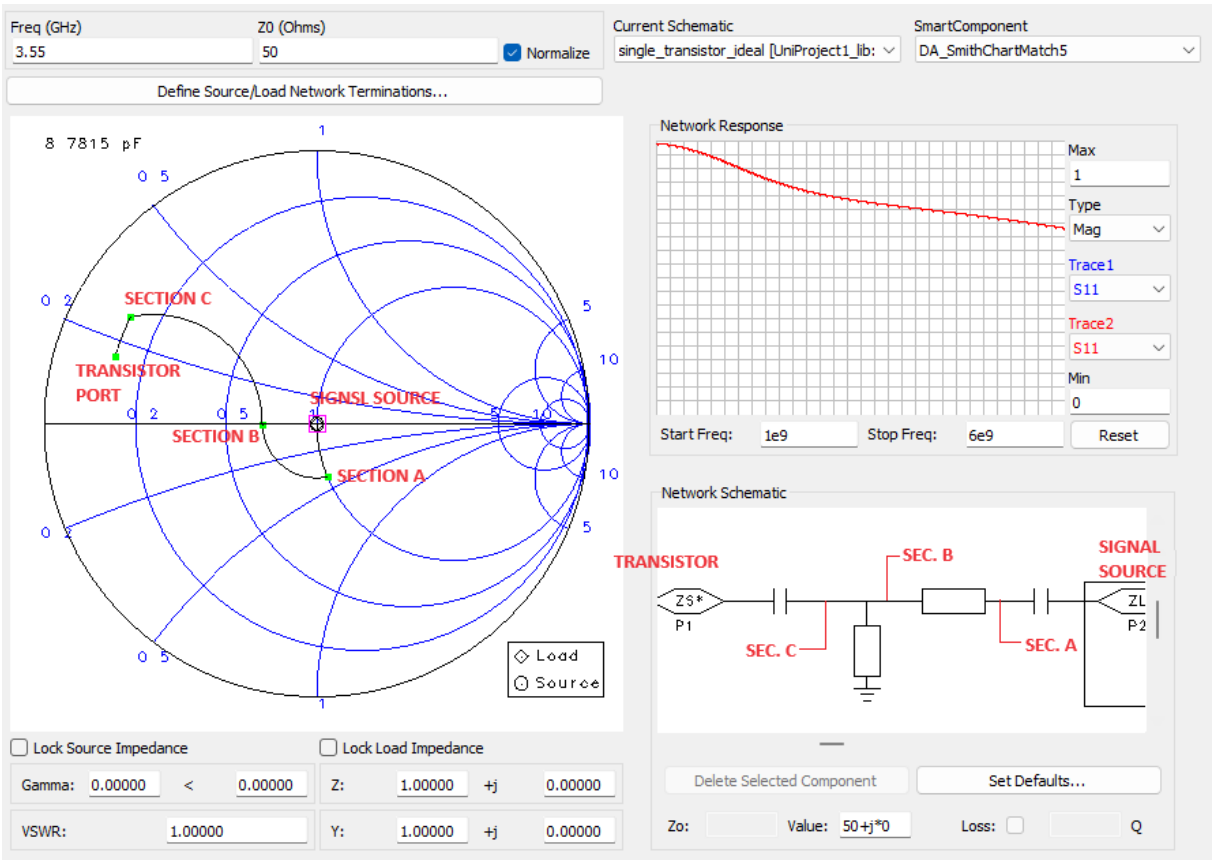


Figure 1.11: Ideal Input Matching Network action

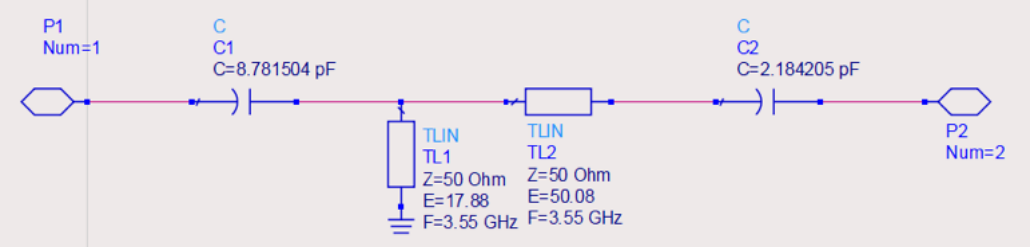


Figure 1.12: Ideal Input Matching Network - Proof of concept version

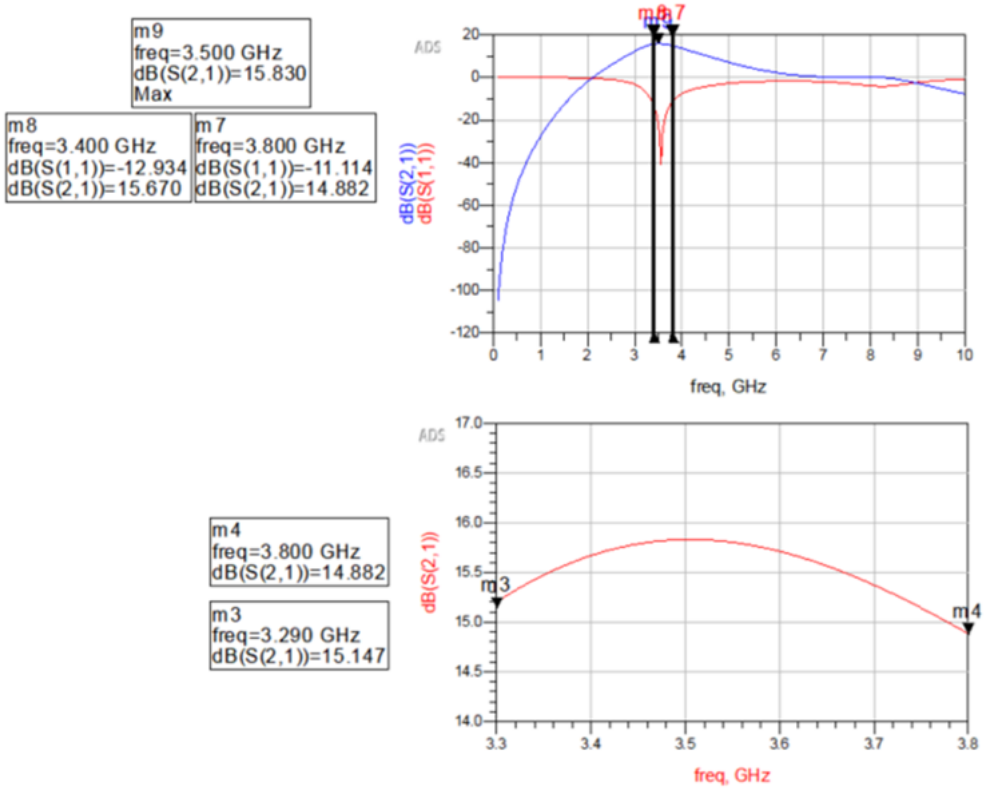


Figure 1.13: Scattering Parameters simulation of the Single Transistor Amplifier - proof of the good matching

By simulating for different frequencies the schematic explained right above and shown in Figure 1.4, the performances in Figure 1.14 are obtained: the saturated output power is 37 dBm, the average maximum efficiency in the band of interest is 55% and the average small signal gain is 14.5 dB. These performances coincide with what was expected from the Load Pull simulation (Figure 1.7).

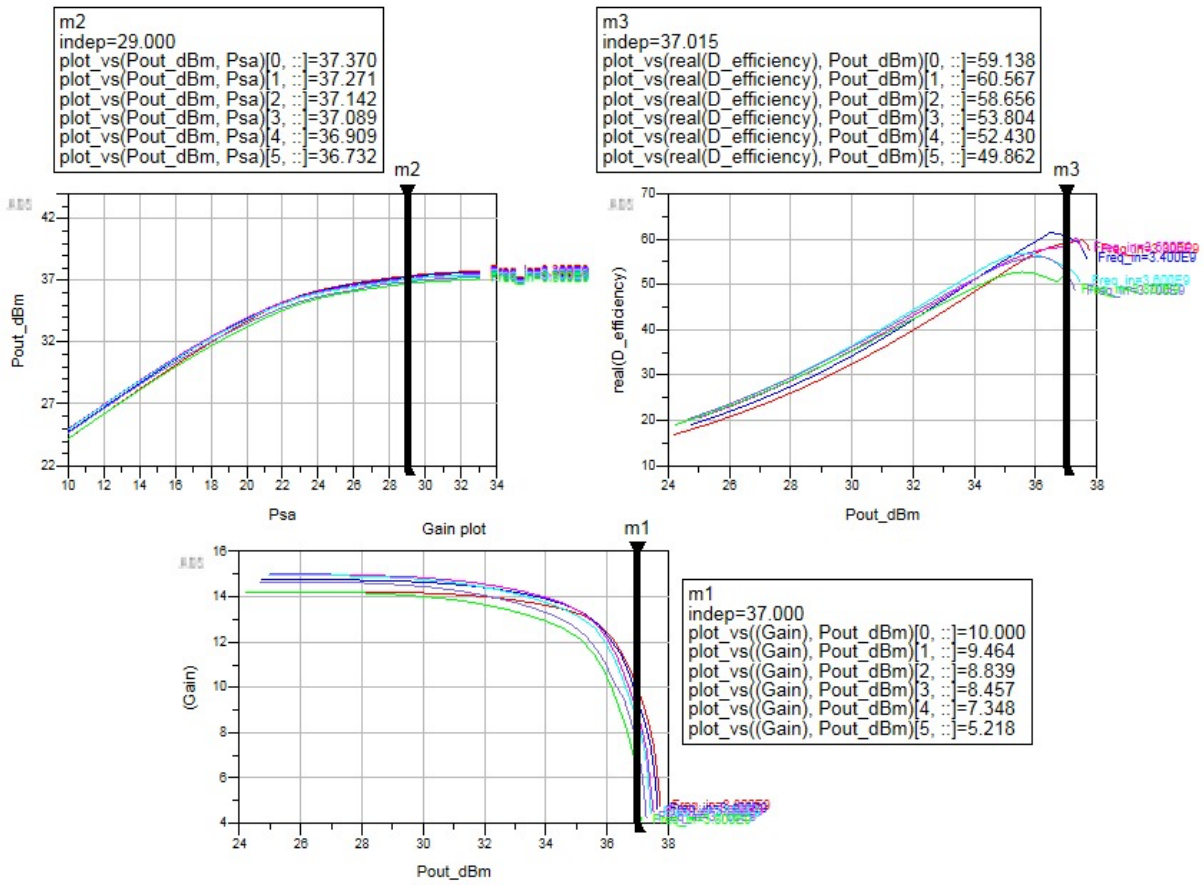


Figure 1.14: Single transistor amplifier performances - proof of concept version

1.3.2 Balanced Amplifier (BA)

The Balanced Amplifier is obtained doubling the single transistor schematic in Figure 1.4 and adding the input and output couplers, as shown in Figure 1.15. The couplers used are ideal in this proof of concept simulation, just like all the other components, and they show a 50 Ω input impedance, so the isolated port is closed on 50 Ω to avoid reflected waves. Figure 1.16 shows the ideal BA performances: it allows to obtain 40 dBm output power, that means it's doubled with respect to the Single Transistor Amplifier, 55% efficiency and 14.5 dB average small signal gain, just like the single transistor case, as expected.

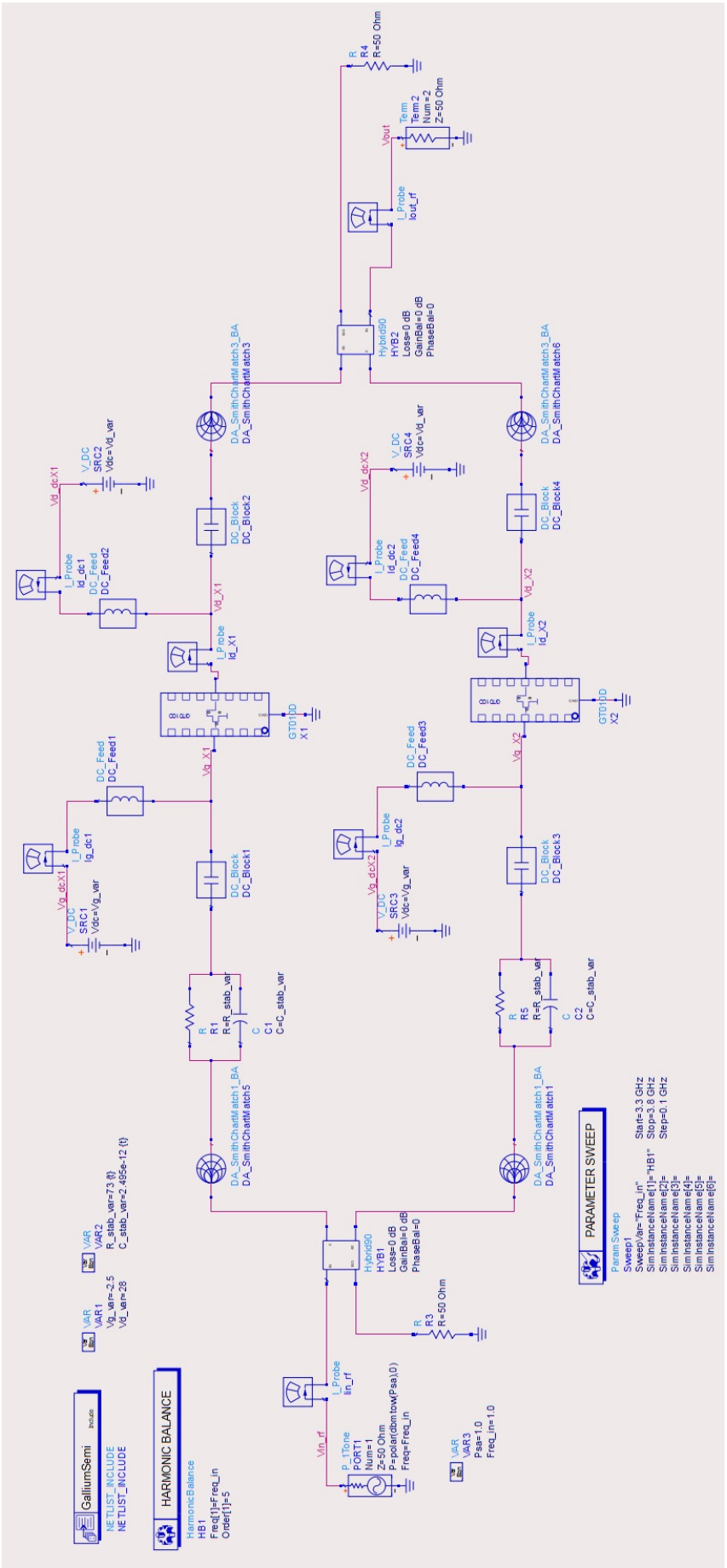


Figure 1.15: Balanced Amplifier schematic for proof of concept simulation

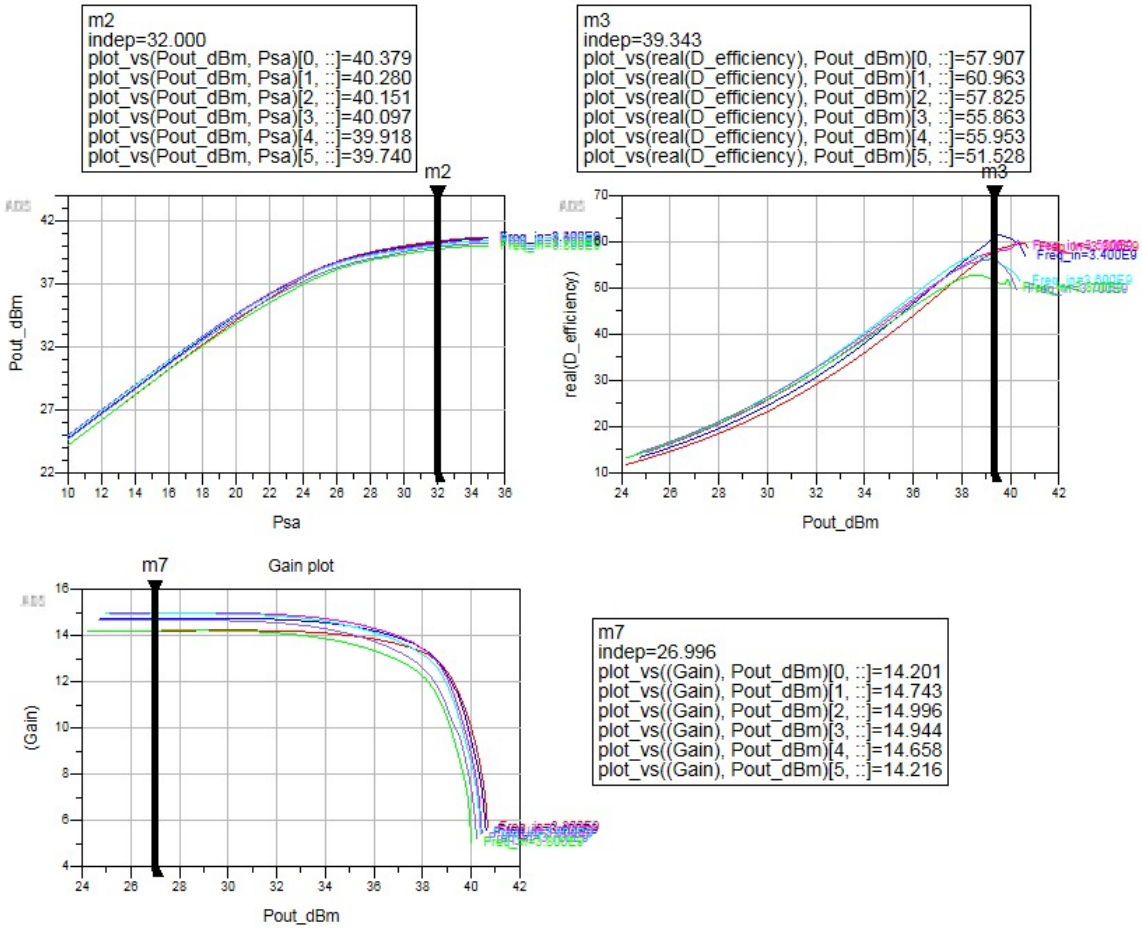


Figure 1.16: Balanced Amplifier performances - proof of concept version

1.3.3 Two inputs LMBA

By starting from the schematic in Figure 1.15 and injecting a control signal into the normally isolated port of output coupler, the LMBA is obtained. Making the two transistors see the optimum load in order to maximize the efficiency is the aim of this amplifier, as already mentioned. Those values for the load impedances are found by performing the load pull simulations again, but by considering also the IMN and the stabilization networks, which are known at this stage (Figure 1.17) and are shown in Figures 1.12 and 1.4 respectively. The simulation must be repeated for different frequencies belonging to the bandwidth of interest (3.3 - 3.8 GHz) and also for different input power levels. This second sweep is needed because the aim of the LMBA is to improve efficiency when the output power is backed-off.

The resulting impedances are collected in Table 1.1.

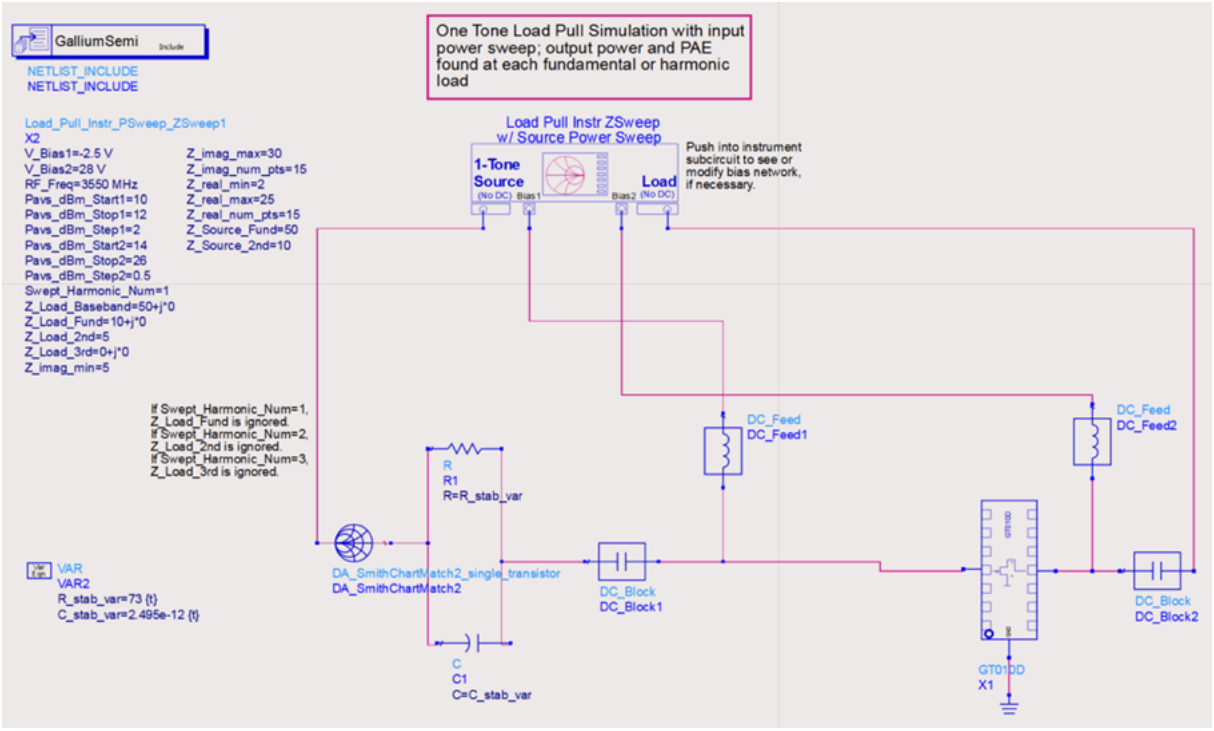


Figure 1.17: Load Pull simation schematic - proof of concept case

Figure 1.18 depicts the optimum impedances on the Smith Chart. The left chart is obtained by considering the saturated output power level, which highlights the trajectory followed by the optimum impedance when the frequency varies. The right one is referred to 3.55 GHz, which highlights the trajectory followed when the input power varies [6]. The left chart clearly shows how the optimum impedance rotates counterclockwise when

P_{out}	3.3 GHz	3.55 GHz	3.8 GHz
$P_{sat} = 37dBm$	$10.214 + j22.857$	$8.571 + j19.286$	$8.571 + j15.714$
3 dB OBO	$6.929 + j24.643$	$4.57 + j21.07$	$4.57 + j18.57$
6 dB OBO	$4.21 + j24.643$	$3.643 + j21.07$	$3.643 + j19.286$

Table 1.1: Optimum impedances for maximum efficiency - proof of concept case

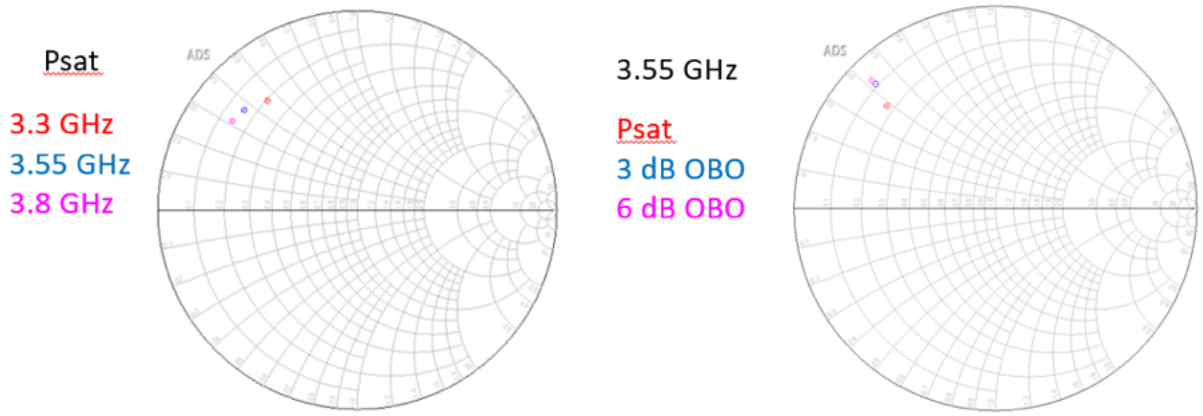


Figure 1.18: Optimum impedances trajectory for saturated output power and 3.55 GHz - proof of concept case

the frequency increases. On the right side instead, the frequency is kept constant at 3.55 GHz and the input power level is changed: the optimum load gets further from the Smith Chart's center when the output power backs off.

Figure 1.19 shows an LMBA schematic where the amplitude and the phase of the control signal are both swept in order to obtain the same contours shown in Figure 1.3. This schematic is useful to find the proper values for the control signal allowing to obtain the impedances in Table 1.1. Figure 1.20 shows how to do it graphically by plotting the load impedance desired (the red dot in figure) and the contours created by sweeping the amplitude and the phase of the control signal through the simulation in Figure 1.19 (pink lines). Marker **m2** points out the amplitude and the phase needed to match a certain value of the load. It results that both the required amplitude and the phase change when the frequency or the input power level varies.

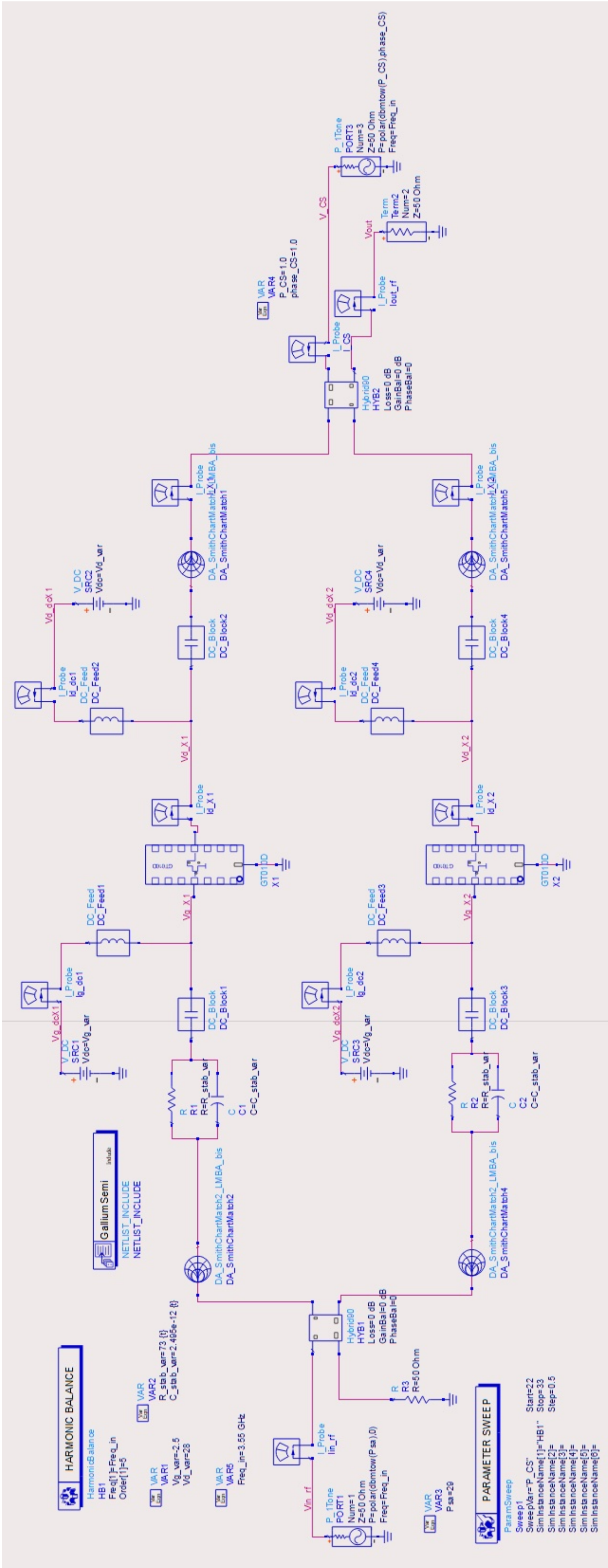


Figure 1.19: Two inputs LMBA schematic to determine the proper control signal values - proof of concept version

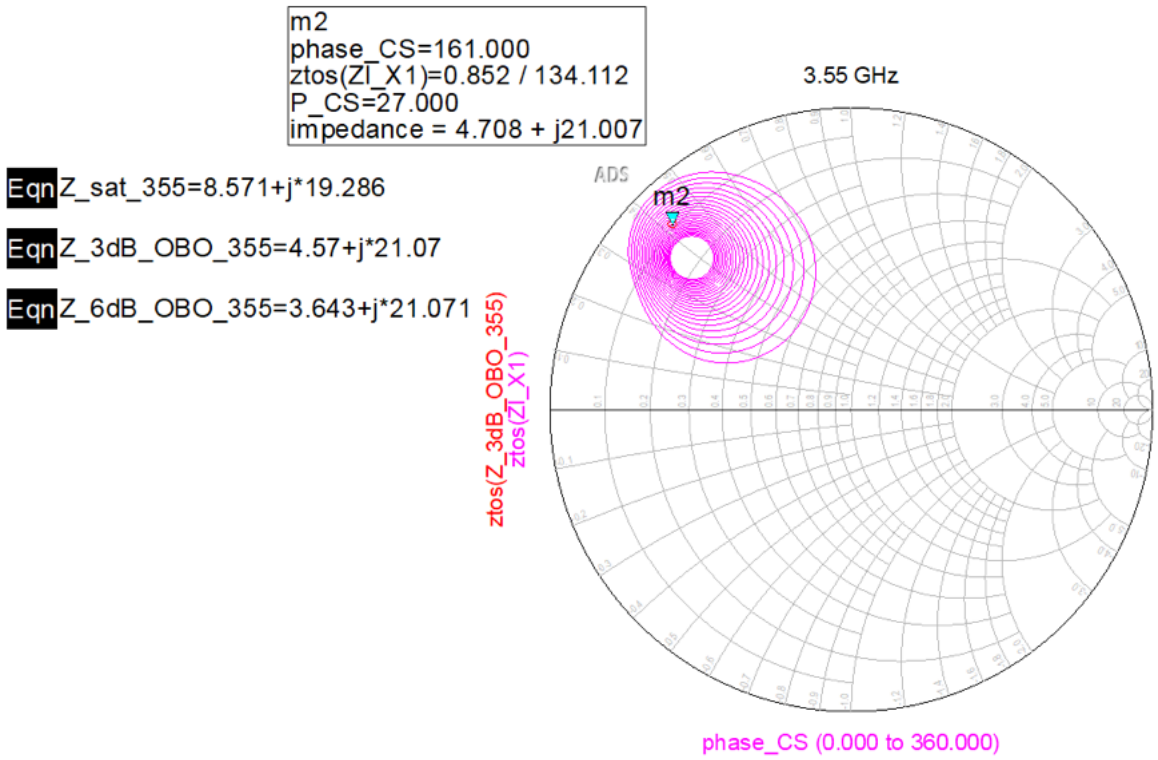


Figure 1.20: Establishment of the proper values for the control signal: example at 3.55 GHz and 3dB OBO - proof of concept version

Table 1.2 shows the required values for the phase; whereas as far as the amplitude is concerned, an average value is selected for a given OBO level between the ones gathered when the frequency varies. This choice will simplify a lot the control signal generation for the next simulation (Figure 1.21). Table 1.3 shows the picked values.

	P_{out}	3.3 GHz	3.55 GHz	3.8 GHz
Control Signal Phase	P_{sat}	99	140	225
	3 dB OBO	124	159	235
	6 dB OBO	140	163	240

Table 1.2: Control Signal Phase for different back off levels and different frequencies - proof of concept version

P_{out}	*Control Signal Amplitude*
P_{sat}	22 dBm
3 dB OBO	25 dBm
6 dB OBO	26.5 dBm

Table 1.3: Control Signal Amplitude for different back off levels - proof of concept version

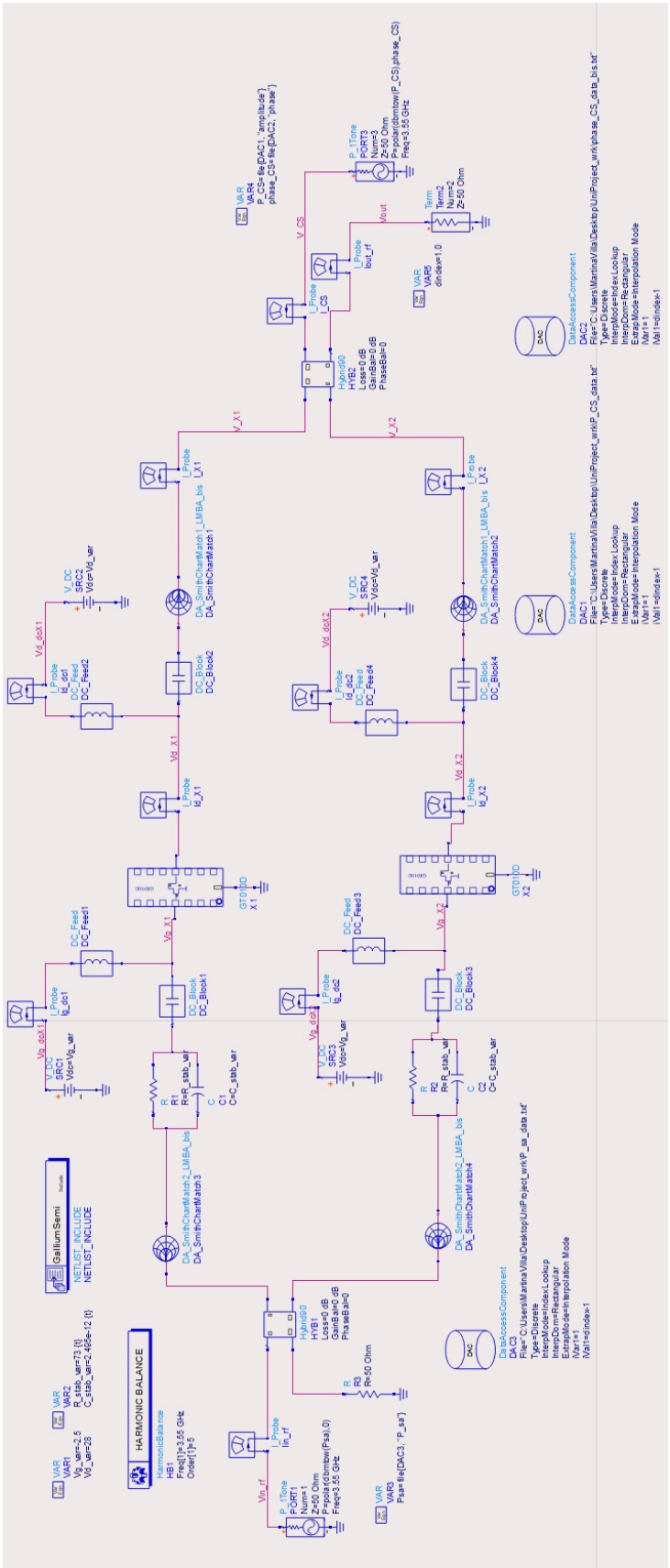


Figure 1.21: Two inputs LMBA schematic by using DAC components - proof of concept version

The values in the tables are tested with the schematic in Figure 1.21, where Data Access Components (DAC) are used to associate the control signal value to the input power level and the selected frequency. The results shown in Figure 1.22 reveal the desired efficiency improvement compared to the Balanced Amplifier in Figure 1.16. The efficiency indeed appears higher and almost constant from the output power's saturation level to the 3 dB OBO level.

dIndex	wtodbm(Pin_rf)	Pout_dBm	P_CS	phase_CS	ZI_X1	ZI_X2	D_efficiency
0.000	28.000	38.462	22.000	140.000	7.248 + j21.201	7.248 + j21.201	52.252
1.000	28.000	38.462	22.000	140.000	7.248 + j21.201	7.248 + j21.201	52.252
2.000	25.000	37.124	25.000	159.000	5.592 + j20.956	5.592 + j20.956	52.476
3.000	22.000	35.444	26.500	163.000	4.336 + j20.912	4.336 + j20.912	48.563

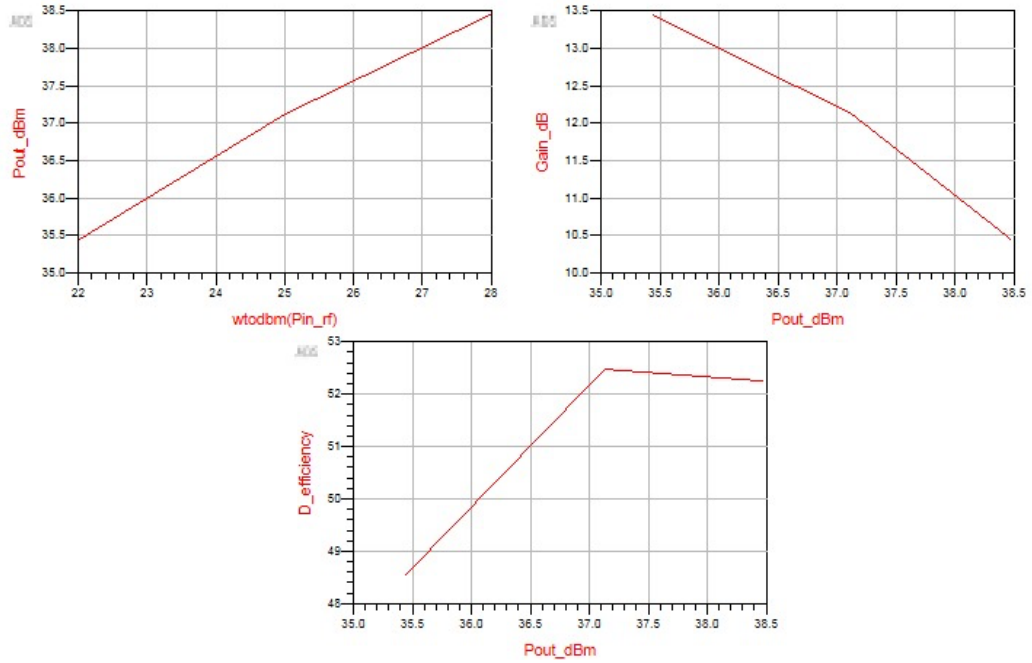


Figure 1.22: Performances of the two inputs LMBA by using DAC components - proof of concept version

The output power at a certain input power level increased too. This is related to the control signal power getting added to the output power of each transistor, as explained at the end of Section 1.2 with the equation 1.15. Figure 1.23 shows the equivalence expressed by the equation 1.15.

The usefulness of LMBAs has hence been proved with a two inputs kind of schematic.

wtodbm(Pin_rf)	wtodbm(Pmain)	wtodbm(P_control_signal)	2*Pmain+P_control_signal	Pout_rf	Pout_dBm
28.000	35.353	22.000	7.018	7.018	38.462
28.000	35.353	22.000	7.018	7.018	38.462
25.000	33.839	25.000	5.157	5.157	37.124
22.000	31.841	26.500	3.503	3.503	35.444

Figure 1.23: Control Signal power recovery of the two inputs LMBA by using DAC components - proof of concept version

Chapter 2

LMBA's design

A few results of a very simple version of the LMBA have been presented in the previous Chapter. The design steps are now described in this section to realise an LMBA prototype and test the theoretically explained mechanism.
The chosen substrate for realising the LMBA is Rogers RO4350 [1], with a substrate thickness of 20 mil, a design dielectric constant of 3.66, a conductor thickness of 17 μm and a dielectric loss tangent of 0.004. The conductor used is copper.
As already mentioned, the transistors chosen for the board realization are the GT010D by Gallium Semiconductor, which is biased with 2.5 V gate voltage and 28 V drain voltage to obtain 16 mA quiescent current.
Off-the-shelf ATC 600F capacitors are used to realise the Matching Networks and Stabilization Networks,.

2.1 Schematics

2.1.1 Stabilization Network

The Stabilization Network's components have the same value used in the ideal component case (Figure 2.1), demonstrated in section 1.3.1.

2.1.2 Matching Networks

The Output Matching Network has been created by performing S Parameters simulations and trying to obtain the same matching of the ideal components case.

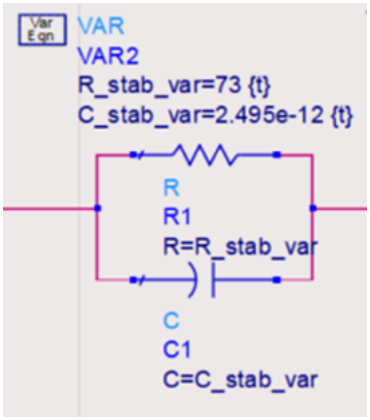


Figure 2.1: Schematic of the Stabilization Network

The OMN schematic in Figure 1.9 can be developed with some considerations. The schematic in Figure 2.2 is obtained in the end. First of all, the two ports of the Output Matching Network need to be connected to the transistor on one side (P1) and to the output load in the single branch case, or the output coupler in the BA or LMBA case, on the other side (P2) respectively. This is the reason why the component to place at the beginning and at the end of the OMN is a transmission line (TL8 and TL12). The second component placed right after the transmission line connected to P1 is a short-circuited parallel stub (Figure 1.9). This stub (TL9 and TL10) will be useful in the next steps regarding the layout of the Matching Networks, because it will be merged with the bias network of the transistor. The ground connected to the parallel stub in Figure 1.9 is now substituted with a large capacitor (X9 and X7), that behaves like a short circuit to ground at the frequencies of interest from 3.3 GHz to 3.8 GHz, so that it will be useful like bypass capacitor when this matching network will work as a bias network too. This short circuit remains a short-circuit also at the second harmonic placed at 7.1GHz. This is useful to delete the distortion coming from the second harmonic impedance that is located near the border of the Smith Chart. Compared to Figure 1.9 the second transmission line (composed by TL11 and TL13) and the series capacitor (X8) are preserved. An additional small shunt capacitor (X10) is then added to insert another degree of freedom to control the matching better. Since this capacitor's value is really small, it appears close to an open circuit. Additional components like MCROSS and MSTEP are used to take into consideration the width changes from one transmission line to another. The final result is shown in Figure 2.2.

The structure of the Input Matching Network (IMN) (Figure 2.3) has been created in a

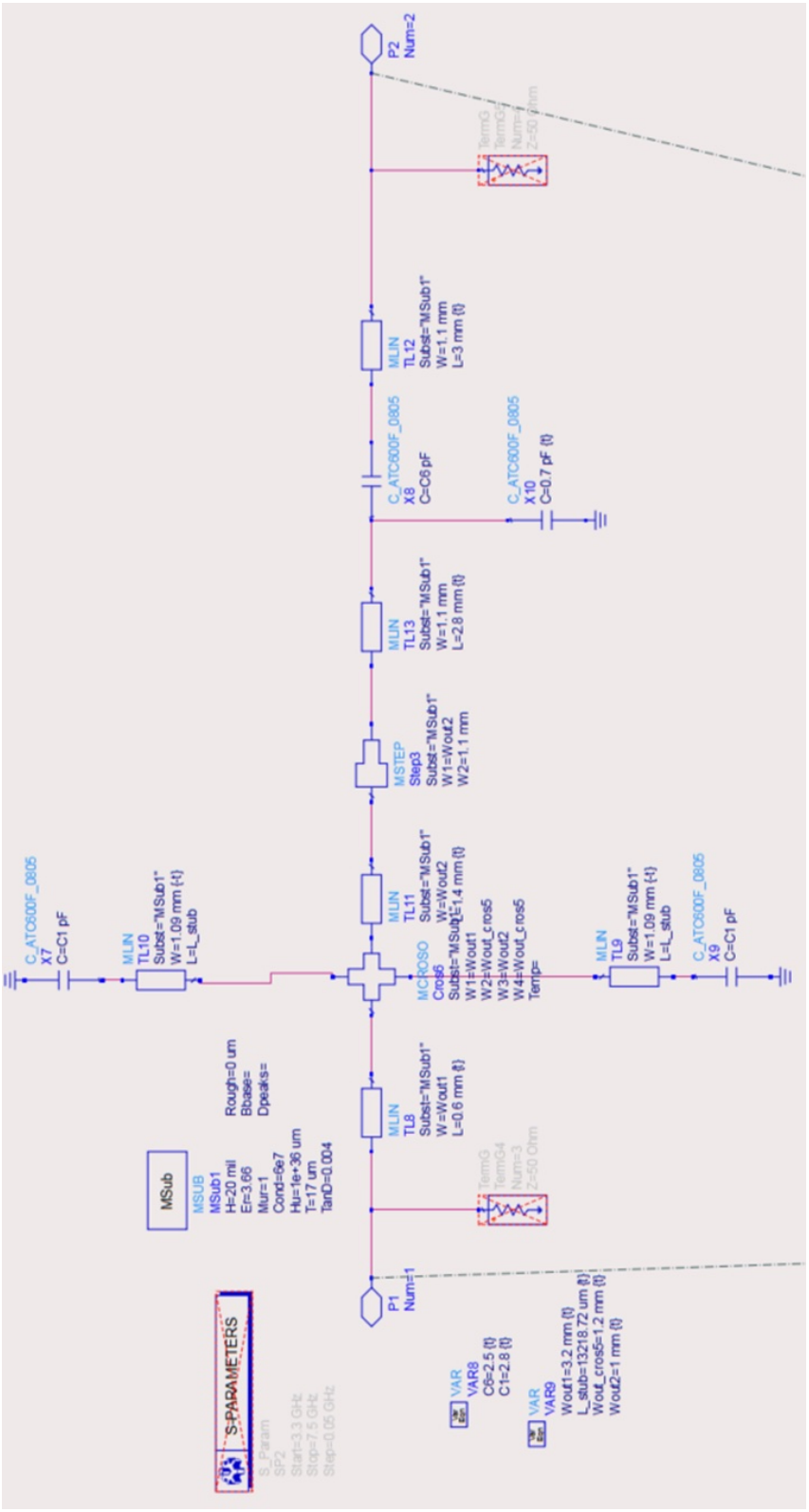


Figure 2.2: Schematic of the Output Matching Network by using real components

similar way as it was done for the OMN, if we consider that port P1 will be connected to the transistor side, precisely to the stabilization network, and P2 to the signal source. The capacitors connected to the shunt Transmission Lines are also introduced in the IMN.

Figure 2.3 also takes into consideration additional larger bypass capacitors (C1 and C2 equal to 10 nF) to short circuit lower frequencies.

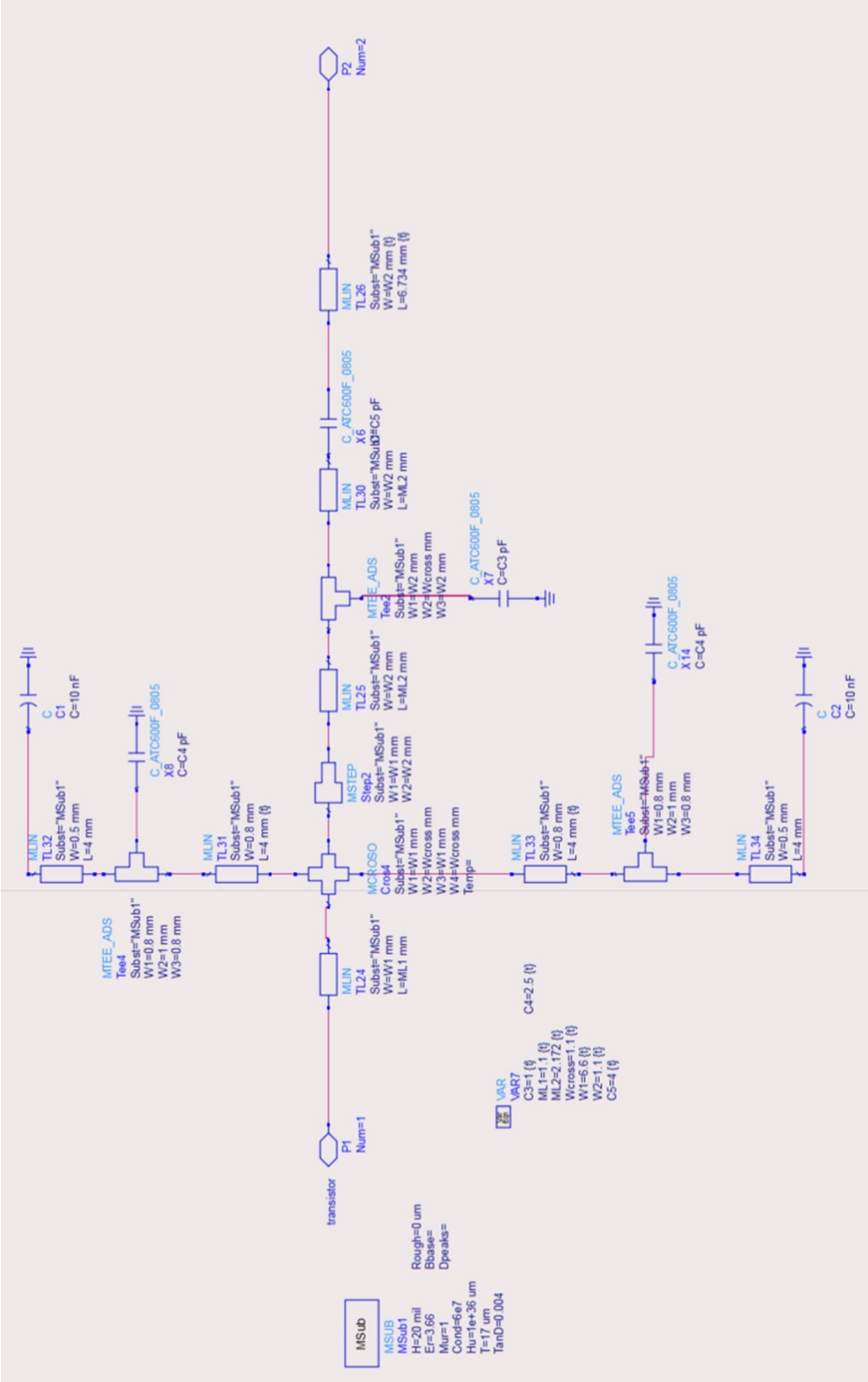


Figure 2.3: Schematic of the Input Matching Network by using real components

The values of the capacitors and the lines' dimensions of the Matching Networks were

determined by performing an Harmonic Balance Simulation of the Single Transistor Amplifier in the first place and then of the Balanced Amplifier. The simulations were performed in the tuning mode in order to find the proper values allowing to match the ideal components case's performances with the real components ones. All this is depicted in Figures 2.4 and 2.5, where the blue lines are related to the real components case and the red lines to the ideal components case.

The IMN and OMN in Figures 2.2 and 2.3 make the performances match the ideal component behavior, which means obtaining an average 3dB OBO Drain Efficiency equal to 38% over the 3.3 - 3.8 bandwidth.

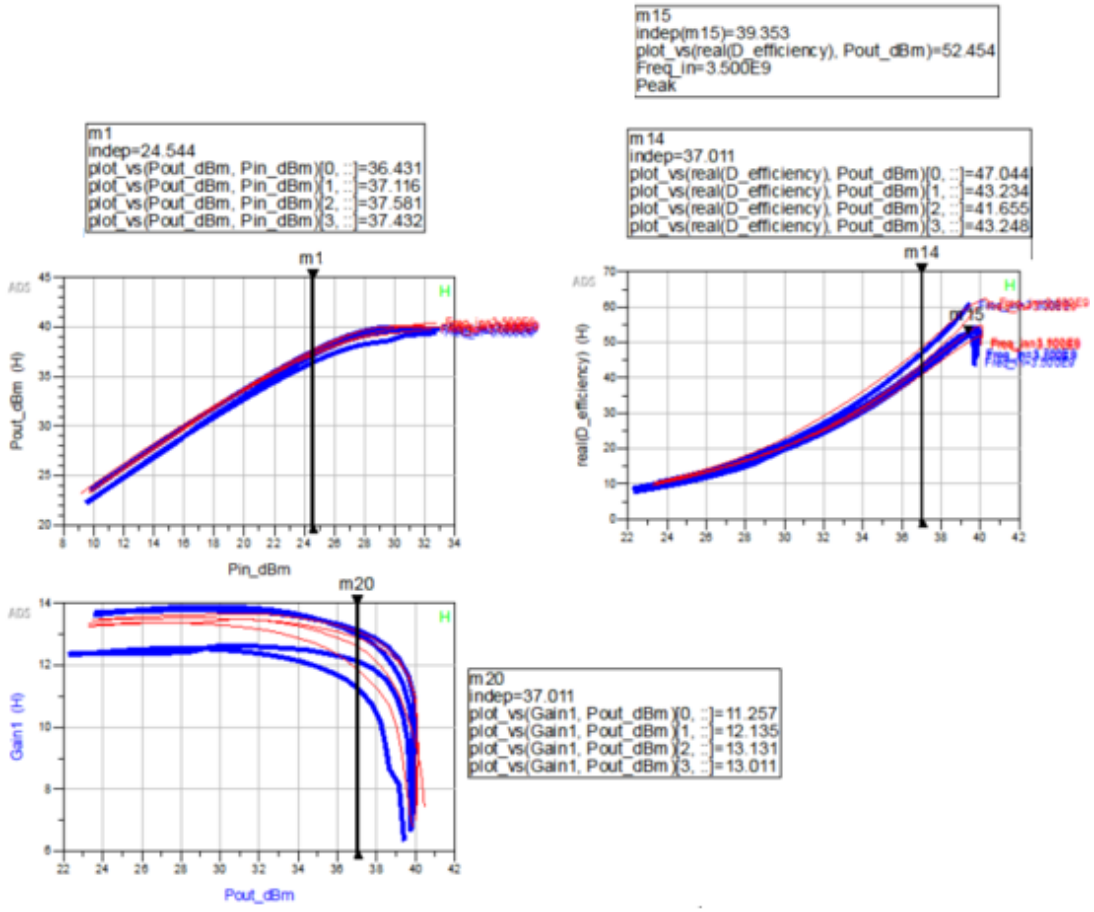


Figure 2.4: Single Transistor Amplifier's performance comparison between the ideal components case and the real components case

Previously the LMBA's working principle has been proved through simulations where the control signal was changing with the frequency and input power by using DAC components, as showed in section 1.3.3. The LMBA's simulation discussed in the current section has been performed by keeping the control signal's amplitude and phase constant, as a

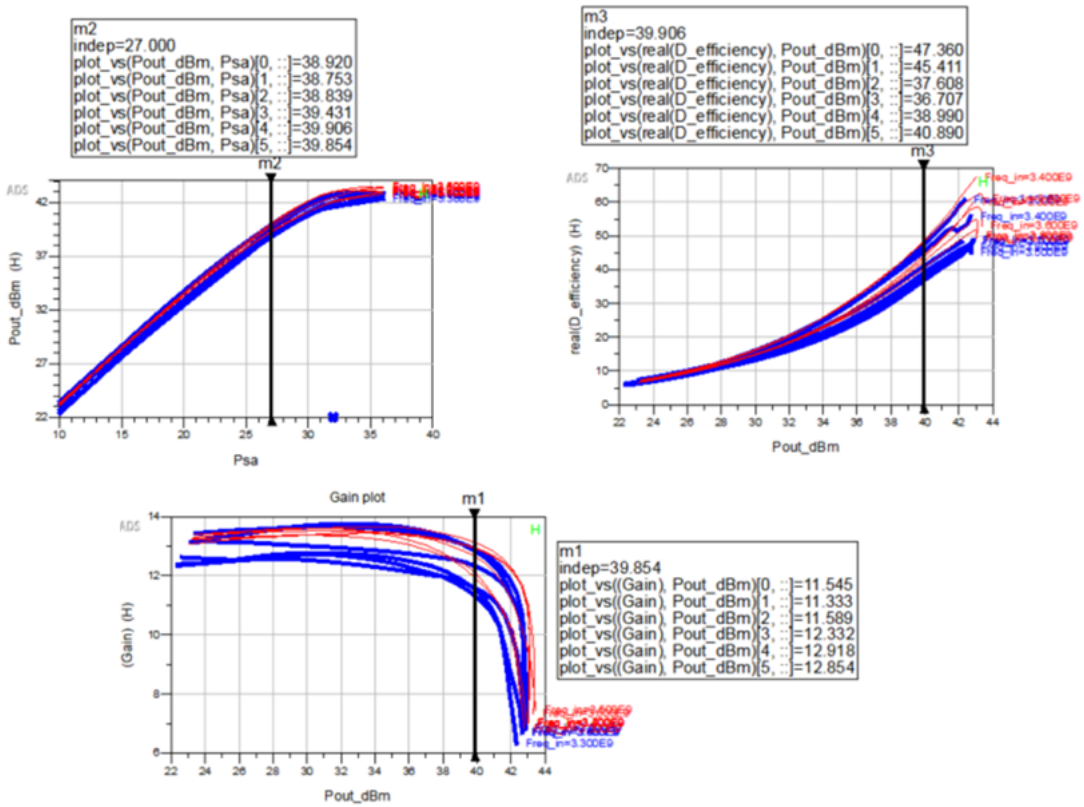


Figure 2.5: Balanced Amplifier's performance comparison between the ideal components case and the real components case

simplification. The selected values are 31dBm for the amplitude and 110° for the phase. They were obtained by performing Harmonic Balance simulations in the tuning mode and trying to maximize the drain efficiency. Additionally in this simulation, the control signal generator has been turned on only when the Source Available Power Psa was higher than 20dBm [7]. This is done in order to focus on the power range of interest, given that the control signal's contribute to the output power is predominant on the output power of the two main branches $2P_{main}$ when the input power is very low. So the real amplification of the input signal wouldn't be the principal term in the summation 1.15 and it's useless to consider those values.

The final simulation's schematic and results are depicted in Figures 2.6 and 2.7. In this last picture, the ideal components case's Drain Efficiency is also shown in order to compare the results better. Plots in Figure 2.7 have an irregular evolution due to the sudden starting of the control signal's generator.

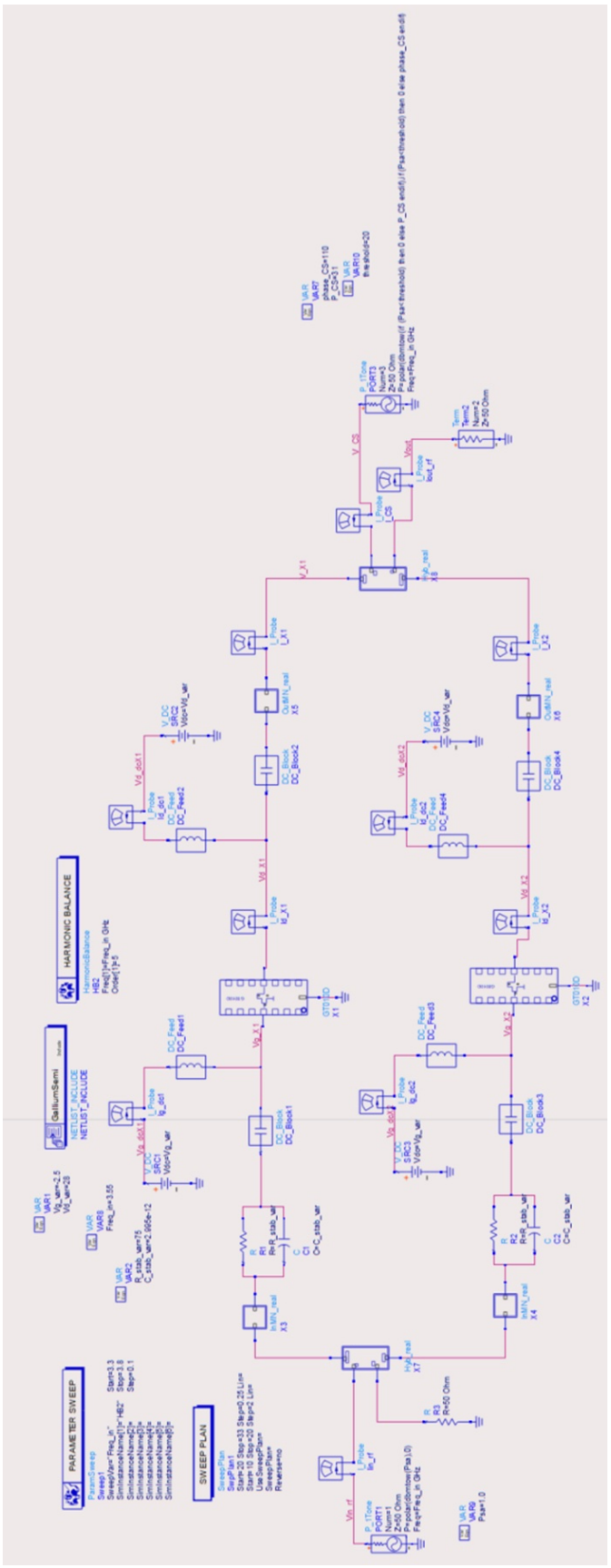


Figure 2.6: LMBA's schematic by using real components and using a 31dBm control signal's amplitude and 110° control signal's phase

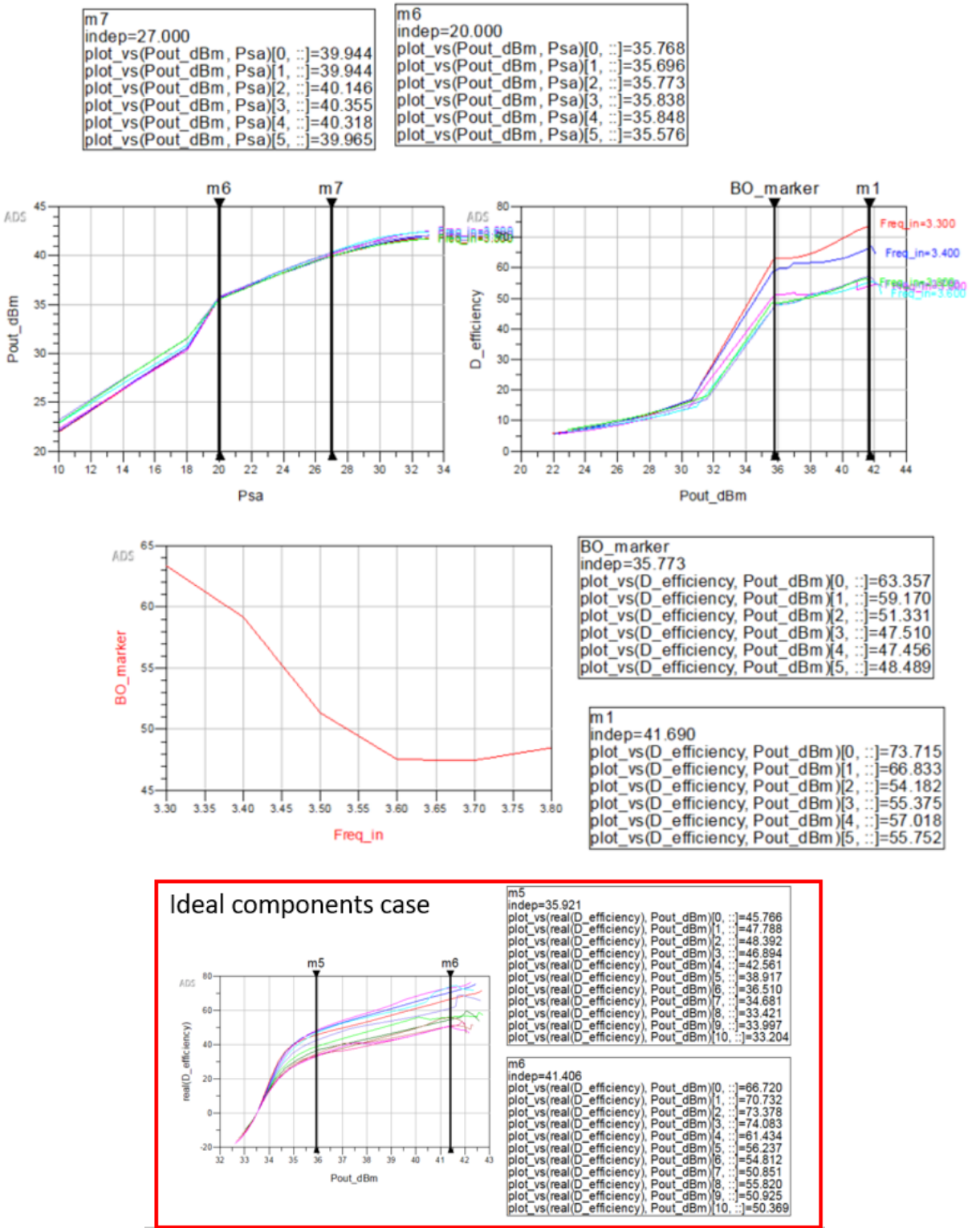


Figure 2.7: LMBA's performances by using real components and using a 31dBm control signal's amplitude and 110° control signal's phase

2.2 Layout

By starting from the schematics presented in the previous section, the corresponding layout of the circuit can be obtained. After having created the layout, EM simulations can be performed to take into consideration effects that a schematic simulation doesn't, such as coupling between transmission lines and edge effects.
The ADS EM simulator tool allows to create the layout, perform the EM simulation and use the resulting S-parameter for hybrid EM - schematic simulations.

2.2.1 Output Matching Network's layout

By considering the Output Matching Network in Figure 2.2, the corresponding layout is created by putting together the Matching Network and the Bias Network. The series capacitor in the MN can be exploited as DC block and the parallel transmission line as DC feed.
The dimensions of the transmission lines (TL) need to respect the component's dimensions, for example the width of the closest to the transistor Transmission Line (TL8 in Figure 2.2) has to be equal or higher than 4.2 mm, that is the pin region's width of the transistor GT010D. Furthermore, capacitors' width needs to be respected in order to connect them to the transmission lines. ATC 600F capacitor's width is 1.1 mm, and the capacitor length is also important to consider for the series capacitor connection. Figure 2.8 shows the selected dimensions for the Output Matching Network, that is used as Bias Network too. Figure 2.9 shows the connection with the other components and their values.

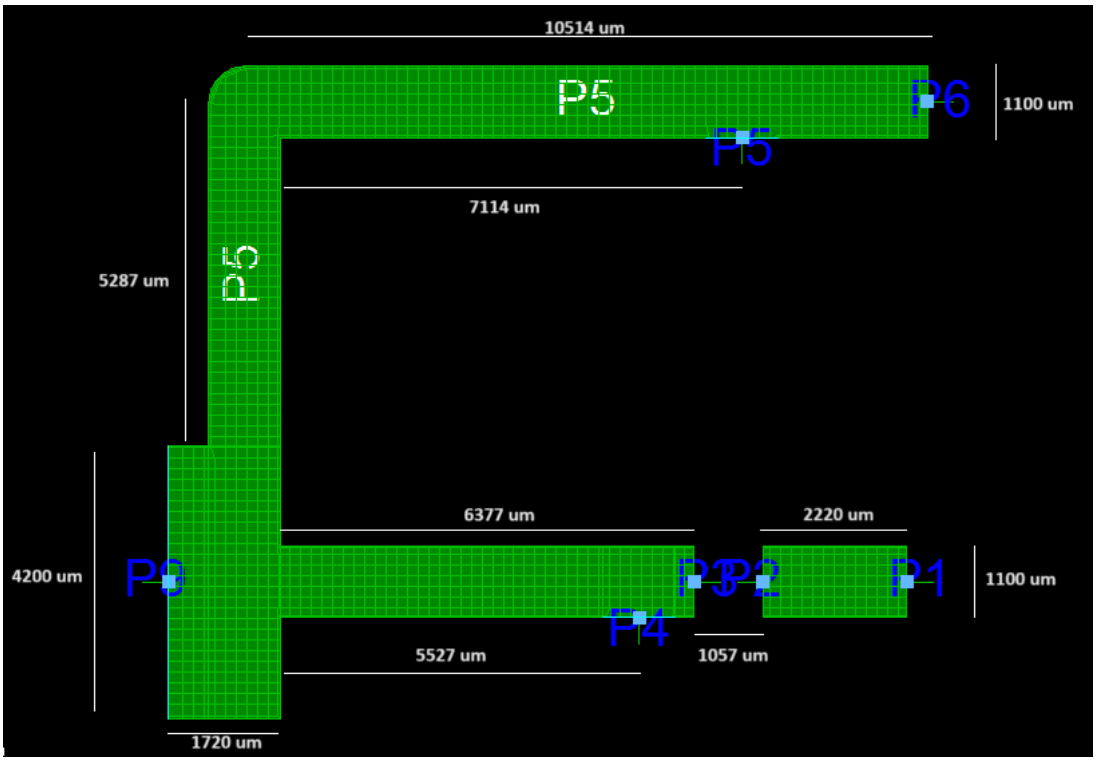


Figure 2.8: Output Matching Network and Bias Network's layout

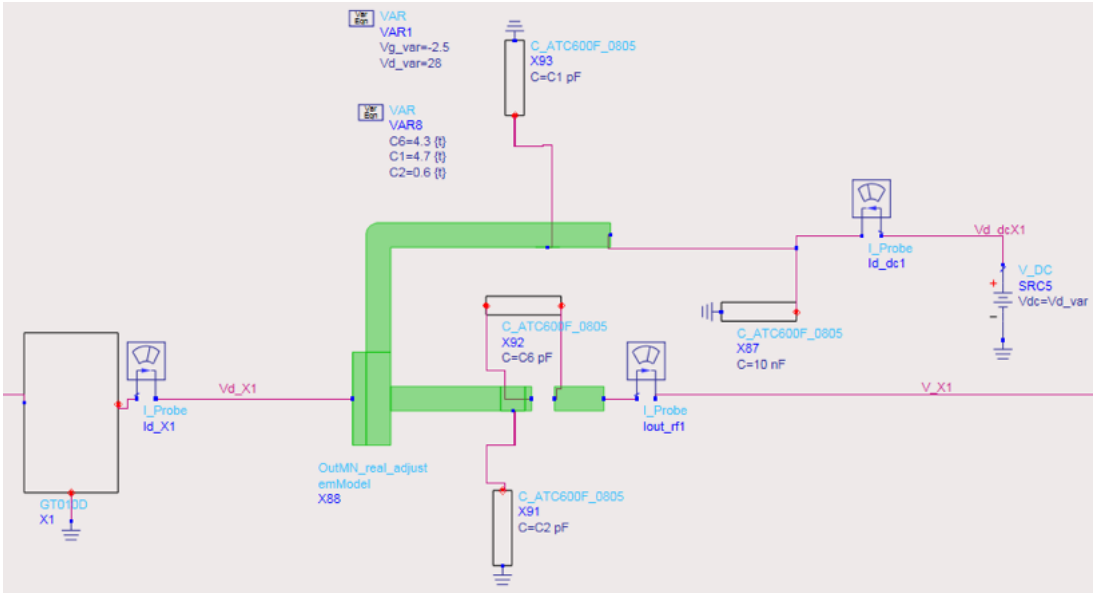


Figure 2.9: Output Matching Network and output Bias Network's layout connection

2.2.2 Input Matching Network's layout

The same reasoning can be repeated for the Input Matching Network's layout, but by considering the Stabilization Network as well. The IMN, the Input Bias Network and the Stabilization Network are indeed gathered together. It's hence needed that some space is left for the stabilization network's insertion. The transmission lines connected to this network need sufficient width to hold both the components (1 mm wide each) by considering 1 mm distance between each other. The Stabilization Network is desirable to be connected as closest as possible to the transistor, leaving sufficient space for the DC feed's connection. Considering the schematic in Figure 2.3, the right section where to place the Stab Network is between Cros4 and TL25.

The IMN's parallel transmission line (TL31, TL32, TL33, TL34) has been enriched with a resistor (R5 in Figure 2.11), whose role is biasing the transistor and provide an additional level of freedom in the design. The value of this additional resistor doesn't have to be particularly high thanks to the presence of the parallel transmission line operating as RF choke together with the bypass capacitors X14 and C2.

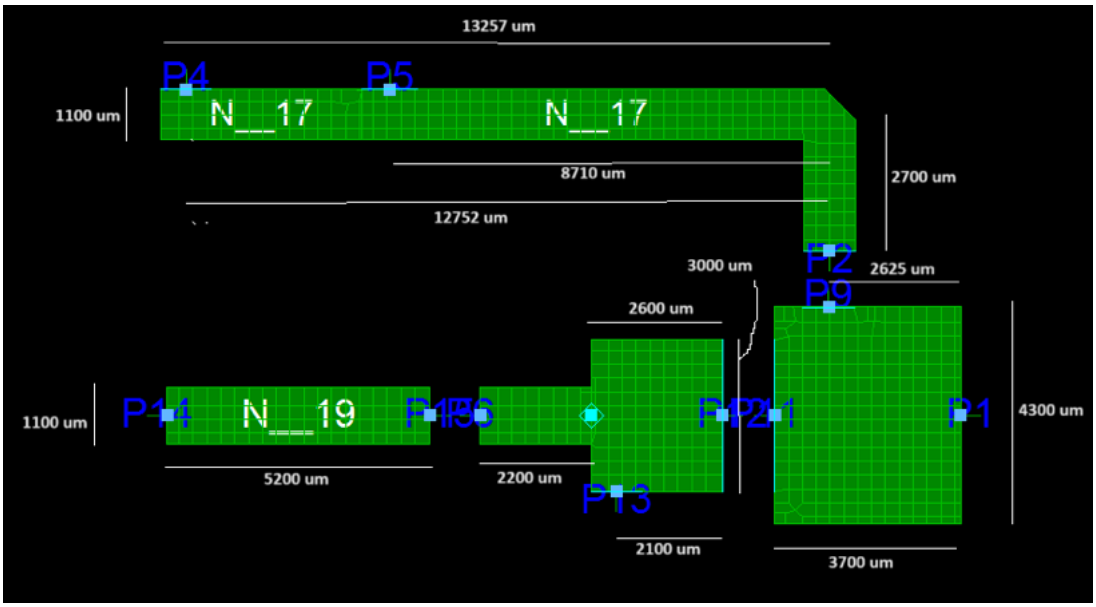


Figure 2.10: Input Matching Network and Bias Network layout

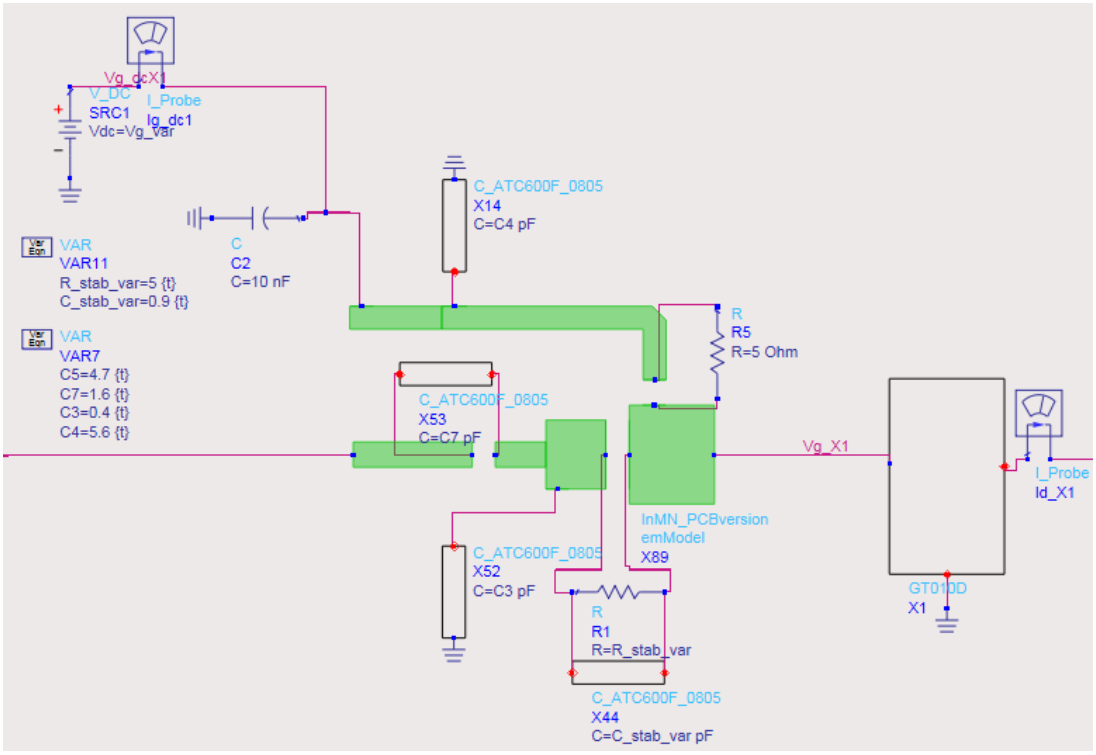


Figure 2.11: Input Matching Network, Stabilization Network and input Bias Network's layouts' connection

In both the IMN and the OMN an additional bypass capacitor has been placed, whose value (10 nF) is higher than the one closer to the transistor, in order to short circuit lower and lower frequencies.

It's possible to notice that the Matching Networks' layouts present just one of the two parallel transmission lines which were present in Figures 2.2 and 2.3. This is needed with the aim of realizing the final LMBA circuit on a PCB, whose area is limited. The LMBA is indeed composed by two identical branches, so if each branch showed symmetrical parallel transmission lines, the two branches would bump into each other. By realizing asymmetrical matching networks the problem is solved, as depicted in Figures 2.8 and 2.10.

The dimensions of the transmission lines and the values of capacitors and resistors were obtained by means of Harmonic Balance simulations in the tuning mode of the Balanced Amplifier and by monitoring how the drain efficiency was changing.
The Stabilization Network was also changed during the tuning process, resulting in a 5Ω resistor in parallel with a 0.9 pF capacitor. Figure 2.12 shows the simulated schematic and 2.13 the results of the simulation. By injecting a control signal in the BA in Figure 2.13, the LMBA's performances can be tested. As in the previous section, the control signal's amplitude and phase are kept constant during the simulation at 33dBm and 103° respectively. They turned out to be the optimum values for this schematic taking into consideration the networks' layout. As in the simulation in Figure 2.6, the control signal is turned on only when the source available power is higher than 20 dBm. The results are depicted in Figure 2.14.

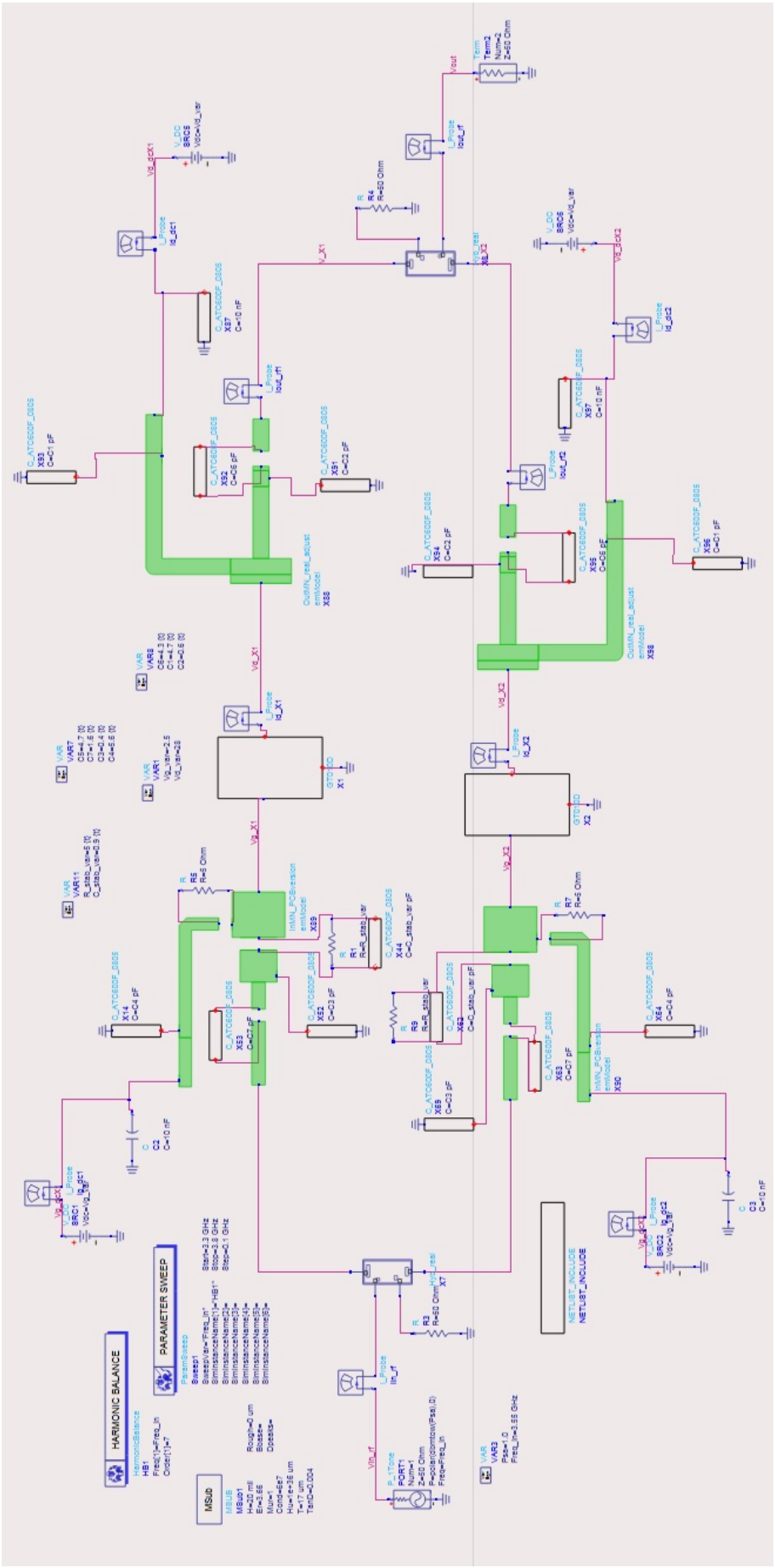


Figure 2.12: Balanced Amplifier schematic considering the Matching Network's layout

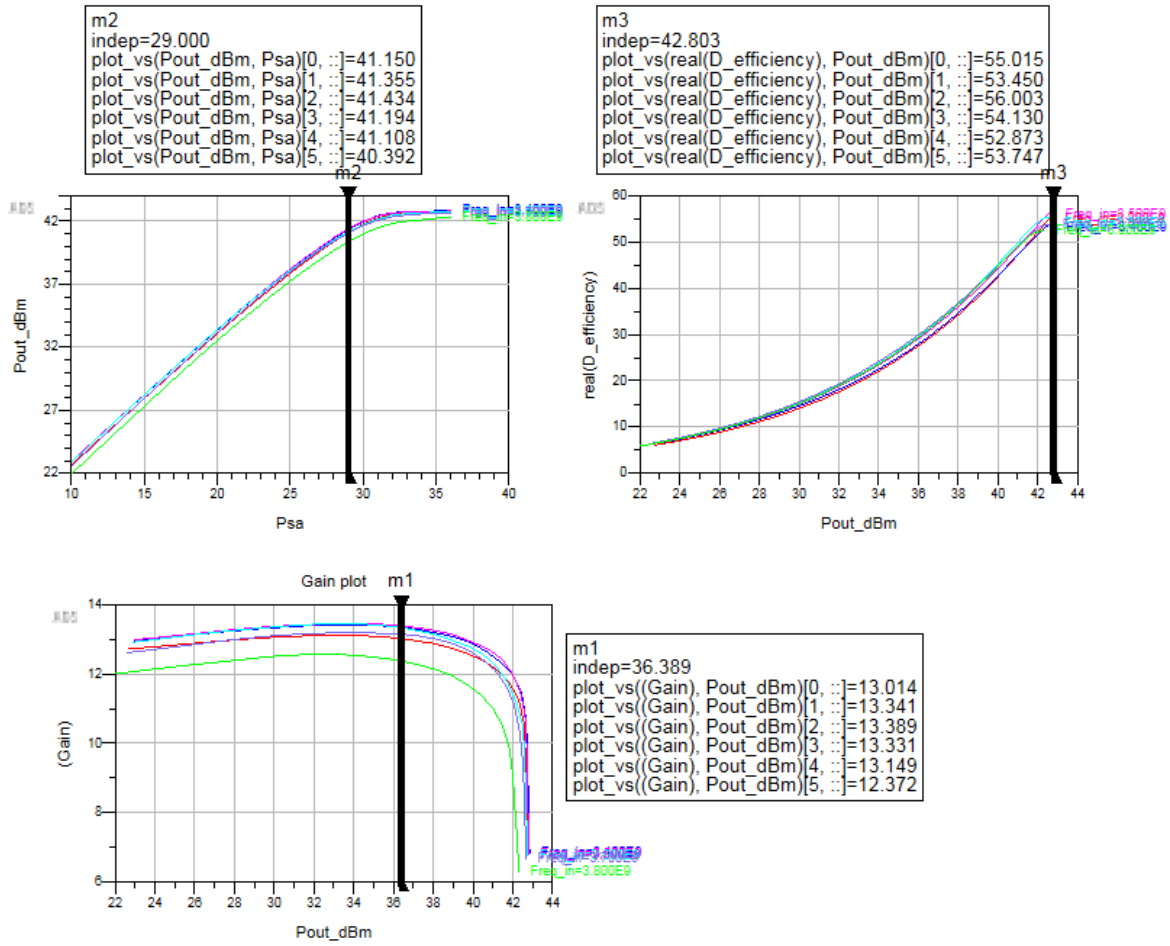


Figure 2.13: Balanced Amplifier schematic considering the Matching Network's layout - performance

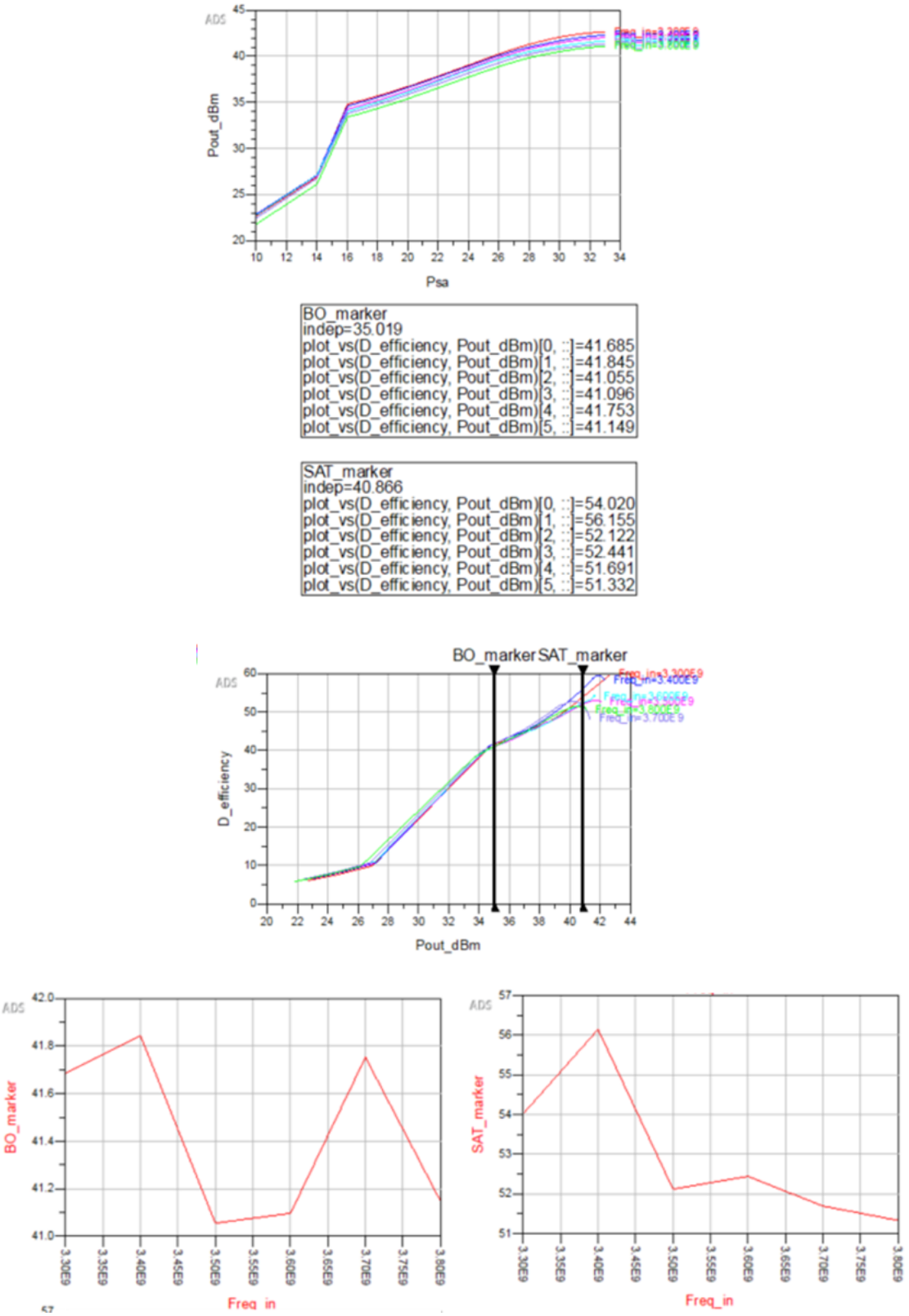


Figure 2.14: LMBA considering the Matching Networks' layout and with control signal's amplitude equal to 33 dBm and phase equal to 103° - performance

The last shown schematic represents the final version of the Balanced Amplifier and can be realised on a PCB. The board's dimensions are 70mm x 50 mm and the final layout is depicted in Figure 2.15.

The drawing displays the full circuit, also considering the pads for the Power Supply connection, the large Bypass Capacitors and also the path from the Coupler's ports to the board's border, where the connectors will be placed. Pads for the current sensing are also considered, together with high value resistors (R7, R8, R10, R11, R5 and R6).

This board implements the Balanced Amplifier's layout, but it can also be used in the Single Branch configuration performing a simple single transistor amplifier.

Figure 2.15 shows not only the paths but also the components' placement. The position of capacitors C29, C30, C31 and C32 determines which configuration is realised: the Single Transistor or the Balanced one. The depicted arrangement performs the Single Branch configuration, bypassing the input and output Couplers and avoiding the bottom transistor from receiving the input signal. By removing C30 and C31, placing C29 vertically and C32 horizontally, the Balanced Amplifier configuration is obtained.

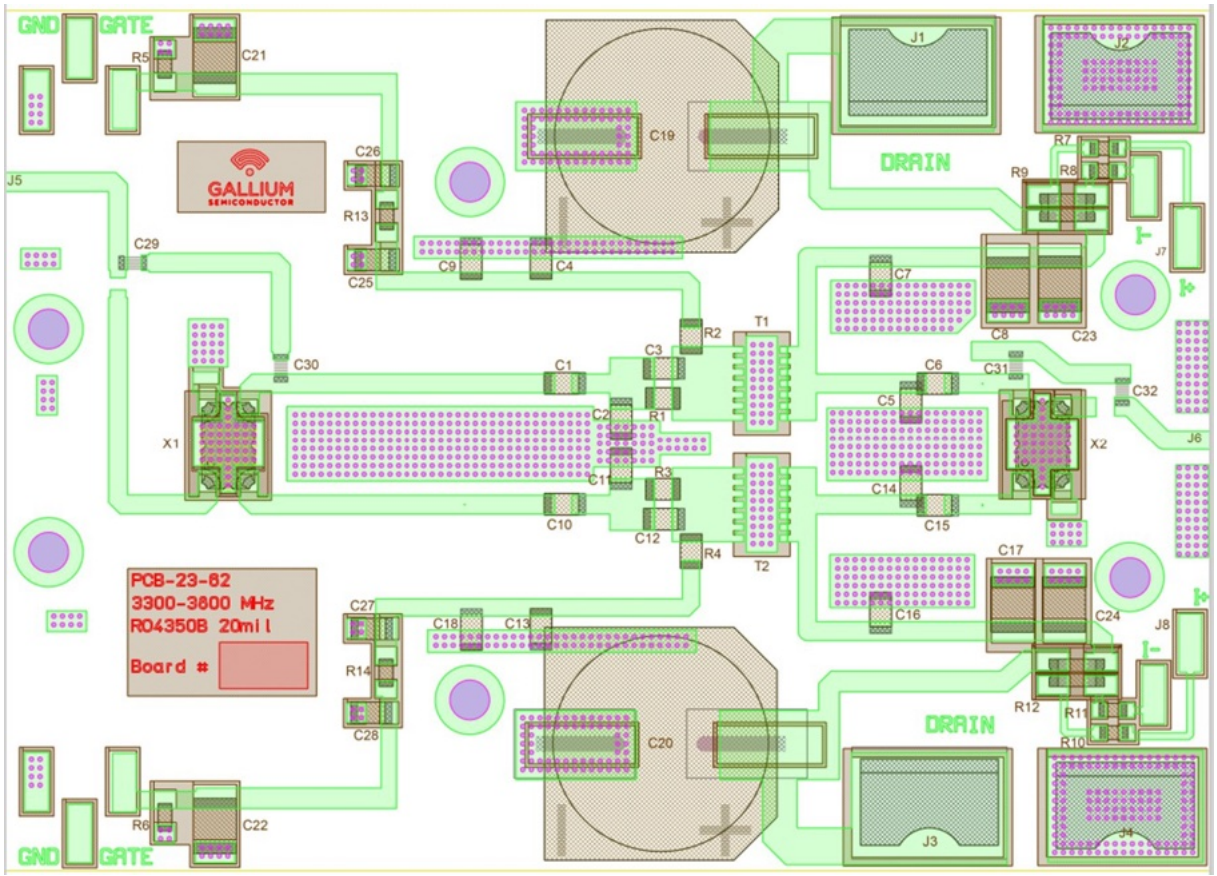


Figure 2.15: Balanced Amplifier's layout for the realization on a PCB

The layout in Figure 2.15 has only one output port, but the LMBA needs a second port at the output for injecting the control signal. Figure 2.16 shows the rerouted version of the layout with two output ports, one of which will be committed to the control signal's injection (the top one). This version of the layout can only be used as an LMBA or in the Balanced Amplifier configuration, connecting the additional output port to a 50 Ω termination. The Single Branch configuration can't be obtained because the Couplers can't be bypassed here.

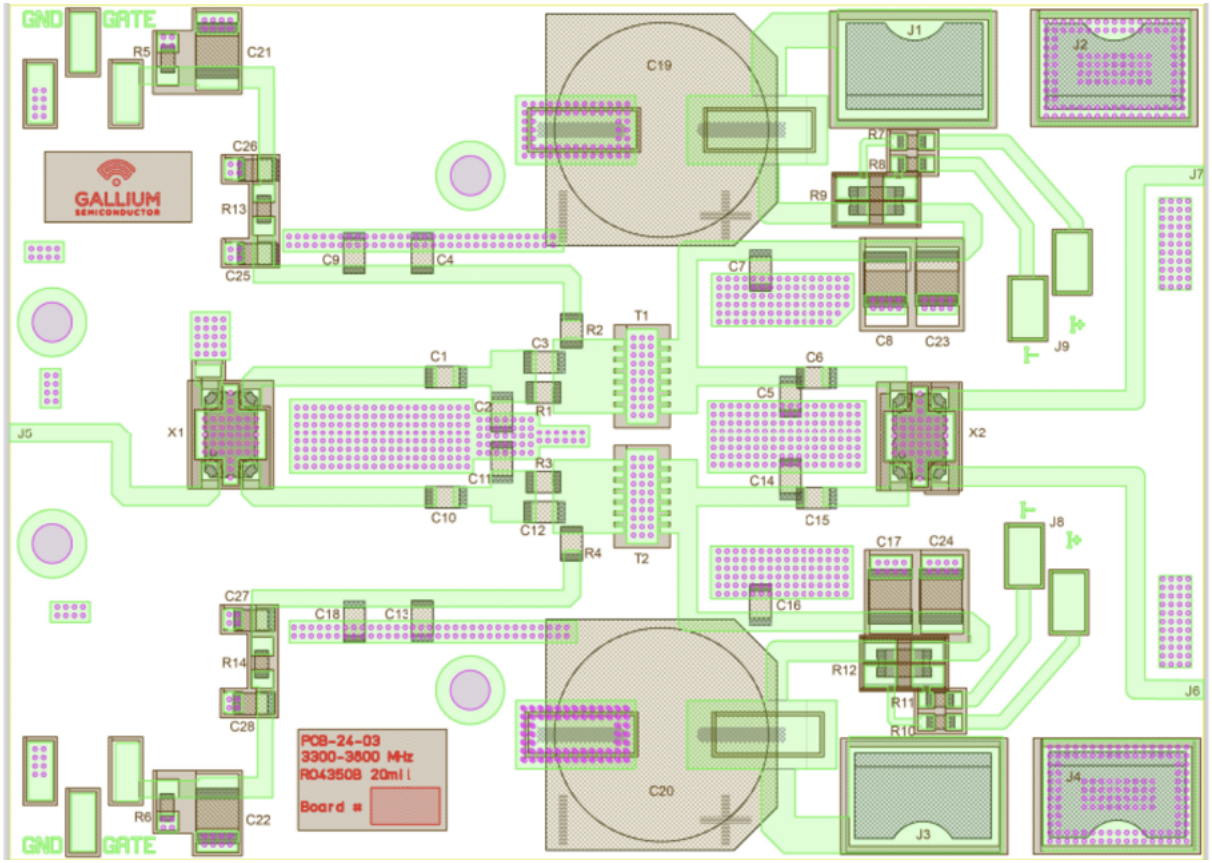


Figure 2.16: Balanced Amplifier's layout for the realization on a PCB - rerouted version

Chapter 3

Measurements

Three different boards were realised on a ROGERS RO4350 substrate: the Single Branch Amplifier, the Balanced Amplifier and the Balanced Amplifier with two output ports to be used as LMBA. The substrate selected has a 3.66 dielectric constant and a 20 mils substrate thickness, 17 μm conductor thickness and 0.004 dielectric loss tangent.
Figures 3.1, 3.2 and 3.3 show the pictures of the PCBs, each of them has dimensions measuring 70 mm x 50 mm.
These three boards were tested in order to verify their functioning and to find the proper values of the components in comparison to the simulated ones.
The Single Branch Amplifier has been tested first, since it is the simplest and the starting point for the realization of the LMBA. Scattering Parameters and Continuous Wave Single Tone measurements were performed.
The Balanced Amplifier board has been tested in the second place and finally the LMBA's board by using two different signal generators for the input signal and the control signal.
All the three boards were tested with the transistors biased with a 16 mA quiescent current and 28 V drain voltage.
In the next pages the measurements of the three circuits are discussed.

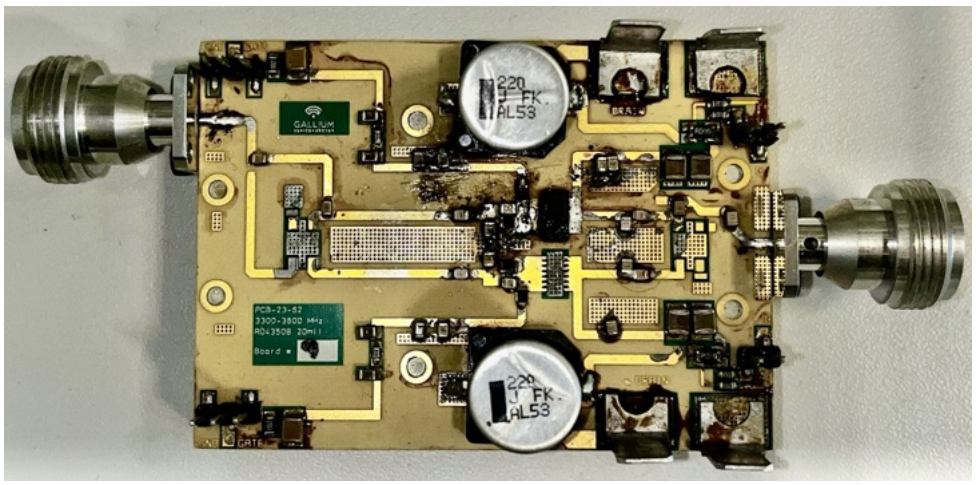


Figure 3.1: PCB of the Single Branch Amplifier

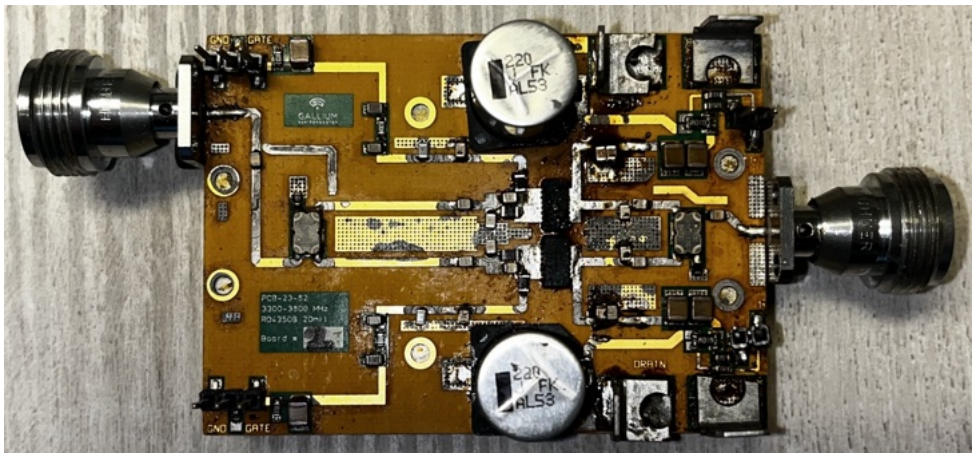


Figure 3.2: PCB of the Balanced Amplifier with one output port

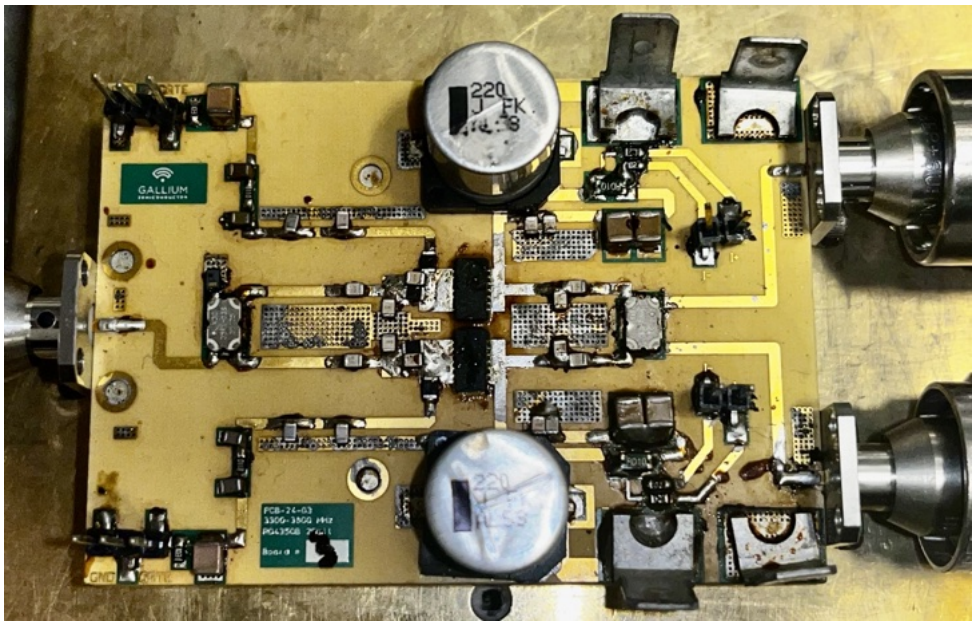


Figure 3.3: PCB of the Balanced Amplifier with two output ports allowing to inject the control signal and realise an LMBA

3.1 Single Branch Amplifier

Figure 3.4 shows the setup diagram used to test the Single Transistor Amplifier. The later shown results were obtained by modifying some component's values. The final Bill of Materials (BoM) related to the Single Branch Amplifier's PCB is shown in Table 3.1.

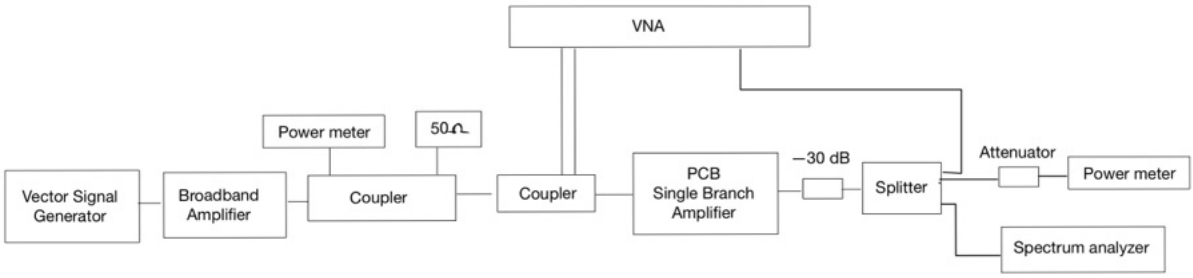


Figure 3.4: Measurement setup diagram for testing the Single Branch Amplifier PCB

The first carried out measurement was a Scattering Parameters measure injecting an input power equal to 15 dBm and exploiting the VNA; the results are shown in Figure 3.5: S_{11}'s low value proves good input matching in the bandwidth of interest, especially from 3.5 GHz to 3.8 GHz. S_{21} represents the amplifier's gain, which turns out to be 14.33dB average over the frequency rage, as expected from the simulations.

Table 3.1: Final BoM of the Single Branch Amplifier PCB

Components List	Reference	Part No.	Manufacturing
PCB	RO4350B, 20mil, 35um Cu	PCB-23-62	Euro Circuits
T1	6X3 mm DFN	GT010D	Gallium Semiconductor
C1	3pF Capacitor, 0805. INMAT	ATC 600F3	ATC
C2	0.4pF Capacitor, 0805. INMAT	ATC 600F0R4	ATC
C3	5.6pF Capacitor, 0805. INMAT/Stab network	ATC 600F5R6	ATC
R1	5.1 Ohm Resistor, 0805. INMAT/STAB		Yageo
R2	5.1 Ohm Resistor, 0805. INMAT/Gate Feeder		Yageo
C4	5.6 pF Capacitor, 0805. Gate Feeder (most right position)	ATC 600F5R6	ATC
C5	0.9pF Capacitor, 0805. OUTMAT	ATC 600F0R9	ATC
C9	10 nF Capacitor, 0805. Gate Feeder	GRM2165C2A103J	Murata
C6	4.7pF Capacitor, 0805. OUTMAT	ATC 600F4R7	ATC
C7, C16	4.7 pF + 1.8 pF right side Capacitor, 0805. OUTMAT/ Drain Feeder	ATC 600F4R7 + ATC 600F1R8	ATC
C8, C23	10 µF Capacitor, 1210. Decoupling	GRM32EC72A106K	Murata
C19	220 µF Electrolytic Capacitor, 12.5 mm	EEV-FK1J221Q	Panasonic
C21	22 µF, 1210	GRM32ER71C226K	Murata
R5	10 kOhm, 0603	RT0805DRD0710KL	Yageo
C25	100 nF Capacitor, 0805	GRM21BR7cx2C2A104K	Murata
C26	10 µF Capacitor, 0805	GRM21BC71E106K	Murata
R13	10 Ohm, 0603	RC0603JR	Yageo
J5, J6	Female SMA connector, 12.7 mm flange	23_SMA-50-0-2/111_NE	Huber+Suhner
C29, C30, C31, C32	10 pF Capacitor, 0603. Coupler Bypass	ATC 600F100	ATC

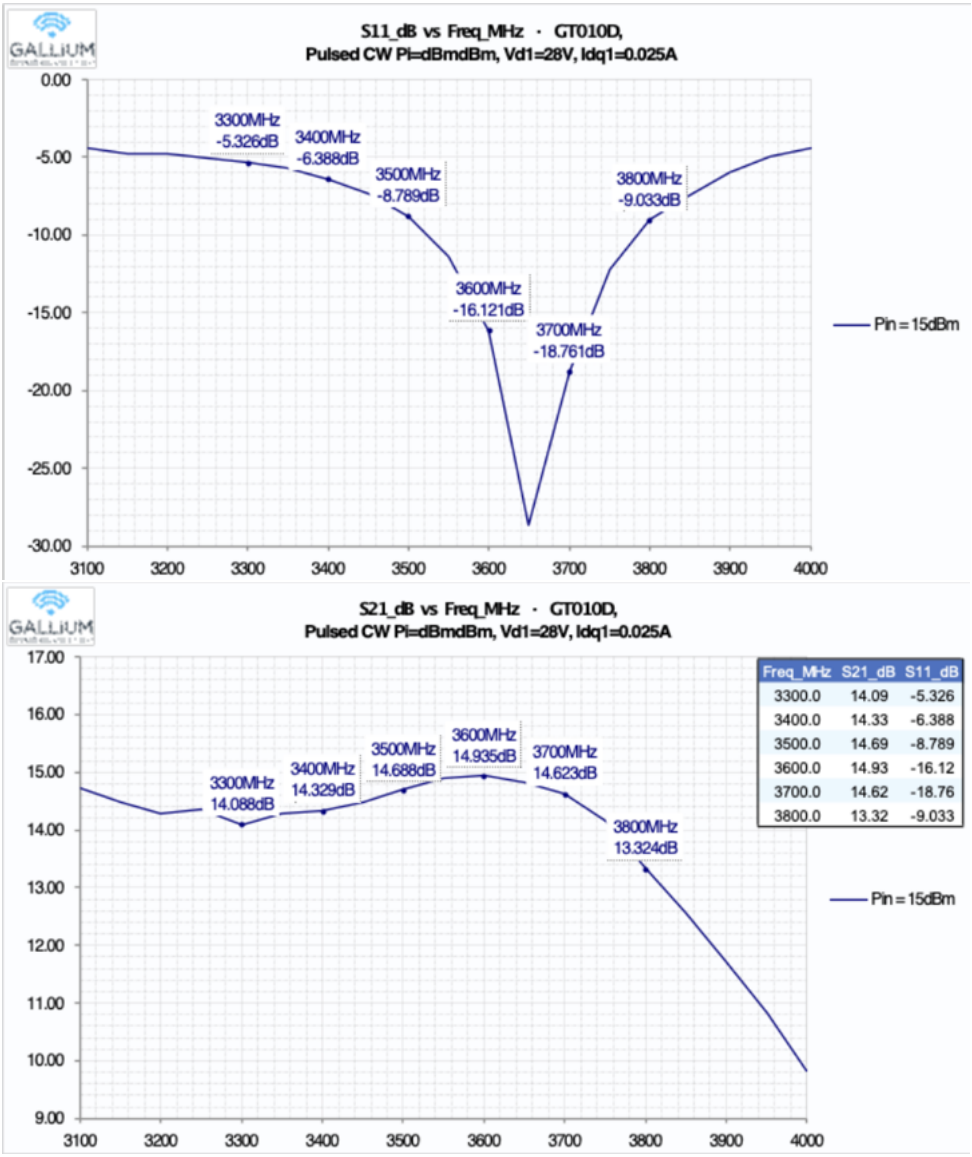


Figure 3.5: Single Branch Amplifier PCB's measurement: S-Parameters

One Tone measurements can be performed by injecting an input power equal to 25 dBm and sweeping the frequency from 3.3 GHz to 3.8 GHz, so drain efficiency and gain can be tested. The measurement's outcomes are really close to the simulations' results. Figure 3.6 shows the saturated output power obtained at different frequencies, which is equal to 38.7 dBm on average. This value is really close to the simulated one, that is 39.7 dBm on average.

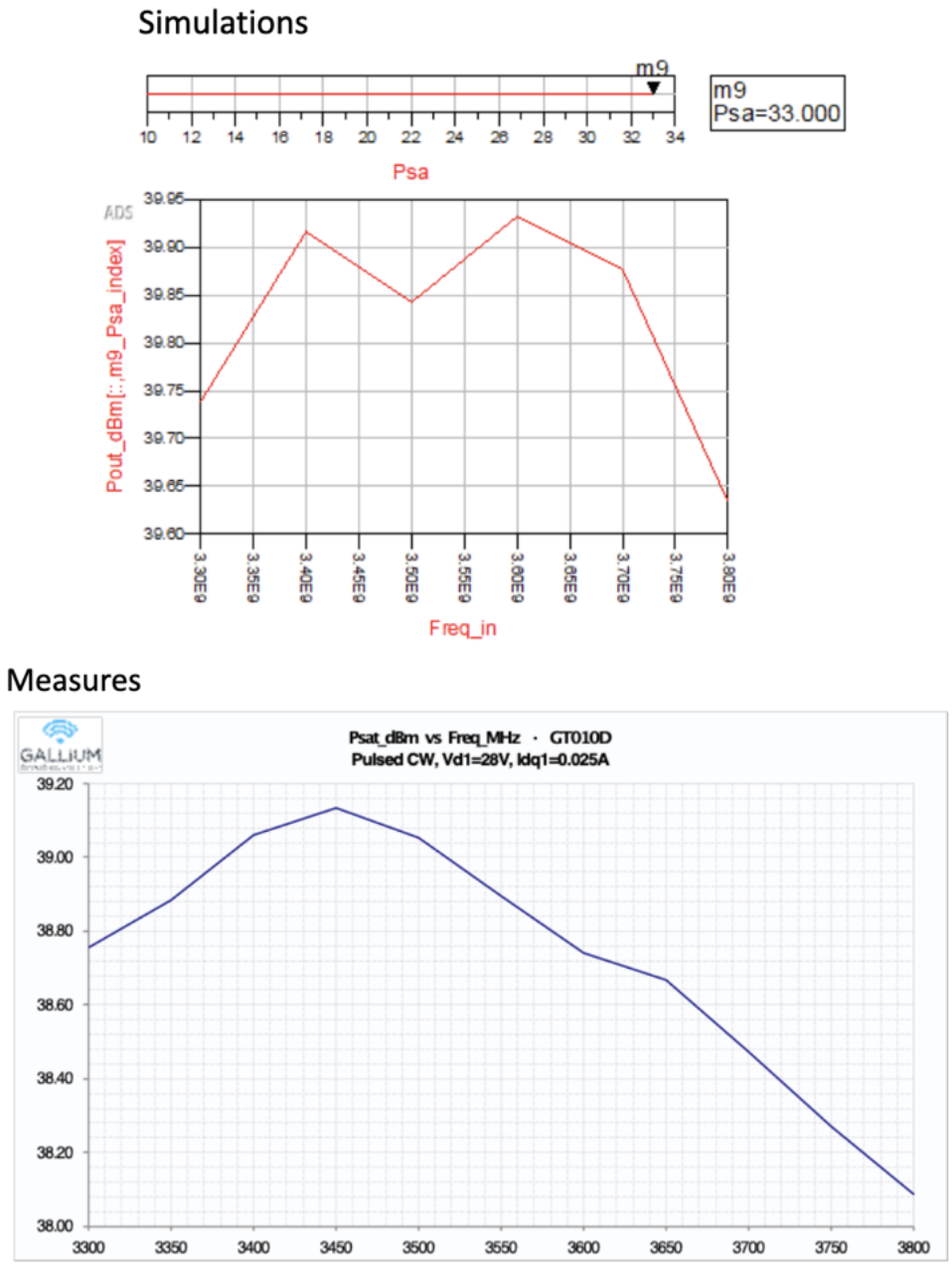


Figure 3.6: Single Branch Amplifier PCB's measurement: Saturated output power - comparison with the corresponding simulation

Figure 3.7 compares the amplifier's gain obtained through the simulations and the gain measured. Considering a 6 dB back-off point, the measured gain (bottom) is equal to 14.42 dB on average, whereas the simulated gain (top) is equal to 13.83 dB on average.

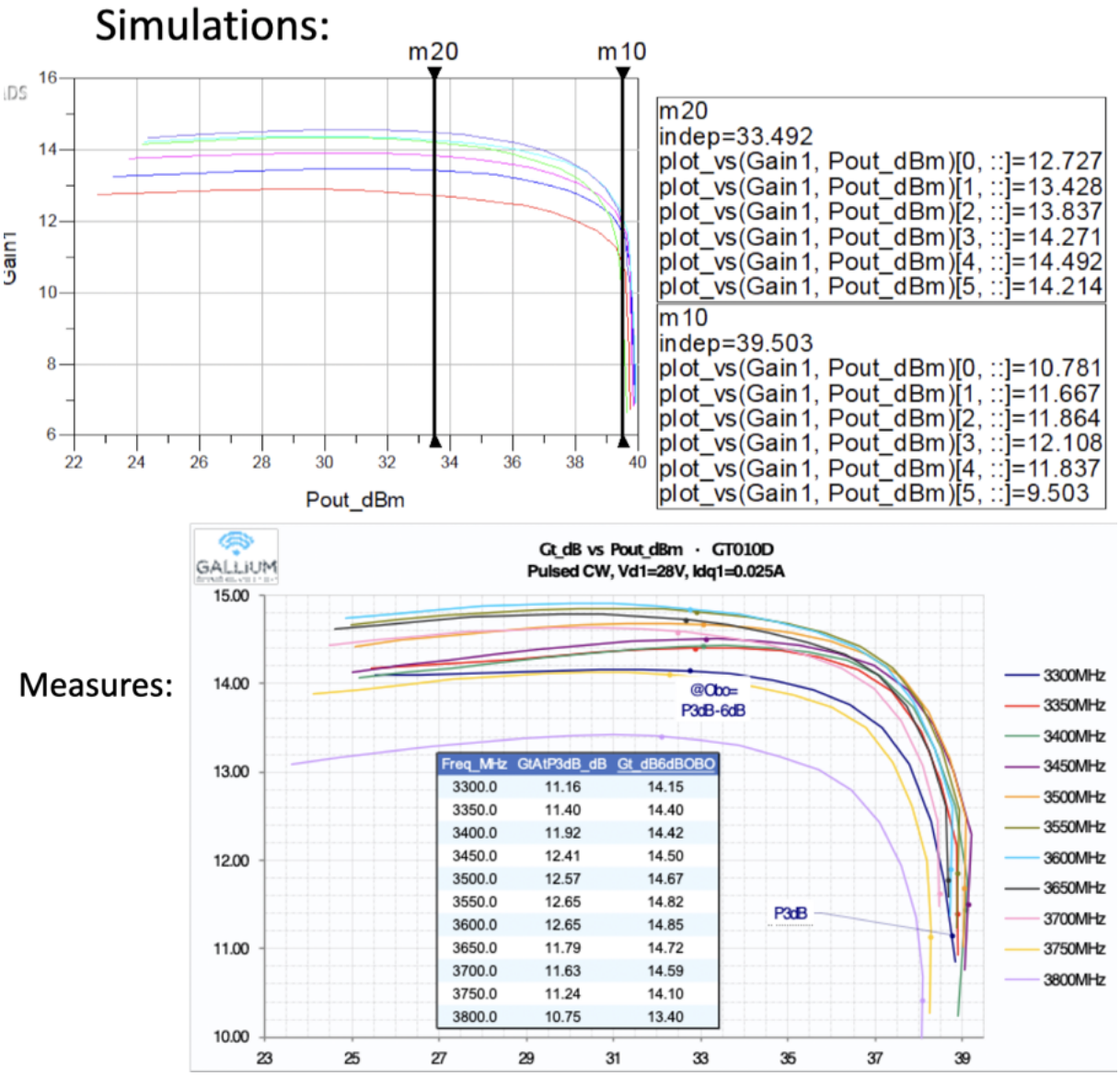


Figure 3.7: Single Branch Amplifier PCB's measurement: Gain - comparison with the corresponding simulation

As depicted in Figure 3.8, the maximum Drain Efficiency obtained from the simulations is equal to 53% and to 29.37% at 6dB of output back-off. The measurements case turn out to be even better: the maximum achievable efficiency is 58.29% on average and at 6dB of back-off is equal to 31.50%.

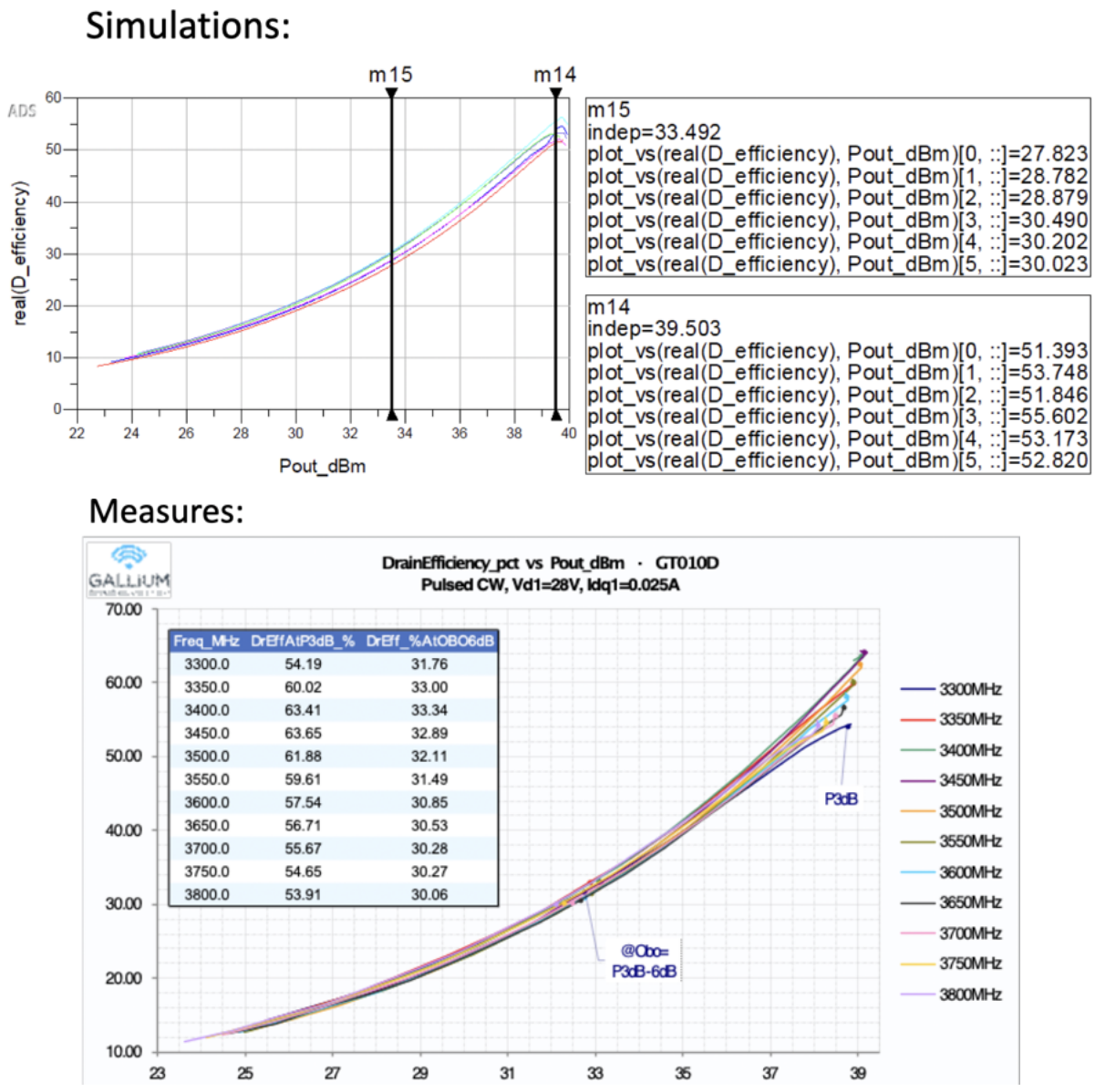


Figure 3.8: Single Branch Amplifier PCB's measurement: Drain Efficiency - comparison with the corresponding simulation

3.2 Balanced Amplifier

Since it was proved that the Single Branch Amplifier works properly, the Balanced Amplifier can be tested. Figure 3.9 shows the setup diagram and Figure 3.10 a photo of the corresponding setup.

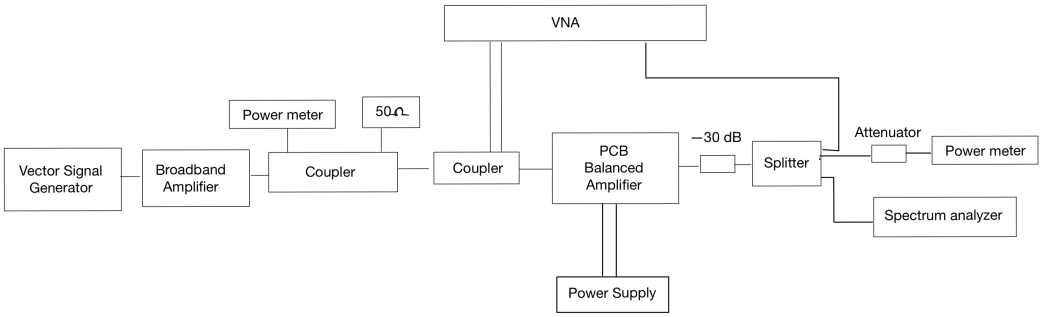


Figure 3.9: Measurement setup diagram in order to test the Balanced Amplifier PCB

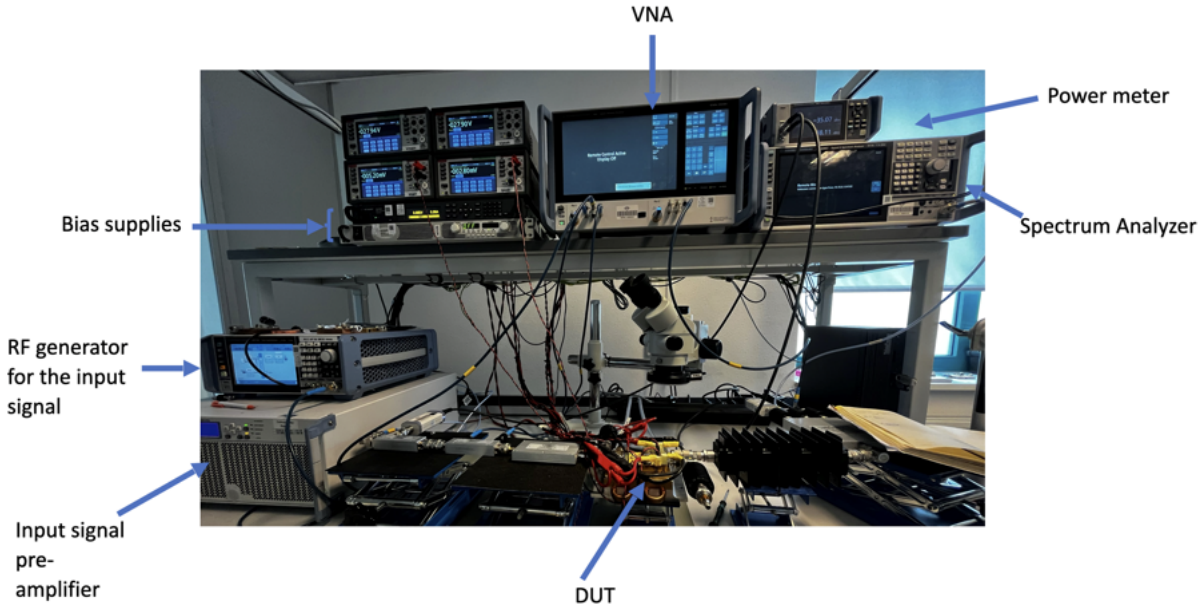


Figure 3.10: Measurement setup in order to test the Balanced Amplifier PCB

By acting in the same way as in the Single Branch Amplifier case, the first performed measurement was the Scattering Parameters one, which employs the VNA: Figure 3.11 shows S_{21}'s evolution through frequency. The average measured value is 14.34dB as in the Single Transistor Amplifier's measure (Figure 3.5), as expected.
S_{11} is not shown because it's irrelevant due to the presence of input and output couplers. When the S-Parameters measurements were performed at the ends of the Balanced Amplifier's board, the return loss was measured considering the couplers, which are designed for providing good matching at 50 Ω. This is the reason why S_{11} is now ignored.

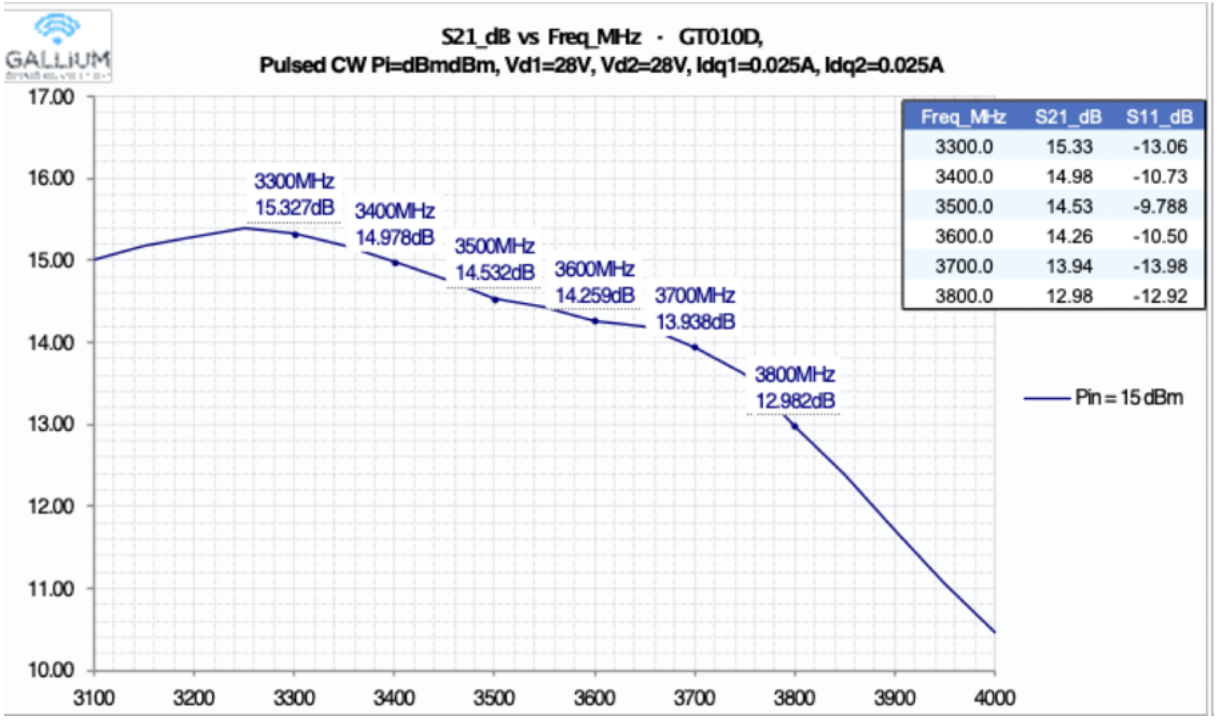


Figure 3.11: Balanced Amplifier PCB's measurement: S-Parameters

The Balanced Amplifier's input power split equally in two parts thanks to the input coupler. Consequently the input power level used in the Single Branch Amplifier for performing One Tone measurements needs to be doubled, in order to compare properly the results. Hence, the input power level used is 28 dBm while the frequency sweeps across the bandwidth of interest. Given the presence of two amplifying branches, the saturated output power is expected to be doubled with respect to the Single Branch case. Figure 3.12 shows the comparison between the saturated output power related to the Balanced Amplifier and the one related to the Single Branch Amplifier. The first one is 41.34 dBm on average and the second is 38.67 dBm on average, meaning that the output power's doubling actually takes place.

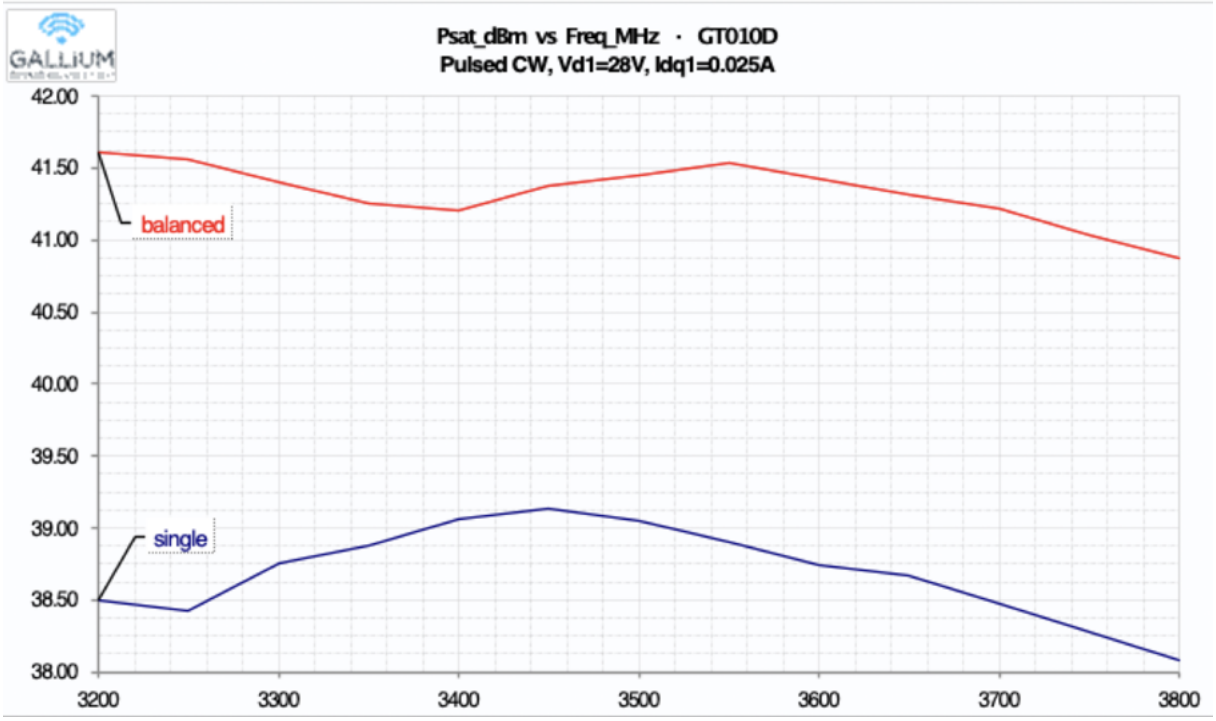
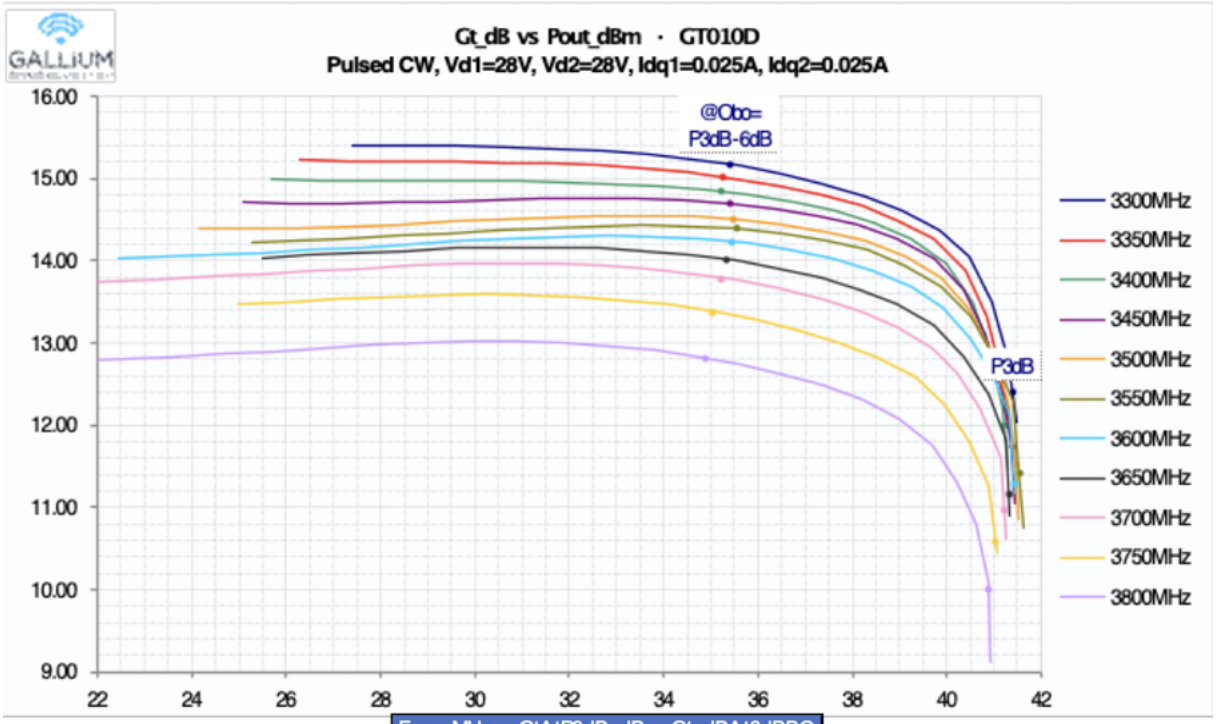


Figure 3.12: Balanced Amplifier PCB's measurement: Saturated Output Power - comparison with the Single Branch Amplifier measure

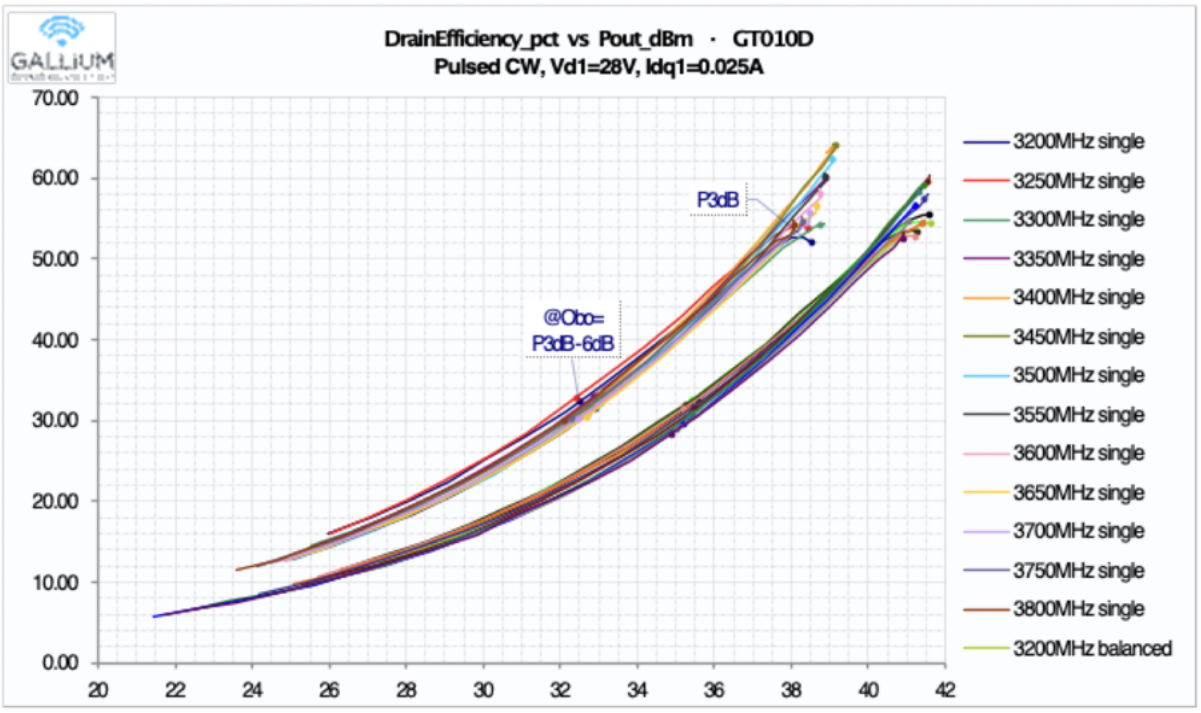
Figure 3.13 shows the Balanced Amplifier's Gain. Its average value over frequency is 14.26 dB, which is in line with the average value measured in the Single Branch Amplifier case (14.42 dB). The BA's gain is a little bit lower than the Single Branch's value because of additional losses due to the couplers.



Freq_MHz	GtAtP3dB_dB	Gt_dBAt6dBBO
3300.0	12.41	15.17
3350.0	12.23	15.02
3400.0	12.00	14.85
3450.0	11.75	14.70
3500.0	11.54	14.51
3550.0	11.43	14.39
3600.0	11.30	14.23
3650.0	11.17	14.02
3700.0	10.97	13.79
3750.0	10.59	13.38
3800.0	10.02	12.82

Figure 3.13: Balanced Amplifier PCB's measurement: Gain

The last performance parameter analysed and compared is the Drain Efficiency. Figure 3.14 shows the Drain Efficiency's evolution versus the Output Power. The same parameter regarding the Single Branch Amplifier is plotted on the same graph. It's difficult to compare the different curves because of the output power level difference between the two amplifiers. Figure 3.15 shows the comparison at 3 dB and at 6 dB of Output Back-Off. The Single Branch and the Balanced Amplifiers show the same Drain Efficiency at the same back-off level.



Freq_MHz	DrEffAtP3dB_%	DrEff_%At6dBBO
3300.0	54.56	32.49
3350.0	53.40	31.91
3400.0	52.86	31.43
3450.0	54.38	31.55
3500.0	57.39	31.66
3550.0	59.59	31.44
3600.0	59.27	30.78
3650.0	58.41	30.37
3700.0	56.62	29.63
3750.0	54.63	28.97
3800.0	52.65	28.29

Figure 3.14: Balanced Amplifier PCB's measurement: Drain Efficiency

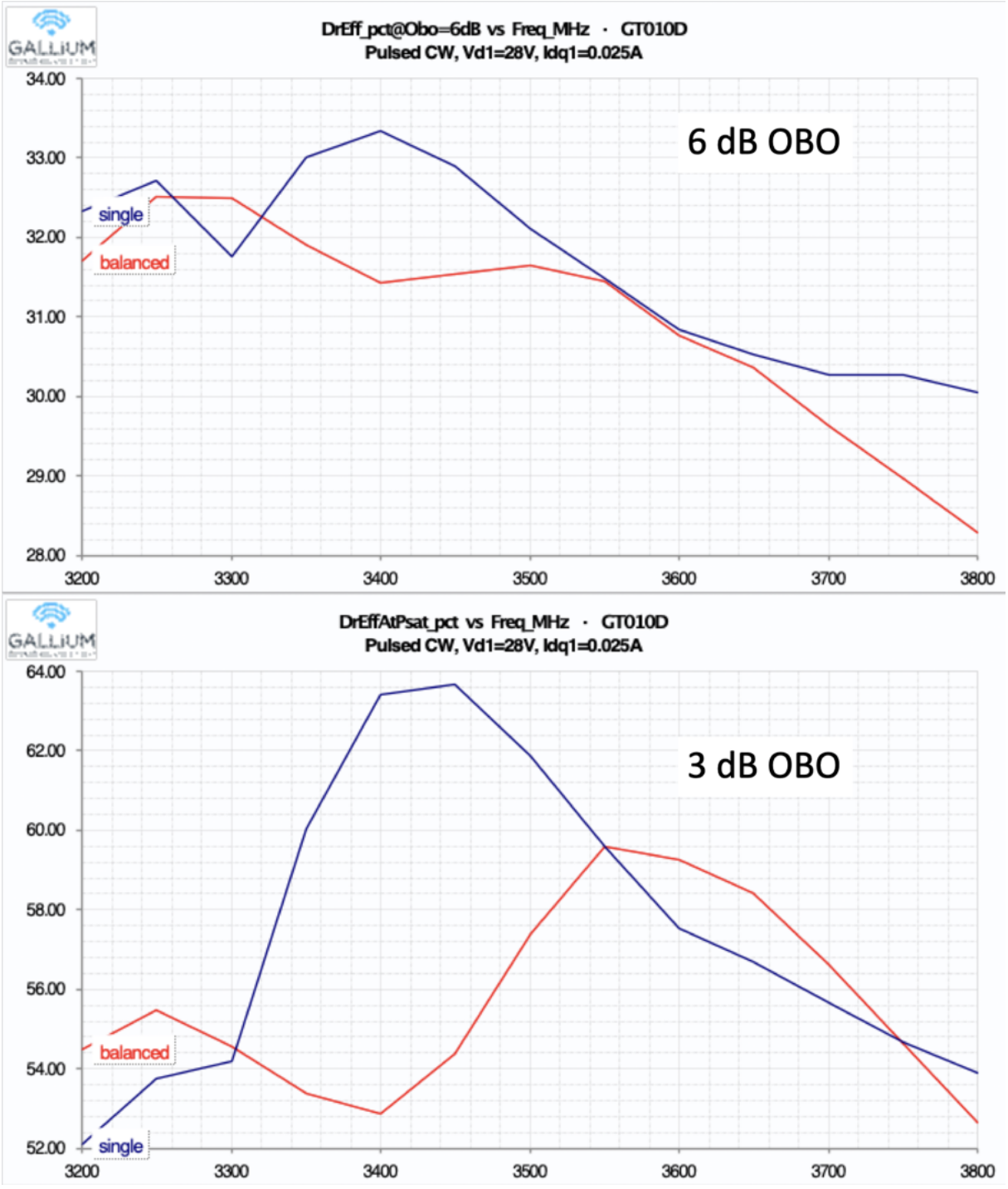


Figure 3.15: Balanced Amplifier PCB's measurement: Drain Efficiency - Comparison with the Single Branch Amplifier case

The values of some components needed to be changed in comparison to the Single Branch Amplifier BoM (Table 3.1) due to the presence of the input and output couplers which aren't ideal components. Hence, the return loss related to the output port and the one related to the coupled port are different and the two ports don't display exactly 50 Ω.

In order to obtain the desired performances, which were presented above for the Single Transistor Amplifier, and keep the two branches equal, the values displayed in the following BoM are needed (Table 3.2).

Table 3.2: Final Bill of Materials of the Balanced Amplifier

Components List	Reference	Part No.	Manufacturing
PCB	RO4350B, 20mil, 35um Cu	PCB-23-62	Euro Circuits
T1	6X3 mm DFN	GT010D	Gallium Semiconductor
T2	6X3 mm DFN	GT010D	Gallium Semiconductor
C1, C10	2.7pF Capacitor, 0805. INMAT	ATC 600F1R6	ATC
C2, C11	0.4pF Capacitor, 0805. INMAT	ATC 600F0R4	ATC
C3, C12	5.6pF Capacitor, 0805. INMAT/Stab network	ATC 600F0R9	ATC
R1, R3	5.1 Ohm Resistor, 0805. INMAT/STAB		Yageo
R2, R4	5.1 Ohm Resistor, 0805. INMAT/Gate Feeder		Yageo
C4, C13	5.6 pF Capacitor, 0805. Gate Feeder (most right position)	ATC 600F5R6	ATC
C5, C14	0.6pF Capacitor, 0805. OUTMAT	ATC 600F0R6	ATC
C9, C18	10 nF Capacitor, 0805. Gate Feeder	GRM2165C2A103J	Murata
C6, C15	3pF Capacitor, 0805. OUTMAT	ATC 600F4R3	ATC
C7, C16	4.7 pF + 1.8 pF right side Capacitor, 0805. OUTMAT/ Drain Feeder	ATC 600F5R1	ATC
C8, C23, C17, C24	10 µF Capacitor, 1210. Decoupling	GRM32EC72A106K	Murata
C19, C20	220 µF Electrolytic Capacitor, 12.5 mm	EEV-FK1J221Q	Panasonic
C21, C22	22 µF, 1210	GRM32ER71C226K	Murata
R5, R6	10 kOhm, 0603	RT0805DRD0710KL	Yageo
C25, C27	100 nF Capacitor, 0805	GRM21BR7cx2C2A104K	Murata
C26, C28	10 µF Capacitor, 0805	GRM21BC71E106K	Murata
R13, R14	10 Ohm, 0603	RC0603JR	Yageo
J5, J6	Female SMA connector, 12.7 mm flange	23_SMA-50-0-2/111_NE	Huber+Suhner
C29	10 pF Capacitor, 0603. (vertical)	ATC 600F100	ATC
X1, X2	RF DIR COUPLER	X3C35F1-03S	TTM Technologies

Modulated Measurements were performed on the Balanced Amplifier in order to verify its linearity, too. The modulated signal chosen for the measurement is an LTE signal with a 5 MHz bandwidth and 8 dB PAR (Peak to Average Power Ratio). The input signal's spectrum is shown in Figure 3.16.

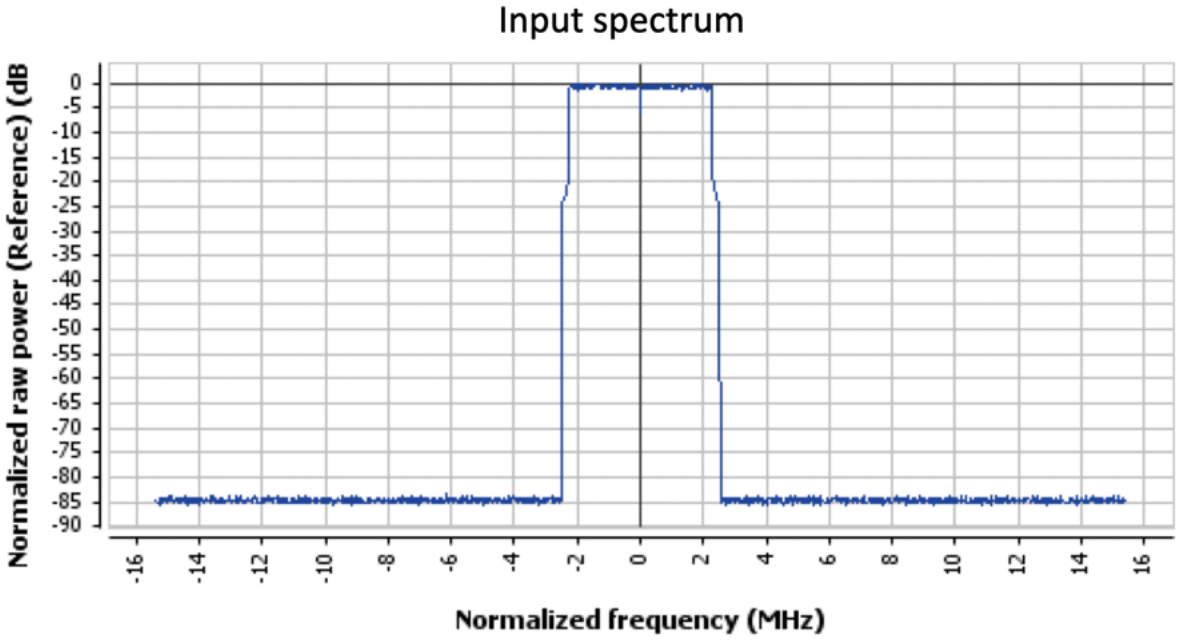


Figure 3.16: Spectrum of the input signal for Modulated Measurement: LTE signal 5MHz bandwidth and 8 dB PAPR

The measurement has been repeated for different frequencies belonging to the bandwidth of interest and each of them reveled good linearity showing a good ACPR (Adjacent Channel Power Ratio), which is always less than -33.92 dBc (Figures 3.17, 3.18, 3.19 and 3.20).

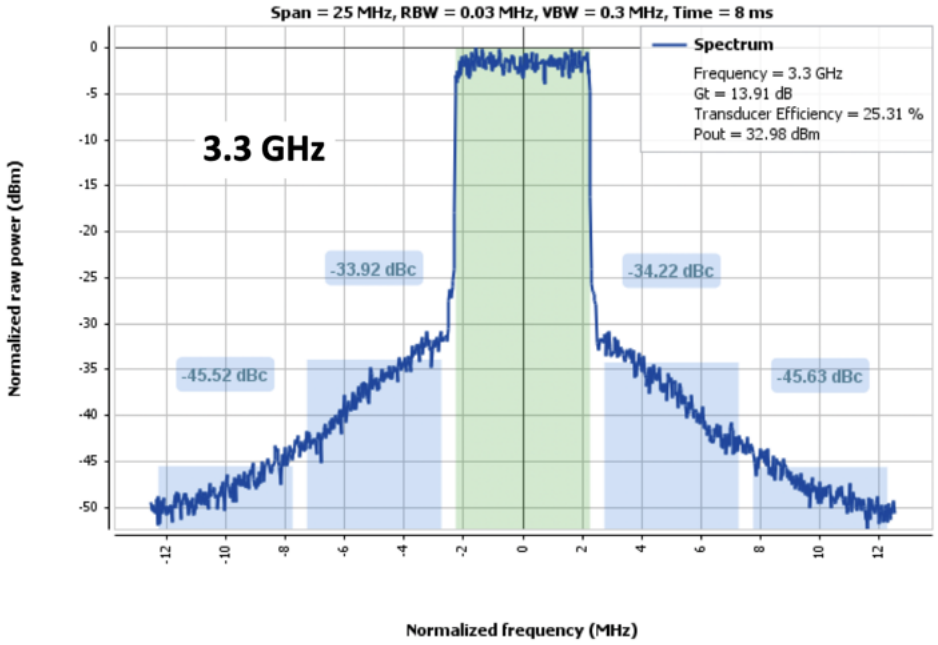


Figure 3.17: Spectrum of the output signal for Modulated Measurement of the Balanced Amplifier - 3.3GHz

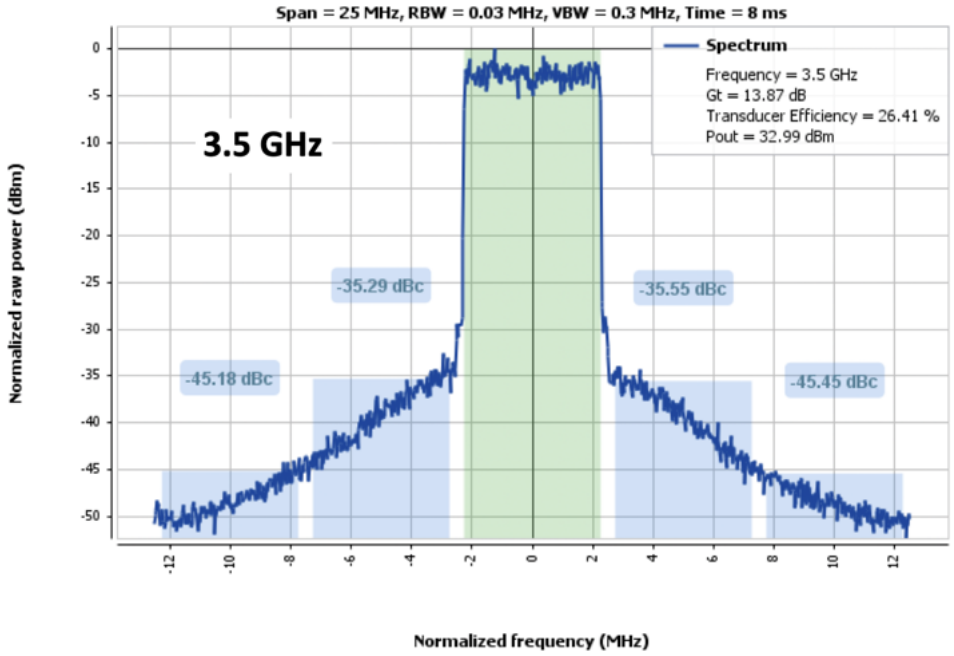


Figure 3.18: Spectrum of the output signal for Modulated Measurement of the Balanced Amplifier - 3.5GHz

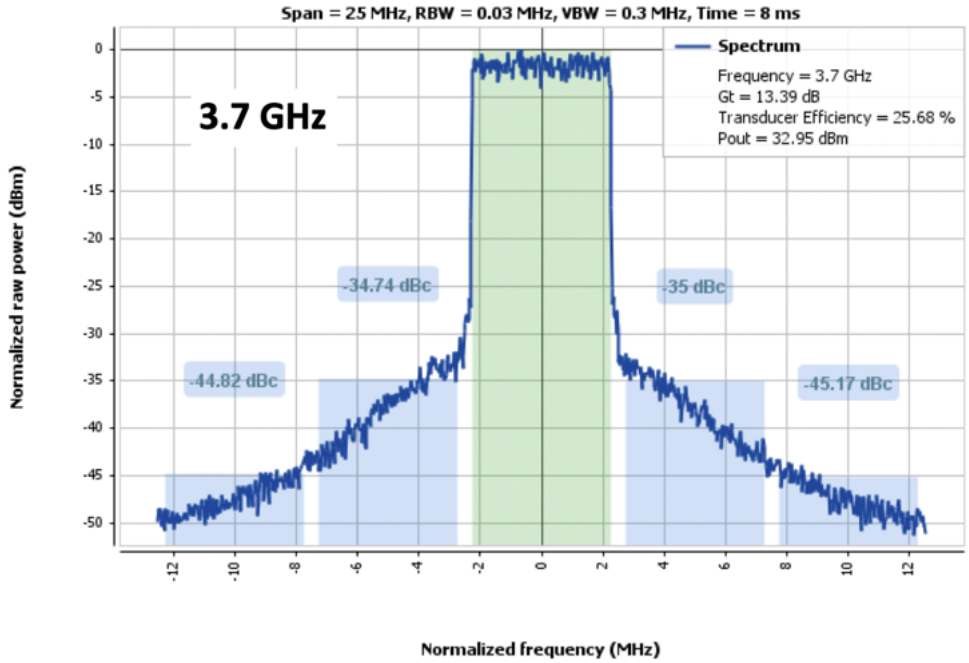


Figure 3.19: Spectrum of the output signal for Modulated Measurement of the Balanced Amplifier - 3.7GHz

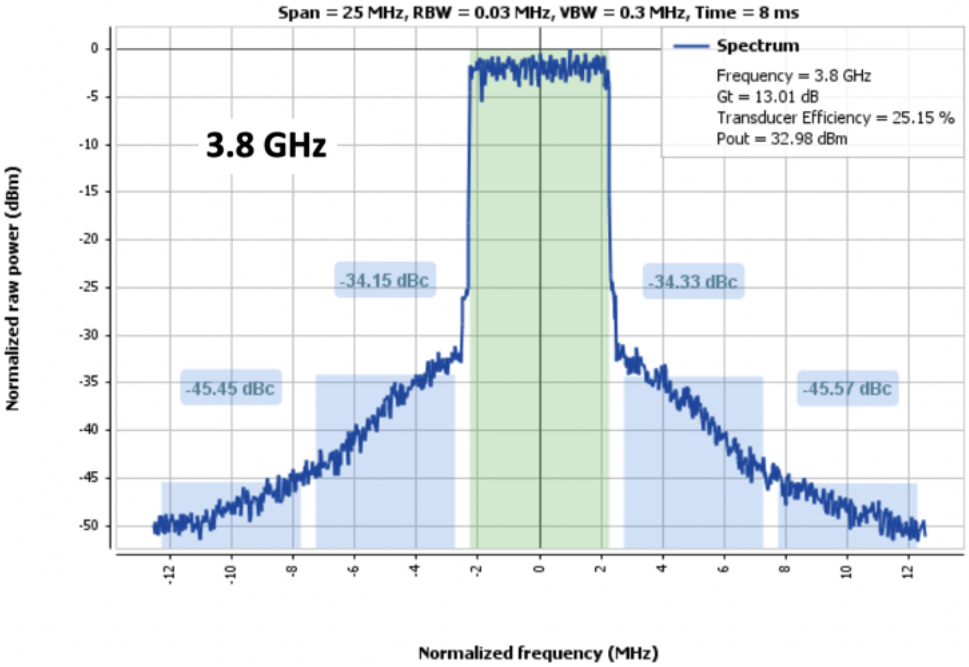


Figure 3.20: Spectrum of the output signal for Modulated Measurement of the Balanced Amplifier - 3.8GHz

3.3 LMBA

The board depicted in Figure 3.3 needs to be tested in the end. Since it has two output ports, the board allows to inject the control signal in one of them. The BoM used is the one obtained by tuning the values of the Balanced Amplifier's components (Table 3.2).

Figure 3.21 shows the setup diagram for executing measurements on the LMBA. The setup realization is showed in Figure 3.22.

The control signal is here generated by a second signal source, in order to control its amplitude better and to be able to sweep the phase in a simple way. The two sources share the same reference signal, so they can be synchronized. The usage of two different signal sources for the input signal and for the control signal allows to change the control signal phase independently.

As previously described, the efficiency of the Load Modulated Balanced Amplifier depends on the amplitude and the phase of the control signal injected. Some measurements were performed by keeping the control signal amplitude constant at 32 dBm and changing the phase from -180° to +180°. The Drain Efficiency proves to be rotating around the Balanced Amplifier's value on a Drain Efficiency versus Output Power graph [2], as shown in Figure 3.23. Those plots reveal the importance of choosing the right phase for the control signal, which could cause a deterioration of the performance. Therefore, by looking at those plots the optimum phase value can be selected to maximize the efficiency, without decreasing the output power too much.

The selected values of the phase of the control signal generated by the corresponding generator for each frequency won't be displayed here. They are indeed peculiar to the shown setup because of the uncontrolled phase shifts caused by cables and connectors with respect to the phase shift imposed by the signal generator.

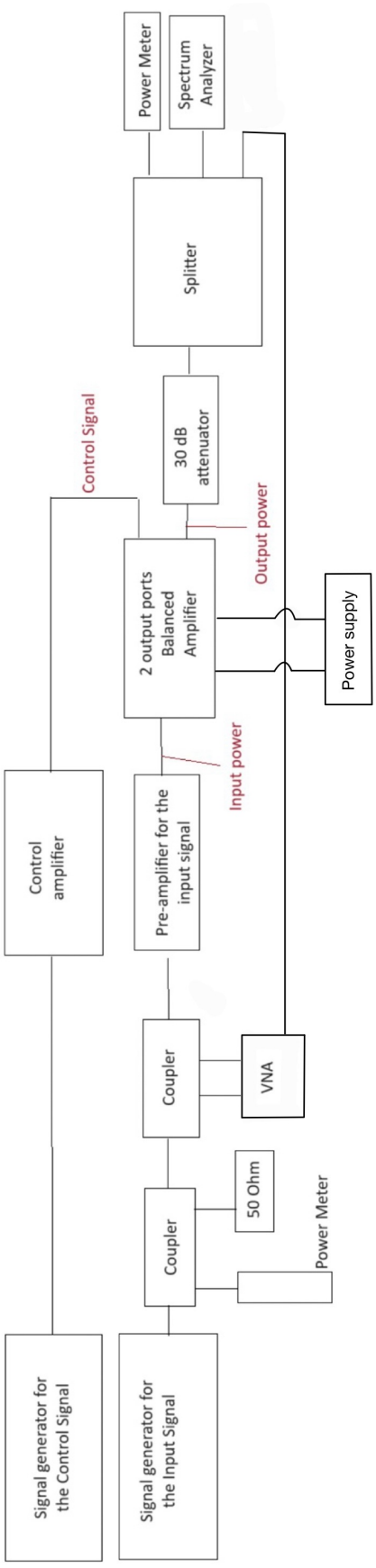


Figure 3.21: Measurement setup diagram to test the LMBA PCB

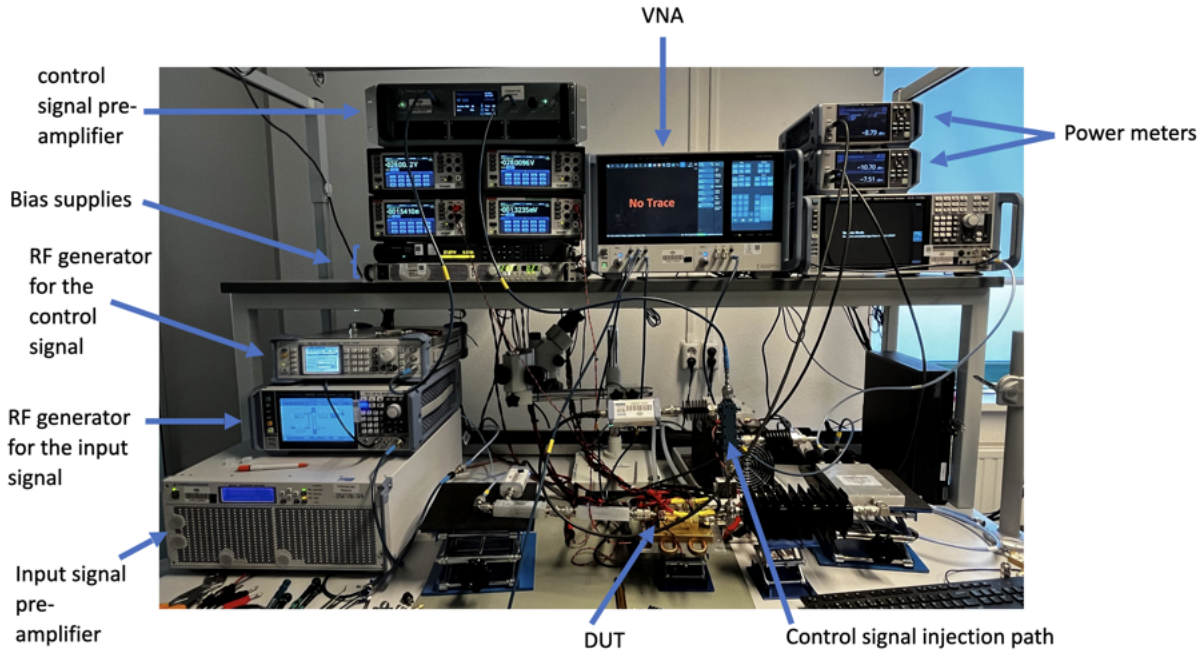


Figure 3.22: Measurement setup to test the LMBA PCB

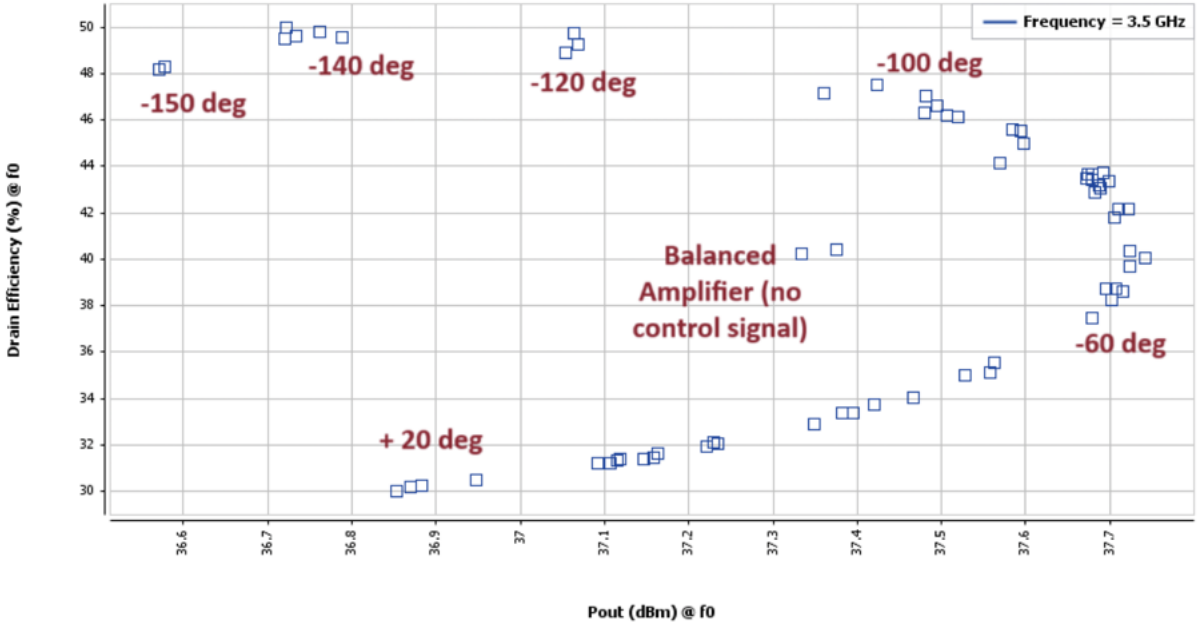


Figure 3.23: Drain Efficiency Contours - measurements

The final performances are shown in Figures 3.24, 3.25, 3.26 and 3.27.
The first and the second pictures show the output power plot versus the input available power. The plot related to the LMBA is shown in the first graph, whereas a comparison between the LMBA and the BA cases is shown in the second one. The saturated output power is placed around 40 dBm in both cases.

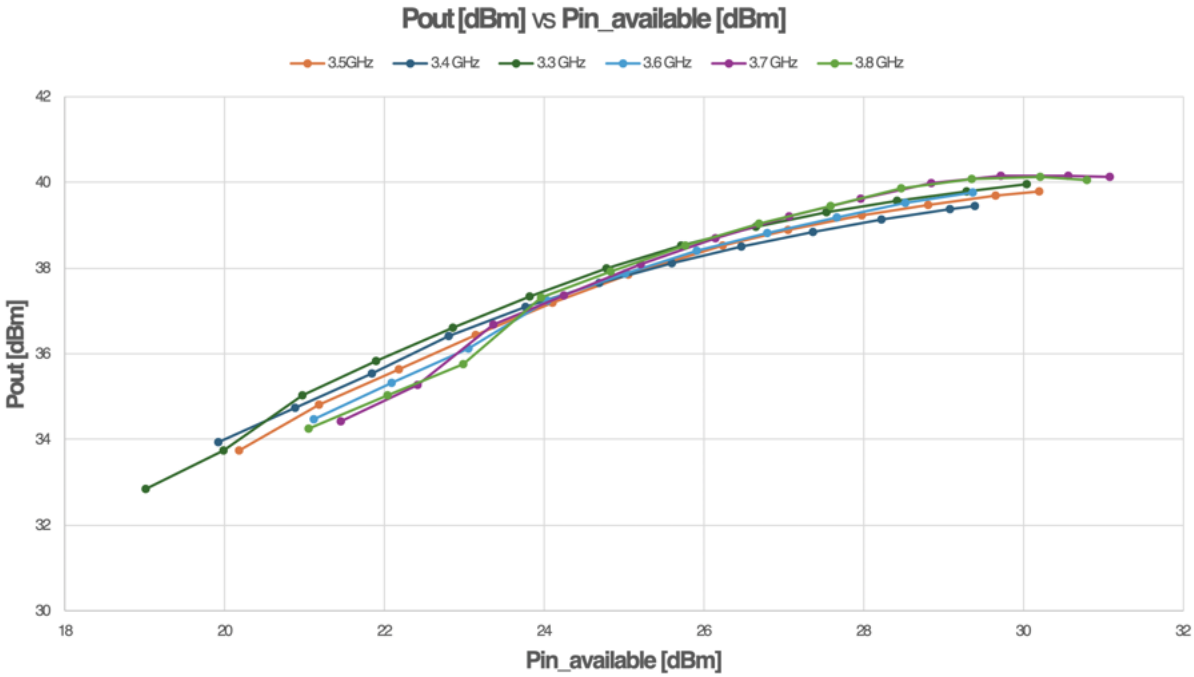


Figure 3.24: LMBA PCB's measurement: Pout VS Pin

The Gain plot is then displayed in the next picture 3.26. Its value is equal to 13.5 dB on average at small signals.
The last picture shows the Drain Efficiency's improvement, which is the ultimate aim of the LMBA amplifier, moving from 30% at 6 dB OBO for the Balanced Amplifier to 52.2% for the LMBA.

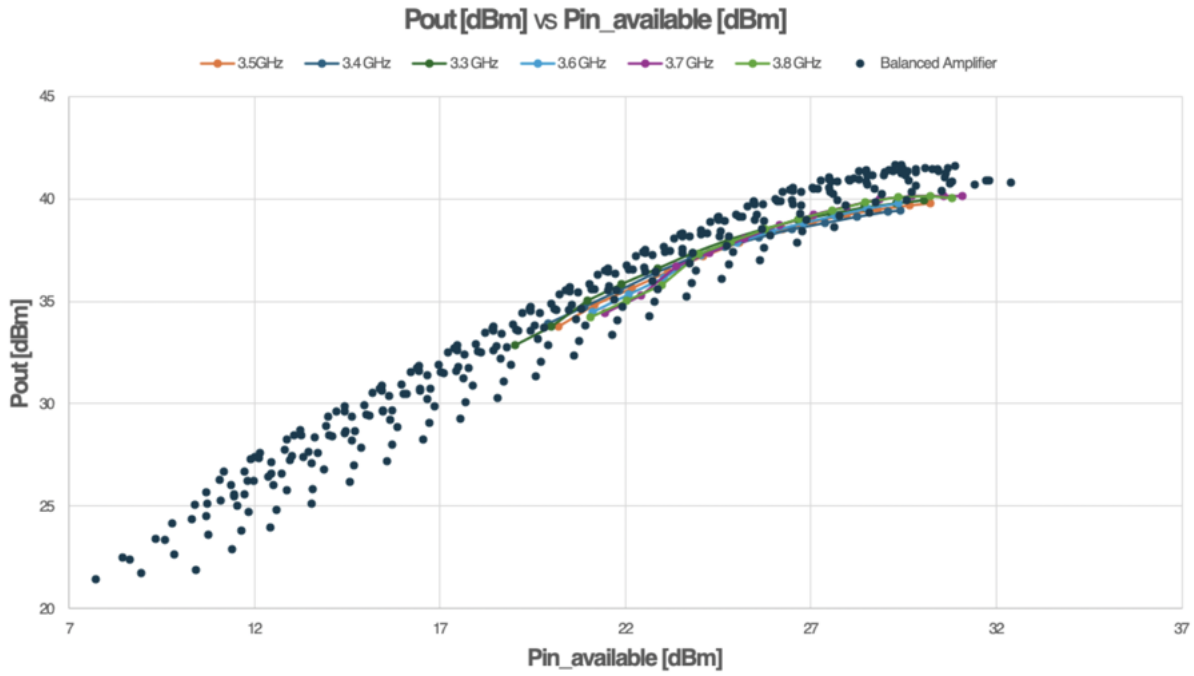


Figure 3.25: LMBA PCB's measurement: Pout VS Pin - comparison with the Balanced Amplifier

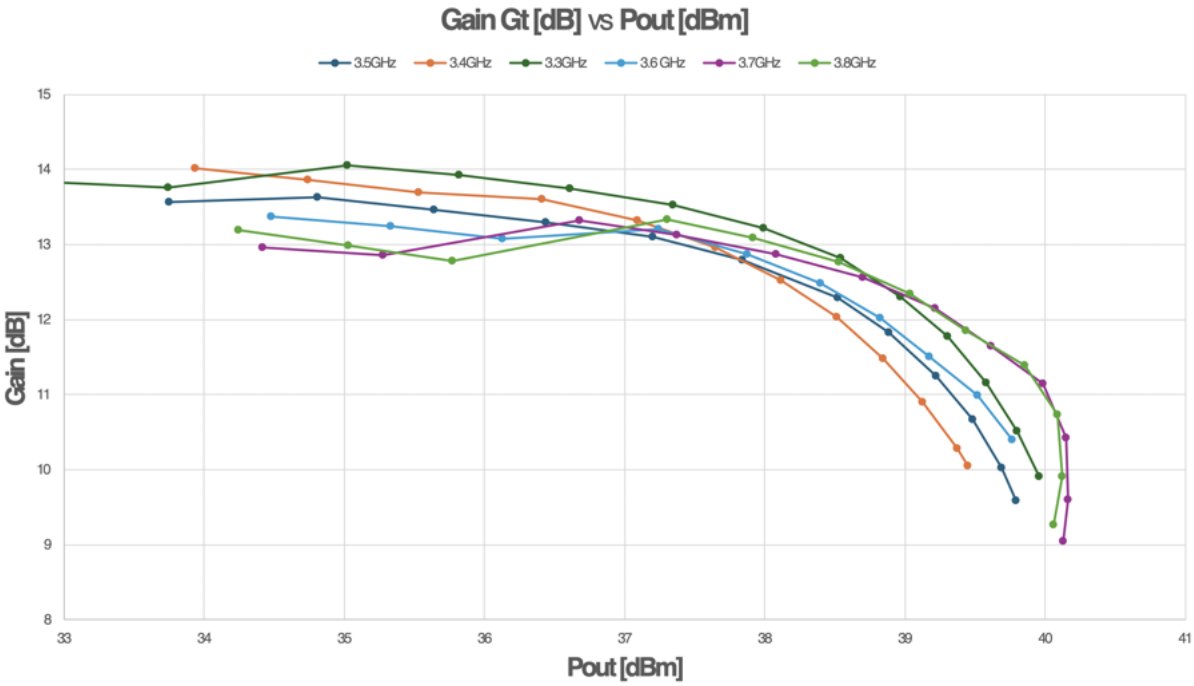


Figure 3.26: LMBA PCB's measurement: Gain

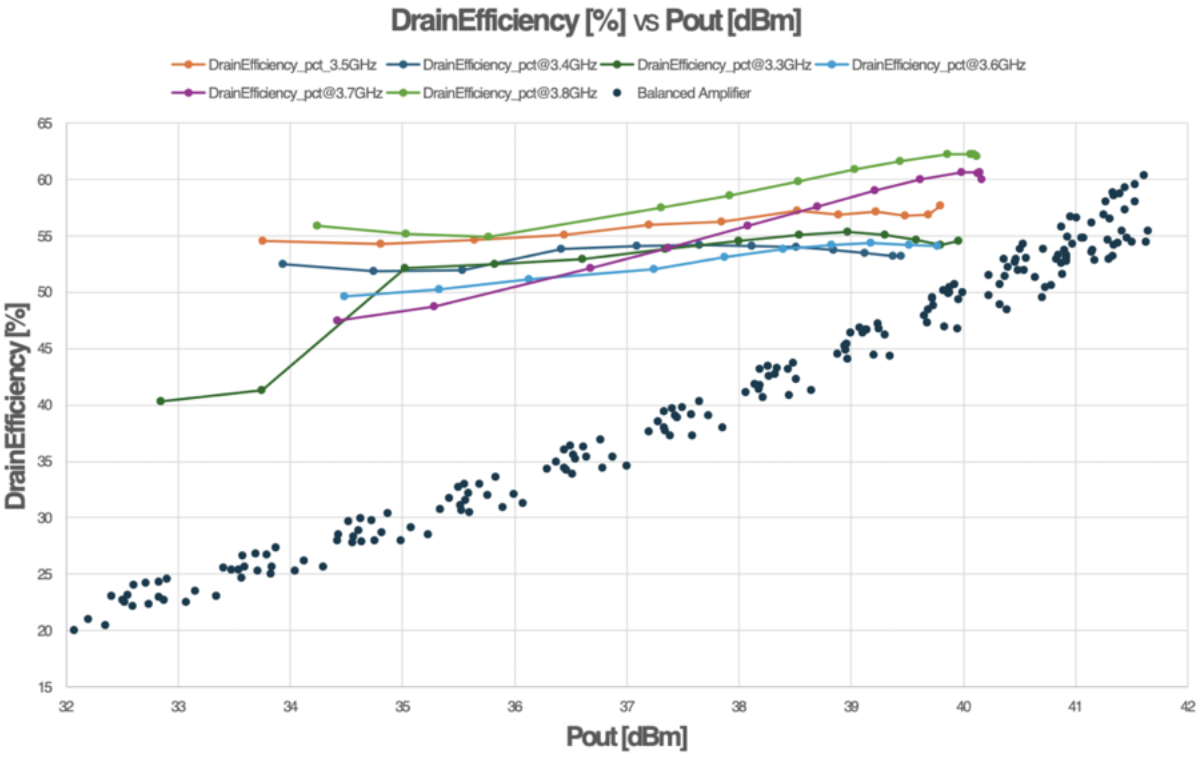


Figure 3.27: LMBA PCB's measurement: Drain Efficiency - comparison with the Balanced Amplifier

The last performed measurements were Modulated ones at some different frequencies included in the range of interest. The spectrum of the input signal employed was the same used for the Balanced Amplifier's tests, which is shown in Figure 3.16: an LTE signal with a 5 MHz bandwidth and 8 dB PAR. The two signal sources configuration of the LMBA isn't suitable for performing measurements with modulated signal, because it would require an external modulator to generate the control signal [4]. For this reason an off-the-shelf divider was used to split the signal generated in two equal parts: one goes to the input port of the DUT and the other to the control signal port. By using attenuators, the control signal amplitude is kept at the desired value of 32 dBm, which is in the middle between the 31dBm used in the schematic simulation in Section 2.1 and 33 dBm used in the layout-schematic simulation in Section 2.2. Figure 3.28 shows the setup diagram, whereas the real setup realised is shown in Figure 3.10. The measure has been repeated for 3.35GHz, 3.5GHz, 3.65GHz and 3.8GHz and each of them revealed good linearity showing a good ACPR (Adjacent Channel Power Ratio), which is always less than -27.85 dBc (Figures 3.30, 3.31, 3.32 and 3.33).

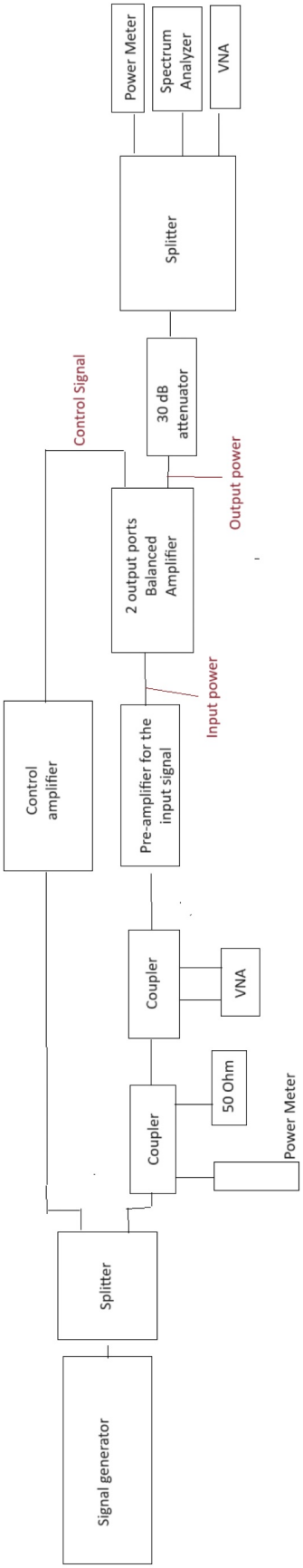


Figure 3.28: Measurement setup diagram for performing modulated measurements on the LMBA

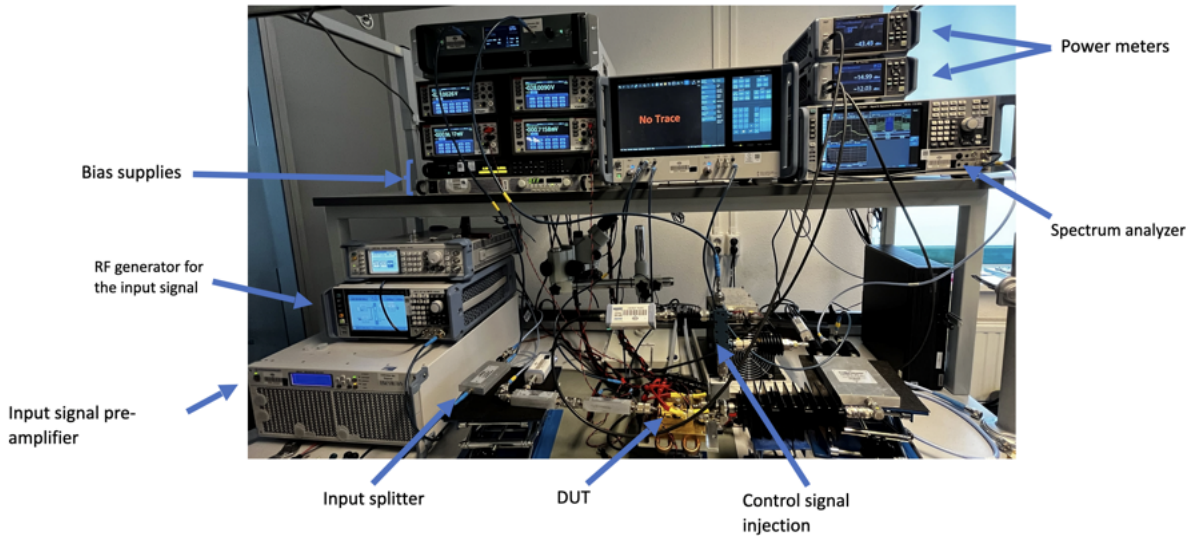


Figure 3.29: Measurement setup for performing modulated measurements on the LMBA

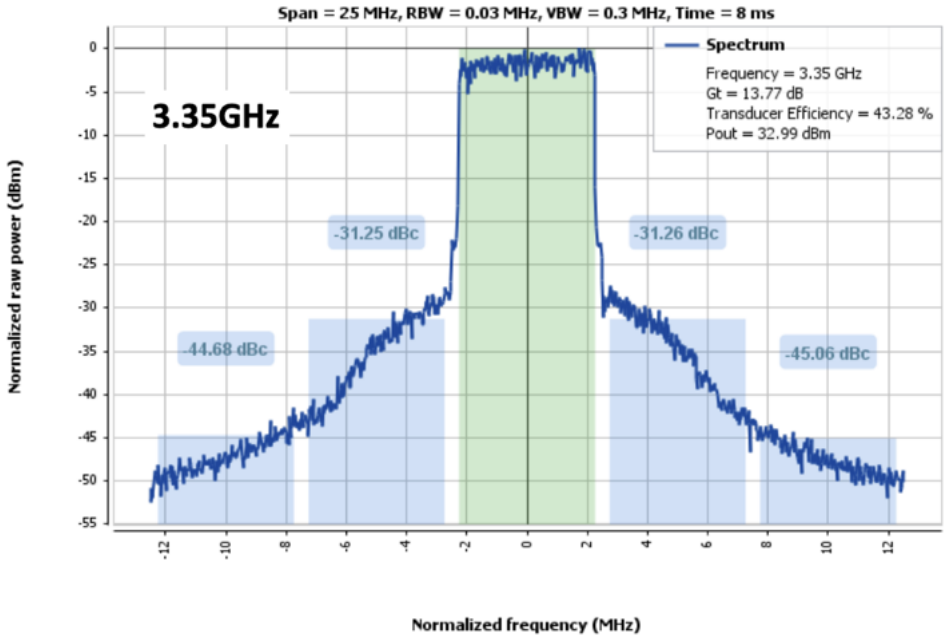


Figure 3.30: Spectrum of the output signal for Modulated Measurement of the LMBA - 3.35GHz

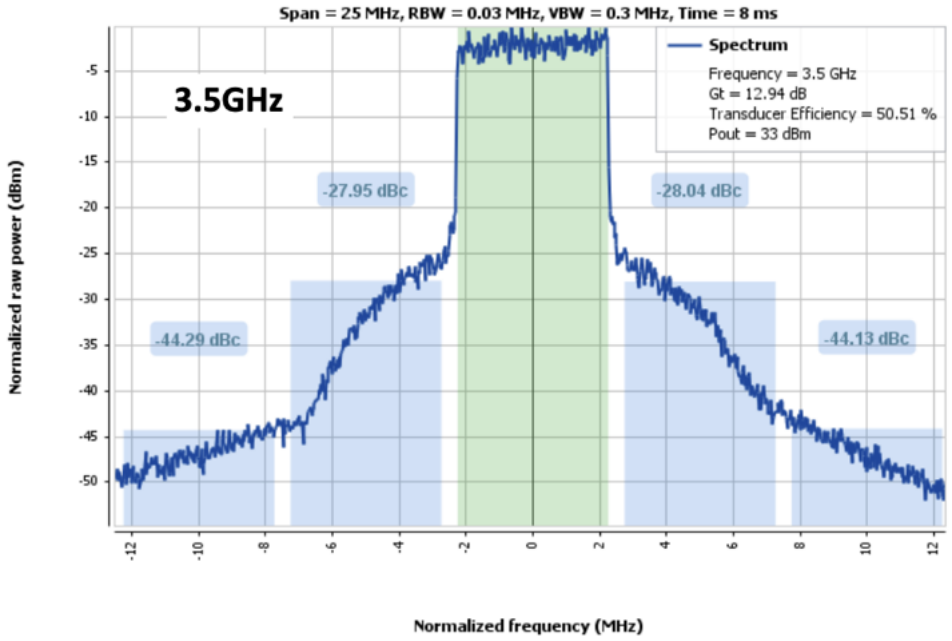


Figure 3.31: Spectrum of the output signal for Modulated Measurement of the LMBA - 3.5GHz

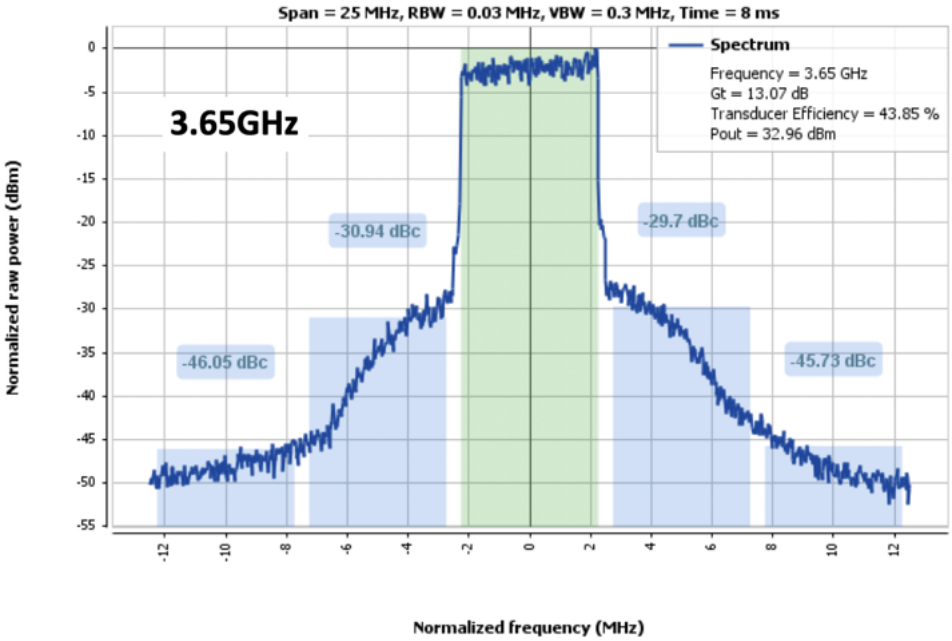


Figure 3.32: Spectrum of the output signal for Modulated Measurement of the LMBA - 3.65GHz

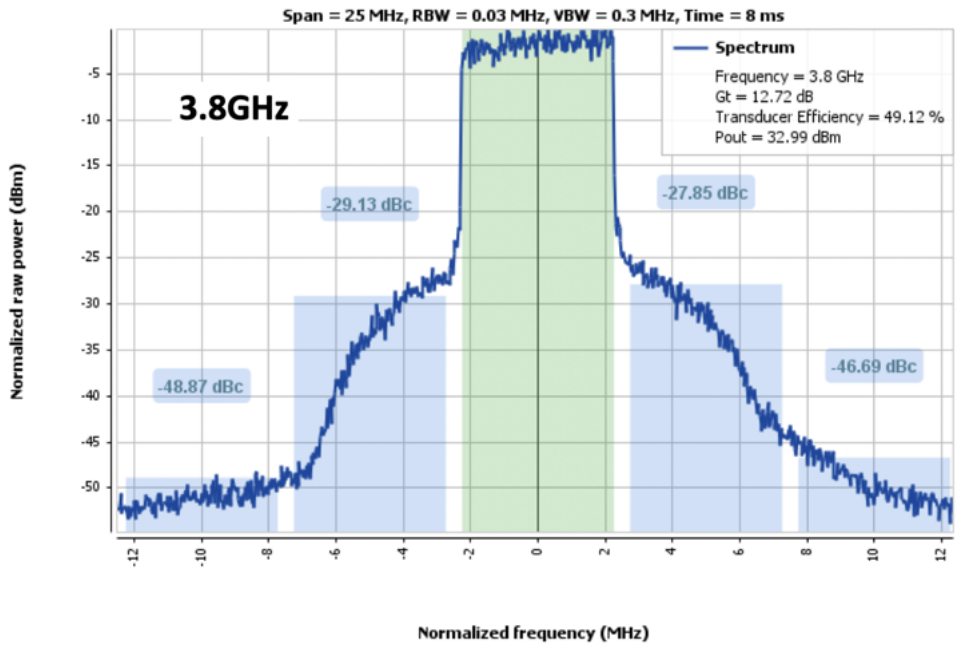


Figure 3.33: Spectrum of the output signal for Modulated Measurement of the LMBA - 3.8GHz

Conclusion

The recently introduced Load Modulated Balanced Amplifier architecture has been analysed, designed and demonstrated in this thesis work.

The design process has been carried out to make the amplifier work from 3.3 GHz to 3.8 GHz. The study started with a simple single transistor amplifier in order to obtain a stable and good matched amplifier working in class AB. In the second place, this single branch has been doubled to obtain a Balanced Amplifier, which developed into an LMBA when a control signal was injected into the normally isolated port of the output coupler, having realised a board with two output ports. The LMBA's working principle has been confirmed since an average efficiency equal to 52.5% at 6dB OBO was obtained with a peak output power of 40 dBm on average. Furthermore, the LMBA was proved to have a good linearity even without the introduction of Digital Pre-Distortion, showing a maximum ACPR equal to -27.85 dBc over the band.

The amplitude of the injected control signal was kept constant as a simplification and the LMBA was tested by employing two different signal generators, except for the modulated measurements.

Future developments of this project could include the design of a control signal amplifier modifying the control signal amplitude with the input power level. This RF input version of the LMBA can be implemented by designing a Control Amplifier working in class C and turning on at an input power level congruent with the range of the application. The usage of the control signal is reasonable, indeed, only for quite high values of the input power. For very low values of the input power, the control signal power level risks to be higher than the output power coming from each of the main branches of the LMBA, which makes the usage of the LMBA meaningless.
Another open challenge for future development is trying to precisely control the phase shift of the control signal at the normally isolated port of the output coupler.

Appendix A

Equations for performance calculation

Equations used for obtaining the performance of an ADS simulation:

Input Power in Watt: $P_{in,rf} = \frac{1}{2} * real(I^*_{in,rf} * V_{in,rf})$

Input Power in dBm: $P_{in,dBm} = 10 * log_{10}(P_{in,rf}) + 30$

Output Power in Watt: $P_{out,rf} = \frac{1}{2} * real(I^*_{out,rf} * V_{out})$

Output Power in dBm: $P_{out,dBm} = 10 * log_{10}(P_{out,rf}) + 30$

DC Power: $P_{DC} = I_{g,DC} * V_{g,DC} + I_{d,DC} * V_{d,DC}$

Gain in dB: $Gain_{dB} = P_{out,dBm} - P_{in,dBm}$

Load: $Z_l = \frac{V_d[1]}{I_d[1]}$

Drain Efficiency for the Single Transistor Amplifier and for the Balanced Amplifier: $DEfficiency = real(\frac{P_{out,rf}}{P_{DC}}) * 100$

Control Signal Power in Watt: $P_{CS} = \frac{1}{2} * real(I^*_{CS} * V_{CS})$

Hypothetical efficiency of the control signal amplifier: Eff_{CS} set at 70% for the calculation

Drain Efficiency for the LMBA: $DEfficiency = real(\frac{P_{out,rf}}{P_{DC} + \frac{P_{CS}}{Eff_{CS}}}) * 100$

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