ALMA MATER STUDIORUM - UNIVERSITÀ DI BOLOGNA

SCUOLA DI INGEGNERIA E ARCHITETTURA

DIPARTIMENTO di
INGEGNERIA DELL'ENERGIA ELETTRICA E DELL'INFORMAZIONE
"Guglielmo Marconi"
DEI

CORSO DI LAUREA MAGISTRALE IN TELECOMMUNICATIONS ENGINEERING

TESI DI LAUREA MAGISTRALE
in
TECHNOLOGIES AND APPLICATIONS OF WIRELESS POWER TRANSFER M

NON-LINEAR MODELLING OF MICROWAVE DEVICES EMBEDDING NANO-FERROELECTRIC MATERIALS FOR REAL-TIME RECONFIGURABLE TRANSMITARRAY

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Anno Accademico
2020-2021
Sessione
III

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INTRODUCTION

0.1 **The challenge of System on Chip radiofrequency circuits**

As the operating frequency of modern applications are continuously moving higher, it is recognized that various integration technologies are playing an ever-increasing important role in the development of antennas, components, and circuits. Over the last few years, silicon-integrated radiofrequency (RF) circuits have received growing attention due to the reduction in size, weight, and costs.

Traditionally, the system-on-board (SoB) arrangement is the most used for the realization of wireless systems. It consists in the assembly of discrete components, such as digital integrated circuits (IC), mixed-signal ICs, radio-frequency integrated circuits (RFICs) and passive components, on printed circuit boards (PCB), either in a horizontal or a vertical fashion, as displayed in Fig. 0-1. SoB solutions lead to the best performance to each component used in the system but also lead to various issues since the overall system occupies a large size and the realization cost is high, especially for the antenna modules, whose dimensions are the largest of the system. In SoB circuits, antennas are designed on a separate PCB, which must be combined with the PCB containing the ICs and other discrete components. In particular, the PCB antenna is connected to the RFIC through bond wires and bond pads which introduce RF transmission loss and uncertainty, especially at very high frequencies.

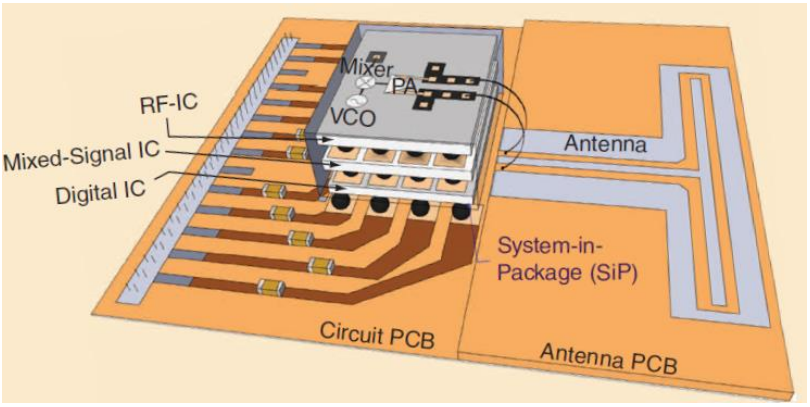


Fig. 0-1: Illustration of SoB integrated with RFIC, various ICs and a separate PCB antenna [1].

Aided by the fast development of new CMOS technologies, system-on-chip (SoC) approach received growing interest in recent years. This solution promises to counteract the problems associated with SoB, where the digital module, the analog module, and RF front-end can be integrated on a single chip, as displayed in Fig. 0-2. The advantages are low costs, the small physical size, the light weight, and the low power consumption.

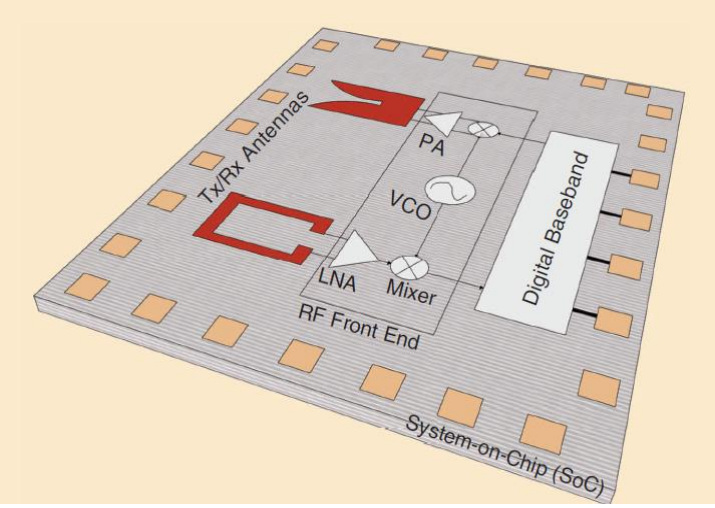


Fig. 0-2: Illustration of a typical System-on-chip module [1].

Within an integrated silicon system, the antenna gains many benefits including dropping matching to 50 ohms but adds new challenges including achieving good radiation efficiencies. In fact, incorporating antennas on low resistive CMOS-grade silicon substrate is to maintain a reasonable radiation efficiency is the hardest challenge. Common silicon substrate typically exhibits a low resistivity (around 10-15Ω*cm) which is beneficial for integrated circuits, but it is disastrous for on-chip antenna design. When the antenna is closely placed on top of low resistive silicon substrate, the electromagnetic (EM) waves find low resistive path in the silicon substrate, thus it absorbs most of the RF power that is dissipated in the substrate trough Joule effect rather than being radiated into the air. As a result, on-chip antenna offers very low radiation efficiency. Furthermore, silicon exhibits a high permittivity value which deteriorates the radiation pattern and the efficiency. For a dipole antenna seeing the vacuum on one side and a dielectric on the other side, the ratio of the power radiated into air to the total radiated power is approximated given by [2]:

$$\frac{P_{air}}{P_{tot}} = \frac{1}{\varepsilon^{\frac{3}{2}}} \quad (0.1)$$

where P_{air} is the radiated power into air, P_{tot} is the total radiated power and ε is the dielectric constant of the medium. From this formula for silicon dielectric, which presents a dielectric constant almost equal to 11.9, a very small portion of the power is radiated into the air (about 3%) and the rest of it couples into silicon, as depicted in Fig.0-3:

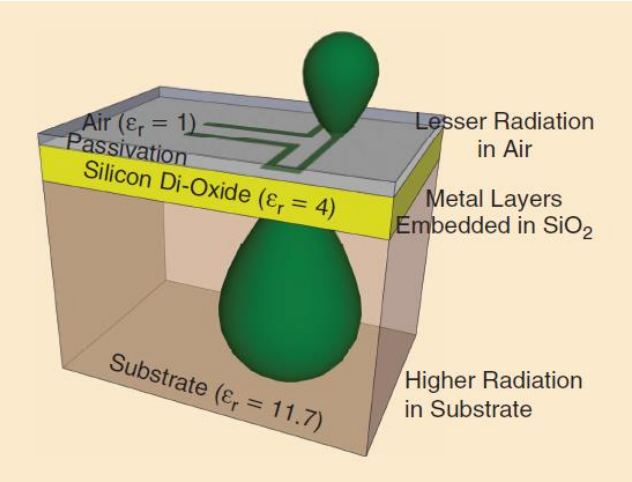


Fig. 0-3: EM radiation from on-chip-antenna in silicon-based technology [1].

Furthermore, the high dielectric constant of the silicon substrate and its large thickness causes the generation of surface waves that affect the antenna radiation pattern and consequently the antenna's radiation performance. Over the years various technique have been proposed with the aim to improve the performance of silicon-integrated antennas. For example, it was demonstrated that a fully-silicon dielectric resonator antennas (DRAs), can reach radiation efficiencies and gains higher than 70% and 4.5 dBi, respectively [3].

Other techniques used to decrease the losses in the silicon substrate are the bulk micromachining and proton implantation [4]. They consist in the modification of the silicon substrate in a selective manner, typically in the area of the on-chip antenna, so that the resistivity is modified only in that region. In particular, bulk micromachining is a fabrication process used to form trenches or cavity structures in the substrate through selective etching. It can be used to thin the silicon substrate under the on-chip antenna area. In this way, the overall permittivity of the mixture of air cavity and silicon substrate under the on-chip antenna strongly decreases, passing from 11.9 to a much smaller value, and the overall loss due to the silicon substrate decreases as well. In [5], an example of this procedure is presented, and as displayed in Fig. 0-4 an air cavity is created at the backside of the on-chip patch antenna via selective etching. With this arrangement it is possible to obtain 28% more efficiency with respect to the traditional case where no cavities are introduced.

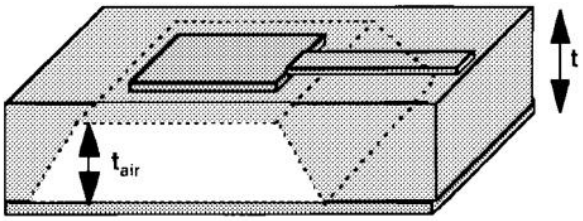


Fig. 0-4: Geometry of micromachined patch antenna [5].

Proton implantation instead, is the process of implanting ions in the silicon substrate. With this procedure the resistivity of the substrate can be increased, and therefore the radiation performance improves. For example, in [6] by means of proton implantation, the substrate resistivity increases from 10 Ω*cm to 106 Ω*cm.

To increase the radiation efficiency, instead of modifying the properties of silicon substrate, reflecting surface and superstrate can be exploited. The former is used to isolate on-chip antenna from silicon substrate. A perfect magnetic conductor (PMC) can be placed in the metal layers under the on-chip antenna to isolate it from the lossy substrate. However, since PMC doesn't exist in nature, researchers have found an approximate equivalent in the form of artificial magnetic conductor (AMC) surfaces that simulate the PMC in a certain frequency range. Placing this kind of surface is advantageous, because in-phase reflection occurs on AMC surface and so it can improve the on-chip antenna's radiation direction and the boresight gain of on-chip antennas. Similarly, by adding a high-permittivity substrate on top of on-chip antenna, also known as superstrate, it is possible to improve the radiation efficiency and high boresight directivity can be achieved. Thanks to all the approaches mentioned above to increase the radiation efficiency and the gain of the on-chip antenna, it is possible to reach a good trade-off between the advantages and the disadvantages of using silicon substrate for antenna design.

0.2 **Reconfigurable antenna array technologies**

In the last years, together with the development of SoC approach, the concept of antenna array, defined by a set of coherently fed radiating antennas arranged and excited in such a way as to produce a radiation pattern having given properties, has gained more and more interest. In fact, with the progress in telecommunications, the need for higher gain, higher directivity and larger bandwidth of antennas has significantly increased, therefore, the use of antenna arrays become essential to overcome these problems.

Operation at mm-Waves frequencies has been proposed as a solution, they are promising candidate technology for realising the key requirements of 5G, like low latency, higher data rates, and higher aggregate capacity for supporting simultaneous users. However, there are challenges associated with operating in the mm-Waves frequency band, that are, high free space path loss, absorption due to atmospheric gases, rainfall, and non-line of sight propagation. Free space path loss, being directly proportional to the frequency and to the distance, at mm-Waves and for long distance degrade the link budget. For that reason, highly directive mm-wave antennas are needed to overcome the high path loss. Moreover, absorption of energy from radio waves, due to atmospheric gases, is very strong in that range of frequencies, reaching its peak value at 60 GHz where the signal attenuation is around 5dB/Km. To overcome this limitation, the antenna should have the ability to reconfigure its radiation pattern to avoid obstacles and maintain the link with another network.

To reconfigure the radiation pattern, it is needed to estimate the direction of arrival of the signal. This is essential as the system need to know in which directions it must reconfigure its beam, to differentiate between the desired signal and the interfering ones and suppress them, and to reconfigure its beam pattern to the new direction of interest to reduce the power dissipated in the unwanted directions. For the latter purpose, beam reconfigurable or steerable antennas are employed with the aim of steering highly directional beams to avoid unwanted signals. This improves the system performance since it reduces the level of interference and the power used in retransmission by focussing the radiation on a specific direction.

Many techniques have been deployed over the years to steer the antenna's radiation patterns. For example, the mechanical steering technique implicates the manual turning of the antenna to face the direction of interest. Mechanical steering is effective since it preserves the gain of the antenna and offers flexibility in the steering range of the antenna. However, the disadvantage is that its use is limited to the static environment due to the limitation in the steering speed. The solution for this problem leads to electronic ways of steering beams called beamforming which is the process of combining signals from an array of elements to form a highly directional radiation beam. It is also used to align the phases of an incoming signal from different parts of an array to form a well-defined beam in specific directions. Another solution to steer the radiation pattern electronically is to use a reflectarray antenna in which the reflector is replaced with thousands of equispaced elements that reflect the incident field with pre-determined phase-shift, as shown in Fig.0-5. The predefined phases are either set actively, by using phase shifters or passively, by shaping and designing the size

of each element of the array. Reflectarray has the advantage of being lightweight and doesn't experience transmission line losses because the elements are fed by quasi-optical means and not via matched transmission lines [7]. However, reflectarrays suffers from losses generated by the phase shifters, and the cost and the complexity increase with the number of elements. Also, they are limited to predefined steering resolutions.

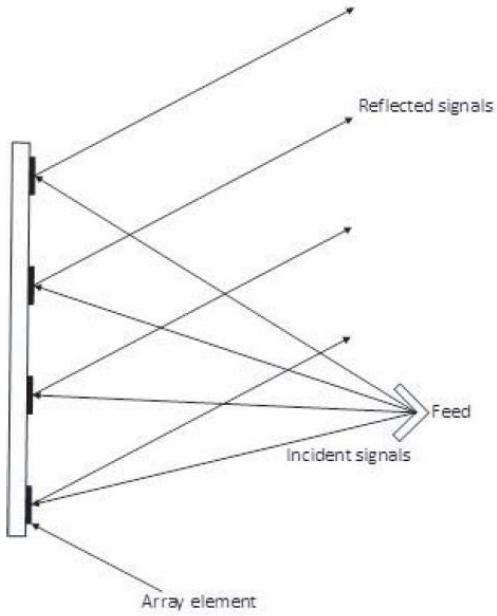


Fig. 0-5: Illustration of a typical reflectarray [8].

Thus, developing a new scanned phased array system without using phase shifters become a crucial task. A valid approach to scan the beam in phased array antenna is by using Huygens's metasurfaces which are 2D man-made structures that are design to obtain electromagnetic properties that cannot be achieved in nature, for instance, their effective permittivity and permeability can be tuned to positive or negative values [9]. For example, in [10] a phased array system composed of metasurface layers placed on top of conventional probe-fed microstrip square patches is proposed. The phase variation between elements in the array depends on the dielectric constant of the metasurface layers. It is verified that by varying the εr from 2.65 to 3.65, it is possible to cover up to 220 degrees in transmission phase. Therefore, it is possible to tune the dielectric constant to achieve the correct phase shift to steer the beam in the desired direction. In recent years, in fact, tuning approaches based on phase change under different external stimuli have played an important role in active surfaces, thanks to the tunability in refractive index of phase change materials, and superconductors. In the microwave range, electrically tunable reconfigurable surfaces can

be created by designing arrays integrating varactor diodes or p-i-n diodes, whose capacitance can be tuned by applied voltages, but they imply high losses and high levels of power. Moreover, the scalability and the low linearity of such devices are strictly limiting factors.

To overcome these limits and so improve the performance in terms of scalability, power consumption, on-chip integrability and fast reconfigurability, nano-structured materials are engaged. In this context, nanoscale ferroelectric materials play an important role.

0.3 **Ferroelectric material properties**

Ferroelectricity refers to many related phenomena specific to ferroelectrics. Ferroelectric is defined to be a material that has a spontaneous electrical polarization P, that can be reversed by the application of an external electric field $\bar{E}$. Spontaneous polarization means that the material can be electrically polarized or have an electric dipole moment without an applied external electric field. In ferroelectric materials their molecules each carry electric dipole moment that jointly and spontaneously align to form a polarized material. There are also materials whose molecules have dipole moments but are not ferroelectric. In a water molecule, for example, since the oxygen atom is slightly negative, and the hydrogen atoms are slightly positive, a net molecular dipole moment is produced. However, the molecular dipole moments of all molecules in water don't spontaneously align, so water is not polarized. Very similar to this is the concept of ferromagnetism and ferromagnets: as well as a bar magnet has a magnetic field, a ferroelectric material has electric dipole moment where one end is positively charged, and the other is negatively charged.

Generally, when a material is electrically polarized, the induced polarization P is almost proportional to the applied external electric field, which leads to a linear dielectric polarization. Some materials, named paraelectric materials, show a non-linear polarization, since the electric permittivity, corresponding to the slope of the polarization curve, is function of the external applied electric field. In addition to being non-linear, ferroelectric materials demonstrate a spontaneous nonzero polarization even when the applied electric field is zero, as can been see in Fig.0-6. In fact, when an electric field is applied it becomes polarized and the crystal structure of the material is permanently deformed even after the field return to zero, leaving a remanent polarization P_r, which is defined as the intrinsic polarization of the ferroelectric when the electric field is not applied. This is one of the two main parameters that represent the main characteristics of any ferroelectric material, together

with the coercive electric field $E_{c,}$ that is the value in correspondence to which the polarization disappears.

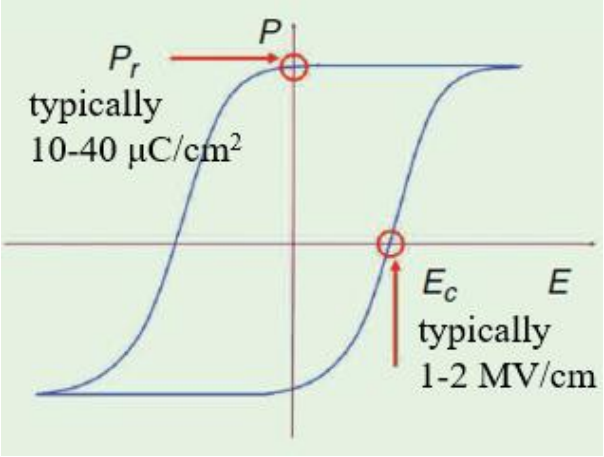


Fig. 0-6: Polarization hysteresis as a function of the applied electric field [11].

The distinguishing feature of ferroelectric is that the spontaneous polarization can be reversed by a suitably strong applied electric field in the opposite direction; the polarization is, therefore, not only dependent on the current electric field but also on its history producing a hysteretic loop, as shown in Fig. 0-6. Although the P-E curve can be measured directly, there are other dependencies where the hysteretic nature of the P-E curve, intrinsic to any ferroelectric, manifests itself. For example, a metal-ferroelectric-metal capacitor exhibits a capacitance-voltage dependence specific to ferroelectrics, and ferroelectric FETs show the same hysteretic behaviour in the I_D-V_G dependence for a certain value of V_D, where I_D is the drain current, V_G is the gate voltage and V_D is the drain voltage; thus, these devices can also have various important applications as ferroelectric memories [11].

Other important properties of ferroelectric materials are piezoelectricity, which is the ability to generate electrical energy when mechanical stress is applied and vice versa, and the temperature dependence of polarization. Typically, they demonstrate ferroelectricity only below a certain phase transition temperature, called Curie temperature, because above this temperature the spontaneous polarization vanishes, and the ferroelectric crystal transforms into the paraelectric state.

The use of devices made using ferroelectric materials have significant advantages over traditional tunable devices based on semiconductors. First, ferroelectric devices have considerably superior tuning capability to semiconductor-based competitors.

Another notable advantage that ferro-electric devices have is that of not having a forward bias conduction, a problem that becomes very present in semiconductor solutions when the input signal has high power. It is in fact known that diodes can be used in varactors when these are polarized in the reverse region. however, when the circuit is in the presence of large signals, the working point of the device can move from the inverse to the direct region, destroying the desired effect. On the contrary, circuits made using ferroelectric materials are not affected by this problem [12].

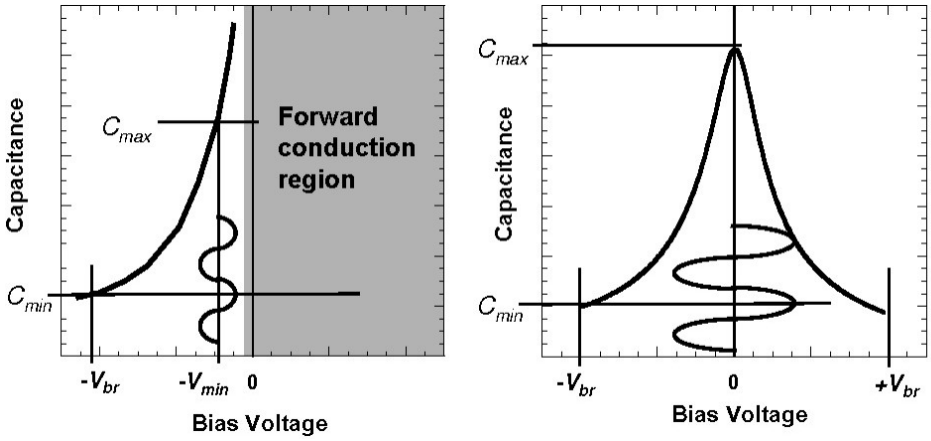


Fig. 0-7: Semiconductor varactor (left) and ferroelectric-base device (right) capacitance trend at different input power levels [12].

The unique properties of ferroelectric materials have made them important for various applications. For instance, in [13] a study of barium strontium titanate (BST) is reported. It, being a ferroelectric material, has a tuneable capacitance that naturally causes the change of relative dielectric permittivity of the material as a function of the biasing electric field provided by a dc voltage source. Therefore in [13], it is used for the implementation of a parallel-plate varactor in which the ferroelectric film is sandwiched between two electrodes, which provides high tuning rates of capacitance in a wide range of frequencies of operation. The non-linear behaviour of the BST thick film is shown in Fig. 0-8.

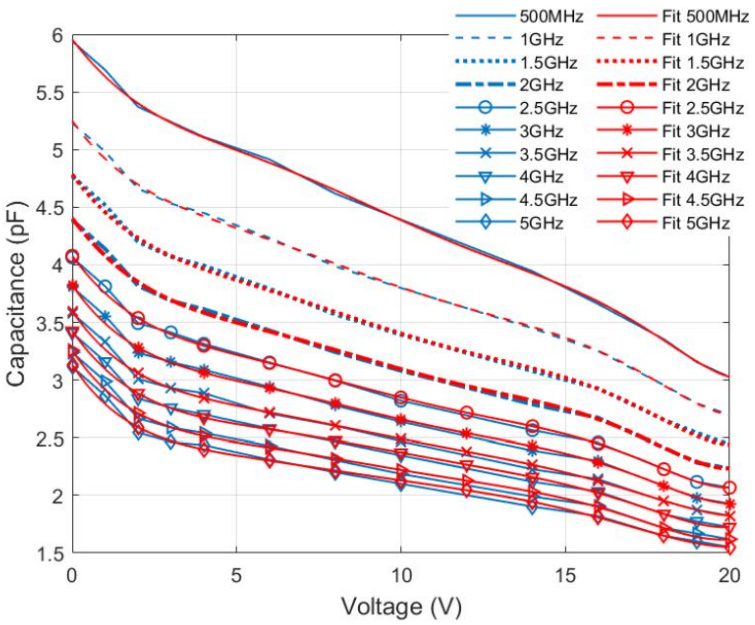


Fig. 0-8: The voltage-dependent capacitance behavior of the BST-based structure reported in [13].

0.4 **Hafnium zirconium oxide applications in RF circuits**

Consequently, to the fast development in terms of miniaturization and integration on silicon for beam-steering applications there is an increased scientific interest in novel complex and nanometric oxide ferroelectrics as tunable materials, like the recently discovered hafnium oxide (HfO_2), zirconium oxide (ZrO_2) and the ternary hafnium zirconium oxide paracrystalline ferroelectrics ($HfZrO_2$).

The ferroelectric phase existence in a nanoscale thin film is explained by the extremely low value of the Gibbs free energy as a function of the simulation time obtained from a molecular dynamic simulation. From this low value is possible to assume that the presence of intercalating zirconium atoms makes the orthorhombic ferroelectric lattice an energetically stable system. In [14], through the molecular dynamic trajectories, the correlation between the dielectric properties and lattice structure of $HfZrO_2$ has been studied since the dielectric response and bandgap of the material are strongly phase dependent. It is verified that the incorporation of ZrO_2 into HfO_2 increases the dielectric constant value of the resulting $HfZrO_2$ up to 35.2 from a value of 5.37 [15] as shown in Fig 0-9. This is associated with the structural phase transformation from mainly monoclinic to orthorhombic phase. Also, the Curie temperature (T_c) of $HfZrO_2$ is 450°. Furthermore, a clear dependence of the dielectric constant on function is revealed.

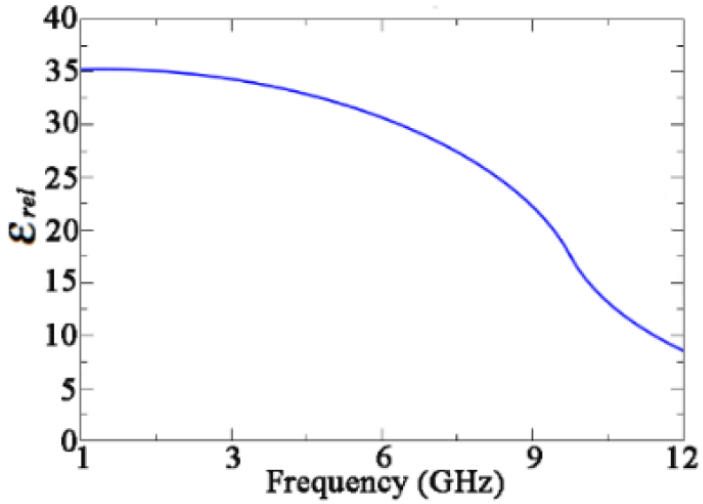


Fig. 0-9: Dielectric constant of $HfZrO_2$ as function of frequency [14]

The above-mentioned results were proven by several experiments. For example, in [16], the scattering parameters, considering the case in a CPW is designed directly on 525µm of high-resistivity silicon (HRSi) and a CPWs on a 525µm HRSi substrate on top of which a 6nm thick layer of ferroelectric HfZrO2 has been deposited via atomistic layer deposition, are measured, as shown in Fig. 0-10. It can be notice that the curves of reflection and the transmission parameters in the case of the CPWs without the $HfZrO_2$ layer and in the case of a CPWs with a $HfZrO_2$ layer biased with 0V are very similar. This is explained by the fact that the layer of HfZrO2 in absence of applied DC voltage its influence on the electrical characteristic of CPW is reduced since its permittivity at 0V is very similar to the HRSi one.

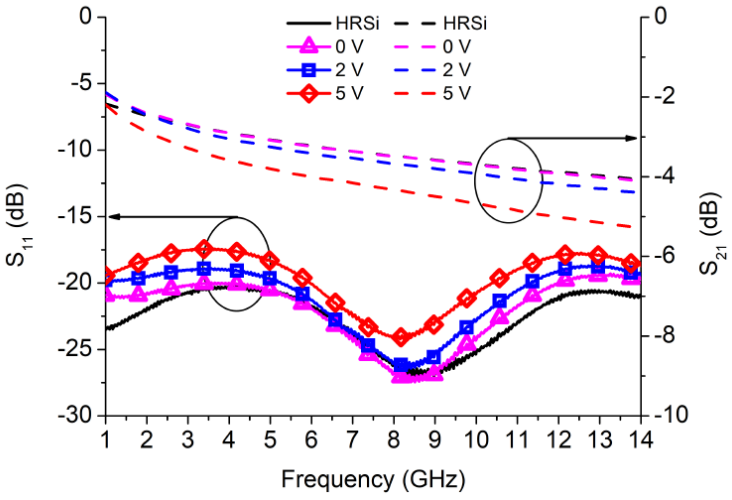


Fig. 0-10: Measured S_{11} and S_{21} as a function of frequency and applied DC bias on different CPWs [16].

From S-parameters the effective permittivity, displayed in Fig. 0-11, can be extracted. In the case of CPWs designed directly on HRSi, there is no variation indeed of the effective permittivity with the applied DC voltage. On the other hand, in the case of a CPWs patterned on $HfZrO_2$, it can be seen that the effective permittivity curve is shifted upward with the applied voltage.

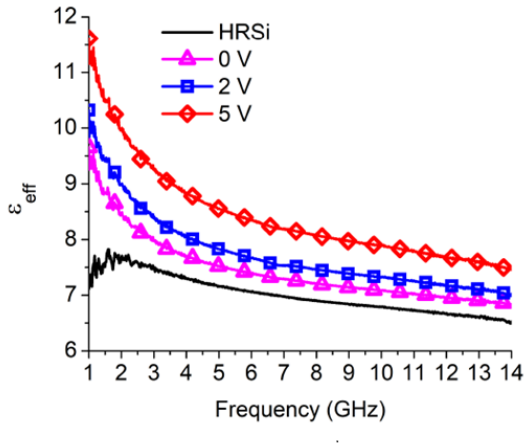


Fig. 0-11: Effective permittivity as a function of frequency and applied DC bias [16].

As already mentioned, nanoscale ferroelectric materials, like $HfZrO_2$, thanks to the properties discussed above, are exploited in many applications. For example, it is demonstrated that it is possible to achieve a phase shift larger than 60 degrees at 1 GHz and 13 degrees at 10 GHz at the maximum applied DC voltages of ±3V by using 1 mm- long coplanar interdigitated capacitor (IDC) placed over a 6nm $HfZrO_2$ ferroelectric grown directly on a high resistivity silicon substrate, as shown in Fig. 0-12(a) [17]. Combining the IDC presented in [17] with a two-elements phased array operating at 2.55 GHz, as shown in Fig. 0-12(b), and presented in [18], it is possible to shift the main lobe with 25 degrees for very low bias voltages of ±1V by means of two interdigital phase shifters, one for each patch antenna.

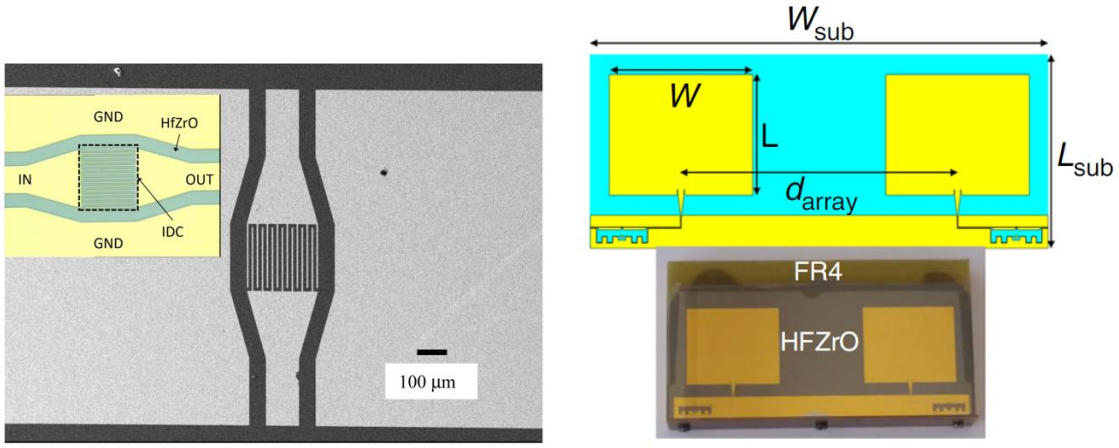


Fig. 0-12: Scanning electron microscope image of the phase shifter based on $HfZrO_2$ [17] (a), and a photography of the phased antenna array presented in [18] (b).

The use of nanometric materials makes the structure very light and compact from the point of view of dimensions but has the disadvantage of making the electromagnetic simulations of the radiating elements that exploit the ferroelectric properties of materials such as $HfZrO_2$ very complex and sometimes not very reliable. For this reason, in this thesis, an IDC-based phase shifter model was developed on a 6nm $HfZrO_2$, compatible with CMOS technology, which faithfully represented the experimental measurements obtained in [17]. The thesis intends to initially focus on the identification of a model that correctly represents the interdigitated capacity used as a phase shifter. Subsequently, through the experimental measurements obtained in [17] from the IMT research center in Bucharest, with which a collaboration activity was carried out during the thesis project within the European project NANO-EH, an analytical function was identified that best describes the behavior of the $HfZrO_2$ when the applied voltage varies. In particular, a user-defined model implemented through the Keysight ADS circuit simulator is developed which reliably describes the behavior of the IDC even for powers higher than 30 dBm. Subsequently, some solutions in CPW technology are proposed where the IDC is placed in series or in parallel to a transmission line, analyzing its performance. Finally, a linear array design for beam-steering is proposed consisting of four patch-type elements, where the operation of the previously modeled phase shifters is verified.

Chapter 1
ELECTROMAGNETIC SIMULATIONS AND IDENTIFICATION A CIRCUITAL MODEL

1.1 **Radiofrequency applications based of Interdigital Capacitors**

Interdigital capacitors have been investigated in many research works, since they have a simple design, low-cost manufacturing, and can be easily combined with other electronic components. They have high performance when used as sensor applications in biology, physics, chemistry, and other scientific fields. The interdigitated capacitor (IDC), shown in Fig. 1-1, enables to realize higher capacitance than traditional gap capacitors. It is composed of long conductors, also called fingers, folded to use a small amount of area, which provides coupling between the input and the output ports across the gaps. The values of the capacitance strongly depend on the geometry of the structure the capacitance increases as the gap (G) decreases or if the length of the fingers(L) increases and decreases if the width (W) of the fingers is reduced. The capacitance can be also increased by increasing the number of fingers there is a trade-off between higher capacitance value and the occupied area.

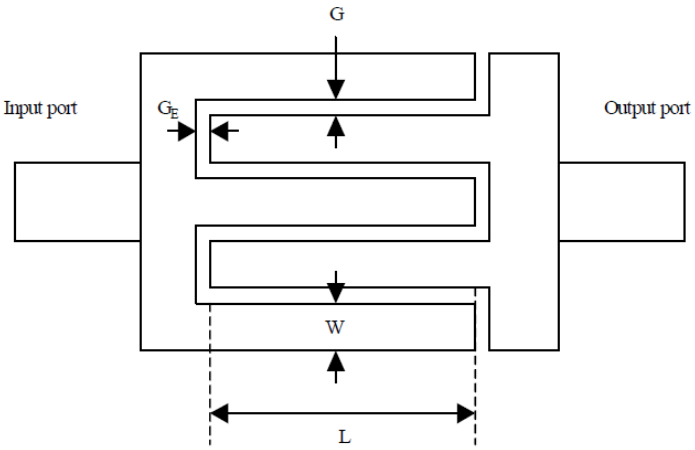


Fig. 1-1: Interdigitated capacitor geometry [19].

As already mentioned, IDCs are implemented in many fields and in several applications. For example, in [20] an interdigital capacitor is used to create a dual-band (DB) filter. The

structure proposed for this application consists of a series interdigitated capacitors placed between two microstrip lines that are shorted by vias. In this way, the vias with the microstrip lines act as shunt-connected inductors, while the series capacitance is realized by IDC. In Fig. 1-2 the equivalent circuit model of the DB filter is reported, where C_{int} represents the series capacitance of the interdigital capacitor, C_p and L_{int} represent parasitic capacitance and parasitic inductance of the interdigital capacitor, respectively. Furthermore, L_{via} represents the shunt inductance of the via hole and C_{LT} and L_{LT} represent respectively the capacitance and the inductance of the transmission line.

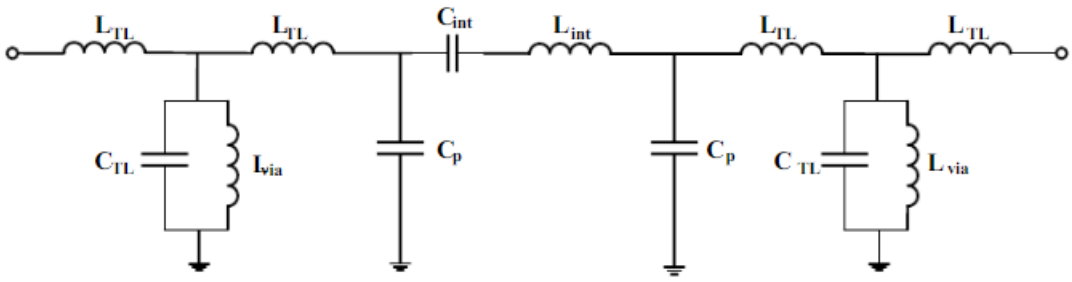


Fig. 1-2: Equivalent circuit model of the DB filter [20].

1.2 **Circuital model of the $HfZrO_2$-based phase shifter realized in IDC technology**

In recent years, a technique that aims to increase the capacitance value is the use of a thin layer of high dielectric constant material such as ferroelectric between the conductors and the substrate. Ferroelectric materials, furthermore, allow achieving voltage tunability of interdigital capacitors. For example, in [21] a 60 GHz phase shifter, based on a CPW transmission line, loaded with ferroelectric hafnium zirconium oxide variable metal-insulator-metal varactors is examined. The design is based on a CPW delay line composed of N unit sections with lumped inductive and capacitive elements, and the equivalent circuit of the elementary section is reported in Fig. 1-3:

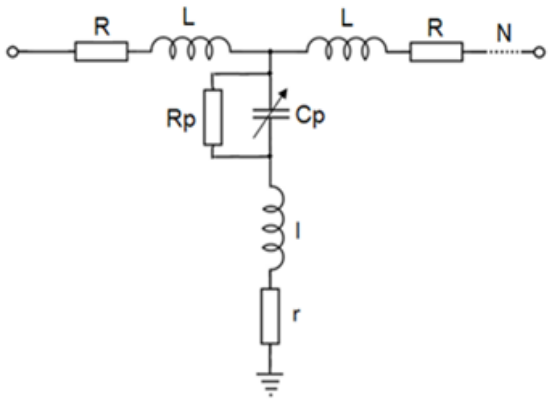


Fig. 1-3: Equivalent circuit of the unit section of periodically loaded delay line [21].

Each unit section is shunted to the ground with a varactor, whose capacitance can be changed by applying a dc bias voltage over a bias tree. The resistance R_p represents the signal losses due to the dielectric losses in the ferroelectric material, while r and R are the resistance of interconnect and the resistance of the electrodes, respectively.

In this thesis an $HfZrO_2$-loaded CPW interdigital capacitor with reconfigurable response is examined, which can provide reconfigurable performance by exploiting the tuning properties of the 6nm layer of $HfZrO_2$ placed between the conductors and the substrate. By applying different bias voltages to the $HfZrO_2$ film, its electrical properties will change. In this way, the response of the interdigital capacitor can be dynamically tuned. Electromagnetic and circuital simulations of the IDC are proposed.

The structure is first electromagnetically simulated by using the software CST STUDIO SUITE 2019, an electromagnetic simulator that considers the circuit as a whole and solves it starting from Maxwell's equations. CST STUDIO SUITE is a general-purpose electromagnetic simulator based on the Finite Integration Technique (FIT), first proposed by Weiland in 1976/1977 [22]. This numerical method provides a universal spatial discretization scheme applicable to various electromagnetic problems ranging from static field calculations to high-frequency applications in the time or frequency domain. Unlike most numerical methods, FIT discretizes the following integral form of Maxwell's equations (1.1 to 1.4) rather than the differential one:

$$\oint_{\partial A} \bar{E} \bullet \overline{ds} = -\oint_{A} \frac{\overline{\partial B}}{\partial t} \bullet \overline{dA} \quad (1.1)$$

$$\oint_{\partial A} \bar{H} \bullet \overline{ds} = -\oint_{A} \left(\frac{\overline{\partial D}}{\partial t} + \bar{J}\right) \bullet \overline{dA} \quad (1.2)$$

$$\oint_{\partial V} \bar{D} \bullet \overline{dA} = -\oint_{V} \rho \bullet \overline{dV} \quad (1.3)$$

$$\oint_{\partial V} \bar{B} \bullet \overline{dA} = 0 \quad (1.4)$$

where, $\bar{E}$ is the electric field in the vacuum, $\bar{D} = \varepsilon_0 + \bar{P}$ is the electric induction, that considers the electrical polarization, $\bar{B}$ is the magnetic field perceived in one point, called magnetic induction, and $\bar{H}=\frac{\bar{B}}{\mu_0} + \bar{M}$ is the magnetic field introduced into the materials. To solve these equations numerically, the software defines a finite calculation domain. Creating a suitable mesh system splits this domain up into many small elements, or grid cells. Then, Maxwell's equations are formulated for each of the cell facets separately.

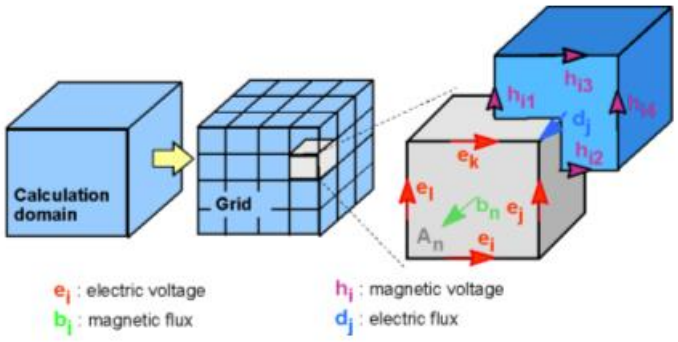


Fig. 1-4: CST domain discretization along the 3D-grid [22].

Since the thickness of the ferroelectric material is very thin in comparison to the entire substrate, for the CPW interdigitated capacitor structure, the mesh step width in the Z direction is imposed equal to the height of the $HfZrO_2$ divided by 5 to intersect five times the nano-layer of the ferroelectric material.

As in [16], a stack-up composed of HRSi, $HfZrO_2$ layer, and metallization is considered. In particular, as shown in Fig. 1-5, it is chosen a narrow CPW with a gap-signal-gap of 10/15/10µm, 1mm wide and 6.671mm long, to better confine the effect of the dc bias into the thin $HfZrO_2$ ferroelectric, as it is demonstrated in [16]. In particular, the gap-signal-gap has been chosen to keep the 50 Ω matching. It is verified that simulating 525µm of HRSi or 50µm of HRSi is the same because the electric field values are negligible for silicon depth values greater than 50 µm. For this reason, instead of 525µm of HRSi, 50µm are considered to reduce the presence of HRSi in the structure and make the simulation faster but still accurate. The cross-section of the simulated structure is shown in Fig. 1-5:

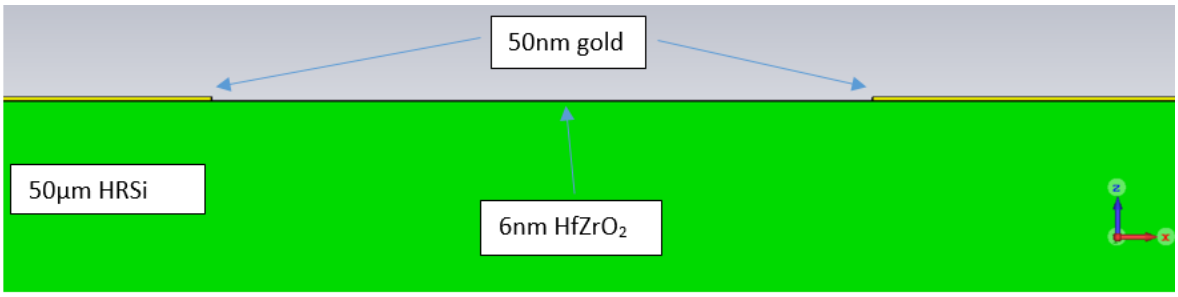


Fig. 1-5: Cross-section of the analyzed CPW structure (yellow: gold, black: $HfZrO_2$, green: silicon).

Firstly, just the characteristic impedance is simulated for different dc bias voltages, in particular 0, 2 and 5 volts. As shown in Fig. 1-6 the relative permittivity of a 6nm $HfZrO_2$ layer grows rapidly as the dc bias increases.

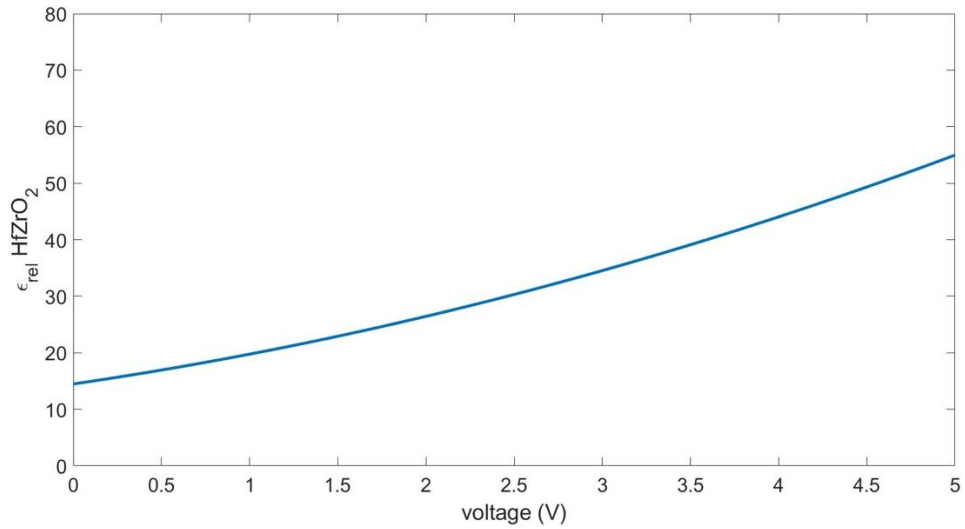


Fig. 1-6: Relative permittivity of $HfZrO_2$ as function of dc bias.

In (1.5) is reported the analytic expression of the CWPs characteristic impedance (Z_0) [23]:

$$Z_0 = \frac{30\pi}{\sqrt{\varepsilon_{eff}}} \frac{K(k')}{K(k)} \quad (1.5)$$

$$\varepsilon_{eff} = 1 + \frac{\varepsilon_r - 1}{2} \frac{K(k')}{K(k)} \frac{K(k_1)}{K(k'_1)} \quad (1.6)$$

where:

$$k = \frac{W}{W + 2S} \quad (1.7)$$

$$k_1 = \frac{\sinh\left(\frac{4W}{\pi H}\right)}{\sinh\left(\frac{(W+2S)\pi}{4H}\right)} \quad (1.8)$$

In the above, K is the complete elliptic integral of the first kind, $k'=\sqrt{(1-k^2)}$, W is the width of the line, S is the gap between the signal and the metallization, and H is the height of the substrate. It is possible to notice a clear dependence of the characteristic impedance of the CPW on the relative dielectric constant ε_r. Simulations showed that the change in bias voltage does not affect the characteristic impedance of CPW, resulting in a poor accurate simulation of the ferroelectric structure.

As the next step, a $HfZrO_2$ layer with a thickness about forty times greater than the original one is considered to increase the effect of the ferroelectric layer. This time the simulations not only include the cross-section of the structure but also the propagation inside the 6 mm long CPW.

In CST, the S-parameters are defined as the quotient between the output signal spectrum and the input signal spectrum. Therefore, the signal spectra must be calculated. This is done by using the Discrete Fourier Transform (DFT).

From the theory, it can be said that in this 2-port case, electrical variables, called incident (a) and reflected waves (b), which are linear combinations of currents and voltages can be defined at the two ports as follows:

$$a_1 = \frac{V_1 + Z_0 I_1}{2\sqrt{Re(Z_0)}} \quad (1.9)$$

$$b_1 = \frac{V_1 - Z_0 I_1}{2\sqrt{Re(Z_0)}} \quad (1.10)$$

$$a_2 = \frac{V_2 + Z_0 I_2}{2\sqrt{Re(Z_0)}} \quad (1.11)$$

$$b_2 = \frac{V_2 - Z_0 I_2}{2\sqrt{Re(Z_0)}} \quad (1.12)$$

The equations (1.9) to (1.12) lead to the 2-port S-parameter matrix defined as:

$$\begin{cases} b_1 = S_{11}a_1 + S_{12}a_2 \\ b_2 = S_{21}a_1 + S_{22}a_2 \end{cases} \rightarrow \boldsymbol{b = Sa}$$

which results in:

$$S_{11} = \left.\frac{b_1}{a_1}\right|_{a_2=0} \quad (1.13)$$

$$S_{12} = \left.\frac{b_1}{a_2}\right|_{a_1=0} \quad (1.14)$$

$$S_{21} = \left.\frac{b_2}{a_1}\right|_{a_2=0} \quad (1.15)$$

$$S_{22} = \left.\frac{b_2}{a_2}\right|_{a_1=0} \quad (1.16)$$

Since the incident and reflected coefficients are functions of the characteristic impedance, their values depend on the applied dc voltage. Electromagnetic simulations have demonstrated no changes in the S-parameters of the structure not only with 6nm layer thickness but also with 220 nm. This is demonstrated, as shown in Fig.1-7, by the fact that, by changing the polarization of the $HfZrO_2$, and so the electric permittivity of the substrate, biasing it with 0 V, 2 V and 5 V, the phase in the frequency range between 2 GHz and 12 GHz doesn't change as well even with a significant discretization of $HfZrO_2$ layer. It can be concluded that the electromagnetic simulator is not suitable to simulate the above-mentioned stack up since it is not able to recognize the presence of the $HfZrO_2$ nano-layer.

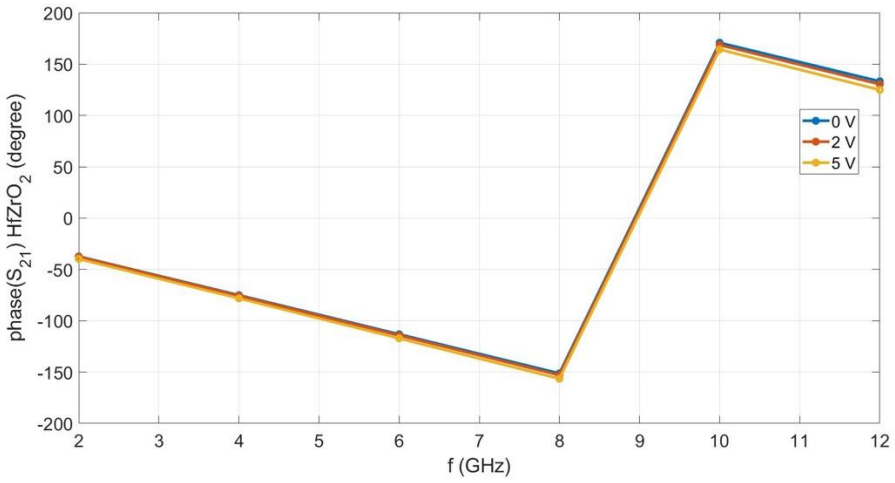


Fig. 1-7: Simulated S_{21}-phase as a function of frequency and dc applied voltage.

Since the results obtained with the electromagnetic simulator are approximate and unreliable, a circuital model of the interdigital capacitor is needed. In this thesis, the latter is

then implemented, and consequently, circuit simulations are performed by means of ADS Keysight, a circuital simulator.

The equivalent circuit chosen to model the $HfZrO_2$-loaded CPW interdigital capacitor is reported in Fig. 1-8. It is composed of five lumped elements that describe the behavior of the measured IDC in [17], C2 represents the nonlinear capacitance across the finger, while C1 and C3 the capacitance between the fingers and the two lateral ground planes. Then L1 and R1 describe the parasitic inductance and the joule-effect losses in the conductor, respectively. The simulations of the circuital model and the extraction of the components value are described in the following chapter.

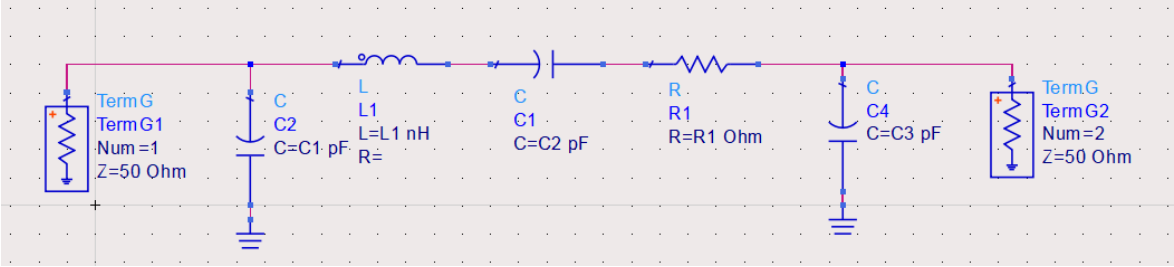


Fig. 1-8: Small signal IDC equivalent circuit model.

Chapter 2
DEVELOPMENT OF THE CIRCUITAL MODEL

2.1 **Identification of the circuit elements values**

As already introduced in the introduction, this thesis aims to develop a model that describes the behavior of an IDC based on ferroelectric materials. From the experimental measurements of the scattering parameters of the $HfZrO_2$-loaded CPW interdigital capacitor obtained in [17], a fitting is performed to derive values of the components of the equivalent IDC circuit model which is composed of both voltage-dependent and voltage-independent components, as a function of the polarization.

S-parameters are described in a small-signal regime. Under small-signal regime, an N-port network is fully described by a N x N matrix linking input and output ports for different bias points over the frequency range of interest. For instance, well known 2-port matrices are the admittance matrix Y, and the impedance matrix Z:

$$\text{Y (admittance): } \begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} \quad (2.1)$$

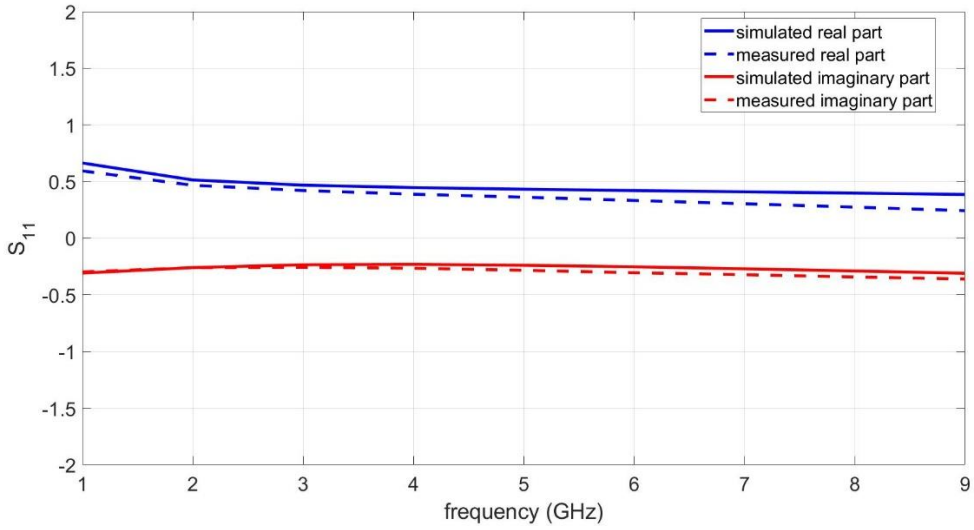
$$\text{Z (impedance): } \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} \begin{bmatrix} Z_1 \\ Z_2 \end{bmatrix} \quad (2.2)$$

To describe a device in terms of the matrices previously described, short or open circuit terminations are needed. Unfortunately, at increasing frequency, characterization setups for the matrices considered so far tend to become troublesome (instability, difficult implementation of wideband short and open circuit port terminations). This leads to the use of scattering matrix S in which a real normalization impedance is introduced: R_0 (>0), whose typical value is 50 Ω, which corresponds to standard port termination in the S-matrix characterization setup. In the presence of resistive terminations, devices tend to show a stable behavior even under high-frequency excitation.

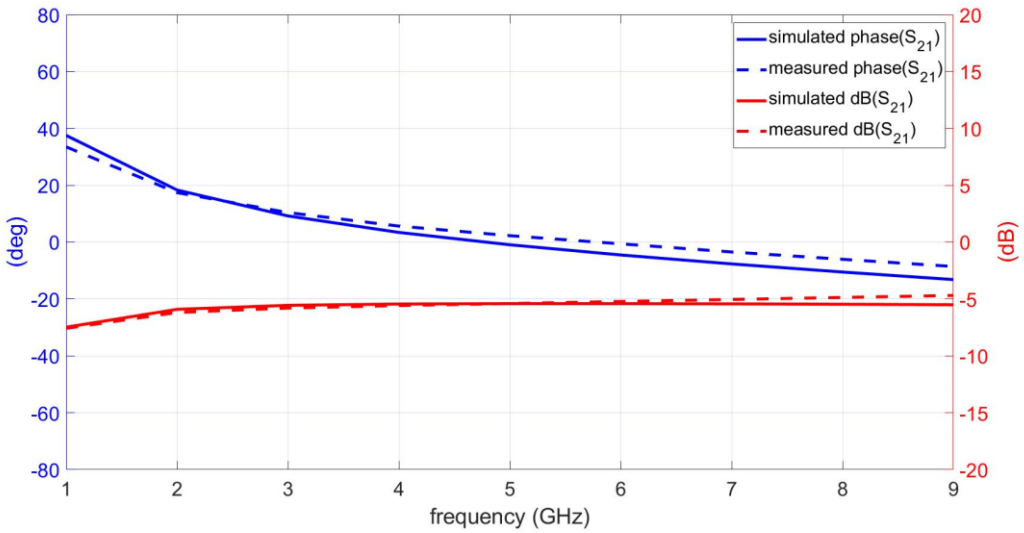
Small signal regime can be assumed whenever the amplitude of the signals is low enough to neglect the nonlinear effect. Therefore, the S-parameters describe what happens when the powers involved are small.

From the measured S-parameters obtained in [17] a fitting over the whole frequency range from 1 GHz to 10 GHz, considering a polarization equal to 0.2 V, is performed, as shown in

Fig. 2-1 where the model simulation is superimposed on the experimental measurements, in order to identify the values of the equivalent circuit model components that are voltage-independent. Resistance and inductance values are considered constant for each polarization because are not affected by the externally applied dc voltage and therefore the changes in terms of the permittivity of the substrate are negligible for these components. Moreover, the non-linear parasitic capacitances are considered equal, constant, and linear for simplicity, since it is verified that by changing the polarization their variation is very small and negligible with respect to the series finger non-linear capacitance.



(a)



(b)

Fig. 2-1: Model simulation and measurements values of S_{11} (a), phase and magnitude of S_{21} (b) as function of the frequency and with constant dc bias of 0.2 V.

From the fitting, the obtained values for the dc voltage independent resistance, inductance, and parasitic capacitances, are respectively 80 Ω, 10^{-4} nH, and 0.08 pF. Maintaining these achieved values fixed in the equivalent circuit, eleven fitting simulations are performed, for dc polarization values from -1 V to 1 V, in a limited frequency range from 2.4 GHz to 2.6 GHz centered around the frequency of interest 2.55 GHz, as shown from Fig.2-2 to Fig.2-4, to extrapolate the values of the series non-linear finger capacitance of the equivalent circuit of the IDC as a function of the polarization.

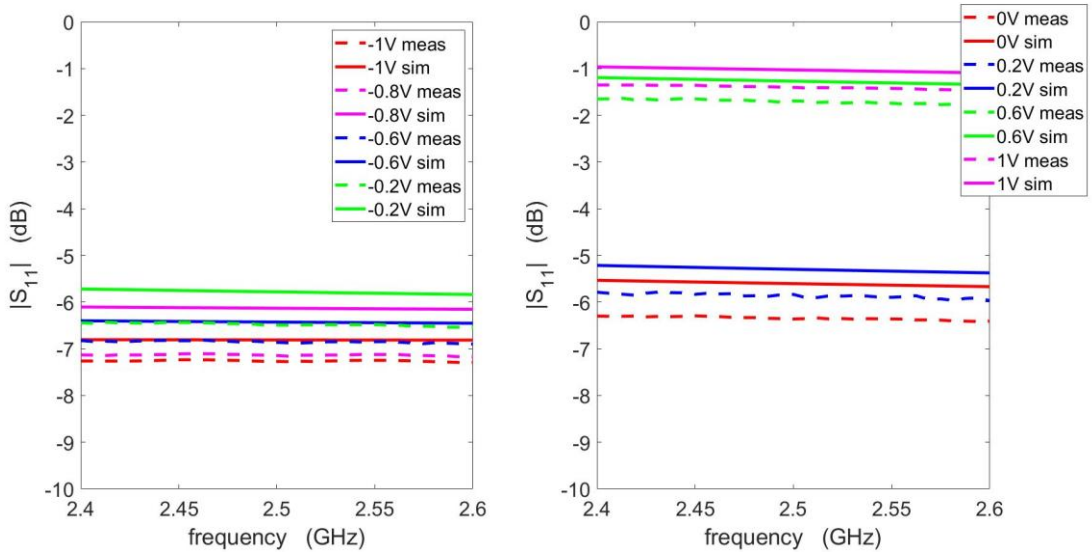


Fig. 2-2: Measured and simulated $|S_{11}|$ parameters as function of frequency and dc bias voltage.

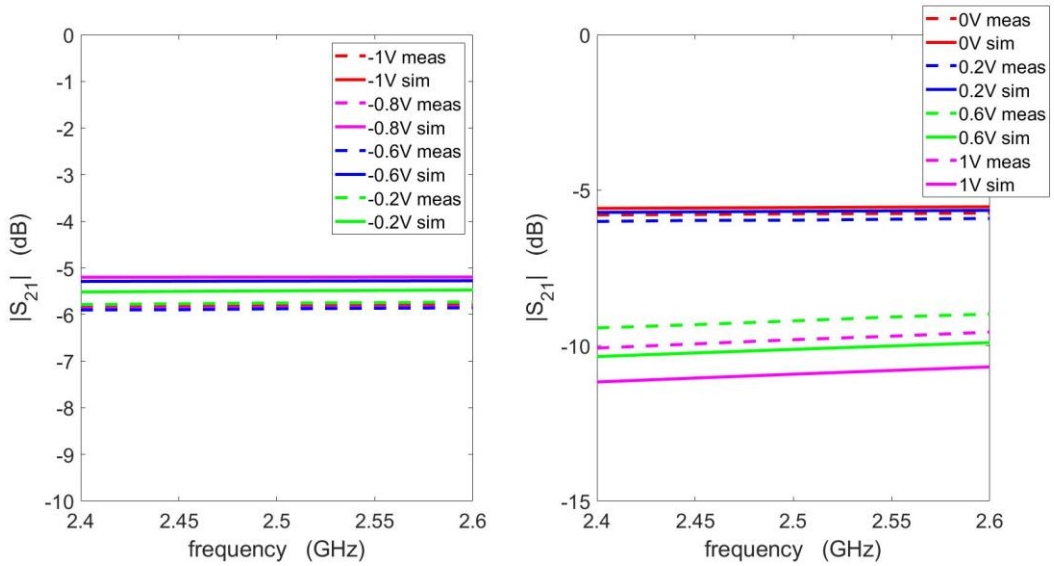


Fig. 2-3: Measured and simulated $|S_{21}|$ parameters as function of frequency and dc bias voltage.

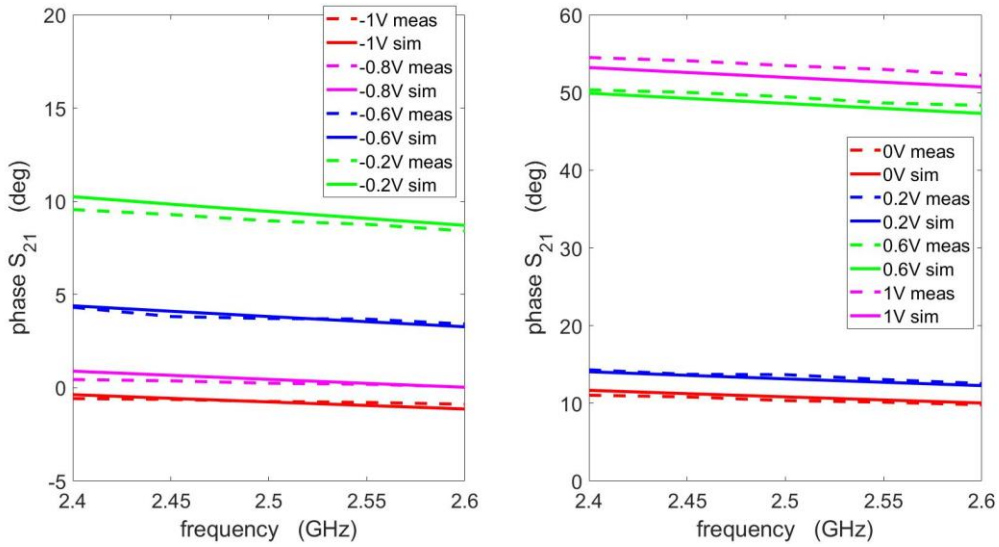


Fig. 2-4: Measured and simulated phase of S_{21} parameters as function of frequency and dc bias voltage.

Simulations reported a very low error between the model and experimental measurements. Also, observing Fig. 2-4 the changes in terms of S_{21} phase is clearly visible. At -1V the phase is about 50°, while at 1 V is 0°. Through the fitting process eleven values of the non-linear voltage-dependent finger capacitance are obtained one for each measured bias level for the frequency of interest (2.55GHz), as reported Fig. 2-5:

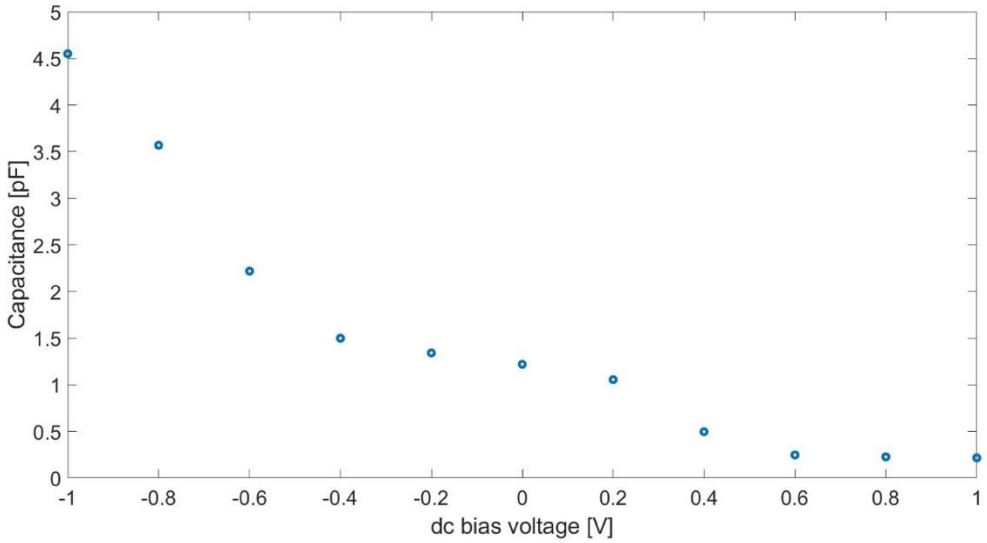


Fig. 2-5: Nonlinear series finger capacitance values as function of the dc bias voltage.

2.2 **User-defined modelling of the IDC**

Once obtained the data points of the non-linear finger capacitance, it is required to interpolate the values. In the mathematical field of numerical analysis, interpolation is a method of constructing new function. With the interpolation, two different curves with different trend lines have been found, as shown in Fig.2-6:

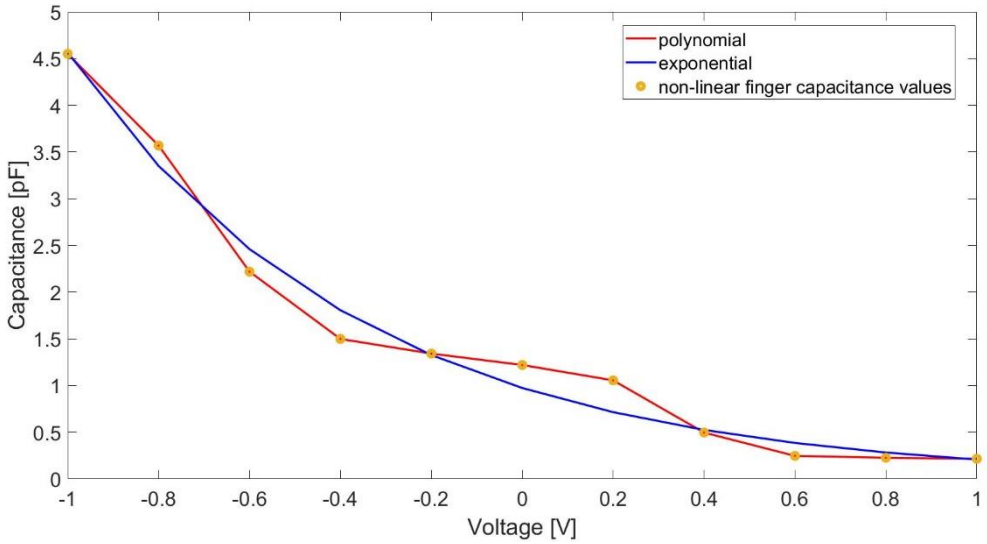


Fig. 2-6: Polynomial and exponential interpolating curves in the interested polarization range.

$$C(v) = [av^{10} + bv^9 - cv^8 - dv^7 + ev^6 + fv^5 - gv^4 - hv^3 + iv^2 - lv + m] \bullet 10^{-12} \quad (2.3)$$

where the corresponding values of a, b, c, d, e, f, g, h, i, l and m are reported in Tab. 1-1:

Table 1-1: Coefficients for the polynomial curve.

a	**b**	**c**	**d**	**e**	**f**
92.35	14.09	-197.1	-28.78	133.2	20.68
g	**h**	**i**	**l**	**m**	
-27.64	-7.72	0.37	-0.43	1.21	

$$C(v) = \left[n \bullet e^{-o^3 \bullet v}\right] \bullet 10^{-12} \quad (2.4)$$

where the corresponding values of *n* and *o* are 0.9734 and -1.156, respectively.

Equation (2.3) describes a polynomial interpolation. This type of fitting, especially for high order polynomial degree, can exactly fit the data values, but usually, the result will be quite dissatisfactory between them, because interpolation is done by few points on exact match of values, therefore the behavior in between those points will be approximate and

usually incorrect in fact, it will not go from point to point as gracefully curved line but will wiggle wildly. Moreover, the polynomial interpolating equation is obtained using a tool that considers only the range of interest of dc bias voltage between -1 V and 1 V. Therefore, it works well in this range, but it doesn't consider what happens outside it. As it can be seen in Fig.2-7, the polynomial curve before -1 V and after 1 V tends to the infinite. This behavior is not reasonable, and unreal for the capacitance behavior, additionally, this becomes a problem when the model is used for high power values since the convergence problem arises. The exponential interpolating equation (2.4), as the polynomial one, works well in the range where the interpolation is performed and saturates for dc voltage values higher than 1 V. Nevertheless, for polarization lower than -1 V, as it can be seen in Fig. 2-15, it quickly increases until it reaches the vertical asymptote in which the function tends to the infinite, leading to convergence problem when high powers are involved.

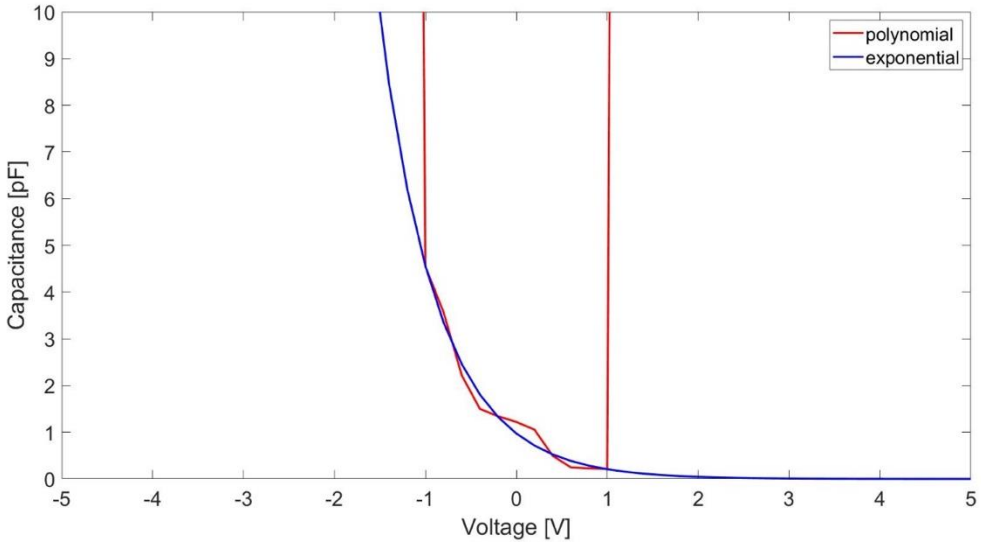


Fig. 2-7: Polynomial and exponential interpolating curves in the extended polarization range.

To prevent the curve blows up outside the limited range of interest and so to avoid convergence problems when high levels of power are involved, the function must saturate to a constant value outside the range of interest. A possible solution could be to use a piecewise function composed of the interpolating equation between -1 V and 1 V and, for example, two straight lines one for values greater than 1 V and the other for values lower than -1 V, nevertheless there are unavoidable equation discontinuities between regions 1 V and -1 V are points of discontinuities since the function is not continuous there.

For all the reasons above mentioned, the curve chosen for the interpolation is the following:

$$C(v) = [5.027 \bullet \tanh(0.1445 \bullet e^{-2.179 \bullet v}) + 0.03008] \bullet 10^{-12} \quad (2.5)$$

where v represents the applied dc bias voltage.

The fit-curve and the data of the series non-linear finger capacitance can be seen in Fig. 2-8:

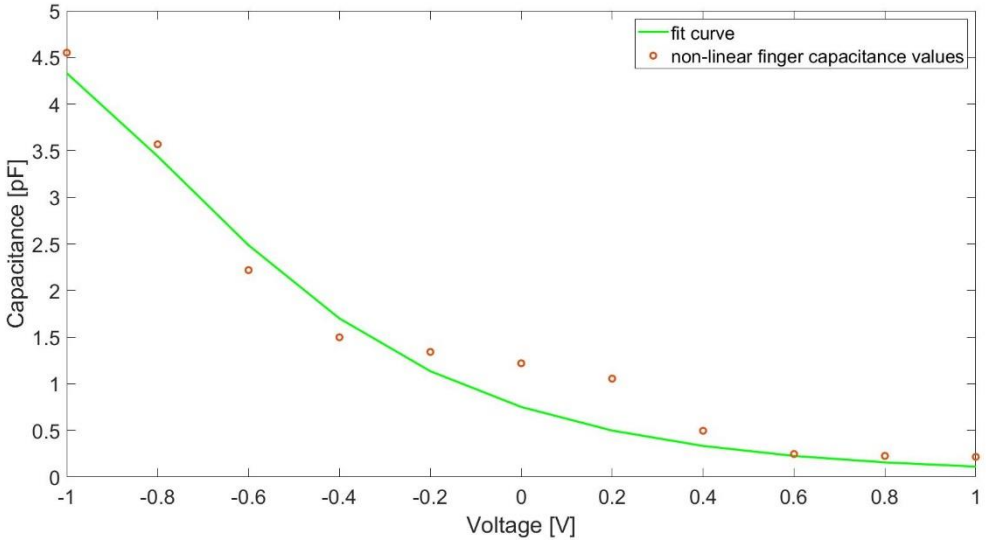


Fig. 2-8: C(v) fit curve to the achieved values of non-linear finger capacitance.

The equation (2.6) shows a good fitting of the voltage-dependent finger capacitance values, presenting a very low root mean square error that measures the differences between values predicted by the model and the values of the capacitance achieved. The hyperbolic tangent function is chosen to prevent C(v) from blowing up outside the polarization range considered. As shown in Fig. 2-9, the curve saturates to a constant value for dc voltage greater than 1 V and less than -1 V. In addition, unlike a piecewise function, it doesn't present discontinuities in these points, so it is continuous and differentiable over the whole domain. Therefore, it is possible to use this model with high levels of power without encountering convergence problems.

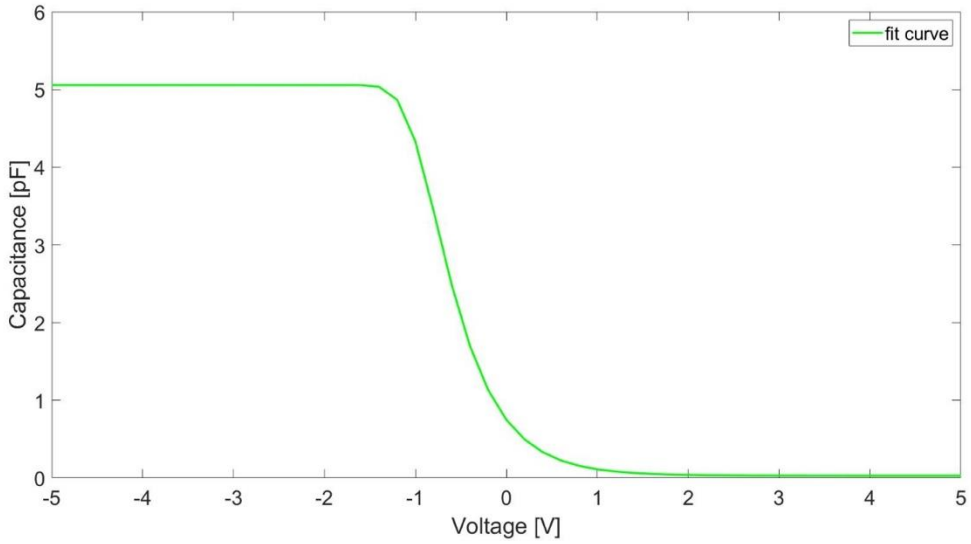


Fig. 2-9: C(v) curve fit to the achieved values of non-linear finger capacitance in the extended polarization range.

Once the best interpolation curve is chosen, the voltage-dependent capacitor is then implemented in ADS Keysight using a symbolically defined.

The symbolically defined device (SDD) is an equation-based component that enables the definition of nonlinear components. It is represented on the circuit schematic as an N-port device and up to 10 ports that can be modeled. An SDD is defined by equations, which relate port currents, voltages, and their derivatives, defined as the function of other voltages and currents. Before the SDD, the techniques that were available for modeling non-linear devices were limited and heavy, moreover, the only technique previously available was to develop a model that simulated both the large-signal and small-signal behavior of a non-linear device required developing source code, which was a complex task. For example, a typical BJT model would require over 4500 lines of code. The SDD instead, offers a simple and fast way to develop a complex non-linear model.

Typically, an N-port device is described by N-equations, called constitutive relationship, that relates the ports currents and the ports voltages. Since the SDD is used to model nonlinear devices, its constitutive relationships are specified in the time domain. They may be described in either explicit or implicit form. The explicit representation is a voltage-controlled expression and can implement only voltage-controlled expression, instead, the implicit representation can shape equations that are voltage-controlled, current-controlled, or use some other control. The constitute relationship should be continuous and differentiable concerning voltage and current, in addition, it is recommended that the

derivatives are continuous to the voltage and the current, because if the latter condition is not respected the simulator may have convergence problems, even at low power levels. These considerations, as already explained, are very important for piecewise-defined devices where the constitutive equations change depending on the region of operation.

Traditionally, a nonlinear network is described in the time domain through generalized parametric equations:

$$\bar{v}(t) = \bar{u}\left[\bar{x}(t), \frac{d\bar{x}}{dt}, \ldots., \frac{d^n\bar{x}}{dt}, \bar{x}_d(t)\right] \quad (2.6)$$

$$\bar{\imath}(t) = \bar{w}\left[\bar{x}(t), \frac{d\bar{x}}{dt}, \ldots., \frac{d^n\bar{x}}{dt}, \bar{x}_d(t)\right] \quad (2.7)$$

where $\bar{x}(t)$ are the state variables, $\bar{x}_d(t)$ are the delayed state variables and $\bar{u}$ and $\bar{w}$ are non-linear algebraic functions. The parametric formulation of the non-linear equations allows the maximum freedom in the non-linear device description. The choice of the state variable is arbitrary. The most suitable state variable for the non-linear device model developed in this thesis is the voltage across the finger capacitance. Therefore, every equation is written in function of the state variable.

As already said, the non-linear capacitance can be implemented using an SDD. Considering one port non-linear capacitance C(v), by definition the currents is described as:

$$i(v) = C(v) \bullet \frac{dv}{dt} \quad (2.8)$$

However, there is no way to implement this equation directly using an SDD because involves product of derivative. To avoid this problem, an intermediate variable $dv\_dt = \frac{dv}{dt}$ is defined. Then the capacitor is described by the equation:

$$i(v) = C(v) \bullet dv\_dt \quad (2.9)$$

The implemented SDD model is reported in Fig. 2-10:

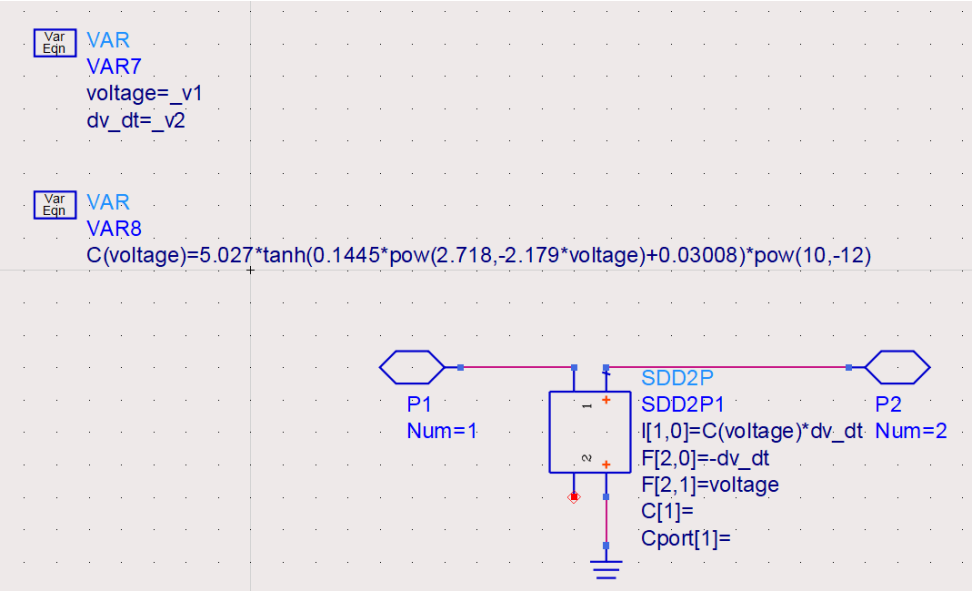


Fig. 2-10: The implemented SDD model.

Each port must have at least one equation. It is possible to specify more than one equation for a port, but they must be either all implicit or all explicit expression. When more than one equation is given for a port, the SDD calculates a separate spectrum for each expression. Each spectrum is weighted by the weighting function, specified for that spectrum. It is a frequency-dependent expression, evaluated in frequency domain, used to scale the spectrum of a port current. There are two predefined weighting functions. In particular, weighting function equal to 0, it is used when no weighting is desired. Weighting function equal to 1, instead, is defined as $j\omega$ and it is used when a time derivation is needed. In the case described in Fig. 2-18, a 2-port device is implemented. The port 2 voltage is defined to be the variable dv_dt. The F [2,0] and F [2,1] implicit expression defines the port 2 relationship, which is that F [2,0] +F [2,1] =0, or equally, $dv\_dt = \frac{dv}{dt}$. If this is plugged into the expression for port 1 current I [1,0], it results that $I(v) = C(v)\frac{dv}{dt}$.

The SDD model is inserted into the $HfZrO_2$ -loaded CPW interdigital capacitor equivalent circuit to reproduce the non-linear finger capacitance, as shown in Fig.2-11.

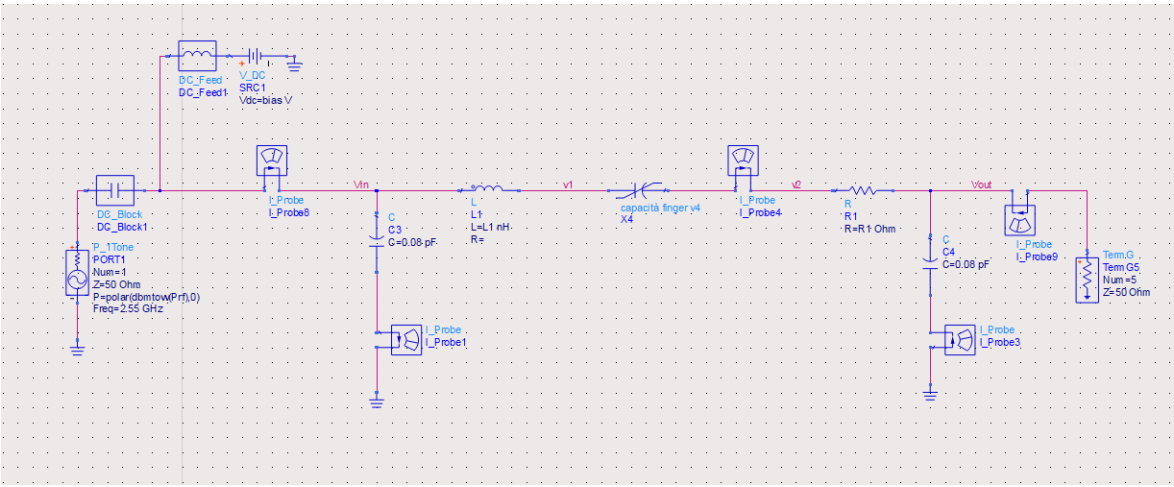


Fig. 2-11: IDC equivalent circuit including the SDD component.

In Fig 2-12 a comparison of the S-parameters obtained from the IDC equivalent circuit and the measured S-parameter are reported. The model is accurate and reliable since the S-parameters curves obtained with the model and the measure of the S-parameters obtained in [17] show the same trend and the error is almost negligible.

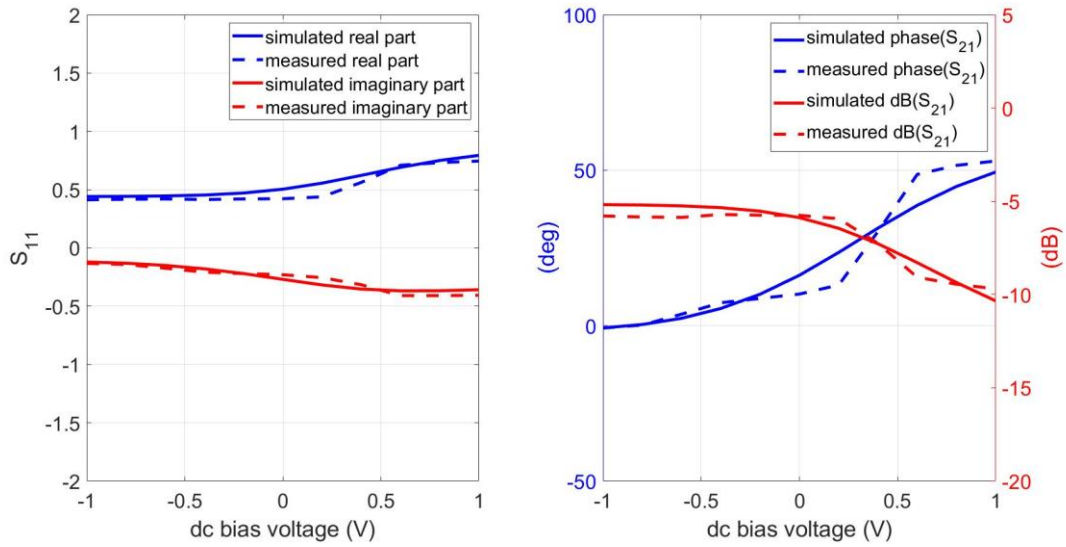


Fig. 2-12: Simulated and measured S-parameters at 2.55GHz of the proposed IDC.

Chapter 3
SIMULATION RESULTS AND MODEL APPLICATIONS

In Chapter 2, small-signal S-parameter simulations have been performed to find the best fitting for the measured values of the IDC proposed in [17]. In this Chapter, an accurate analysis of multiple aspects of the model is proposed. Firstly, the equivalent capacitance of the IDC is calculated. Then, a nonlinear simulation is performed and the results for high power input levels are discussed. Finally, a possible application of the model which exploits the ferroelectric properties of the $HfZrO_2$ is proposed.

3.1 **IDC equivalent capacitance**

The proposed model is a 2-port network composed mainly by three capacitors disposed in π-configuration as described in Fig.3-1, where Y_a and Y_c correspond to the admittance of the linear capacitances, whereas Y_b represents not only the admittance of the nonlinear capacitance, but the admittance of the series of inductance, nonlinear capacitance, and the resistance (C1, L and R). For this reason, it can be described with the π-network admittance matrix [24]:

$$Y = \begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix} = \begin{bmatrix} Y_a + Y_b & -Y_b \\ -Y_b & Y_b + Y_c \end{bmatrix} \quad (3.1)$$

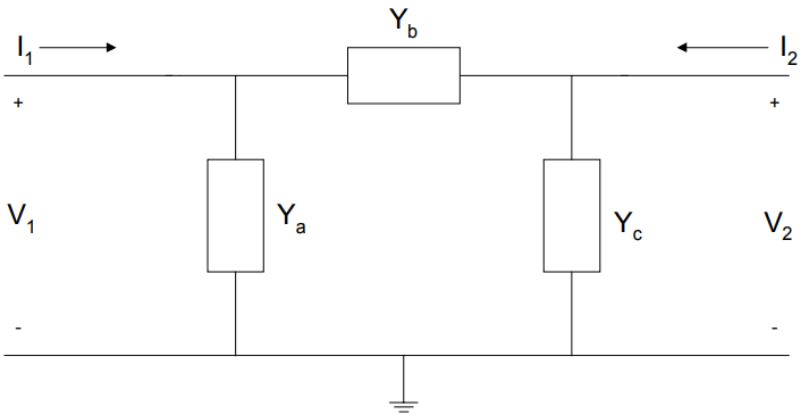


Fig. 3-1: Admittance matrix of a π-network [24].

To compute the capacitance of the network the admittance between output and input port is employed. Therefore, the capacitance is expressed as follows:

$$C_{eq} = \frac{Im(Y_{21})}{j\omega} \quad (3.2)$$

where Y_{21} is defined as the ratio between the output current and the input voltage when the output voltage is shorted to ground:

$$Y_{21} = \frac{I_2}{V_1}\Big|_{V_2=0} \quad (3.3)$$

Fig. 3-2 displays the values of the $HfZrO_2$ based IDC in terms of its capacitance at 2.55 GHz.

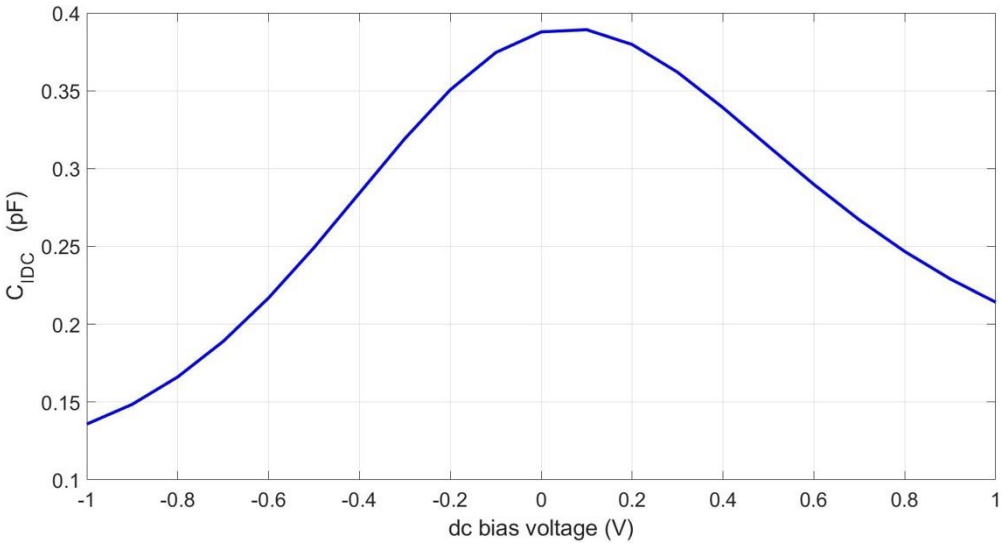


Fig. 3-2: Equivalent IDC capacitance as function of the applied dc bias voltage.

3.2 **IDC Harmonic Balance simulations**

As already mentioned in the previous chapter, here it is demonstrated that the implemented model works well even with high levels of power. By means of the circuital simulator ADS Keysight, Harmonic Balance, simulations are performed to simulate both the small-signal behavior of the circuit, when low levels of power are involved and large signal behavior, when higher levels of power are involved.

In the analyses of the nonlinear circuits, there are two manly used techniques: the time domain analyses and the harmonic balance method. The time-domain analysis is based on the numeric integration of differential equations that are first approximate in incremental ratio computed in discretized time values. Subsequently, for each of these instants, starting from the initial one, a nonlinear algebraic equation is calculated. However, this technique

has several limitations. In fact, in most cases, the time constants of the circuit turn out to be larger than the period of the RF signals, and consequently, integrations over many periods are necessary, considerably lengthening the simulations. Furthermore, in microwave circuits, there are distributed components that do not lend themselves to simulations in the time domain.

The harmonic balance instead, exploits a mixed domain since the linear components (such as matching networks) are described in the frequency domain, while the nonlinear components are described in the time domain.

The circuit is then divided into two subsystems: linear and nonlinear. The nonlinear subsystem is connected to the linear subsystem through N ports. Since the system is nonlinear, it is necessary to know the values of currents and voltages also for all harmonics k=1,.., K, where K is called the cut-off harmonic.

Considering the whole circuit, with for example M ports, the circuit analysis of the linear system can be solved through the following system:

$$\begin{bmatrix} I_{1,k} \\ \cdot \\ \cdot \\ \cdot \\ I_{N,k} \\ I_{N+1,k} \\ \vdots \\ I_{N+M,k} \end{bmatrix} = Y_{lin} \bullet \begin{bmatrix} V_{1,k} \\ \cdot \\ \cdot \\ \cdot \\ V_{N,k} \\ V_{N+1,k} \\ \vdots \\ V_{N+M,k} \end{bmatrix} \quad (3.3)$$

where $V_{i,k}$ is the i-th tension at the port at the k-th harmonic. $I_{i,k}$ is the correspondent current and Y_{lin} is the admittance matrix.

The nonlinear subnetwork is described in the time domain through the generalized parametric equations (2.6) and (2.7). Therefore, the nonlinear currents and nonlinear voltages are express as:

$$V_k = U_k(X) \quad (3.4)$$

$$I_k = W_k(X) \quad (3.5)$$

where the U_k and W_k are respectively the harmonics of $\bar{u}$ and $\bar{w}$.

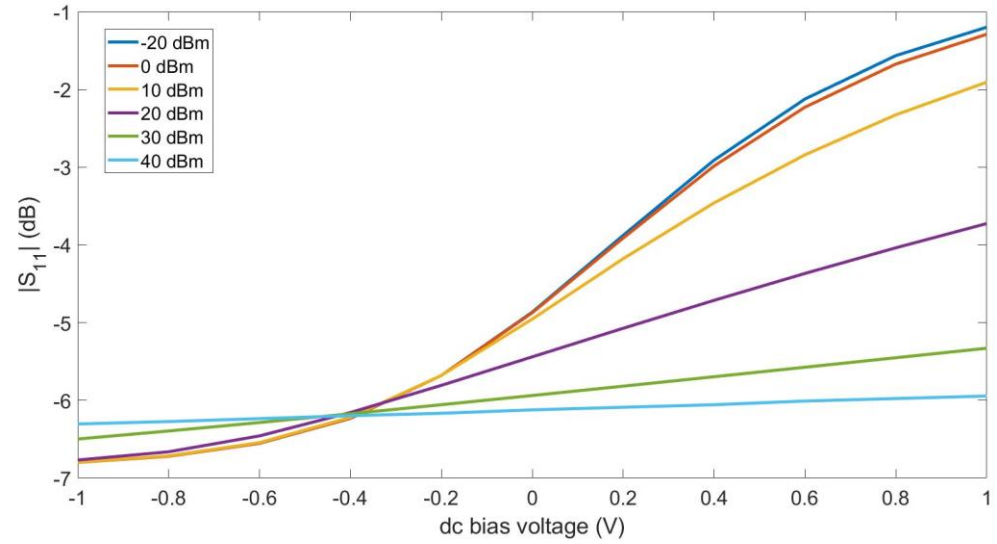
The parametric formulation of nonlinear equations allows maximum freedom in nonlinear description of the devices; it allows to work in cases in which a mathematical formulation that relates voltages to the currents at the ports is not possible.

3.3 **Small and large signal S-parameters simulation**

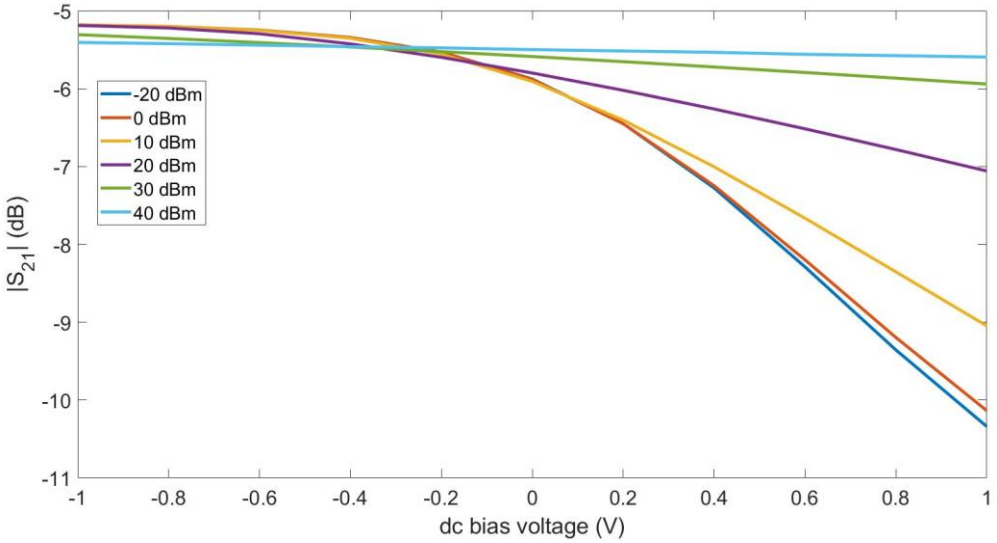
While the small-signal S-Parameters are simulated as a function of the frequency, the large signal S-Parameters (LSSP) are simulated as a function of the power, given the strong non-linearity of the circuit. As the S-Parameters at a small signal, they are defined as the ratio between the reflected and incident wave, as described in the equations (1.13) - (1.16).

In Fig. 3.1 are reported the S-parameters simulated with different levels of input power, from -20 dBm to 40 dBm with a 20-dBm step. The model has been simulated for power levels below -40 dBm but the differences between the solutions for very low power levels and the solutions at -20 dBm are negligible, and this is following the fact that the system is working at small-signal and therefore is linear. Consequently, the S-Parameters don't vary as the power varies. The LSSPs start deviating from the small-signal S-parameters when the applied power exceeded a certain level, and for this reason, they are also called power-dependent S-parameters. This is because, since Harmonic Balance is a large-signal simulation technique, its solution includes nonlinear effects such as compression. This means that the large-signal S-parameters can change as the power levels are varied. In Fig. 3.3 is possible to observe how the S-parameters change as the input power increases considering a Harmonic Balance simulation of order 32.

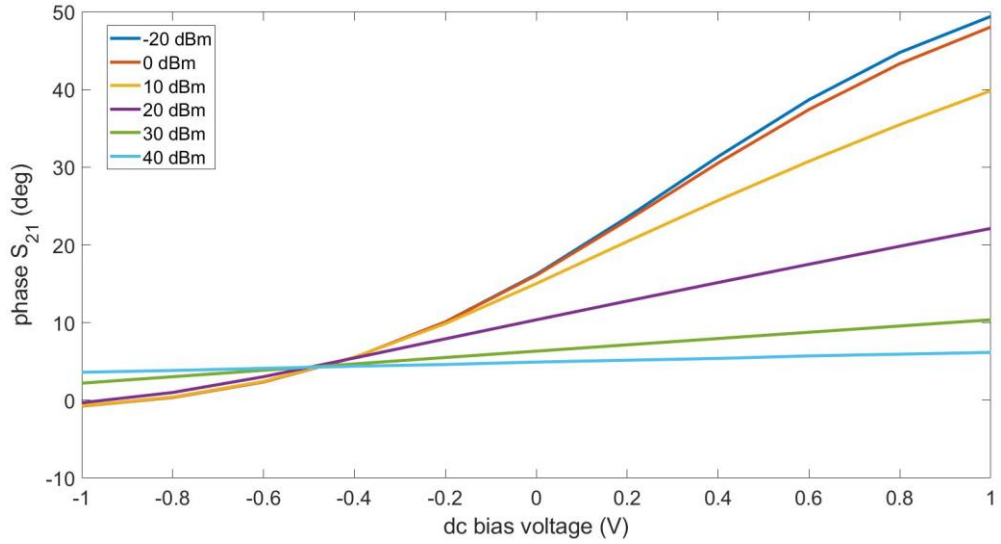
For low power values the phase shift, as a function of the dc applied voltage, increases when the bias moves towards 1V. In Fig.3-3(c) it is possible to see that at small signals the phase of the S_{21} is equal to -36 degrees from a dc bias voltage of -1 V and 13 degrees for a dc bias voltage of 1 V, leading to a 50-degree phase shift. Instead, when 40 dBm is considered, the difference between the two phases for -1 V and 1 V is almost 0°, leading to a negligible phase shift. In the proposed simulations the effects of permittivity dispersion in the frequency band are not considered.


-20 dBm
0 dBm
10 dBm
20 dBm
30 dBm
40 dBm
|S11| (dB)
dc bias voltage (V)

(a)


-20 dBm
0 dBm
10 dBm
20 dBm
30 dBm
40 dBm
|S21| (dB)
dc bias voltage (V)

(b)



(c)

Fig. 3-3: Model simulation values of S_{11} (a), S_{21} (b) and phase of S_{21}(c), as function of the dc bias voltage for a power sweep from -40 dBm to 40 dBm.

When larger signal amplitudes are considered, the nonlinear nature of components gets involved and distortion takes place. For example, in nonlinear components, the power absorbed from a dc power supply unit is partially converted into AC signal power at the outport port. Indeed, frequency conversion is only obtained by means of nonlinear components.

Due to nonlinearity spectral regrowth occurs, as shown from Fig.3-4 to Fig.3-6. The tone at $f_0 = 2.55\ GHz$ is called fundamental tone, the tones at nf_0, where $n \in N$, are called harmonics, and the tone at dc corresponds to AC/dc conversion. Also, the spectral components are a function of the input amplitude. It should be noted that, as the excitation amplitude decreases, the non-linear distortion terms (harmonics, AC/dc conversion, and distortion at the same excitation frequency) tend to vanish faster than the linear term leading to the existence of a range of values of amplitude such that the distortion can be almost neglected, and the behaviour of the device considered as nearly linear. This can be shown in Fig. 3-4, where, when -40 dBm of input power is considered the difference between the current at the fundamental and the second harmonic is 59.24 dB, this means that the presence of the second harmonic doesn't influence the performance of the system. On the contrary, as shown in Fig. 3-6, when the input power increases, the difference between the fundamental and the second harmonic decreases, being only 18.39 dB for 40 dBm. In the latter case, several problems due to non-linearity arise.

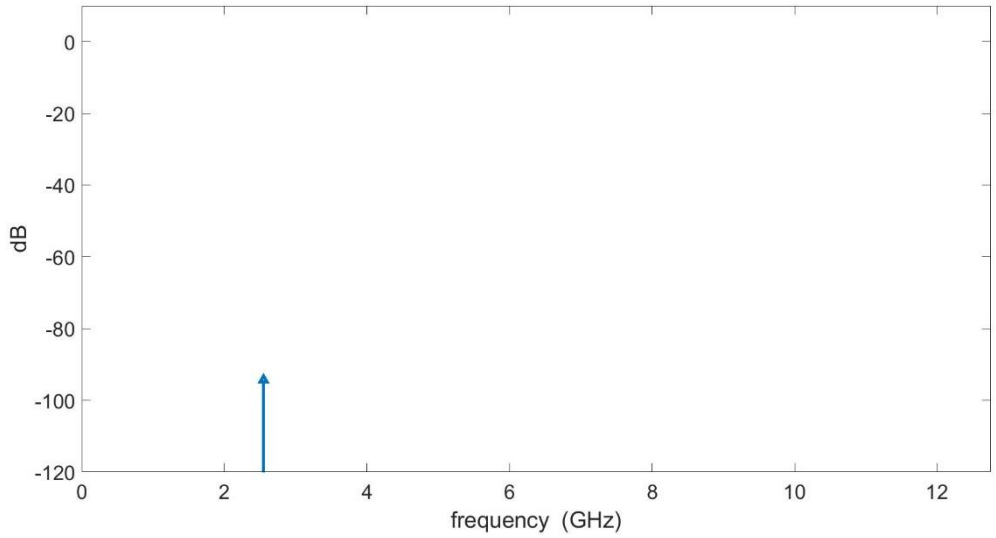


Fig. 3-4: Current spectral regrow for -40 dBm of input power with constant bias voltage of 1 V.

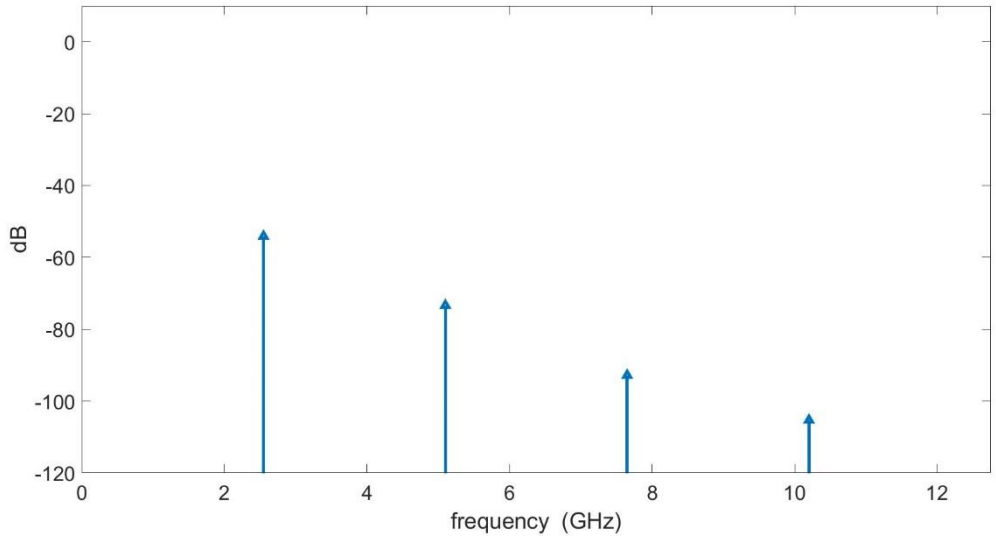


Fig. 3-5: Current spectral regrow for 0 dBm of input power with constant bias voltage of 1 V.

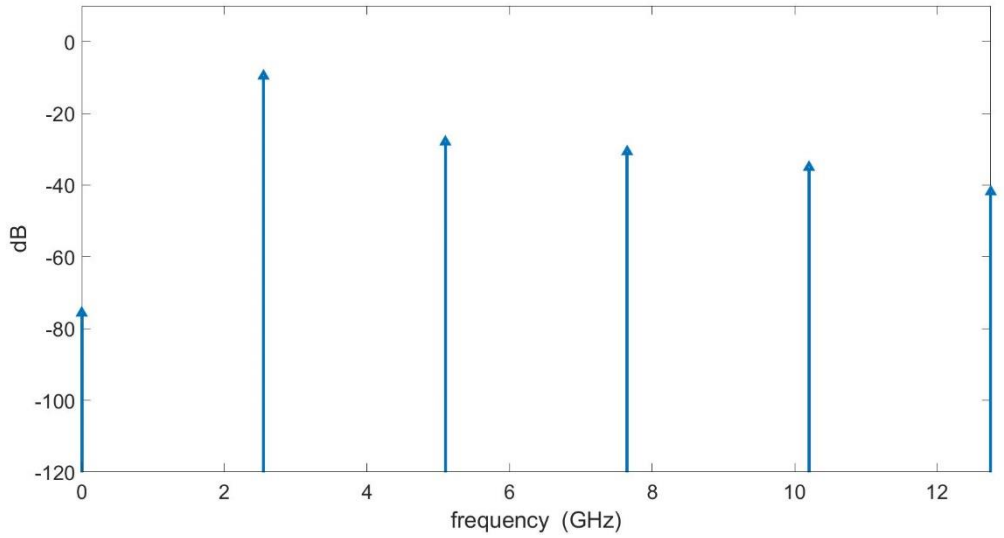


Fig. 3-6: Current spectral regrow for 40 dBm of input power with constant bias voltage of 1 V.

In addition, with nonlinear distortion the application of a sinusoidal input currents results in a periodic output waveform that is non-sinusoidal, as can be seen from Fig.3-7 to Fig. 3-9. At small signal, with an input power equal to -40 dBm, as shown in Fig.3-7, the output current waveform is identical to the input one, except for a scale factor α and a time shift τ, instead when the input power increases, the waveform becomes distorted. However, the nonlinearities arise after 0 dBm of input power, since, as shown in Fig 3-8, with 0 dBm of input power the output current waveform is still sinusoidal.

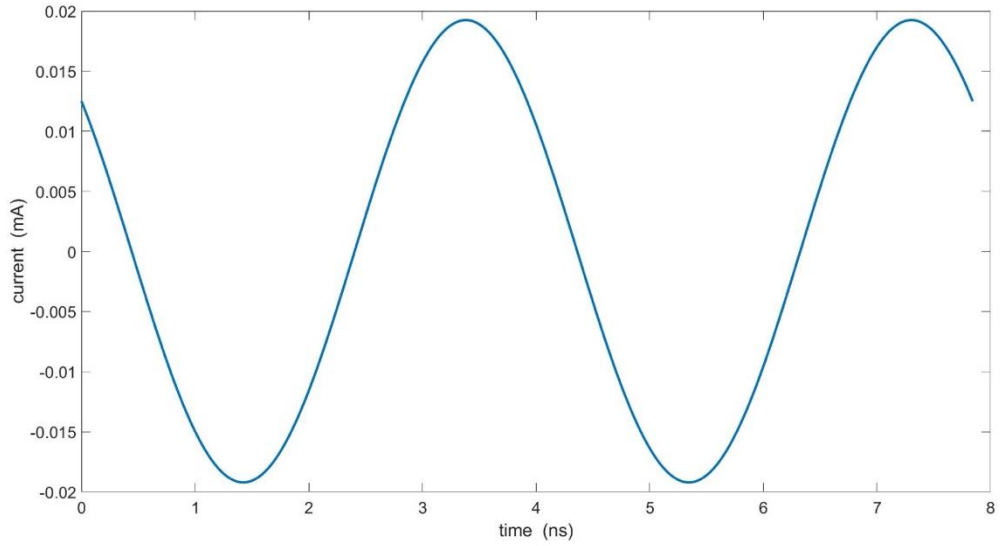


Fig. 3-7: Output current waveform for -40 dBm as input power with constant dc bias of 1 V.

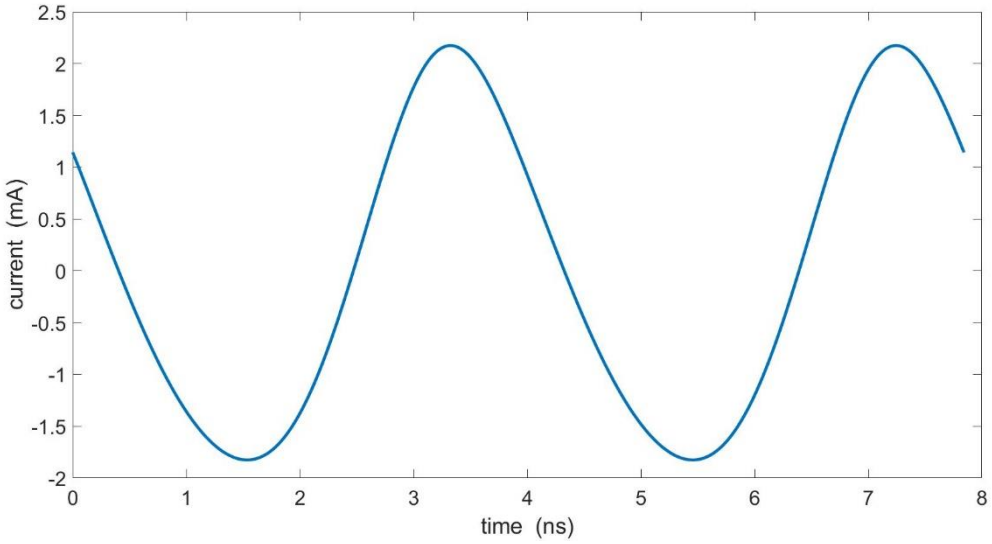


Fig. 3-8: Output current waveform for -40 dBm as input power with constant dc bias of 1 V.

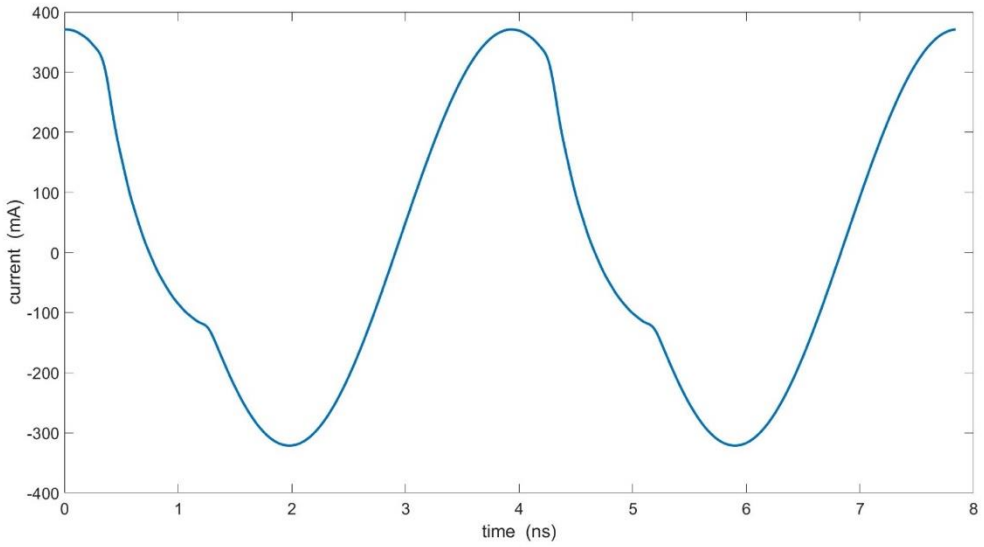


Fig. 3-9: Output current waveform for -40 dBm as input power with constant dc bias of 1 V.

3.4 **Design of a patch on high-resistivity silicon substrate**

As introduced in the first chapter, since the final application of the model is to use the $HfZrO_2$ based IDC as a phase shifter for beam steering applications, an antenna array is designed by means of CST STUDIO SUITE 2019 simulator and subsequently a circuital and electromagnetic co-simulation is performed. Before the realization of the array, a single

microstrip patch antenna resonating at the frequency of interest, that is 2.55 GHz, is designed.

From the literature it is known that when $W << h$ and $h << \lambda$, where W is the width of the hot wire, h is the height of the substrate, and λ is the wavelength of the signal, the structure, if high frequencies are involved, guides the signal. However, when the condition $W << h$ is violated, the guided behavior is not guaranteed anymore, and the structure can be exploited for its radiating properties. The so called microstrip patch antenna shows many advantages over conventional wire and metallic antennas, such as, low profile, light weight and ease of fabrication and integration with RF devices.

The designed microstrip square antenna patch is shown in Fig.3-10:

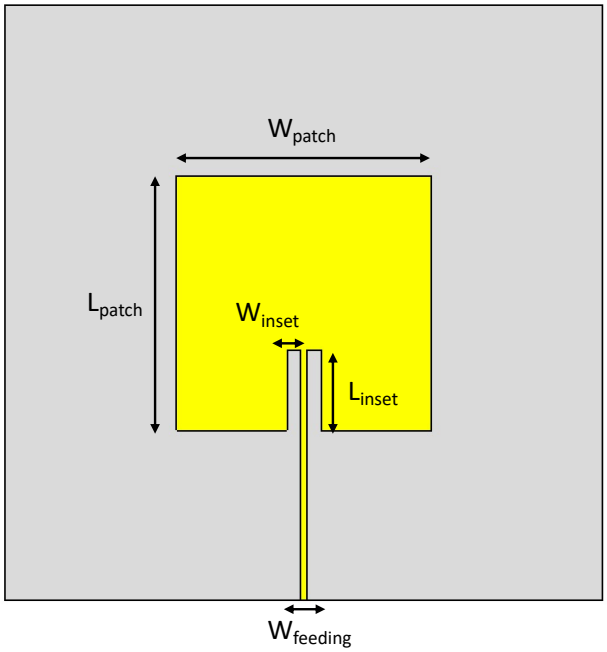


Fig. 3-10: Top view of the square microstrip patch.

Table 3-1: Layout dimensions of the proposed patch antenna.

W_{patch} [mm]	L_{patch} [mm]	W_{inset} [mm]	L_{inset} [mm]	$W_{feeding}$ [mm]
17.09	17.09	0.92	5.42	0.45

This antenna is designed and simulated at resonant frequency of 2.55 GHz using CST STUDIO SUITE 2019 simulator tool. The designed configuration includes three various elements such as gold patch, HRSi substrate, and gold ground plane. The layer on which the antenna is deployed is 525 μm of high resistive silicon, with $\varepsilon_r = 11.9$ and a tangent

loss equal to 0.01. To impose the resonant condition at frequency 2.55 GHz, a first hypothesis of the length of the square patch antenna is:

$$L = W = \frac{\lambda_0}{2 \bullet \sqrt{\varepsilon_r}} = \frac{0.12}{2 \bullet \sqrt{11.9}} = 17\ mm \quad (3.6)$$

where $\lambda_0 = \frac{c}{f} = \frac{3.8 \bullet 10^8}{2.55 \bullet 10^9} = 0.12m$ is the free space wavelength.

To compute the width of the microstrip, the CST impedance calculator is used. Putting the value of the electrical permittivity of HRSi and the value of the impedance of the microstrip, that is 50 Ω, the width of the microstrip is obtained, that is equal to 0.45 mm. Table 3-1 shows the layout dimensions of the proposed microstrip antenna.

Inset feed line is provided at the center of the patch to match the impedance so that the reflection wave can be minimized. For better operation, the return loss should be as low as possible, and this can be done by proper impedance matching. The designed antenna is correctly working at the intended frequency so the return loss at the resonant frequency of microstrip square patch antenna is 43.57 dB. The simulated reflection coefficient of the antenna is shown is Fig. 3-11.

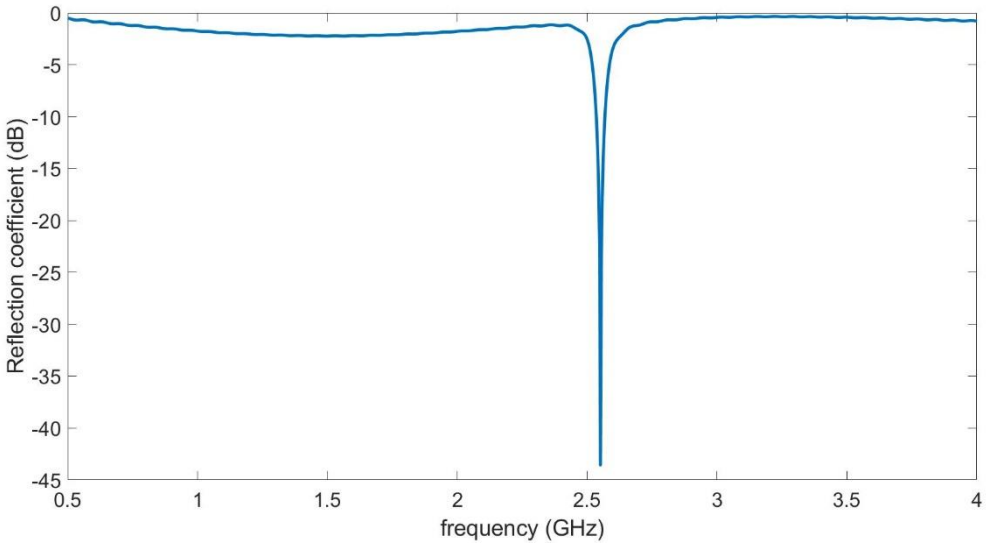


Fig. 3-11: Reflection coefficient plot for the designed square patch antenna.

The radiation efficiency is only 19%, but this is due to the HRSi substrate of the patch antenna, because, as explained in Chapter 1, silicon substrate exhibits a high loss tangent and high permittivity therefore it absorbs most of the RF power that is dissipated through Joule effect rather being radiated into the air, in addition the height of the substrate is large. These aspects affect noticeably the antenna's radiation performance.

The designed antenna radiates in the broadside direction, as can be seen in Fig.3-12, with a gain equal to 0.625. Since gain is given by the product between the radiation efficiency and the directivity, given the small radiation efficiency, also the gain is quite low. Moreover, it presents a good directivity, since it doesn't depend on the radiation efficiency.

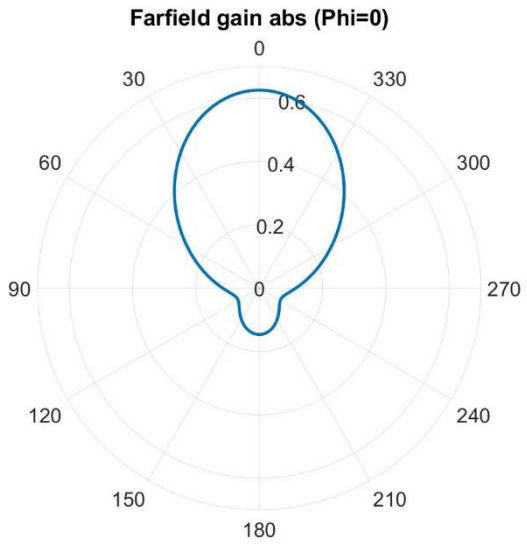


Fig. 3-12: Radiation pattern of the designed single square patch antenna.

3.5 **Phased antenna array design**

A phased antenna array is an antenna array whose single antennas can be fed with different phase shifts. As a result, the common antenna pattern can be steered electronically.

The electronic steering, as already explained in Chapter 1, is much more flexible and requires less maintenance than mechanical steering of the antenna which is limited for the static environment due to the limitation in the steering speed. In a simple antenna array, the radiofrequency current from the transmitter is fed to multiple individual antenna elements with the proper phase relationship so that the radio waves from the separate elements combine to form beams, to increase power radiated in desired directions and suppress radiation in undesired directions. In this case, a phased array composed of two identical patch antennas described before is implemented. The power from the transmitter is fed to the radiating elements through the $HfZrO_2$ based IDCs, which play the role of phase shifters, which can alter the phase electronically, thus steering the beam of radio waves to a different direction.

Before the electromagnetic simulation of the antenna array, the far-field calculation of antenna arrays CST STUDIO SUITE 2019 tool is employed to get a rough idea of the array far-field. This tool offers the possibility to apply the pattern multiplication, that is the product of the element pattern and the array factor (AF), to a calculated far-field monitor to achieve the corresponding result for a specific antenna array composed of identical elements:

$$\bar{E}_{total}(\hat{e}_r) = C \bullet \bar{E}_{single}(\bar{e}_r) \bullet AF(\hat{e}_r) \quad (3.7)$$

$$AF = \sum_n A_n \exp(ik\bar{x}_n \bullet \hat{e}_r + i\varphi_n) \quad (3.8)$$

The application of an array factor described in Eq. 3.8, provides only an approximation to the calculation of an entire array. It doesn't guarantee energy conservation, in fact, the radiated power of the entire array may exceed the total input power of the array. For this reason, the total radiated power of the array is set equal to that of a single antenna element multiplied by the summation of the magnitude of all elements in the array:

$$(P_{rad})_{total} = (\sum_n {A_n}^2) \bullet (P_{rad})_{single} \quad (3.9)$$

This leads to the scaling factor C that is included in the pattern multiplication Eq (3.10):

$$C = \sqrt{\frac{(\sum_n {A_n}^2) \bullet \int \left|\bar{E}_{single}(\hat{e}_r)\right|^2 d\Omega}{\int \left|\bar{E}_{single}(\hat{e}_r)\right|^2 \bullet |AF(\hat{e}_r)|^2 d\Omega}} \quad (3.10)$$

A significant rescaling of the array farfield indicates a poor performance of the array factor multiplication due to strong mutual coupling among the array elements.

As shown in Fig. 3.3(c), as the input power increases, the related phase shift at the output of the capacitance is highly reduced. This implies that if a large steering is needed, a low power at input is necessary and this can lead to the need to use an amplifier at the front-end, given the low radiation efficiency that the type of substrate used can provide. The case in which the input power is equal to 0 dBm, the midpoint of the power range used, is now proposed as a functional test. If the input power is equal to 0 dBm, we have that for a polarization value of the $HfZrO_2$ equal to -1 V, the phase value of the S_{21} is equal to -35 degrees while for a polarization value equal to at 1V, the corresponding phase is equal to 12 degrees, which leads to a relative phase shift of 47 degrees.

Using the tool array factor presented previously and assuming that the antennas are spaced by $\frac{\lambda_0}{2}$, to maximize the broadside radiation [25] and also providing the array with the combinations of polarization -1 V and 1 V, 1 V and – 1 V, the radiation diagram shown in Fig.3-13 is obtained, where the trend of the overall farfield is also shown when the phases

supplied to the two capacities placed in front of the antennas are the same. As shown in Fig. 3-13, for the combinations mentioned above, a beam-steering is obtained equal to 11 degrees to the left or right depending on the combination chosen. Through this type of simulation, it is also possible to calculate the gain of the array: when the phase supplied to the two patches is the same or different, depending on the combinations, the gain remains stable at 1.1.

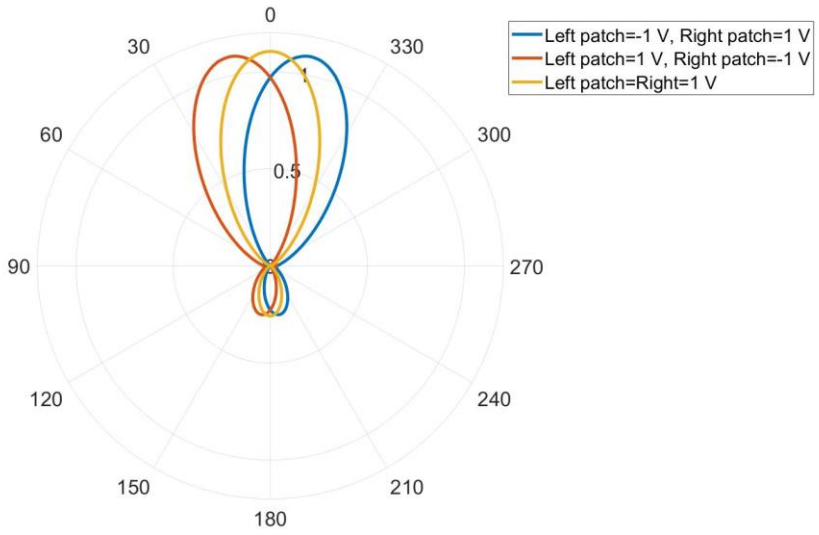


Fig. 3-13: Radiation patterns obtained with array factor tool for different combinations of dc bias given at the input ports of the system.

However, this type of simulation provides an initial, albeit reliable, idea of what the correct radiation pattern is. To make the discussion more coherent, a linear array composed of two patches arranged along the X axis is shown. The electromagnetically simulated system is shown in Fig. 3-14.

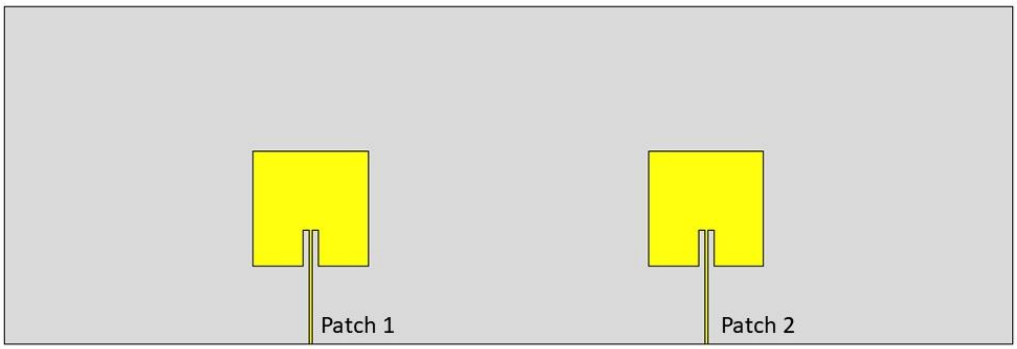


Fig. 3-14: Phased antenna array composed of two patches.

Through the simulation of the entire system, the electromagnetic coupling is also considered, which is minimized by using a distance between the two elements equal to $\frac{\lambda_0}{2}$ but which remains present. In the case presented, the electromagnetic coupling of the two patches is about -35 dB at the operating frequency of 2.55 GHz. Once the array has been simulated, the Touchstone file containing all the antenna information has been exported and simulated on ADS, where two interdigitated capacities modeled as treated in this thesis have been connected in series at the ports of the two antennas. In this way it was possible to simulate the amplitudes and phases of the currents at the input port of the antennas. As expected, the phase values are almost identical to those simulated previously and used in the simulation phase using the array factor tool. This is easy to understand since all the simulations carried out by the IDC on ADS have been performed with output loads equal to 50 ohm and since the antennas are also matched to 50 Ω, the result at the ports is almost identical.

Using a post-processing function present in the CST simulator, it is possible to obtain the overall farfield of the array in real-time by inserting the phases and amplitudes present at the ports. In this simulation it was also possible to insert in the post processing phase the values of the amplitudes at the ports, which made the simulations more truthful. Considering also in this case an input power equal to 0 dBm, a current value equal to 0.003 A and -35 ° at -1V and 0.0018 A and 12 degrees at 1 V, is obtained. The schematic with which the currents were simulated is shown in Fig. 3-15.

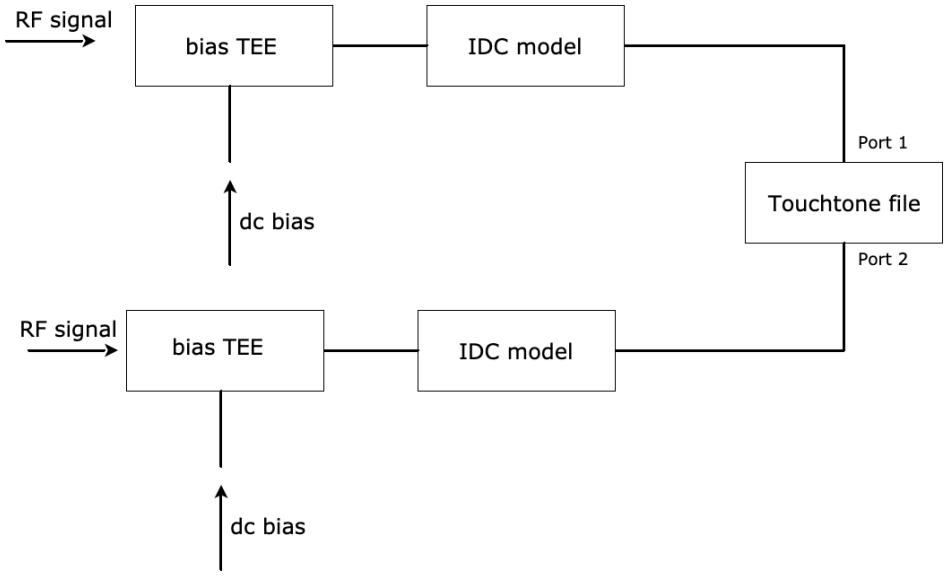


Fig. 3-15: ADS block-schematic used to simulate the currents at the input ports of the antennas.

Fig. 3.16 instead shows the trend of the farfield calculated through the circuit and electromagnetic co-simulation, exporting the touchstone file, and using the post-processing tool. As can be seen from Fig. 3.16, the beam-steering obtained is equal to 11 degrees and the orientation depends on the combination chosen, a value in line with the result obtained previously. As far as the gain is concerned, this differs from the simulation carried out with the array factor tool. In fact, in this case a value equal to 1.05 has been obtained when the phase supplied to the two patches is the same, while a gain equal to 1.02 when the beam-steering is activated. These lower gain values are consistent with the fact that in the previous simulation, effects such as electromagnetic coupling and amplitude of port currents were not considered.

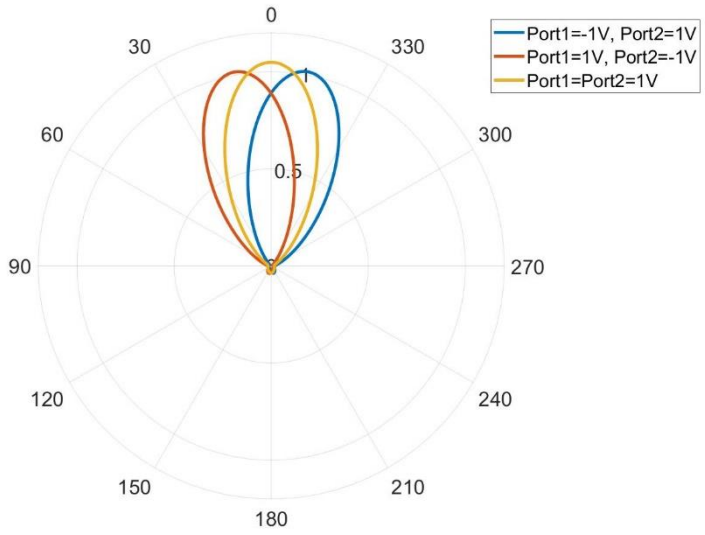


Fig. 3-56: Radiation pattern obtained with the following dc bias: -1 V at the port 1 and 1 V at the port 2 (orange line), 1 V at the port 1 and -1 V at the port 2 (blue line), same dc bias at the two ports (yellow line).

Observing Fig. 3-3(c) it is clear to understand how by using combinations of polarizations in which the difference between the port bias is small, the effect of beam-steering is also reduced. In Fig.3-17 are reported examples for some other combinations of dc polarization.

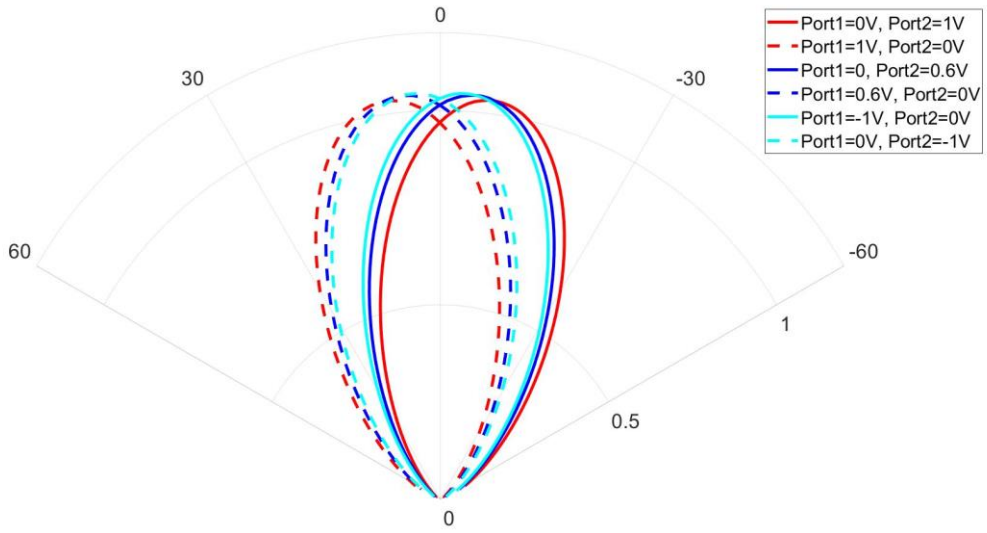


Fig. 3-17: Radiation pattern obtained with combine results tool considering different combinations of dc bias at the input ports.

CONCLUSIONS

In this thesis, the development of a nonlinear model of a tunable phase shifter realized through interdigitated capacitance is proposed. The model was studied starting from measurements of an interdigitated capacitance made on a substrate composed of high permittivity silicon and a ferroelectric material, $HfZrO_2$. In this thesis, the ferroelectric phenomena have been analysed, paying particular attention to those compatible with modern CMOS processes, which will create the future System on-chip. The proposed model was analysed by linear simulation at very low power and tested for high power (> 30 dBm) by nonlinear Harmonic Balance simulation, which demonstrated the excellent stability of the proposed model. As a verification of the model, a linear array of two patches was designed with the task of realizing the beam-steering function. Various combinations of polarization have therefore been proposed and in particular, the one with -1V and 1V supplied to the ferroelectric substrate has been studied with particular attention, demonstrating the ability of the array to realize a beam-steering equal to 11 degrees considering an input power equal to 0 dBm.

The further step of this thesis will be the study and the development of a nonlinear model for general purpose IDC based on ferroelectric materials. In particular, the future model aims to present coefficients that will describe different geometrical properties such as the number of fingers, the length of the latter and so on. This will imply a fast and reliable model which can be exploited in complex but fast electromagnetic and circuital simulations, for example where more than two antennas are used to increase the overall gain of the system. Also, in the future developments, the dispersion of the substrate material will be taken into account in order to model the behaviour of the IDC, not only as a function of the dc bias voltage, but also of the frequency.

The model developed in this thesis was studied within the European project Horizon 2020 'NANOMATERIALS ENABLING SMART ENERGY HARVESTING FOR NEXT-GENERATION INTERNET-OF-THINGS'. NANO-EH has the ambitious vision of creating a pathway for translating forefront knowledge of unique high frequency properties of emerging classes of nanomaterials into advanced device engineering for scalable

miniaturized energy harvesting/storage submodules that are tailored for the specific needs of stand-alone, mobile or portable uses. It aims to surpass the current paradigm of energy harvesting materials by developing non-toxic and rare earth/lead-free materials exhibiting CMOS-compatibility and scalability for low cost and large-scale manufacturing.

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