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In

Power Electronic Circuits M

Hardware-in-the-Loop implementation of Single- and Dual-phase shift control for Dual Active Bridge Converters in EV applications

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To my Professor, Mattia Ricco, and my mentor, Riccardo Mandrioli,
Who has guided me on the correct path and made it possible.

Abstract

Isolated DC-DC converters play a significant role in fast charging and maintaining the variable output voltage for EV applications. This study aims to investigate the different Isolated DC-DC converters for onboard and offboard chargers, then, once the topology is selected, study the control techniques and, finally, achieve a real-time converter model to accomplish Hardware-In-The-Loop (HIL) results.

Among the different isolated DC-DC topologies, the Dual Active Bridge (DAB) converter has the advantage of allowing bidirectional power flow, which enables operating in both Grid to Vehicle (G2V) and Vehicle to Grid (V2G) modalities. Recently, DAB has been used in the offboard chargers for high voltage applications due to SiC and GaN MOSFETs; this new technology also allows the utilization of higher switching frequencies. By empowering soft switching techniques to reduce switching losses, higher switching frequency operation is possible in DAB.

There are four phase shift control techniques for the DAB converter. They are Single Phase shift, Extended Phase shift, Dual Phase shift, Triple Phase shift controls. This thesis considers two control strategies; Single-Phase, and Dual-Phase shifts, to understand the circulating currents, power losses, and output capacitor size reduction in the DAB.

Hardware-In-The-Loop (HIL) experiments are carried out on both controls with high switching frequencies using the PLECS software tool and the RT box supporting the PLECS. Root Mean Square Error is also calculated for steady-state values of output voltage with different sampling frequencies in both the controls to identify the achievable sampling frequency in real-time. DSP implementation is also executed to emulate the optimized DAB converter design, and final real-time simulation results are discussed for both the Single-Phase and Dual-Phase shift controls.

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1. Introduction

Due to continually increasing utilization of petroleum products, especially in the transportation system, carbon particles' emissions damage the earth's atmosphere. The world is shifting into electric vehicles instead of using Gasoline vehicles to reduce these emissions. Batteries are a significant source of electric vehicles, but the problem we encounter in using them is the charging time; comparatively, to fill the tank of classic cars, less time is required for long-range driving. A lot of research has been conducted to fulfill this basic need.

In brief, the battery chargers are of three types: wireless, onboard, and offboard chargers, and their power ratings are divided into three levels, see Table 1. Wireless chargers have many drawbacks in power electronic technologies and should also consider the installation cost. The onboard charger's maximum output range is around 2 to 20 kW, so the charging time is about 1-10 hours, and the charging process takes place in homes or public businesses. On the other hand, the maximum output range of the offboard charger is around 350 kW and the average time required for a full charge is 10/20min. Mostly, this type of charging method takes place at dc fast-charging stations. To achieve a full charge within 10min, the charger and the power electronic components play a crucial role.

Table 1. Charging Power Levels [1]

Power Level	**Type of charger**	**Usage Location**	**Power ratings**	**Charging time**	**Connector**
Level 1	On-board	Home	2 kW	4-11 h	SAE J1772
Level 2	On-board	Public	20 kW	1-4 h	SAE J1772
Level 3	Off-board	Dc fast	350 kW	<30 min	CHAdeMO/ CCS COMBO 2

Power delivery capability depends not only on the charge acceptance of the batteries and the charger's ratings but also on the type of connector and cable between vehicle and charger. Connectors of the EV charger for different levels are defined from the international standards as follows. AC level 1 and level 2 onboard chargers are determined by the Society of

Automotive Engineers (SAE) in North America in the SAE J1772 standard. Whereas IEC 62196-3 standard for DC level 3 offboard chargers are defined as the Configuration AA proposed and implemented by CHAdeMO association (CHArge and MOve), Configuration BB know as GB/T and available only in China, Configuration EE [Type 1 Combined Charging Systems (CCS), adopted in North America], Configuration FF [Type 2 CCS, adopted in Australia]. There is also a unique connecter from Tesla Inc. and used exclusively for Tesla vehicles [2]. Since our primary focus is on DC fast charging systems, the connector's power ratings and standard details are shown in Table 2.

Table 2. Power ratings and Standards of DC fast charging system **[2].**

Standard	**CHAdeMo IEEE 2020.1.1 IEC 62196-3 (Conf. AA)**	**GB/T GB/T 20234.3 IEC 62196-3 (Conf. BB)**	**CCS Type 1 SAE J1772 IEC 62196-3 (Conf. EE)**	**CCS Type 2 IEC 62196-3 (Conf. FF)**	**Tesla**
Maximum Voltage	1000 V	1000 V	600 V	1000 V	410 V
Maximum Current	400 A	250 A	200 A	200 A	330 A
Available Power	400 kW	120 kW	150 kW	175 kW	135 kW

1.1. Design parts of an EV charger

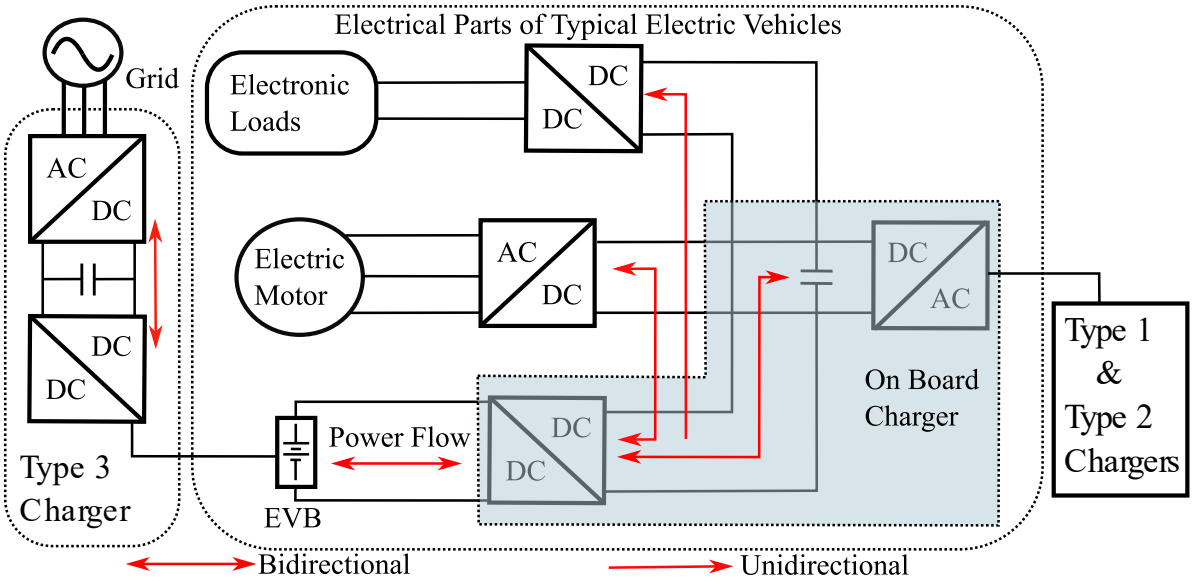

Fig. 1. Charging system configuration for electric vehicles

The charger consists of two stages, and its Configuration is shown in Fig.1. [1], The AC-DC converter and Power Factor Correction (PFC) are the first converter stages, either in bidirectional or unidirectional power flow. PFC is used to improve the charger's efficiency by reducing the wastage of electricity and decreasing heat loss. AC-DC converter types and their studies are not discussed here since our primary interest is on DC-DC converters. An AC-DC converter's output is a fixed DC value, but the battery charging takes place from a wide range of voltages, i.e., from a low voltage (50 V) to high voltage (1000 V). So, using only an AC-DC converter is not sufficient to charge a battery. Here comes the second stage of a charger, i.e., a DC-DC converter. The output of these types of converters is a variable DC value suitable to charge a battery. A comprehensive analysis of DC-DC converters and their classes are provided in chapter 2.

2. Isolated DC-DC converter

Isolation means providing insulation between the grid and the vehicle battery using the Isolated DC-DC converter inside the battery charger. Since EV batteries are not grounded, this galvanic isolation typically uses a high-frequency transformer, protects the batteries, and remains unaffected by the charging system [2]. A high-frequency transformer reduces the size of the magnetic components and decreases the converter's size. Different types of isolated DC-DC topologies are presented below.

2.1. Unidirectional Isolated DC-DC converters

2.1.1. Phase-Shift Full-Bridge (PSFB) converter

The first topology under this category is Phase-Shift Full-Bridge (PSFB) converter, shown in Fig.2. MOSFETs are the best suitable switching device in the converters for the application in the range of few kilowatts. The robust and reliable Zero Voltage Switching (ZVS) method is used to switch the MOSFETs since it has numerous advantages, such as reducing switching losses and the control circuit's noise [3]. The ZVS and ZCS operation was provided in [4] and [5]. The leakage inductance inside the PSFB converter is responsible for Zero Voltage Switching [6]. [3], ZVS range can be extended (for all load conditions) by increasing the size of inductance, but it limits the power transfer capability and increases the duty cycle losses. The technique for improving the ZVS range was given in [7]. While obtaining the wide range of ZVS, the energy stored in the transformer inductance at the secondary side, along with output inductance, causes a voltage ringing across the diodes. Rectifiers Based on current-driven can effectively reduce the voltage spikes and provides Zero Current Switching (ZCS), eliminating the reverse recovery losses across the output diodes. Inductance in series with the transformer primary, which acts as a current source, can achieve current-driven rectifiers. The use of snubber circuits also reduces the voltage spikes but increases the converter's size and cost. Moreover, voltage stress across the diode will be greater than the output voltage, making this topology unsuitable for high voltage applications [3], [6]. Besides, ZVS can achieve high performance, especially while using the trailing-edge pulse width modulation full-bridge control scheme.

From Fig.2, the primary side circuit of the converter contains a conventional full-bridge inverter. However, the lower switches (Q_3 and Q_4) are driven at a fixed 50 percent duty cycle

rather than concurrently forcing the diagonal bridge switches. The upper controls (Q_1 and Q_2) are PWM on the trailing side [8].

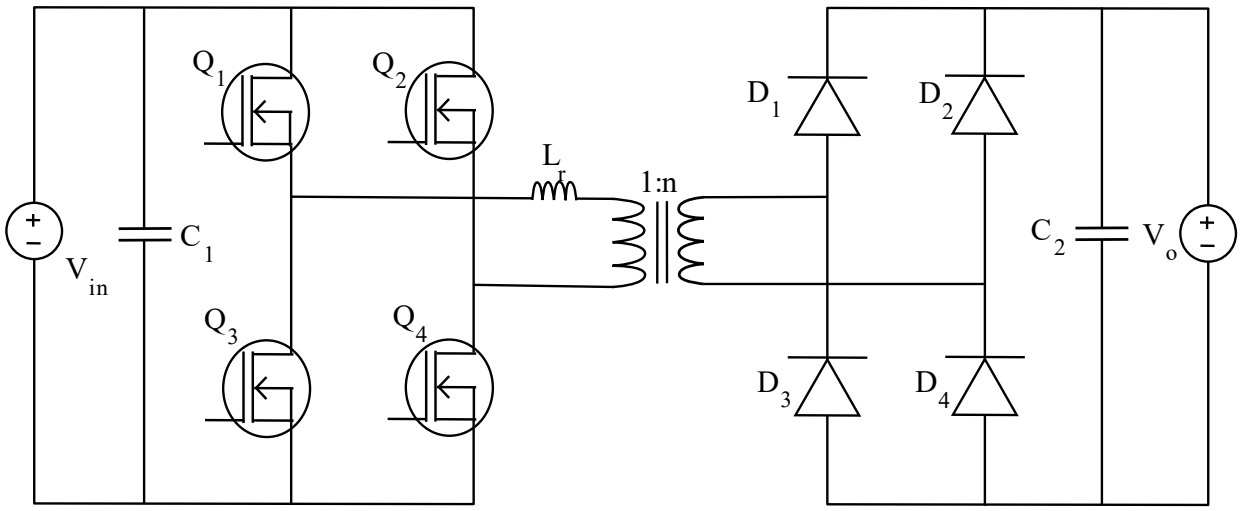

Fig. 2. PWM ZVS full bridge with a capacitive output filter.

The PSFB converter can be operated in either discontinuous conduction mode (DCM), boundary conduction mode (BCM), and continuous conduction mode (CCM). For DCM, BCM, or CCM, this converter has six operating intervals. The ON and OFF states of the four primary switches decide the operating intervals. Detailed operating waveforms of DCM, BCM, CCM are provided in Fig.3 a,b,c., respectively [8].

A. Interval 1 (T0−T1)

Reference to fig.3 (DCM, BCM, and CCM), during Interval 1 (T_o–T_1), the switches Q_1 and Q_4 are ON, and the switches Q_2 and Q_3 are OFF. This interval is the power transfer interval, and the primary current flows through Q_1, the resonant inductor L_R, the primary transformer, and the Q_4. The current $(\frac{di}{dt})$ increase through resonant inductor L_R is proportional to the difference between the input voltage V_{in} and the output voltage V_0. Power flows to output through the rectifier diodes D_1 and D_4 during this mode, and energy is stored in L_R. The current $i_{L_R}(t)$ resonant inductor using the initial $i_{L_R}(0)$= 0 condition is specified [8]

$$i_{L_R}(t) = \frac{(V_{\text{in}} - \frac{V_0}{n})}{L_R}(t - T_o) \quad (1)$$

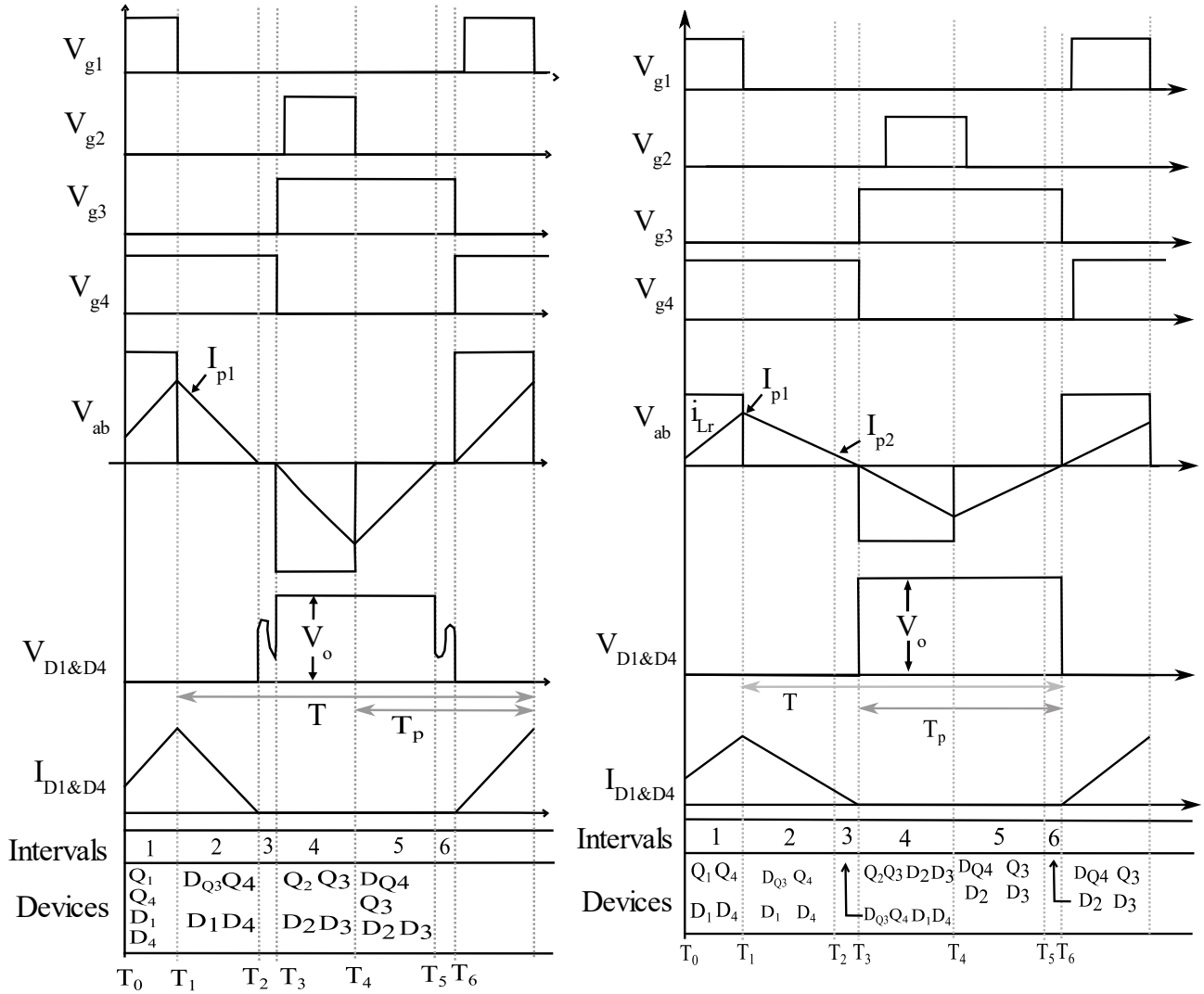

Fig. 3a). Typical operating waveforms to illustrate the operation of the ZVS full-bridge converter in a DCM mode. (left)

Fig. 3b). Typical operating waveforms to illustrate the operation of the ZVS full-bridge converter in a BCM mode. (right)

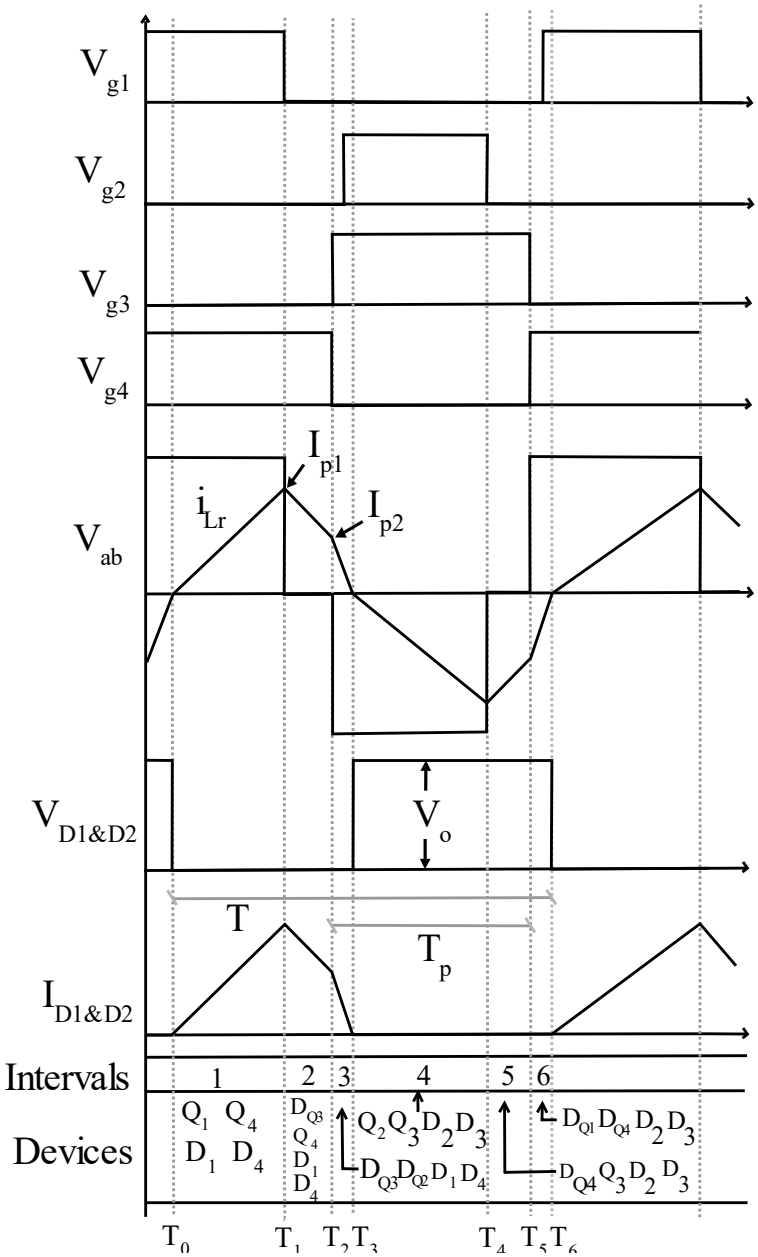

Fig. 3c). Typical operating waveforms to illustrate the operation of the ZVS full-bridge converter in a CCM mode.

B. Interval 2 (T1-T2)

1. *Case (a): DCM operation:* Referring to Fig.3(a). As assessed by the PWM duty cycle, interval two initiate immediately after the Q_1 switches OFF. Current in the primary side seeks an alternative direction and flows through the parasitic switch capacitances of Q_3, and capacitance Q_1 discharges to 0V, and body diode of Q_3 starts conducting. The primary resonant inductor L_R maintains the current circulating through the body diode of Q_3, resonant inductor L_R, primary transformer, and Q_4 route. The rate of the current downslope through L_R is proportional to the output voltage V_0. The power stored in L_R flows to the output

at T_2, and the current becomes null, and the rectifier diodes D_1 and D_4 turns OFF. Using initial condition $i_{L_R}(0) = I_{P1}$, the resonant inductor current $i_{L_R}(t)$ is given by [8]

$$i_{L_R}(t) = I_{P1} - \frac{V_o}{nL_R}(t - T_1) \quad (2)$$

2. *Case (b): BCM and CCM operation:* The only difference in BCM or CCM compared to DCM during interval two is that current at T_2 does not reach zero through the resonant inductor L_R rectifier diodes D_1 and D_4 are still conducting. At the end of this interval, $i_{L_R}(t) = I_{P2}$ [8].

C. Interval 3 (T_2–T_3)

1. *Case (a): DCM operation:* Referring to the DCM waveform, interval T_2–T_3 is very small, and no power transmission will occur to the secondary side of the converter. In this interval, the parasitic capacitance of the rectifier diodes resonates with the L_R. This resonance appears across rectifier diodes D_1 and D_4, as illustrated in Fig.3(a) DCM waveform. The inductor current i_{L_R} remains zero during this interval [8].
2. *Case (b): BCM operation:* The resonant inductor current continues to flow along the direction of body diode Q_3, resonant inductor L_R, main transformer, and Q_4 during this interval, as shown in Fig. 3(b). The downslope rate of the current through L_R is proportional to the V_o output voltage. The total energy stored in L_R flows to the output at T_3 and the current becomes null, and the D_1 and D_4 rectifier diodes switch OFF. Using initial condition $i_{L_R}(0) = I_{P2}$, the resonant inductor current$i_{L_R}(t)$ is given by [8]

$$i_{L_R}(t) = I_{P2} - \frac{V_o}{nL_R}(t - T_2) \quad (3)$$

3. *Case (c): CCM operation:* From Fig.3(c), CCM waveform, Q_3, and Q_4 switches toggled at T_2. This toggle timing is dependent on the resonant delay that occurs before switching ON Q_2. The primary resonant inductor current flowing through Q_4 sought an alternative path by charging/discharging the parasitic capacitance of switches Q_4 and Q_2 until the body diode of Q_2 is forward bias. Switch Q_2 can achieve ZVS if the resonant delay is correctly tuned. The energy stored in L_R is

transfer to the output, the current becomes null, and the rectifier diodes D_1 and D_4 turn OFF. The resonant inductor current $i_{L_R}(t)$ using initial condition $i_{L_R}(0) = I_{P2}$ is given by [8]

$$i_{L_R}(t) = I_{P2} - \frac{(V_{\text{in}} + \frac{V_0}{n})}{L_R}(t - T_2) \tag{4}$$

D. Interval 4 (T_3–T_4) through interval 6 (T_5–T_6)

Interval 4 to 6 are the negative equivalents of intervals 1 to 3.

From the above-operating intervals, we can conclude that when the converter operates in CCM mode, it requires a sizeable resonant inductor leading to an increase in the transformer's turn ratio, thus increasing the stress across MOSFETs. Also, the converter's secondary side has significant reverse recovery losses and voltage ringing due to high $\frac{di}{dt}$ while operating in this mode. Thus, the converter is designed to work in DCM and BCM. The proposed topology achieves soft switching for the full-bridge primary switches in these operating modes, naturally clamping the voltage across the output rectifier to the output voltage and having low reverse recovery losses due to low $\frac{di}{dt}$ [8]. Moreover, in [9], a unique switching technique was introduced to improve the efficiency of PSFB operated under light load conditions without using any auxiliary components. And the dead time required to obtain the ZVS technique with PSFB was given in [10].

2.1.2. LLC Resonant Converter

Another Unidirectional Isolated DC-DC converter is the LLC Resonant converter**,** as shown in Fig.4. This topology consists of a series capacitor C_r and inductor L_r and magnetizing inductance L_m parallel with the transformer. Hence it is called LLC resonant. It has two resonant frequencies, which play an essential role in the converter operation. We can get the converter's DC characteristics curve by changing the frequency for different load points and running the simulation [11]. From these characteristics, we can define the two resonant frequencies, f_1 and f_2 and a Quality factor Q_s which describes the load conditions. From Fig.5.

If Q_s is low, the curves belong to lighter loads, and for higher Q_s values, the curves represent heavy loads. The frequency f_1, f_2, and Quality factor Q_s from Fig.5. are defined as follows.

Note: The term R_l in the Q_s is obtained from the equivalent resonant circuit, and the voltage across it is an output voltage from the transformer.

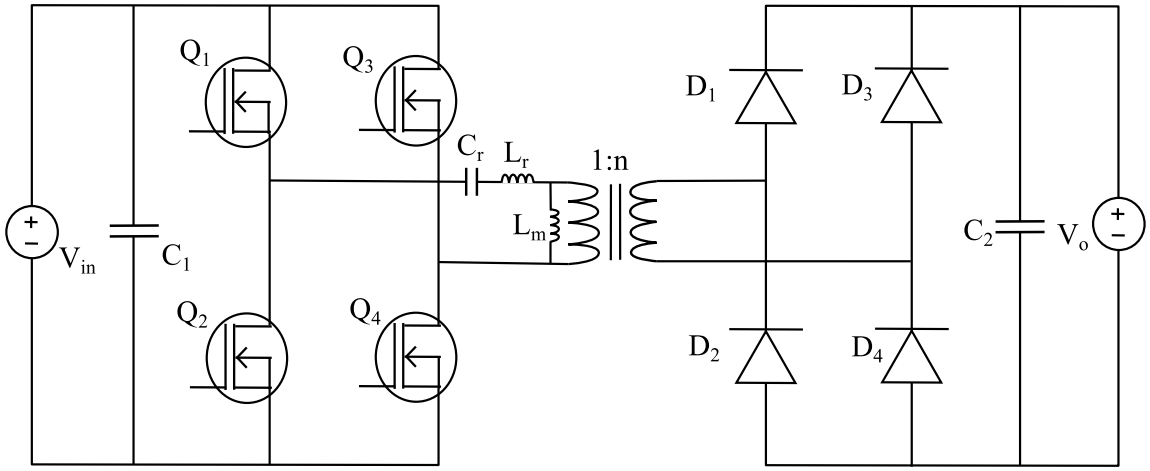

Fig. 4. LLC Resonant converter.

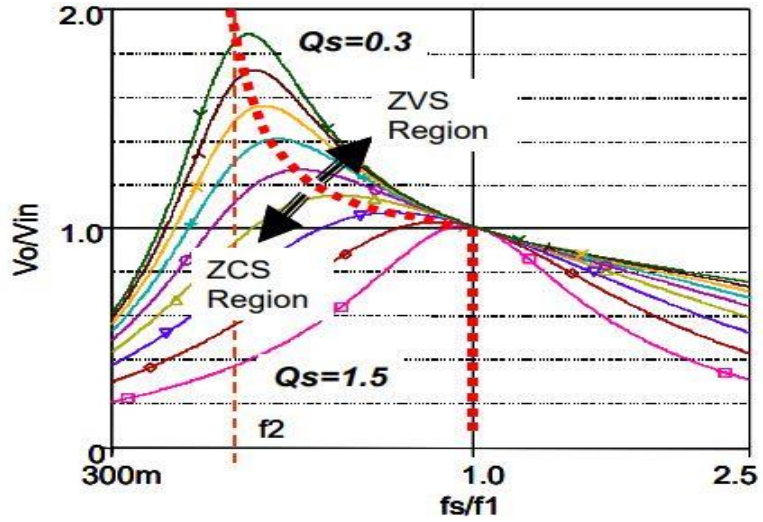

Fig.5. DC characteristics of LLC resonant converter [6]

$$f_1 = \frac{1}{2\pi\sqrt{L_r C_r}} \tag{5}$$

$$f_2 = \frac{1}{2\pi\sqrt{(L_r + L_m) C_r}} \tag{6}$$

$$Q_s = \frac{\sqrt{L_r/C_r}}{R_l} \tag{7}$$

From the converter's DC characteristics, we can observe that when the battery is fully charged (approaching light load), the peak of the gain reaches the resonant frequency f_2, where the magnetizing inductor L_m comes into consideration enables the characteristics of the parallel resonant converter (PRC). The opposite happens when the gain peak moves to the resonant frequency f_1 i.e., heavy loads and the circuit shows the characteristics of the series resonant converter (SRC). Analysis and design of a three-level LLC series resonant converter were given in [12]. In SRC, magnetizing inductance starts charging linearly with output voltage, not participating in the resonance. Another exciting thing is that when the switching frequency is equal to a resonant frequency f_1, all load curves meet at one point and have a unity gain [11].

The operation region is divided into two: the ZVS and the ZCS region. When the switching frequency is higher than f_1, the converter operates in the ZVS region. Similarly, when f_s is more elevated than f_2, the converter operates in the ZCS region. Lastly, when switching is between f_1 and f_2, the load condition determines if the converter is working in either ZVS or ZCS. Switching frequency range and MOSFET turn-off current chooses the size of L_m. If L_m is smaller, the f_s range can be lower, but the MOSFET turn-off current increases, increasing the switching losses [11]. As mentioned above, when the battery is charged, f_s will be greater than f_2, and L_m comes into action, leading to large circulating currents, increasing the conduction power losses. When switching frequency is far greater than the resonant frequency, the first resonant half-cycle doesn't complete by the time and interrupts the second switching half cycle, increasing the MOSFETs turn-off losses, and ZVS turn on failures and diodes in the secondary side will have hard commutation [13].

In LLC resonant converter using magnetizing current, ZVS can be achieved, which is not related to load current [11]. To have a wide range of voltage operations, we need to increase the size of L_m. But we already discussed that L_m is associated with the switching frequency. The switching frequency will be high for large L_m values, and the ZVS range gets narrowed and, core losses of magnetics and losses in the gate drive circuit will increase. Various control schemes, including PWM, Phase-shift, and other hybrid modulations, are proposed to narrow the switching frequency while broadening the output range.

Let us discuss the hybrid phase-shift control scheme for LLC resonant converter. Using the conventional Phase shift (CPS) modulation technique, it isn't easy to maintain ZVS under light load conditions [14]. Therefore, switching frequency is confined to a limited value, and soft

switching is compromised to keep the core losses and drive circuit losses under control. Another downside of CPS at light loads is that when either the upper switches or both the lower switches are conducting, the power semiconductors have a downward impedance path for the current to circulate. For light load conditions, there are many strategies suggested preserving soft switching. These techniques are categorized as:

1. Soft switching with active auxiliary circuits:
2. Soft switching with passive auxiliary circuits:
   Both active and passive auxiliary circuits can provide soft switching independent of load. Generally, they make the power converter complicated, reduce reliability, and contribute to all power losses [15].

So, to avoid these drawbacks, we use a controller named Hybrid Phase Shift. It has two sub-modulators; one is a low-power phase shift (LPPHS), and the other a high-power phase shift (HPPHS). Either of these modulators is active depending upon the power single status PS. If PS = 0, the LPPHS modulator generates the gate pulses of the full-bridge inverter and vice-versa. In general, the hybrid phase-shift modulator receives four input signals. They are switching frequency, f_s the phase-shift between the leading and lagging leg's gate pulses, ψ, the current is flowing out of the full-bridge inverter, i_p and a digital signal representing the power status, PS [15].

LPPHS modulator for light loads has two significant advantages: it provides soft switching, eliminating extra circuitry. The other is reducing the current oscillation by using the damping effect of antiparallel diodes. Similarly, the HPPHS modulator for heavy loads gives more or less the same results. It synchronizes with the transformer to optimize the soft-switching process. Hence the hybrid phase-shift modulator provides a better control strategy to achieve ZVS for light load conditions [15].

2.2. Bi-directional Isolated DC-DC converter

Instead of using diodes in the rectifier bridge to achieve the bidirectional power flow, we use MOSFETs. The most commonly used topology for this purpose is Dual Active Bridge (DAB) Fig.6. due to its high power density, low stress across the switches, high efficiency, buck-boost capabilities. The DAB converter was not widely adopted when introduced in 1991 because of the high-power losses and a relatively low switching frequency of the power semiconductor devices. Quite recent times, due to the capabilities of the modern SiC and GaN-based power

semiconductor devices and developments in nanocrystalline and amorphous soft magnetic materials, the DAB converter has begun to attract interest, allowing converter efficiency and power density improvements [2]. Silicon carbide (SiC) is a semiconductor with a wide bandgap with numerous advantages over Si technology. Because of SiC's high breakdown electric field, the voltage blocking layers can be tailored to have an enormous advantage in on-state resistance over Si. When compared to a Si device with the same current rating, the active area of a SiC

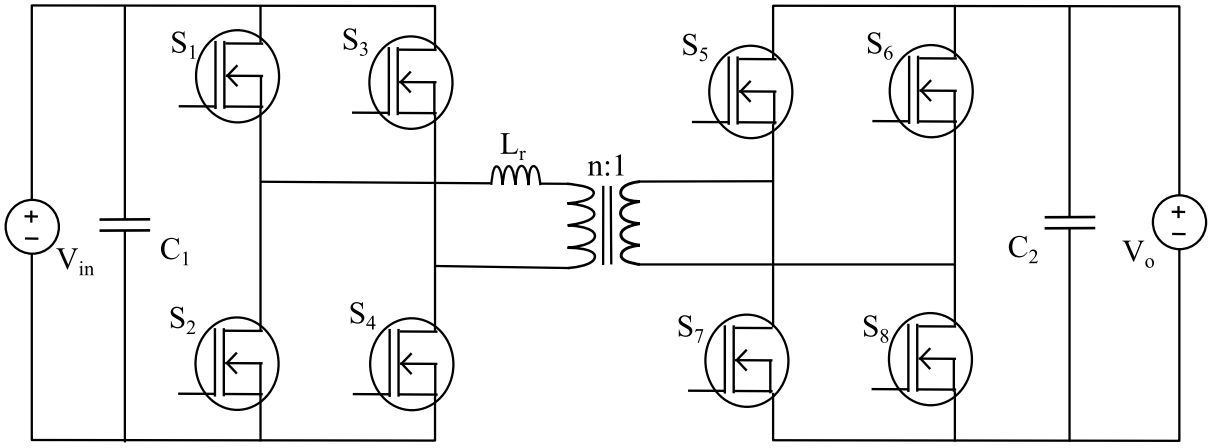

Fig.6. Dual Active Bridge

device can be lowered, lowering the device capacitance and allowing for higher switching frequencies. The comprehensive bandgap features enable greater junction temperatures, and the solid thermal conductivity and low coefficient of thermal expansion make SiC power device packaging more dependable over a wide temperature range [16]. Thus, compared with Si devices, SiC MOSFETs are used in DAB.

Moreover, the phase-shift full-bridge and LLC Resonant converters are used in onboard and offboard chargers. From a commercial point of view, ABB developed an offboard charger named Terra 53/54 series with LLC resonant converter in modular connection along with AC/DC converter. This modular system is developed by repeatedly replicating the same circuit. The number of active stages varies according to the output requirements. A full-bridge LLC resonant converter, especially in Terra 54, reaches around 400 to 800 volts with a 95% peak efficiency [17].

Tesla has also succeeded with modularity in offboard chargers with phase-shift full-bridge designed for model S and Model X with two supercharging network versions, facilitating single and three-phase ac inputs with their corresponding charging rates. A combination of 13 units

in a single cabinet can charge one vehicle with up to 150 kW of power and a documented efficiency of 92% [17].

The Dual-Active Bridge is dedicated to only onboard chargers with 1.9 to 2.2KW power ratings for vehicle-to-device application purposes. In recent times CHAdeMO developed a offboard charger for vehicle-to-device applications with a 400KW rating. It was not sure that they were using a Dual-Active bridge for this application. Much research is going on with DAB in modular, interleaved, and Multi-Active bridges with a single magnetic core to apply in bidirectional power flow [17].

2.3. Dual Active Bridge

Working Principle: Consider the power flow between the two voltage buses in a power system. And these two voltage buses are connected by a line reactance, as shown in figure 7.

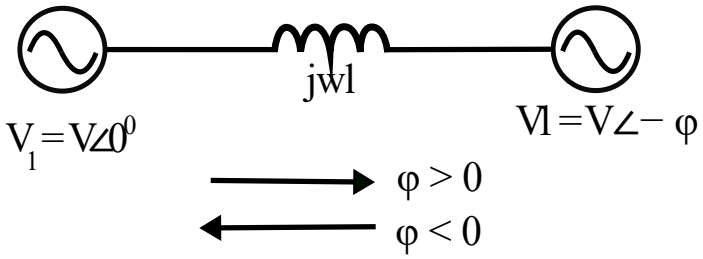

Fig.7. Power transfer between voltage bus.

From fig.7, the voltage source from the left leads with respect to the voltage source in the right. Hence, the power transfer takes place from left to right as per the equation given below.

Similarly, power transfer occurs in a dual-active bridge, where the switching action of MOSFETs generates two high-frequency phase-shifted square waves in the primary and

$$P = \frac{V_1 V_2 \mathrm{Sin}\varphi}{wL} \qquad (8)$$

secondary sides of the transformer. And the resultant phase shift changes the voltage across the transformer's leakage inductor to regulate the power flow direction and magnitude. Thus power is transferred from the leading bridge to the lagging bridge, and the direction of power flow can be easily changed by reversing the phase shift between the two bridges. As a result, bidirectional power transfer is simple in a dual-active bridge [18].

So, the power flow control depends on the transformer's leakage inductance, leading to an increase in circulating power and the current stress when the voltage ratio $\frac{V_{in}}{nv_o}$ diverges far from one, where n is the transformer's winding ratio. Various control schemes are there to improve the output of DAB, in that the most popular are Single-phase-shift, Extended-phase-shift, Dual-phase-shift, and Triple-phase-shift [19]. Our primary focus is on Single Phase shift (SPS) and Dual-Phase shift (DPS) control schemes. We try to understand the SPS and DPS theoretically and practically by implementing those schemes in the simulation software PLECS and followed by experimental results.

Chapter 2 gives general information about the three topologies and their pros and cons, shown in table 3. And we are moving forward with a Dual-Active bridge converter because of its bidirectional power flow.

Table 3. Comparison of all the three topologies [2].

Converter	**Switches/Diodes**	**Power Flow**	**Pros and Cons**
Phase shift Full Bridge	4/4	Unidirectional	Simple control; Wide output range High switching losses on the primary side and secondary side. Hard to realize ZVS under light load.
LLC Resonant converter	4/4	Unidirectional	Low reactive current, ZVS on the primary side and ZCS on the secondary side. Hard to maintain high efficiency and ZVS under a wide operating range.
Dual-Phase shift	8/0	Bidirectional	Wide output range, High efficiency compared to PSFB and LLC converter. Trade-off between reactive power and ZVS range.

3. DAB Control

3.1. Single Phase shift control

A single-phase shift is applied between the two bridges of the DAB converter, causing the power transfer from source to load or load to source.

3.1.1. Switching Sequence

Primary and secondary bridges are controlled simultaneously in a single-phase, dual-active bridge. All switches are set to a 50% duty ratio. The diagonal switches turn on and off together, resulting in a square wave at the output of each bridge. The switching sequence is divided into four intervals based on the inductor current waveform and the phase shift between the transformer's primary and secondary voltages. Fig. 10 depicts the voltage and current waveforms. The inductor current waveform is positive and negative during interval one, so the current commutation follows the scheme shown in Fig. 8 and 9 [18].

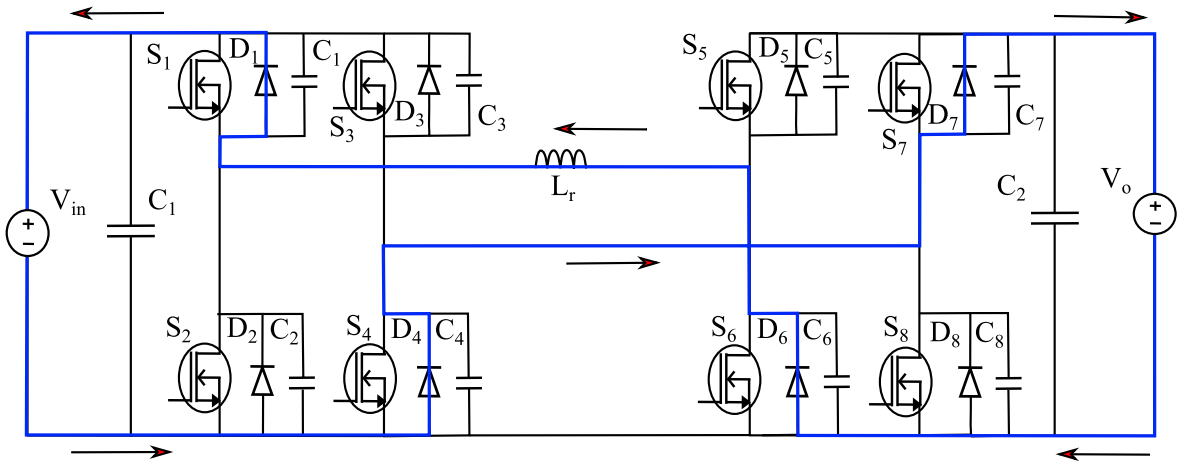

Fig.8. Negative Inductor Current.

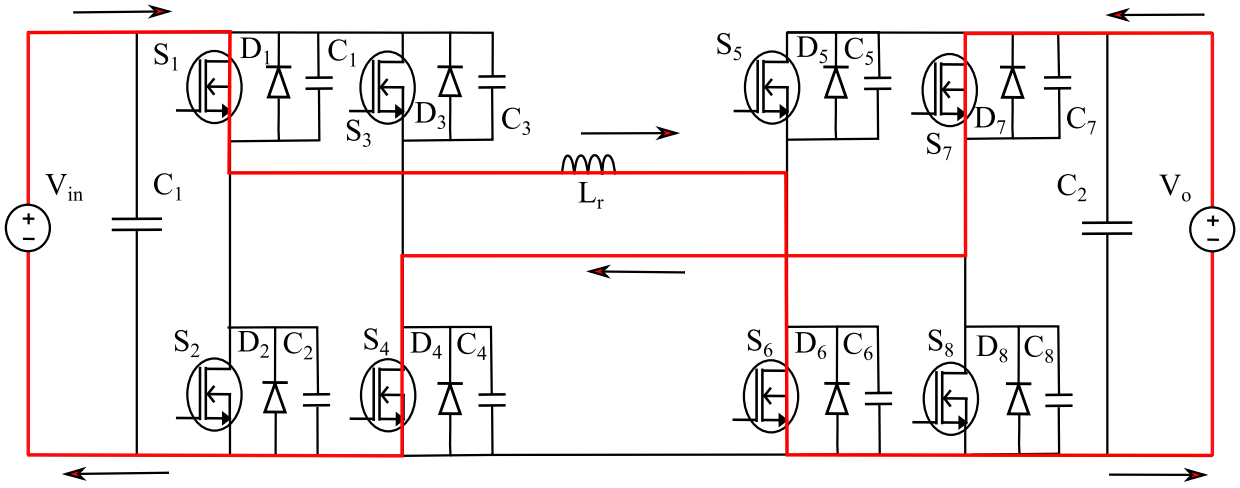

Fig.9. Positive Inductor Current

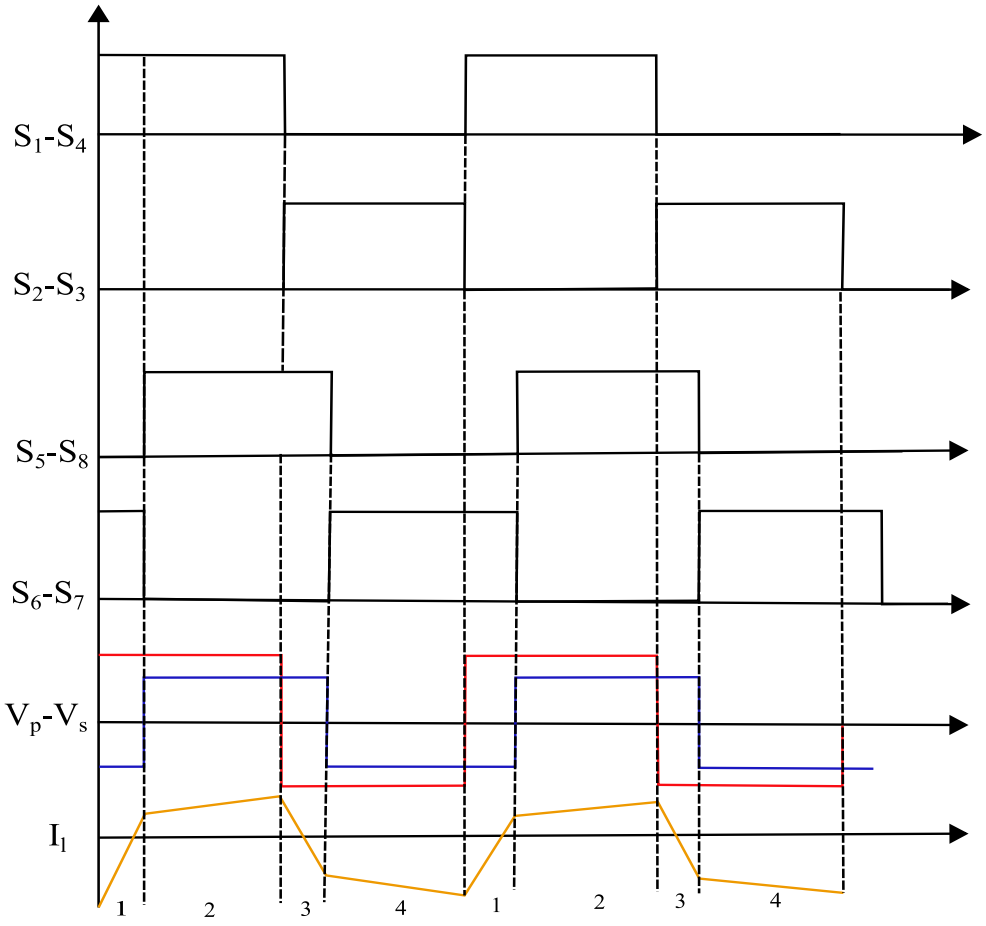

Fig.10. Switching Sequence.

The voltage across the primary, V_p is equal to V_1 during this interval, and the voltage across the secondary, V_s is similar to V_2. The difference between these voltages appears across the leakage inductor, and Equation 9 can approximate the current slope during this interval [18].

$$\frac{di}{dt} = \frac{V_1 + V_2}{L} \tag{9}$$

The inductor current is positive during interval two. The voltage across the primary winding of the transformer is positive and equal to V_1, and the voltage across the secondary winding is positive and similar to V_2. As a result, the difference between these two voltages appears across the leakage inductor, and Equation 10 can be used to calculate the slope of the rising current during this interval [18].

$$\frac{di}{dt} = \frac{V_1 - V_2}{L} \tag{10}$$

Switches S_1 and S_4 remain switched on; however, since the voltage across the secondary has increased to V_2 and the inductor current is now positive, switches S_5 and S_8 turn on to conduct current. There is a brief period of inactivity between the turns of S_6 and S_7 and S_5 and S_8. The phenomenon of zero voltage switching (ZVS) occurs during this dead time. The commutation sequence for the second interval is shown in Fig 11 [18].

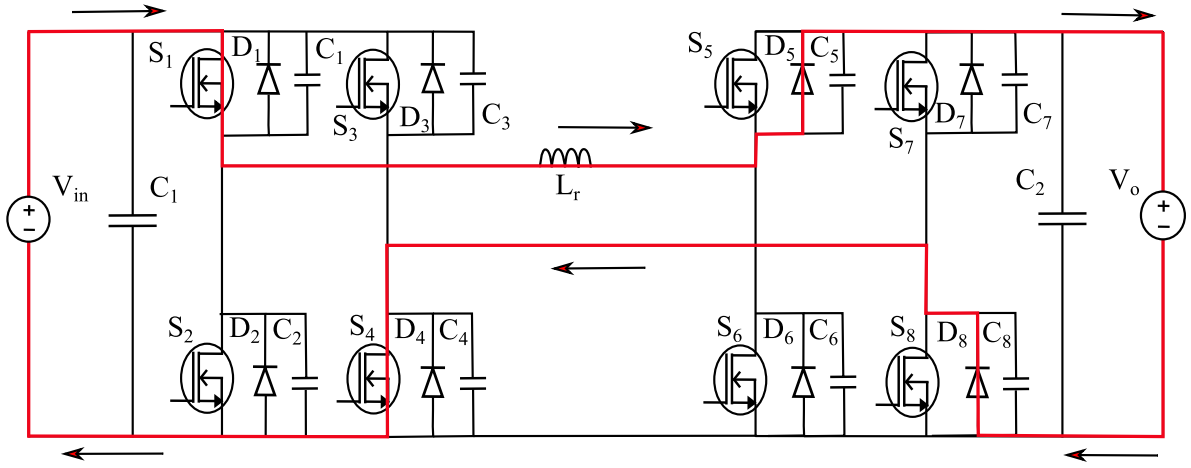

Fig.11. Interval 2.

As shown in Fig 10, the inductor current begins to ramp down from its positive peak to a negative value during interval three. The voltage across the primary in this interval is $-V_1$, and the voltage across the secondary is V_2. The difference between these voltages ($-V_1$-V_2) is visible across the inductor. As a result, as shown in Equation 11, the current ramps down with a negative slope [18].

$$\frac{di}{dt} = -\frac{V_1 + V_2}{L} \tag{11}$$

Switches S_5 and S_8 remain turned on during this interval, but the voltage across the primary has now dropped to $-V_1$, switches S_2 and S_3 turn on to conduct current. Fig. 12 and 13 depict the conduction for both directions of the inductor current IL < 0 and IL > 0 [18].

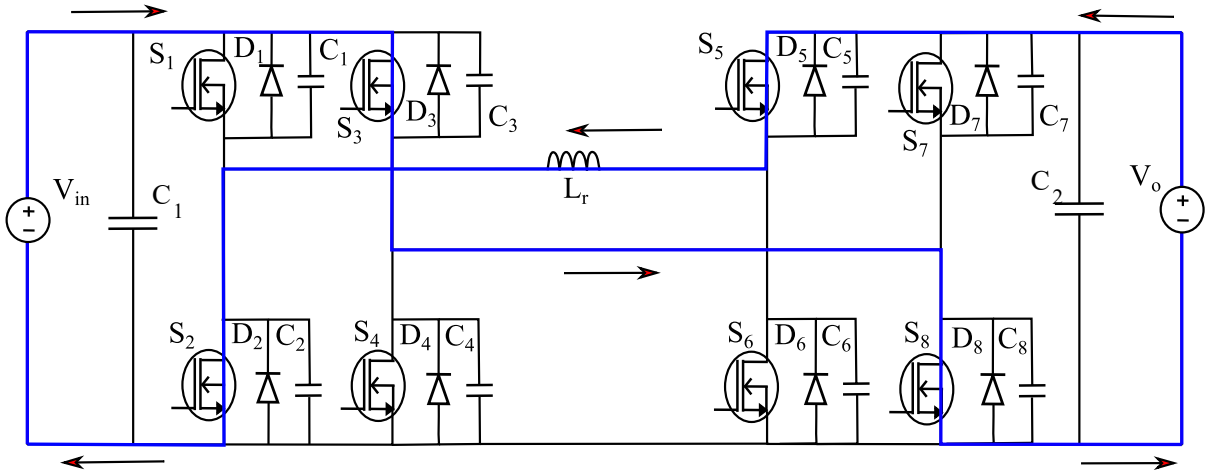

Fig.12. Negative Inductor Current.

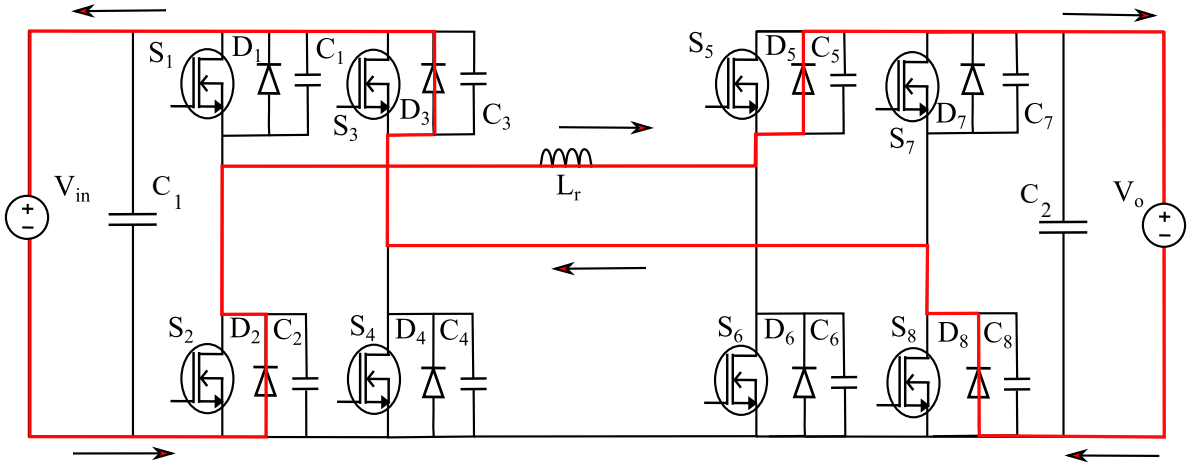

Fig.13. Positive Inductor Current.

The inductor current remains negative during interval four. The voltage across the primary is $-V_1$ during this interval, and the voltage across the secondary is $-V_2$. The difference between these voltages ($-V_1+V_2$) is visible across the inductor. As a result, as shown in Equation 12, the current ramps down with a negative slope [18].

$$\frac{di}{dt} = -\frac{V_1 - V_2}{L} \tag{12}$$

During this time, switches S_2 and S_3 remain turned on, but because the voltage across the secondary has dropped to $-V_2$, switches S_6 and S_7 turn on to conduct current, as shown in Fig.14 [18].

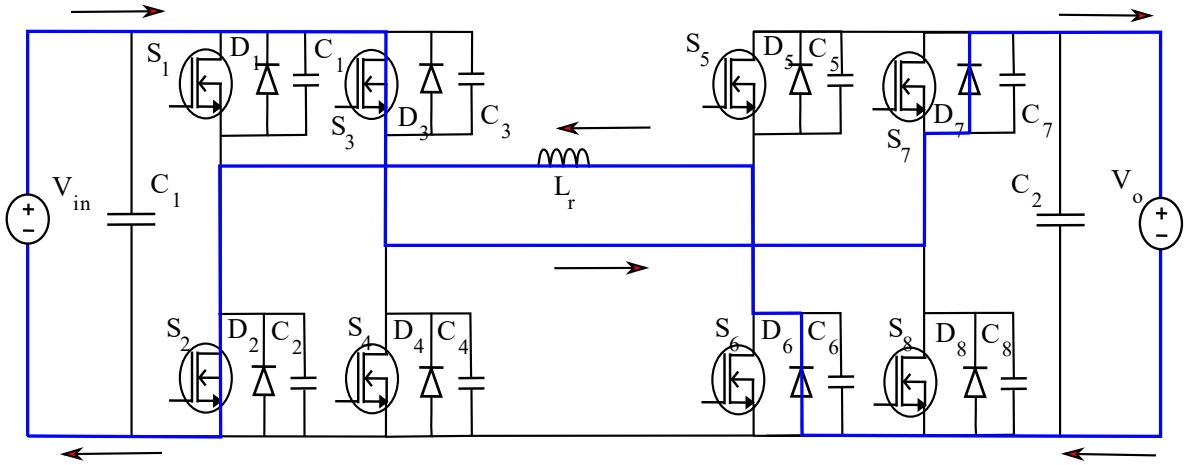

Fig.14. Interval 4

The above discussion is about the switching sequence of single-phase shift control, divided into four intervals, as shown in Fig.10. Whenever the inductor current is positive and voltages (V_1 and V_2) are negative or vice versa, we have huge circulating currents inside the converter. These circulating currents reduce the overall system efficiency, thus not suitable in practical applications. However, to minimize these circulating currents and increase the efficiency, we choose a Dual-Phase shift controller. In addition, ZVS is lost when the voltage varies widely, increasing the switching losses [20]. So, Dual-Phase shift control can be implemented to overcome these problems.

3.1.2. Dual Active Bridge - Zero Voltage Switching:

There is a short dead time between intervals one and two not shown in fig.10, where the inductor-stored energy discharges the output capacitances of the MOSFETs and holds them close to zero voltage before they are turned on. When the voltage across the MOSFET is close to zero, the turning on phenomenon is zero voltage switching (ZVS). Achieving ZVS is a significant advantage of this topology, in which the inductive stored energy causes ZVS of all lagging bridge switches and some leading bridge switches due to the natural lagging current in one of the bridges. And it depends on the stored inductive energy available to charge and discharge the output capacitances of MOSFETs [18]. In SPS, the ZVS depends on the voltage ratio and the phase shift angle. Likely in SPS, ZVS is not always achieved in DPS, as it depends on the current direction. The analysis of ZVS conditions are given in [21], [22].

For example, when the transition from interval one to two occurs, the primary side switches S_1 and S_4 continue to conduct. In contrast, the secondary side switches S_6 and S_7 turn off, and S_5 and S_8 turn on. When S_6 and S_7 are performing, their voltage is initially zero, and S_5 and S_8 block the entire secondary voltage. All the secondary switches are turned off during the dead time. The inductor-stored energy circulates current, discharges the capacitor across MOSFETs S_5 and S_8 to zero, and charges the capacitor across MOSFETs S_6 and S_7 to the entire secondary voltage. Since current must continue to flow after the capacitors have been charged and discharged, it will flow through diodes D_5 and D_8, as shown in fig.15, clamping the voltage across MOSFETs S_5 and S_8 to zero. Hence S_5 and S_8 will turn on at zero voltage during the next interval, eliminating turn-on losses completely. Similarly, the ZVS procedure will be identical in the primary bridge [18].

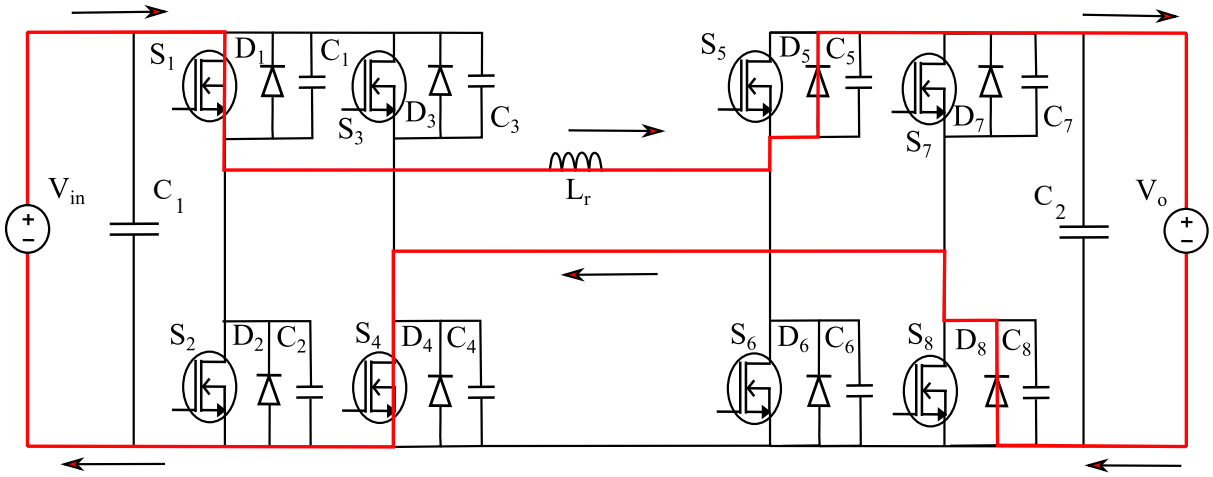

Fig. 15. Zero Voltage Switching in S_5 and S_8 Switches.

3.2. Dual-Phase shift control

Here in DPS control, we have two degrees of freedom. This means introducing another phase shift between the leg pairs of each bridge; we call it inner phase-shift control. The cross-connected switch pairs in full bridges are switched with an inner phase-shift ratio, and the inner phase-shift ratios are equal in both bridges. The output alternating current voltages of both bridges are then three-level waves. Compared to SPS control, DPS control can reduce current stress and steady-state current, improve efficiency, expand the ZVS operation range, and minimize output capacitance. Under certain operating conditions, dead band compensation can also be easily implemented in the DPS control without using a current sensor [23]. In this thesis, our concern is not about the dead band. This paper shows how the inductor current changes with SPS and DPS and verifies that circulating currents are reduced. And also, we will analyze the steady-state error of the output voltage of the DAB by reducing the size of output capacitance.

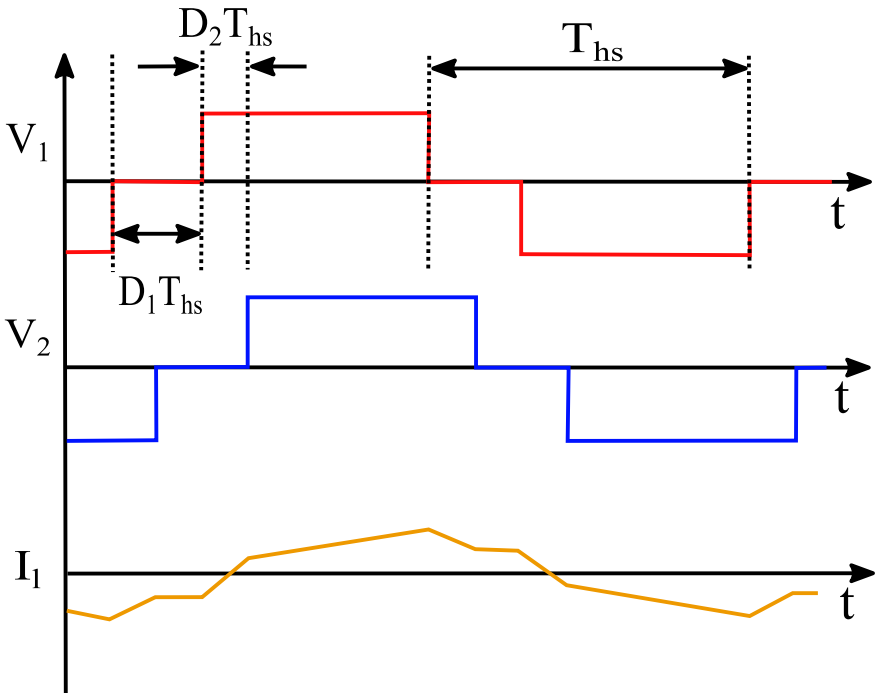

Fig.16. Voltage and Inductor current waveforms of DPS control.

Voltage waveforms and inductor current behavior of a DPS control are shown in Fig.16. 'T_{hs}' is half of the sampling period, I_l is the inductor current, V_1 and V_2 are the voltages across the inductor, D_1 is the inner phase shift, and D_2 is the outer phase shift. $D_1 + D_2 \leq 1$, if the sum is not less than 1, the power flow control is not possible with the D_2. To maintain the constant

power flow, infinite combinations of D_1 and D_2 can be used. Within the D_1 and D_2 ratio between 0-1, the power flows from primary to secondary, and to change the direction of power flow, D_2 should be less than zero [24]. The slopes of Inductor current change accordingly in charging and discharging modes can be seen in [25].

3.3. PLECS Simulation Tool

PLECS is a toolbox for piece-wise linear simulation of electrical circuits within the Simulink environment. It is mainly used for power electronic systems but can also be used for any electrical network. PLECS includes the ability to model controls and various physical domains like thermal, magnetic, and mechanical in addition to the electrical system. Comparing to other simulation tools like Saber, Simulink/Power system Blockset, Simulink/PLECS uses less CPU time. PLECS has been proven a valuable tool compared to others regarding speed, accuracy, and stability [26]. Having the PLECS standalone/ blockset license and RT box tool (Real-Time box), we can quickly generate the code for real-time simulations. The procedure for deploying code from PLECS to RT box can be seen in the coming chapters. Hence, to design and model the Dual-Active bridge and its controller and simulate it offline and in real-time, we choose PLECS standalone version 4.5.6.

3.4. DAB Simulation with Single-Phase Shift control

Fig.17 gives the overall schematic of the Dual-Active bridge and the single-phase shift modulator implemented by a closed-loop voltage control digital PI regulator with a Forward-Euler approximation.

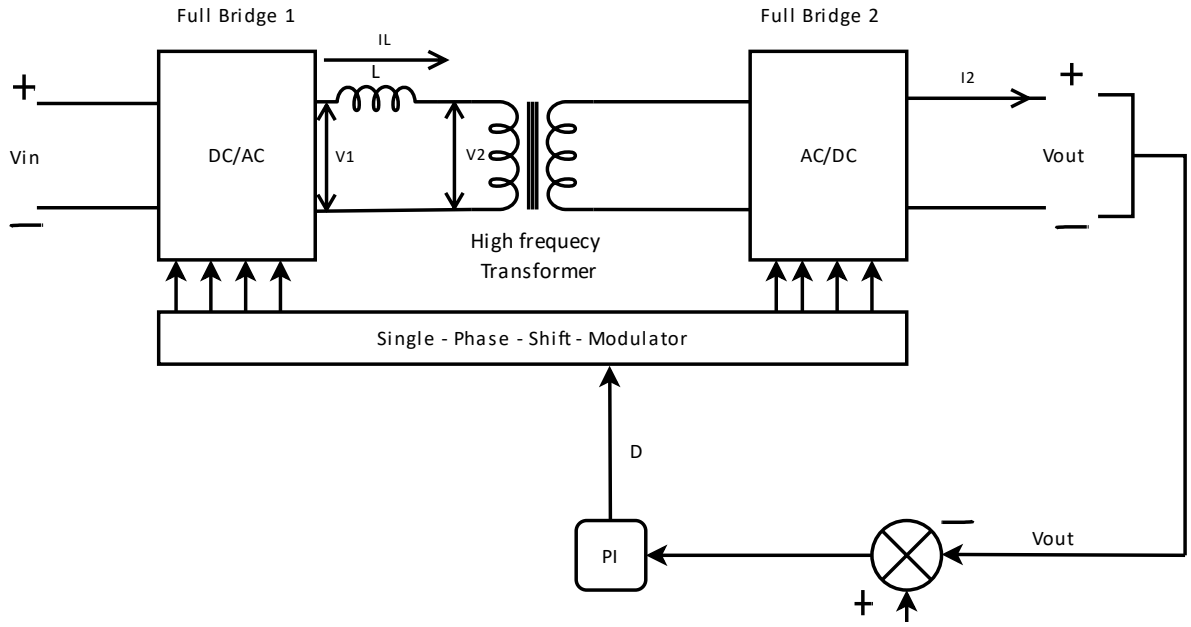

Fig.17. Block diagram of SPS control.

The detailed PLECS schematic, its controller, and parameters considered are shown below.

3.4.1. DAB Converter Model

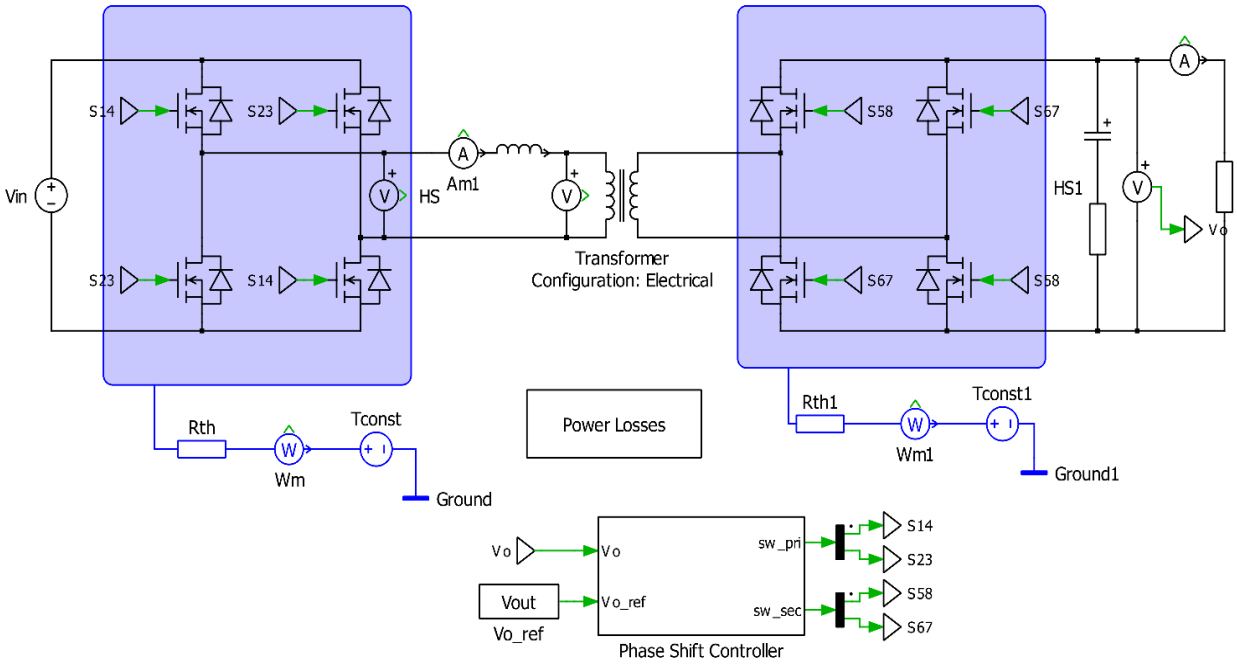

Fig.18. DAB with SPS control.

This demonstration shows a dual active bridge converter with identical primary and secondary side full-bridges using Silicon Carbide (Sic) MOSFETs, a high-frequency transformer, power transfer inductor, and DC-link capacitors. In this thesis, the transformer that we consider is an ideal model with a 1:1 turns ratio. So, in the offline simulation, we analyze the circulating currents in both the controls. In contrast, we examine the output voltage with a fixed switching frequency and different sampling frequencies in the real-time simulation to understand the maximum switching frequency achievable for the considered modeled parameters. Additionally, we include the thermal behavior of MOSFETs for both bridges in both single-phase shift and dual-phase shift controls, respectively, using the PLECS thermal domain to analyze the power losses [27]. Instead of using a battery, all the simulations are done on the 10KW resistive load. The size of the leakage inductor, high-frequency transformer, and all other simulation parameters are considered from the attached reference [18]. Whereas the regulator parameters Kp, Ki, are considered from the demo model developed by the PLECS since they give the stable operation for the evaluated parameters.

The following table is the system specification along with PI parameters used to simulate SPS control.

Table 4. System Specifications

Parameter	Value
Input Voltage[V]	800
Output Voltage[V]	500
Leakage Inductance[μH]	36
Output Capacitance[μF]	250
Capacitor ESR[Ω]	0.05
Switching frequency 'f_{sw}'[Khz]	100
Transformer turns ratio 'n'	1:1
Resistive Load[Ω]	26
Proportional gain 'Kp'	0.11173*0.015
Integral gain 'Ki'	0.11173
Sample Time 'Ts'	1/ f_{sw}

In order to identify the current, voltage across the switch, we need to provide the switch parameters. Here are the switch specifications on both the primary and secondary side full bridge.

Table 5. Primary bridge switch specification.

Primary side switch specifications	Value
MOSFET on resistance[mΩ]	30
Diode forward voltage[V]	4.5
Diode on resistance[mΩ]	5
External gate resistance[Ω]	2.5
Thermal resistance case-heatsink[K/W]	0.5

Table 6.Secondary bridge switch specifications

Secondary side switch specifications	Value
MOSFET on resistance[mΩ]	65
Diode forward voltage[V]	4.5
Diode on resistance[mΩ]	5
External gate resistance[Ω]	2.5
Thermal resistance case-heatsink[K/W]	0.5

3.4.2. Controller

Each switch is activated for half of its respective switching period. The switch pairs in the two bridges all have the same switching period [27]. Still, they are operated to introduce a phase shift between each bridge that varies depending on the modulation derived from feedback measurements. Based on a setpoint value, an output voltage error signal is generated and fed through a digital PI regulator to generate the phase shift ratio for the PWM modulator [27].

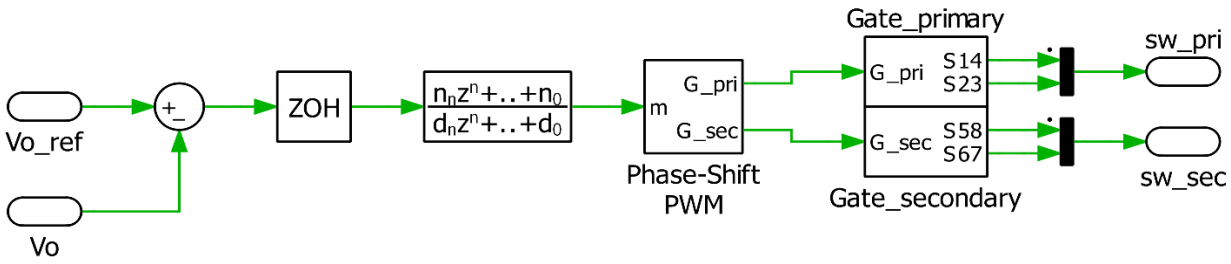

Fig.19. Phase-shift Controller.

PWM is generated using SR flip-flop by giving two signals from the carrier and the hit crossing to SET and RESET, thus creating two opposite pulses used for the switches on the same leg. The figure below shows the PWM used to drive the switch and the phase shift between the two bridges.

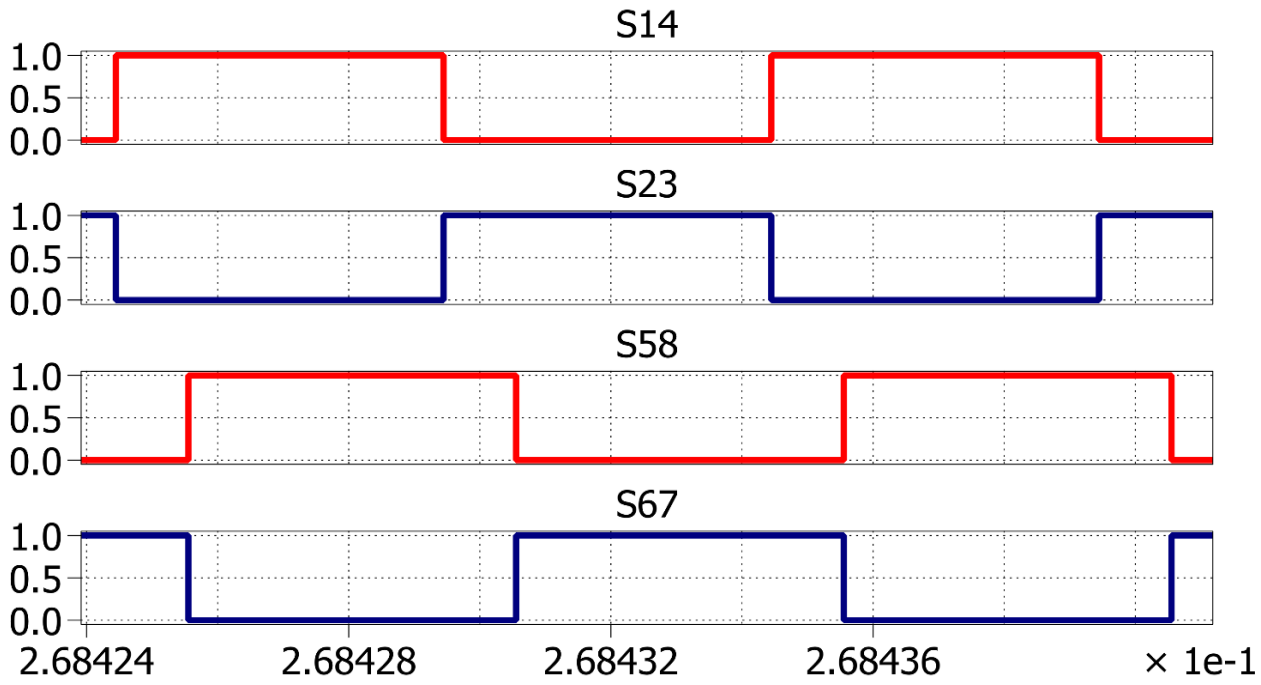

Fig.20. PWM and the Phase-shift betweeen two bridges.

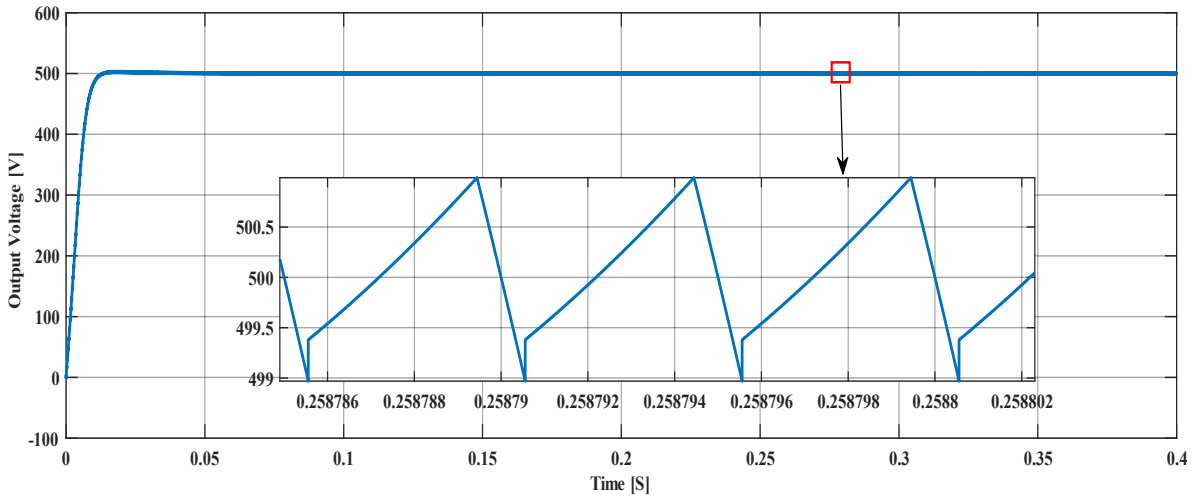

Fig. 21. Output voltage using SPS control.

The output voltage in volts across the load is as shown in fig 21. It reaches a steady-state within 0.015seconds, and the ripple from the picture-in-picture is in the acceptable range. The current flowing through the leakage inductance and the voltages across it are discussed, along with the results of DPS in a comparative way.

3.5. DAB Simulation with Dual-Phase shift control

Single-phase-shift (SPS) control is the most commonly used algorithm, but it can only operate efficiently when the voltage conversion ratio is equal to one. When the voltage amplitudes of the two sides of the transformer do not match (this is our case in SPS & DPS), the current stress increases significantly, necessitating the use of devices with higher voltampere ratings. Furthermore, to reduce the size and weight of the converter, the switching frequency must be increased. Under these conditions, increasing the current stress results in higher switching losses and a significant reduction in efficiency, especially if the voltage amplitudes of the two sides of the transformer do not match [28]. Since this is our case, we use the current stress algorithm from [28] to generate an inner phase shift ratio between the legs of each bridge. This algorithm improves the system's overall performance. The idea in designing the DPS is as shown in fig.22.

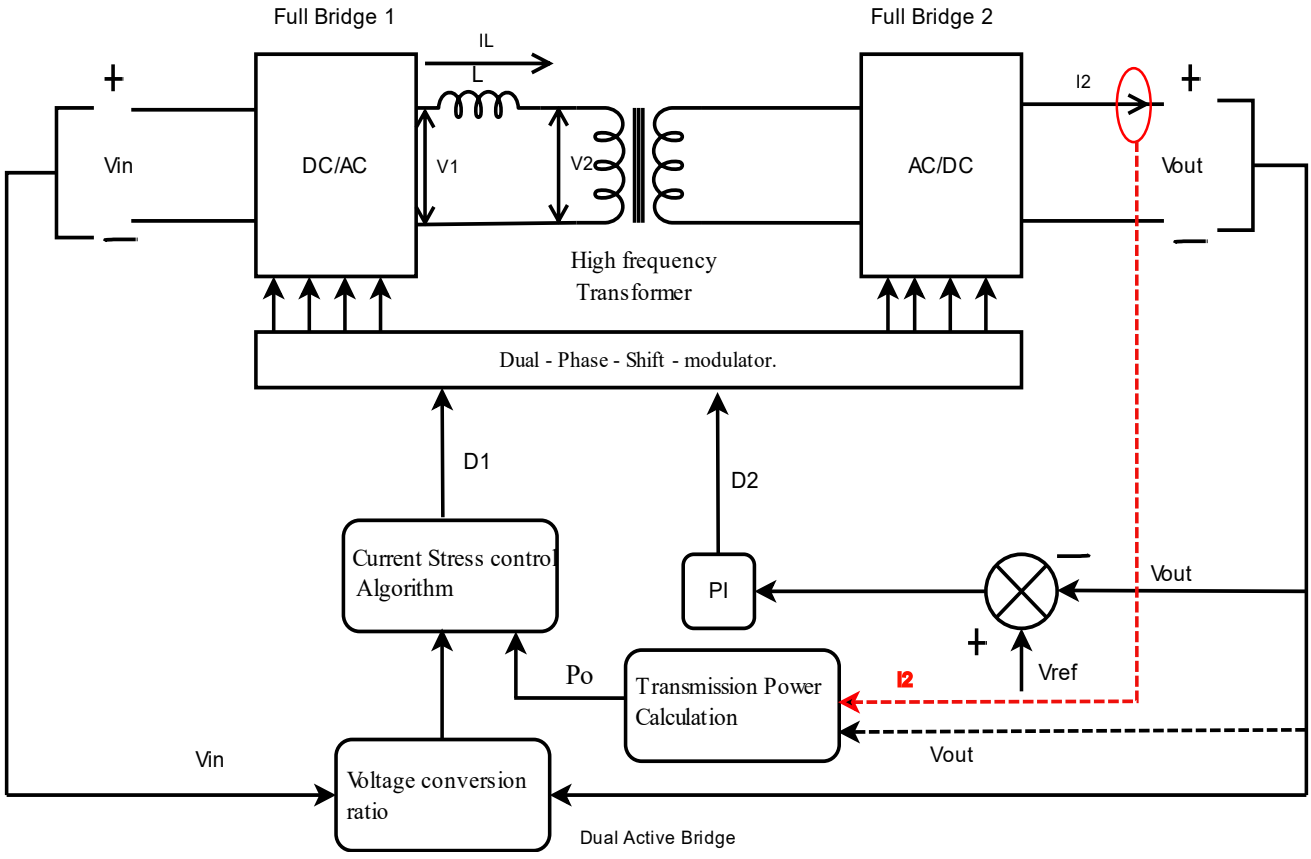

Fig. 22. Block diagram of DPS control.

3.5.1. DAB Converter Model

The converter design looks similar to the SPS control model except for the controller since another phase shift between each bridge's legs has been introduced. The following figure is the converter designed in the PLECS.

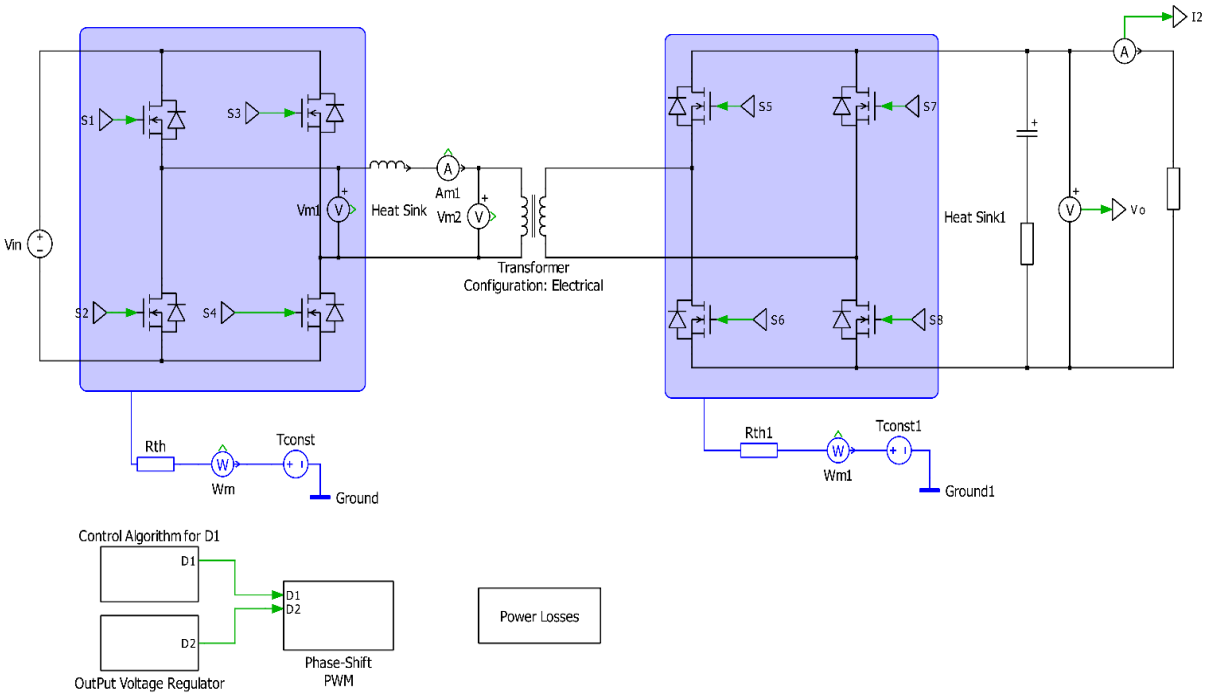

Fig. 23. DAB with DPS control.

The parameters considered to design the schematic is same as shown in Table 4, 5, and 6 except for the output capacitance and respective ESR. The output capacitor size is reduced to 50µF; ESR is reduced to 3.2mΩ so that the impact on output voltage ripples can be seen in fig 26.

3.5.2. Controller

The control algorithm mentioned above is implemented in the PLECS using a C-Script block from the library files. The code developed in the C-Script using C99 language is shown in Annexure 1. The output of the C-Script is the modulation used to generate the inner phase-shift ratio given to each bridge's legs. The inputs of the C-Script block are the transmission power, and the voltage conversion ratio referred to [28] are shown below, respectively, in equations 13 and 14.

$$P_o = \frac{8 f_{sw} L I_2}{n V_1} \tag{13}$$

$$K = \frac{V_1}{n V_2} \tag{14}$$

From equations 13 and 14, the I_2 is the output current, and V_2 is the output voltage in the converter taken as the feedback reference to generate P_o, and K. Whereas V_1, L, n, f_{sw} is the input voltage, inductor, transformer turns ratio, switching frequency, respectively. The digital PI regulator generates the modulation used for the outer phase-shift ratio between each bridge from the output voltage as feedback measurement. The following figure shows the phase-shift generator in the DPS.

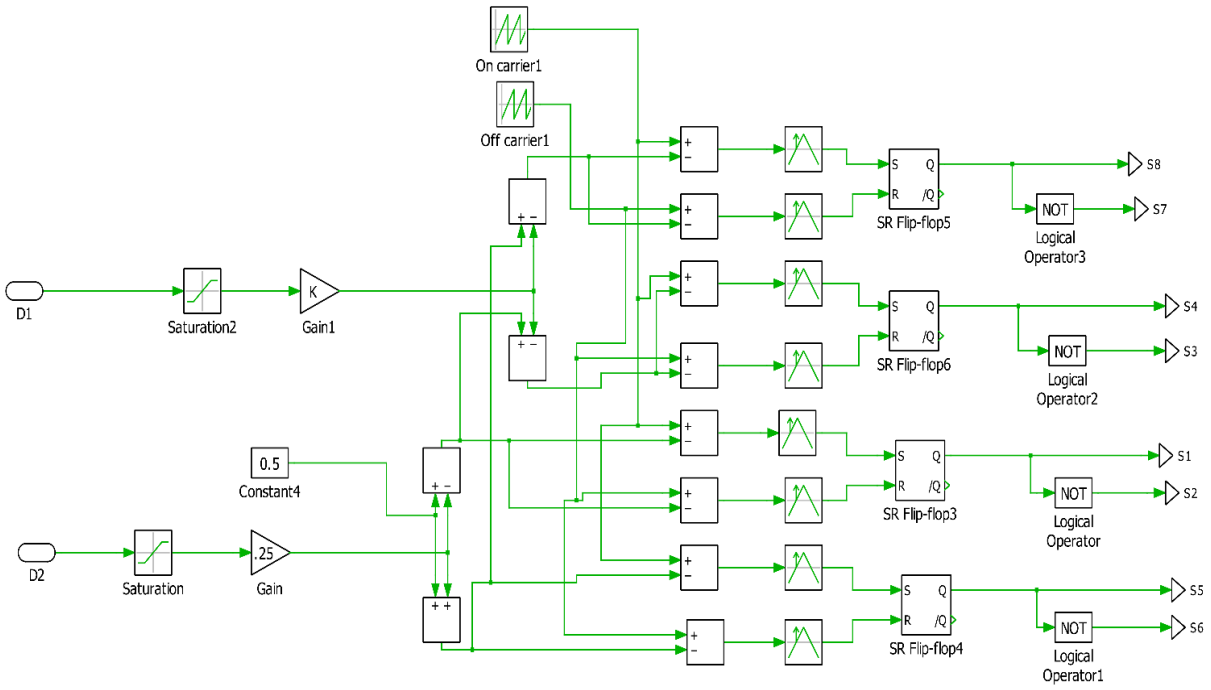

Fig. 24. PWM generator in DPS.

Unlike in SPS, we have two modulation signals here, so we use four SR-Flipflops to generate eight PWM signals with desire phase-shift, as shown in fig 25.

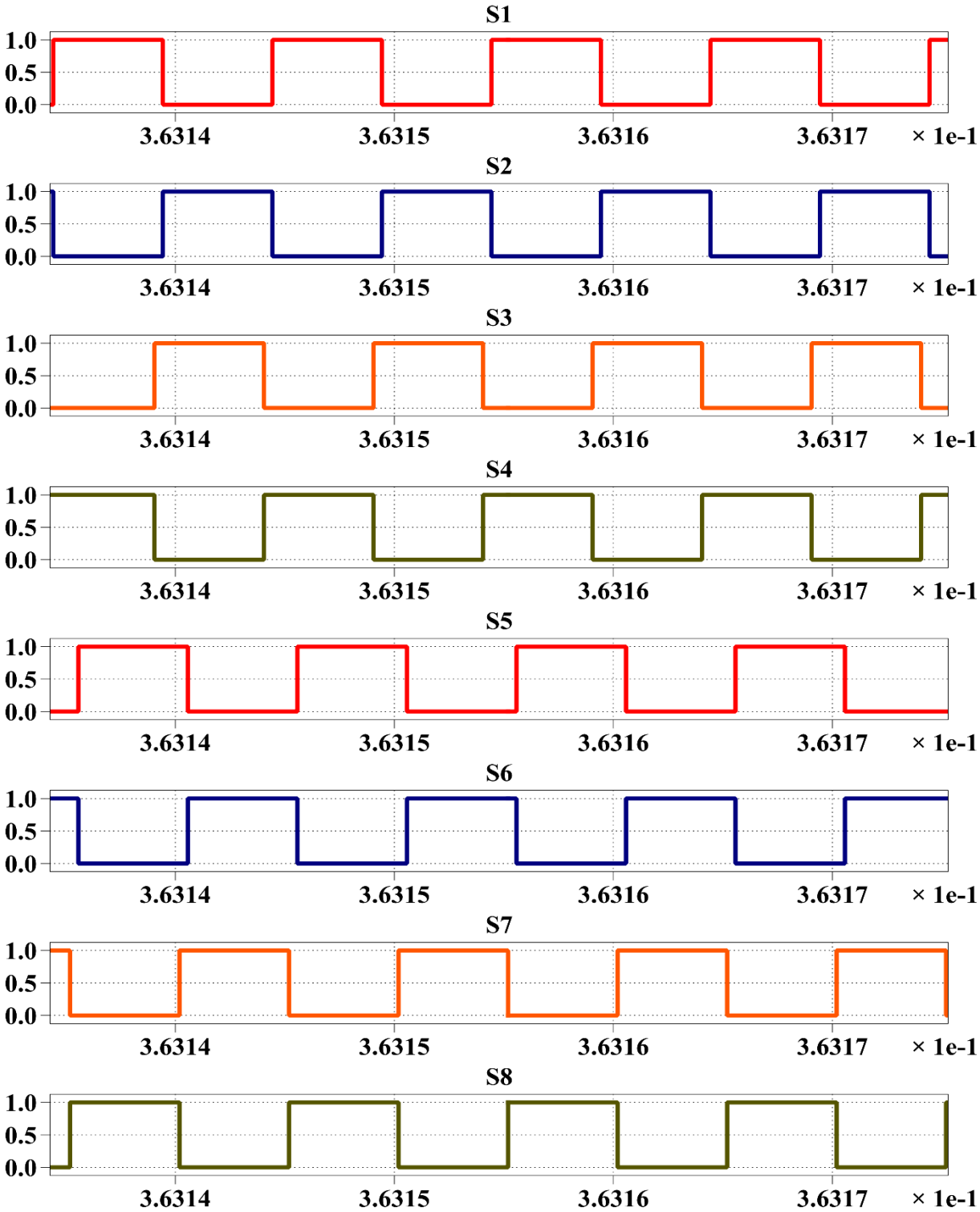

Fig. 25. PWM in DPS control.

We can observe from fig.25 an inner phase-shift between the switches S_1/S_2 and S_3/S_4 and between S_5/S_6 and S_7/S_8, respectively. Similarly, an outer phase-shift between the switches S_1/S_2 and S_5/S_6 and between S_3/S_4 and S_7/S_8, respectively.

Fig.26 shows us the output voltage of the dual-active bridge converter operated under dual-phase shift control. From fig.21 with fig.26, that the ripple error is almost identical in both the controllers even though the output capacitance is reduced to five times lower in DPS than SPS. Hence, this proves that using the DPS control allows us to minimize the output capacitance.

3.6. Simulation Results on Circulating Currents

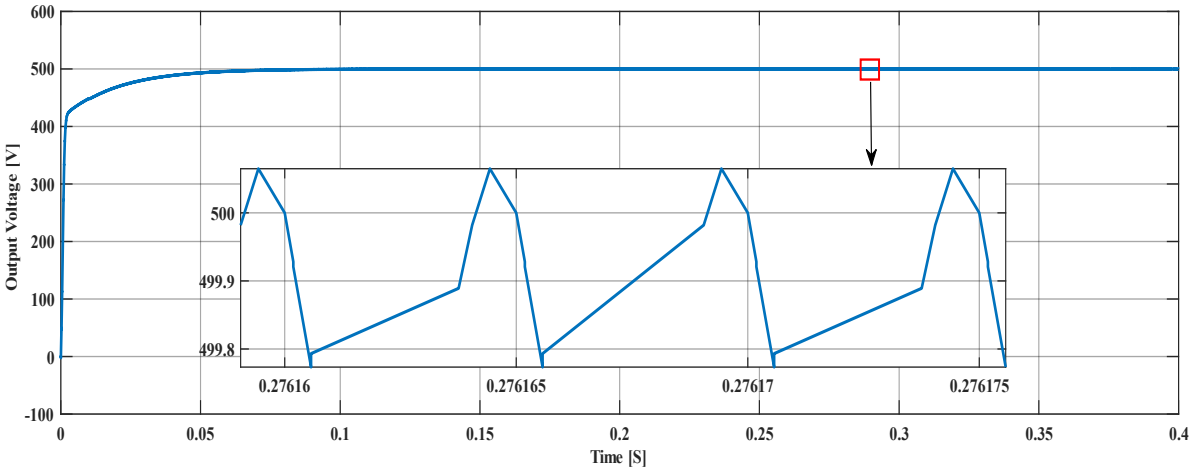

Fig.26. Output voltage using DPS control.

During Single-phase shift control, the voltages across the leakage inductance and the current flowing through it are shown in fig.27. As mentioned earlier, the input voltage is equal to the primary voltage of the inductor. Similarly, the output voltage is equal to the secondary voltage of the inductor. We can observe in fig.27 that V_1 = 800V and V_2 = 500V, and they appear as single-level voltages. When the voltage is positive and the current is negative in any interval during transmission, there generates the reactive power, also called circulating currents. From fig.27, the shaded region is the reactive power generated during the single-phase shift control. And the maximum inductor current is I_{lmax} = 36.09A.

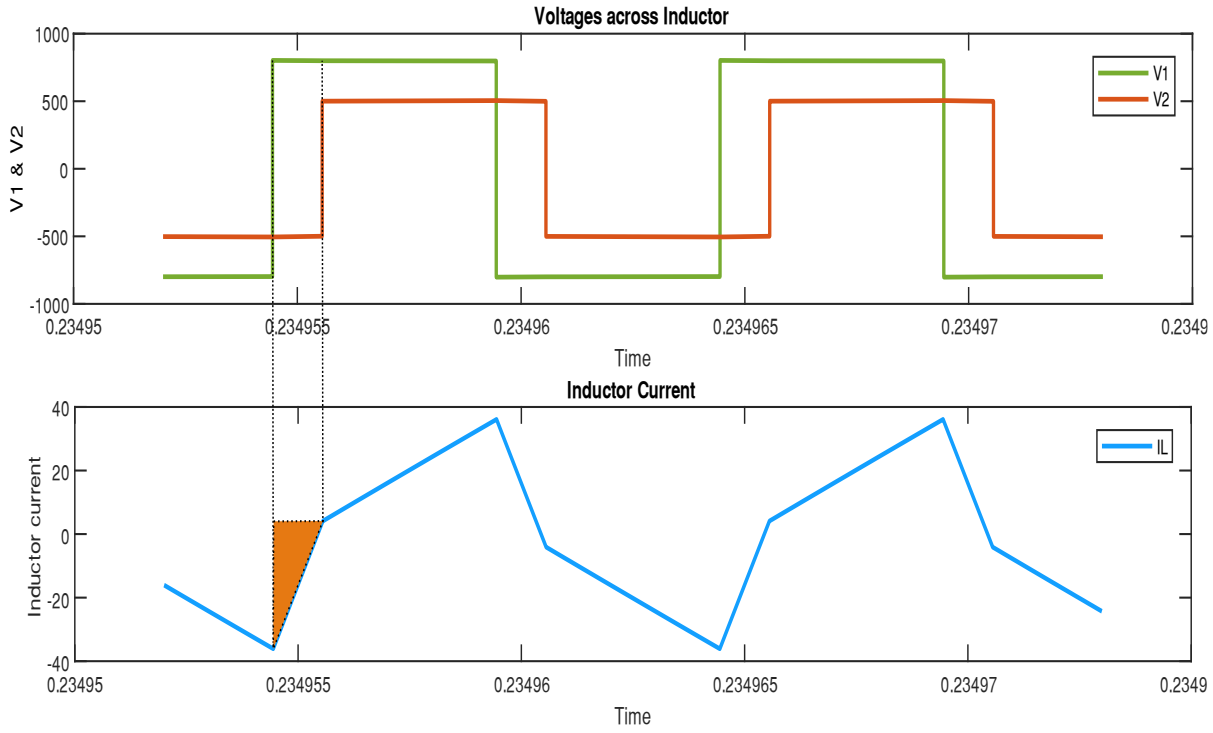

Fig. 27. Inductor Voltages and current in SPS control.

Similarly, in dual-phase shift control, the primary and secondary voltages are 800 and 500V, respectively. And the maximum inductor current is I_{lmax} = 34.9A. Due to the introduction of another phase shift between each bridge's legs, the voltages across the leakage inductor appear three-level, as shown in fig 28. The peak to peak inductor current is reduced in DPS control, thus reducing the losses in the inductor and transformer [29]. The transformer losses are discussed in [30].

The shaded region in fig.28 is the circulating currents during the dual-phase shift control. Moreover, if we compare figures 27 & 28, the shaded area in the dual-phase shift control is less than that in the single-phase shift control. This proves that introducing another phase shift between each bridge's legs will reduce the reactive power inside the converter. An optimized phase shift control is given in [31] to minimize the reactive power flow. Compared with Triple-Phase Shift (TPS) control, the Dual-Phase shift control shows better results in low switch stress and higher efficiency [32]. The detailed analysis to improve the current characteristics in TPS is explained in [33].

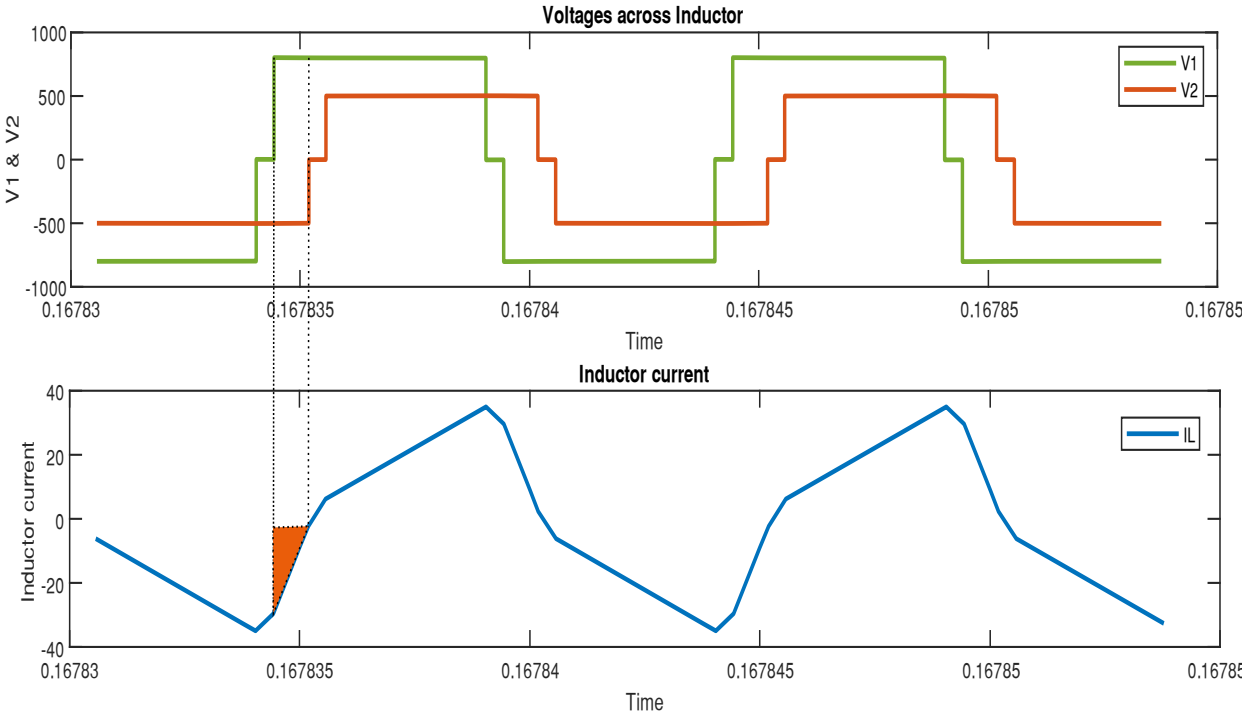

Fig. 28. Inductor voltages and current in DPS control.

3.7. Power Losses Evaluation

In this thesis, we consider the transformer as an ideal model, and we neglect the power loss calculation of both transformer and leakage inductance. Hence we only evaluate the losses in switches using PLECS.

3.7.1. General theory

Switching and conduction losses are the two types of losses that exist in the switch. Switching losses in semiconductor devices are caused by continuous switching (on and off) transitions in which a device is exposed to high voltage and current at the same time. Although the DAB operates in zero voltage switching (ZVS) by default, it only does so during the "ON" switching transition. Conduction losses in DAB are further subdivided into those that occur in semiconductor devices (MOSFETs) and those that arise in transformers and inductors [34].

3.7.2. Switching Losses

In general theory, we calculate the Switching losses of MOSFETs from the following formula

$$P_{sw} = \frac{1}{2} V_{DS} I_{DS} t_{off} f_{sw} \quad (15)$$

$V_{DS}$and $I_{DS}$are the voltage and current at the time of switching, t_{off} is the MOSFET turn-off time, and f_{sw} is the switching frequency. Since DAB undergoes ZVS, the switching losses at the ON state transitions are zero; hence we only have to identify the losses during the OFF state transition. Note that Power Loss P_{sw} represents the switching loss in one switch per leg during the OFF state transition. Therefore, to calculate the total bridge losses, we need to multiple P_{sw} with four. Fig.29 shows the OFF state switching transition of a single switch [34].

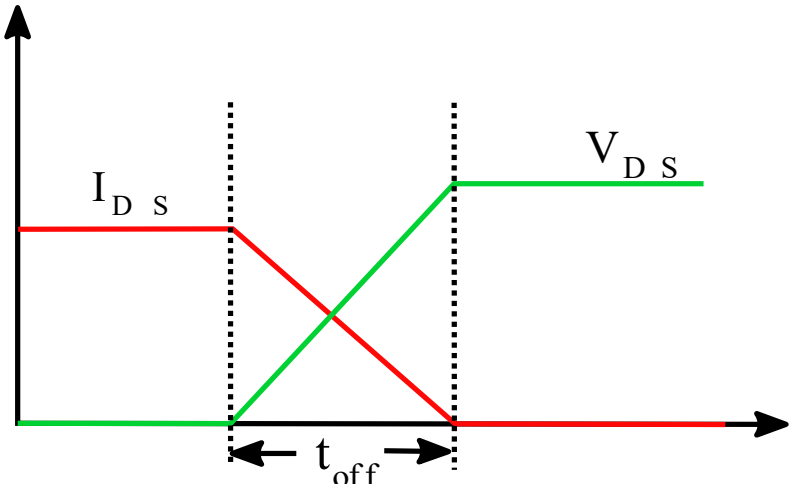

Fig.29. OFF state switching transition.

3.7.3. Conduction Losses

The MOSFET ON-State resistance R_{on} and forward voltage V_f across the body diode of MOSFET are considered to calculate the conduction losses. When the current across the switch is positive, R_{on} is considered. If the current is negative, V_f is considered. The following formulas define the conduction losses of a MOSFET [35].

$$P_{con} = 4\, R_{on,lv}\, {I_{rms}}^2 + 4\, R_{on,hv}\, {I_{rms}}^2 \quad (16)$$

$R_{on,lv}$, $R_{on,hv}$are the MOSFET on-state resistance on both low voltage bridge(lv) and high voltage bridge(hv) respectively.

$$P_{con} = \frac{V_f}{T_{sw}} \int_0^T I_{DS} \tag{17}$$

Equation 17 gives the conduction losses when the current flows through the diode instead of a switch. Plecs simulation has two separate blocks, MEAN and RMS, used to calculate the average and RMS value of current through the switch I_{DS} and I_{rms} respectively, if we want to do power loss calculation analytically. In our example, $R_{on,lv}$, $R_{on,hv}$, and V_f are given in the parameters table.

PLECS can calculate the power losses by adding a heat sink to semiconductor devices without all these formulas. In fig.18 & 23, we can observe a blue shade on the MOSFETs called a heat sink. For calculating losses, we need to add the relevant data provided in the MOSFET datasheets into the thermal library of PLECS. Thus, conduction losses are the continuous thermal conduction losses in watts(W), whereas switching losses are the instantaneous thermal switching losses in joules(J).

The datasheet used for bridge1 is: Cree C3M0030090K Silicon Carbide MOSFET (wolfspeed.com)

The datasheet used for bridge2 is: Cree C3M0065090D Silicon Carbide MOSFET (wolfspeed.com)

Using these datasheets and updating the corresponding values into the thermal library, we can use two blocks available in Plecs to calculate conduction and switching losses. They are Periodic Average and Periodic Impulse Average.

The Periodic Average block will determine the average conduction losses. In contrast, the Periodic Impulse Average block will determine the average switching losses by providing the Average time 'T_{sw},' which is the switching period of each MOSFET.

Table 7 gives the total power losses in semiconductor devices of single-phase shift control and dual-phase shift control, respectively, calculated by the PLECS.

Table 7. Power Losses calculated using PLECS @100 kHz switching frequency.

Power Loss	Power [W]
Power Loss in SPS control	132.54
Power Loss in DPS control	109.94

The above two figures show that the power loss in SPS control is 132.54W, and in DPS control is 109.94W. The load we considered is 10KW, so the total power transfer in SPS control is 9867.46W, and in the DPS control is 9890.06W. PLECS calculated these losses using the sampling time of 10μs within 0.8 secs time span. Here, we can not talk about the efficiency because we neglected the losses in the transformer and the leakage inductance. But we can say those power losses are more in SPS control than in the DPS control from the figures. This again proves that the DPS control is better than the SPS control. A detailed mathematical approach is given in [36] to calculate the power losses of DPS control

After successfully understanding the dual-active bridge converter in offline mode, we were interested in implementing the model in a Real-Time simulator to understand the achievable maximum switching frequency with different sampling frequencies. Since we don't have physical prototypes, we implement our Model in Hardware-In-The-Loop (HIL) simulation. Using PLECS for HIL, we need a Real-Time box (RT-box) 1 or 2 or 3 developed by Plexims. The different RT-box variants have different performance levels. For example, RT-box 1 has a maximum sample rate of 2Msps, whereas RT-box 2 and 3 have a maximum of 5Msps. For other differences, refer to the Plexim website. In my thesis, we were using RT-box 1, and the idea was to deploy the converter and its controller in a single box. Chapter 4 discusses the RT-box setup, Library files used to design the model, and SPS and DPS control simulation results.

4. Hardware-In-The-Loop

4.1. RT-box Setup

Before using the RT box, installing the Target Support Package from the Plexim website is mandatory. This Target Support Package helps to design the converter for real-time applications. A connection must exist between the RT box and a host computer to build the simulations into the RT box. In our case, an Ethernet cable is used to connect the RT box and the PC for communication purposes. And for network configuration, a Static IP address is used. It is a fixed IP address assigned to the RT box. For different types of connection settings and steps, refer to the document [37]. Our interest is in the Hardware-In-The-Loop application, so we connect the RT box Analog Input/Output and Digital Input/Output ports using the cables as shown in the figure.

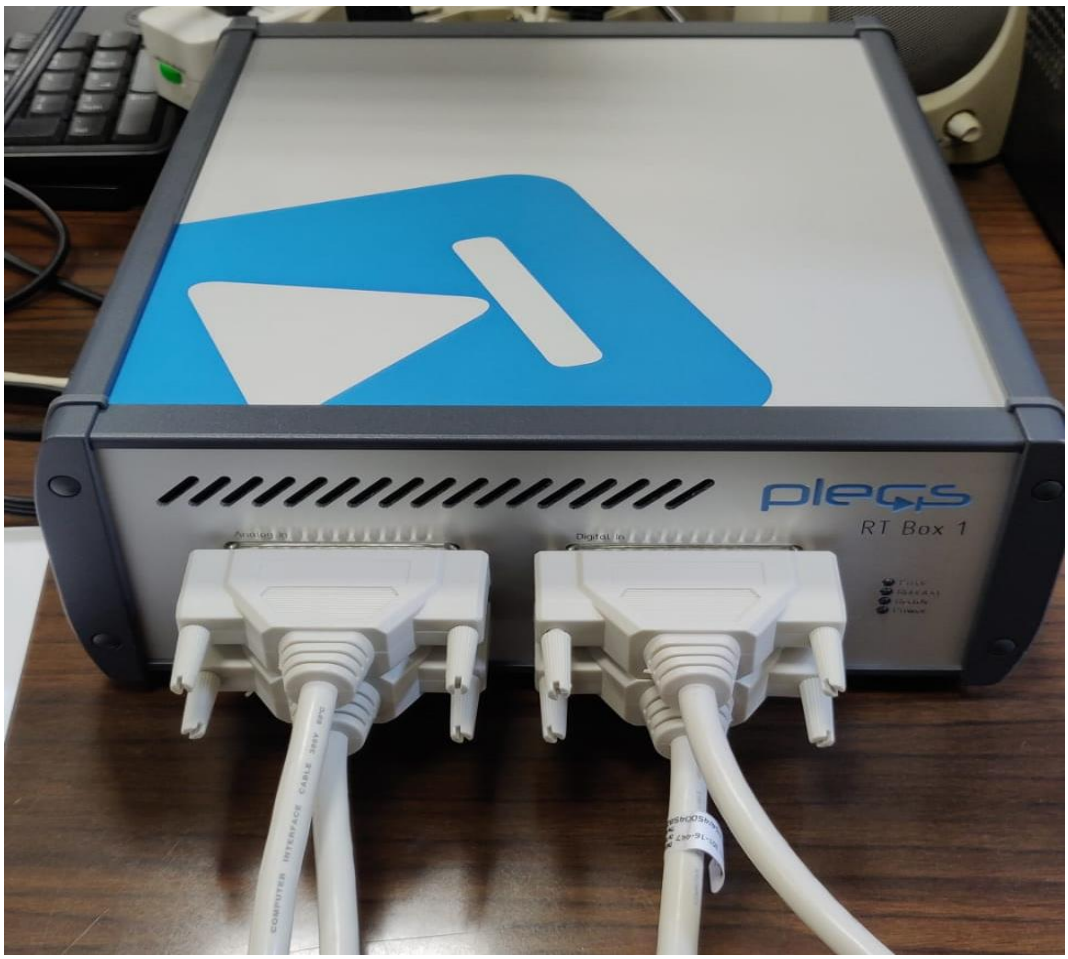

Fig. 30. Hardware-In-The-Loop setup.

4.2. Library files used in the simulation

4.2.1. Analog In

The purpose of this block is to give the measured voltage at an analog input channel. The output signal is scalable and can be used with an offset. The output signal is calculated as input*scale+Offset. The parameters include Analog input channel(s), Scale, and Offset. In the Analog input channel(s), we need to specify the index value. For vectorized input signals, a vector of input channel indices must be defined. Scale factor and Offset value can be determined for the input signal in the Scale and Offset blocks [37].

4.2.2. Analog Out

The purpose of this block is to set the output voltage of an analog output channel. Similar to Analog In, we can scale the output voltage as output*scale+offset. Further, an output voltage limitation can be set in the parameters block [37].

4.2.3. PWM Out (Variable)

The PWM Out (Variable) block generates PWM signals on one or more of the RT Box's digital output channels. If the block uses multiple channels, the modulation index for each channel must be provided via the input signal m, which must be vectorized [37].

The carrier frequency f_c is shared by all channels within the same block. The scalar input signal $'f_c$ can be used to control it during the simulation. The resulting carrier frequency f_c is calculated as the product of nominal carrier frequency specified in the block parameters and the input signal $'f_c$. A constant value one must be fed into the block for a continual carrier frequency. If the PWM generation is synchronized to the RT Box's simulation steps, the carrier frequency is rounded to the nearest integer multiple of the simulation frequency [37].

The vectorized input signal ′ph can be used to control the phase shift between the carriers of the individual PWM channels. Each element of ′ph specifies the phase delay of the PWM carrier in the corresponding channel. The delay is expressed in p.u. of the carrier period and must be between 0 and 1 [37].

4.2.4. PWM Capture

The purpose of this block is to average a digital input throughout a model step.

The PWM Capture output indicates the percentage of time that a digital input signal was active during the previous model step period. The active polarity of PWM capture can be changed from channel to channel. The percentage of time spent in the active state over the previous interval is calculated during an offline simulation [37].

4.3. Single-Phase shift control design

The design is entirely different from the offline model. The DAB power stage was built using the DAB power module from the PLECS library instead of using ideal MOSFET switches. This enables us to use the "Sub-step events" implementation, which improves calculation accuracy by performing sub-step calculations within a single simulation step, resulting in the calculation of as many inductor current values as switching combinations encountered in a single simulation step [38].

4.3.1. Parent Schematic of SPS control

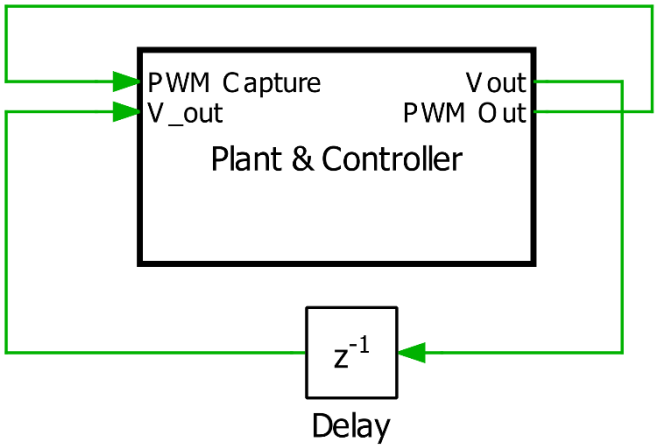

Fig. 31. SPS control for Real Time.

During offline simulation, there are inherent delays of the closed-loop control. Therefore, a delay block with sample time equal to controller sampling time is added to the offline simulation. From fig.31, the Subsystem is enabled for the code generation. The "Plant & Controller" runs on one RT box. It's a complex design since the discretization steps are identical for both Plant and Controller, but the average execution times are different. The plant & controller design from the parent schematic is shown in fig 34.

4.3.2. Plant Model

Fig 32 shows the DAB connected to an 800Vdc on the primary full bridge and 500Vdc on the secondary full bridge. The parameters mentioned in table 4 are considered to implement the 10KW power converter.

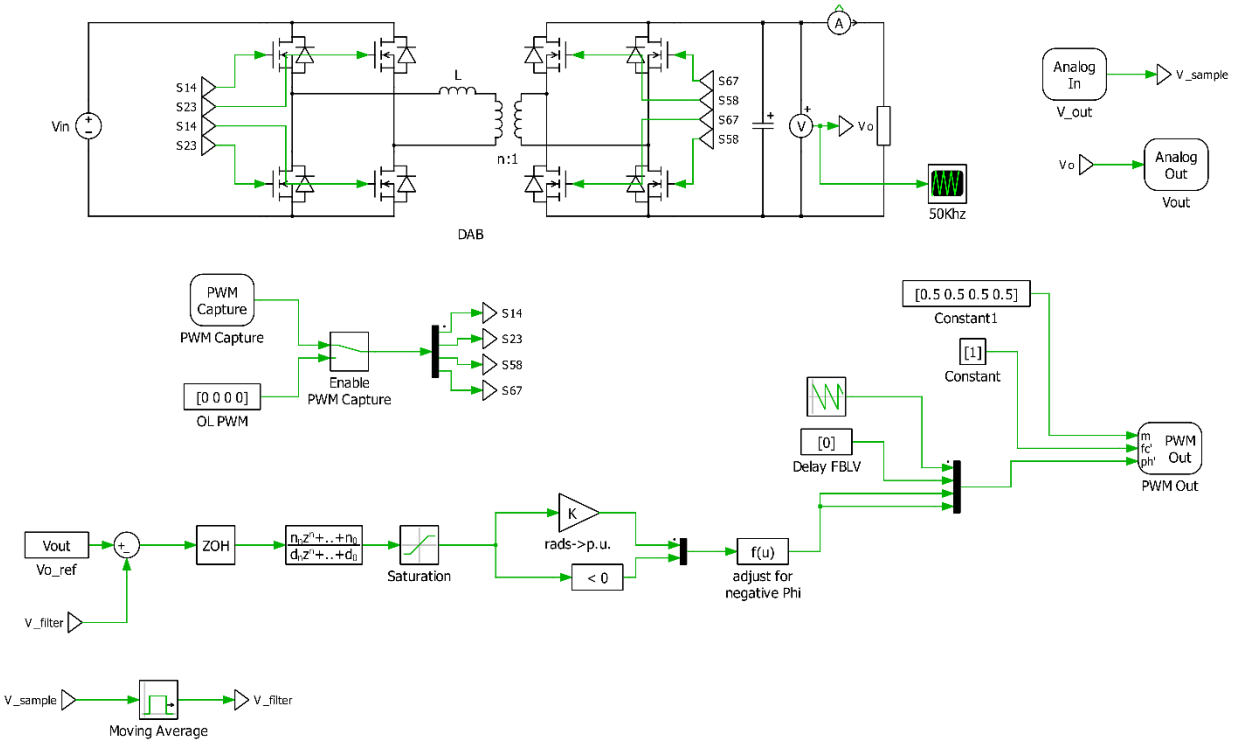

Fig. 32. Plant and Controller schematic.

The PWM capture block samples incoming switching signals every 7.5ns. For the high-fidelity resolution of the PWM inputs, the sampled switching signals are time-averaged over each model step[38]. Generally, we are using a variable time-step solver. PLECS software supports this solver to make use of the ideal switch approach to obtain the fast simulation. The switching instant can be precisely defined, and simulation steps can be performed immediately before and after the switching event. When simulating discontinuous systems, variable-step solvers provide the highest accuracy without the need for many simulation steps in between the discrete events. Thus we chose to use a variable time step solver [39].

But in the fixed time-step solver, a switching event can only be detected after it has occurred in the simulation step. An error is introduced into the simulation result because the new switching state is accounted for with an unknown delay. The error is proportional to the user-specified discrete simulation step size. To meet specific accuracy requirements, the simulation step size can be minimized, and thus the error can be arbitrarily reduced in offline simulation

software. Minimizing the step size in real-time simulators for power electronic systems, on the other hand, is not a viable option in general because the step size sets a hard limit to the time available for computing a new simulation step. To overcome the limited resolution of sample switching signals, there are some developed methods in that time-averaged is one. Thus the PWM capture blocks used the time-averaged method [39].

The analog signals required by the controller subsystem, such as output voltage, are provided by Analog Out blocks. The scale and offsets parameters are set to avoid saturation of the RT Box's analog outputs and match the connected hardware or controller IO requirements [38]. The scaling factors are as follows:

```
% Output voltage analog out
Vo_max = Vo;
Vo_AO_range = 20;
Vo_AO_scale = Vo_AO_range/Vo_max;
Vo_AO_offset = -Vo_AO_range/2;
```

Vo is the output voltage given in Table 4. It doesn't matter which IO channels are configured, but the channel IDs must match the "Plant" and "Controller" [38].
The transformer used in the DAB model is ideal with a series of resistive-inductive impedance representing the transformer winding resistance and leakage inductance [38]. And there is no capacitance equivalent resistance (ESR) in this model because, with the ESR, the model runs into the algebraic loop, generating an algebraic loop error and terminating the simulation.
A moving average filter is used to find the average value of output voltage during the switching period. The average voltage is sampled once per switching cycle, synchronizing with the control execution time [38].

4.3.3. Controller

The controller used in the offline mode is the same controller used in the Real-time simulation with some changes. The output of the PI regulator is fed to the PWM out (Variable) block, which is available in the Target Support Library. To generate four signals, we need to define the four channels in the block parameter as [0:3] and given a constant duty cycle value of 0.5. The generation of phase shift angle is described below. The first channel defined in the PWM block serves as the master, the phase shift specified for the remaining channels determines the phase shift concerning the master channel. It should be noted that the block does not accept negative phase shift values [38].

To adapt the phase shift angle from radians to p.u. and account for negative values, the

following implementation is provided:

$$\varphi_{p.u.} = sign(\varphi_{rad}) + \frac{1}{2\pi}\,\varphi_{rad} \qquad sign(\varphi_{rad}) = \begin{cases} 0, & if\ \varphi_{rad} \geq 0 \\ 1, & if\ \varphi_{rad} < 0 \end{cases} \tag{18}$$

As mentioned above, the DAB operating under SPS needs four different PWM signals generated, two for each full bridge. Two PWM signals for the same full-bridge are phase-shifted 180º. And additionally, we need another phase shift between the two full bridges of the converter. In total, four phase shift angles need to be provided [38]. If the sampling and switching periods are equal, there is no need to give the first (master) PWM channel a phase shift. However, our model is designed to achieve oversampling. Therefore the first PWM has to be shifted. The reason is that the counters customized with the PWM out block will restart

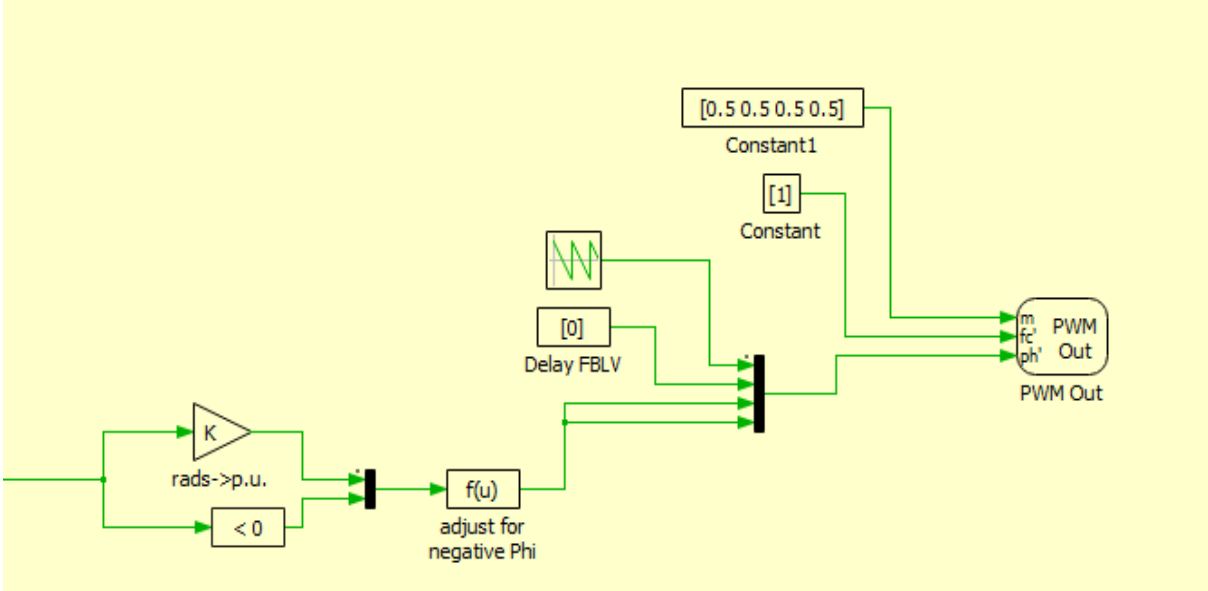

Fig. 33. Schematic of Phase shift generator.

every time executed, every sampling period mainly. Since the sampling period is smaller than the switching period, the PWM signals are not generated correctly. The solution for this problem is to shift the master PWM signal. Fig 33 shows the "phase shift generator."

Another block that comes under the controller is Analog In. Analog In provides the output voltage from the plant. The input signals are scaled and offset, similar to the Analog Out block. The scaling factors are as follows:

```
% Output voltage analog input
Vo_AI_range = 20;
Vo_AI_scale = Vo_max/Vo_AI_range;
Vo_AI_offset = Vo_max/2;
```

To avoid introducing the high-order/complex physical filters in the DAB plant, the output voltage in SPS and both the output voltage, output current in DPS are used as feedback for the control. This approach requires oversampling methods to calculate the average converter current and voltage over a switching period. This implementation allows for a faster model response at the cost of a more complex controller structure [38].

After connecting the cables, as shown in fig 30, built and run the system in RT-Box. The switching frequency and sampling frequency are not mentioned, which are required to run the model. These are included in the final results and are discussed later after designing the Dual-Phase shift control for real-time applications.

4.4. Dual-Phase shift control design

The design is similar to the SPS control from the RT box model, except there is an inner phase shift between each bridge's legs. The parent schematic is shown in the fig 34.

4.4.1. Parent Schematic of DPS control

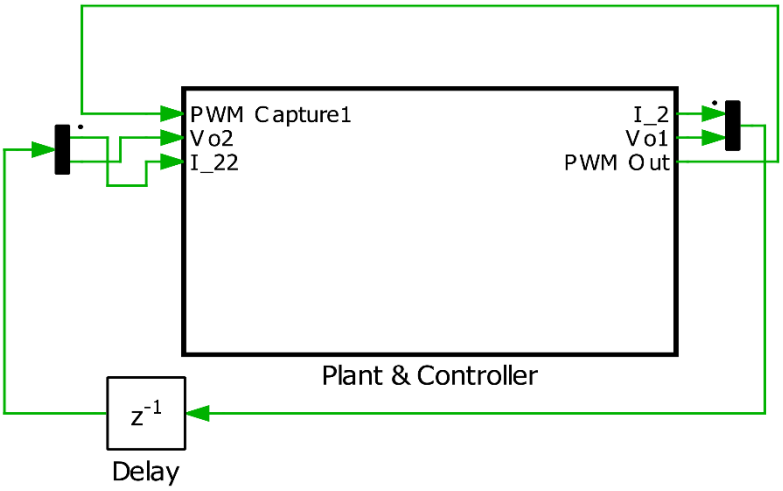

Fig. 34. DPS control for Real-Time.

Similar to the SPS control, there is a delay block for the offline simulation. The code enabling procedure is also the same. The only difference is in the controller, and the parameters considered to design the model are shown in Table 4, along with the same output capacitance.

4.4.2. Plant & Controller Model

There is no change in the DAB model compared with the SPS control model and using the same "sub-step events" to improve the calculations. DPS requires a phase shift between the two bridges, a phase shift between each bridge's legs, and a 180º phase shift for the signals in the same portion. So, PWM Out (Variable) block generates the eight PWM signals for eight switches using eight channels. A constant eight duty cycle, each value of 0.5, is used. The carrier signal with minimum signal value 0, maximum signal value 1, Duty cycle 0, and phase delay 0, along with the switching frequency, is used, and frequency details are discussed in the results. The design is illustrated in fig 35.

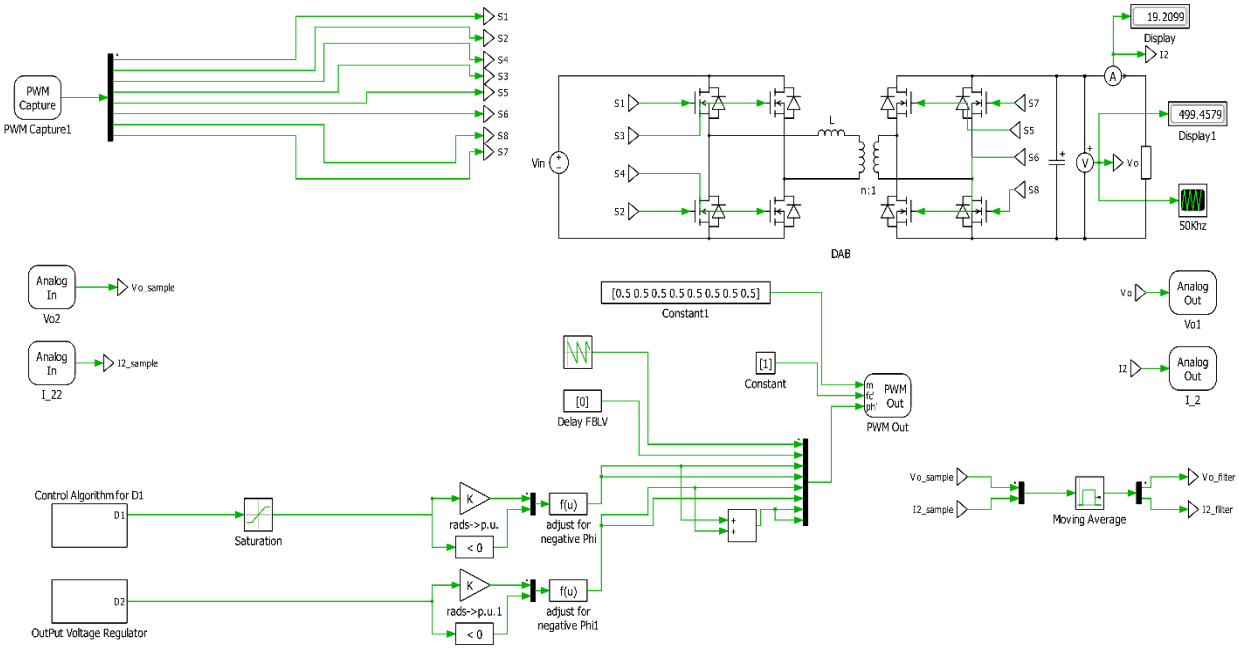

Fig. 35. DPS plant and controller schematic.

We know that to generate modulation signal for inner phase shift ratio using current stress algorithm, we required power conversion ratio and voltage conversion ratio mentioned in Equations 13 and 14. Therefore from that equation, it's clear that the feedback control depends on the converter output current I_2 and output voltage V_2. And to measure I_2 and V_2, we need two Analog Out/In blocks, as shown in fig 35. The scaling and offset factors of the Analog block are given below:

```
% Output voltage analog out
Vo_max = Vo;
Vo_AO_range = 20;
Vo_AO_scale = Vo_AO_range/Vo_max;
Vo_AO_offset = -Vo_AO_range/2;

% Output voltage analog input
Vo_AI_range = 20;
Vo_AI_scale = Vo_max/Vo_AI_range;
Vo_AI_offset = Vo_max/2;

% Output current analog out
I2_max = 20;
I2_AO_range = 20;
I2_AO_scale =I2_AO_range/(I2_max*2);
I2_AO_offset = 0;

% Output current analog input
I2_AI_range = 20;
I2_AI_scale = I2_max*2/I2_AI_range;
I2_AI_offset = 0;
```

After defining all the parameters, we can build the code into the RT box following the same procedure mentioned in the SPS control model. Now, we can connect to the RT box and enable the auto triggering to find out the results.

We didn't discuss the switching frequency and sampling frequency because we don't know the limitations of RT box 1 for our models. In order to understand the RT box limitations, we try different switching and sampling frequencies to conclude our results.

4.5. SPS & DPS Real-Time Simulation results

A 100kHz switching frequency is used during offline simulation, so implementing the real-time simulations with a 100khz switching frequency and 2MHz sampling frequency. And an error is generated. Even with 1MHz, 500kHz, and 250kHz, an error is obtained in building the code into the RT box. That means it's understandable that building the plant and the controller together into a single RT box crosses the limitation and gives us an error. The same thing happened with an 80Khz switching frequency. Later we chose 50kHz switching frequency and 2MHz sampling frequency. In this consideration, an error is generated due to the maximum step size of the RT box is less than 1μs. So a 50kHz switching frequency and 1MHz sampling frequency are considered to execute the models. We can build the SPS control model into the RT box at this stage, but the execution time is a problem. As we know that real-time runs at

the same rate as the actual system. In particular, the execution time and sampling time has to be:

$$T_{ex} \leq T_s \tag{19}$$

If $T_{ex} > T_{s,}$ we need to decrease the sampling frequency or reduce the execution time by reducing the complexity or changing the digital platform. Reducing the complexity or changing the digital platform are not our options, so decrease the sampling frequency. With 50kHz switching frequency and 1MHz sampling frequency, the execution time 'T_{ex} ' increased more than the systems sampling period '$T_{s.}$' Therefore, we reduced the sampling frequency to 500kHz. And now, we can build the SPS control model into an RT box and get the results. The execution time and sampling time for SPS control are shown in Table 8.

Table 8. Sampling time and Execution time of the SPS control.

Sampling Time [µs]	Execution Time [µs]
2	1.76
4	1.82

From Table 8, the sampling time and the execution time are obeying the rule (19). And fig 36, and 37, shows the output voltage from the real-time simulation.

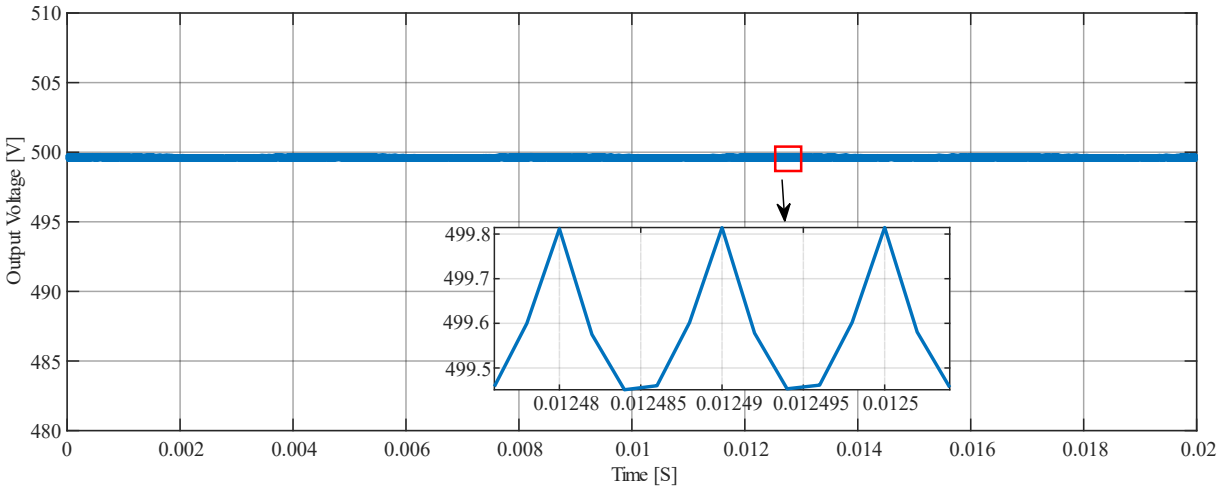

Fig. 36. SPS control Output Voltage from the Real-Time simulation with 500Khz sampling frequency.

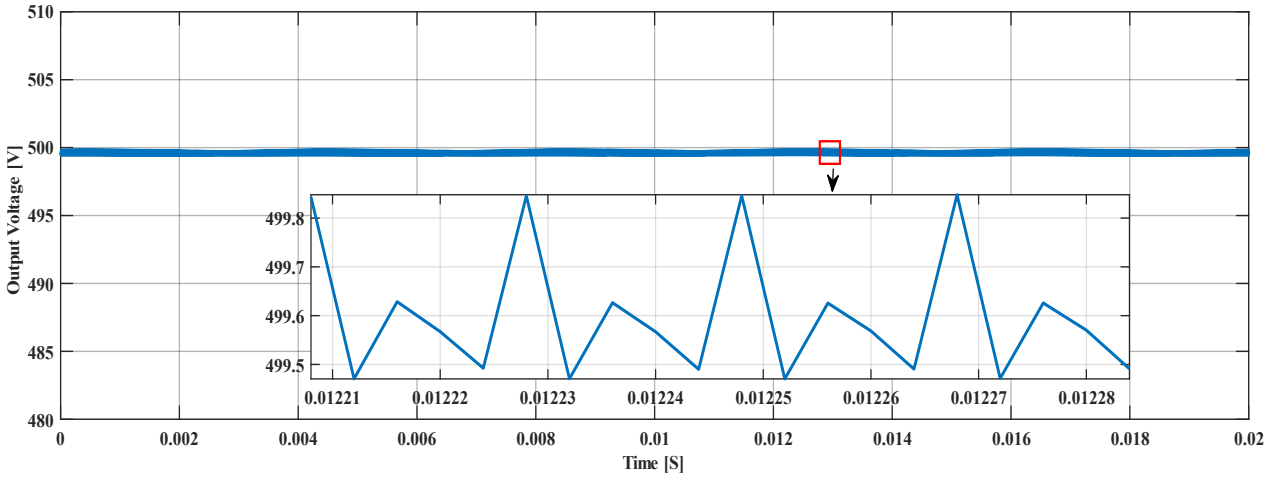

Fig. 37. SPS control Output Voltage from the Real-Time simulation with 250Khz sampling frequency.

From fig 36 and 37, As the number of samples decreases, the model tends to be ideal. And hence the distortion is higher in 250kHz than in 500kHz sampling frequency.

The complexity of the controller has increased due to the implementation of the inner phase shift ratio in the dual phase-shift control. The controller cannot hold the condition (19) with a 50kHz switching frequency and 500kHz sampling frequency. Table 9 shows the sampling time and execution time of a DPS control. Since the 500kHz sampling frequency violates the rule, the only option is implementing the DPS control with 250kHz. DPS control model result is shown in fig 38.

Table 9. Sampling time and Execution time of the DPS control.

Sampling Time [µs]	Execution Time [µs]
2	2.64
4	2.91

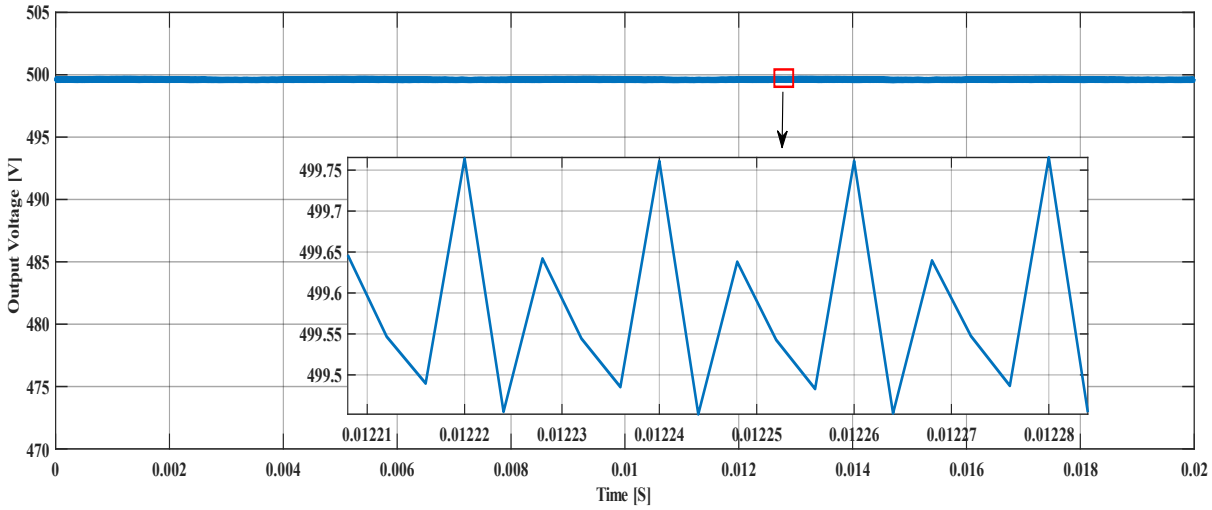

Fig. 38. DPS control Output Voltage from the Real-Time simulation with 250kHz sampling frequency.

After understanding the SPS and DPS models switching frequency, it's easy to calculate the errors between output voltage for different samples. For calculating errors between output voltage ripples using different sampling frequencies, offline simulation results are considered.

4.6. Root-Mean-Square-Error calculation in SPS control

By determining the output voltage signal at the 2MHz sampling frequency as a reference, we calculate the error for 1MHz, 500kHz, 250kHz sampling frequencies signals using Root Mean Square Error (RMSE). RMSE is used to measure the difference between the values of the estimator and the observed values. Here, 2MHz signals are designated as an estimator and the remaining signals as observed values. The Root-Mean-Square-Error formula is given below:

$$RMSE = \sqrt{\frac{\sum_{t=1}^{T}(Estimated\ values - Observed\ values)^2}{T}} \qquad (20)$$

Fig 39, 40, 41, and 42 show the output voltage with different sampling frequencies along with their ripples.

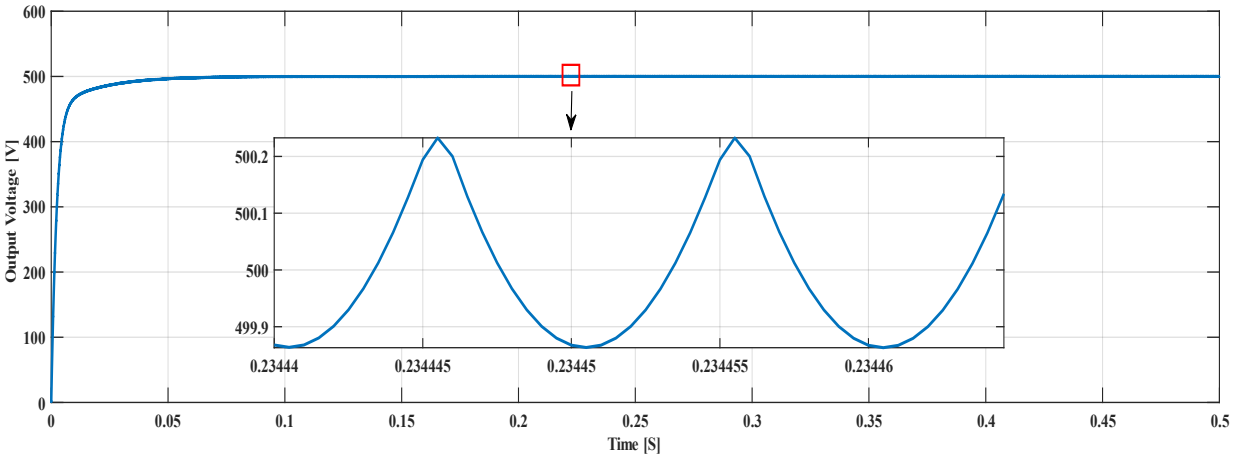

Fig.39. 2Mhz Sampling frequency Output voltage in SPS control.

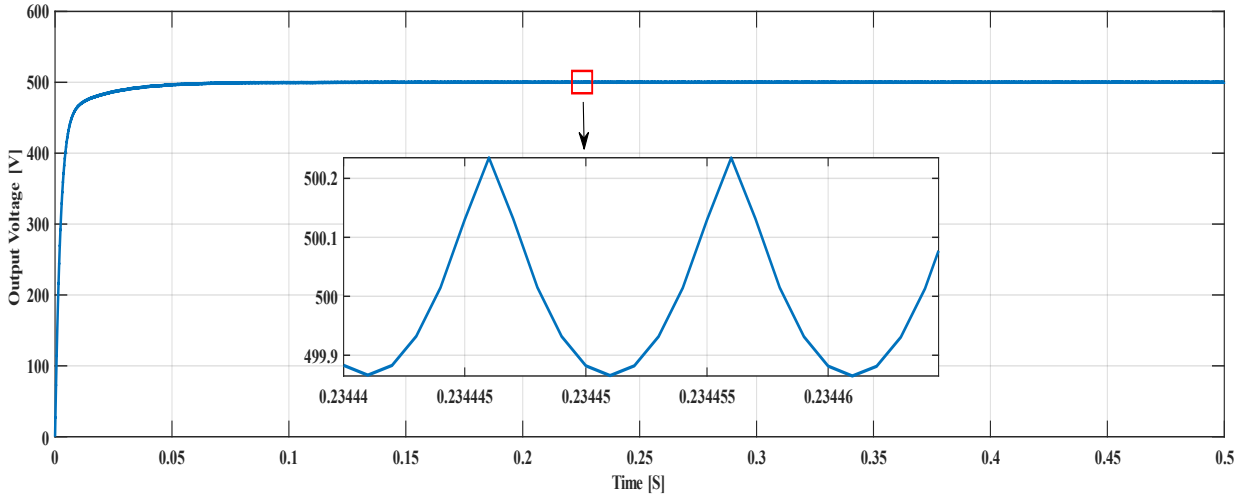

Fig.40. 1Mhz sampling frequency output voltage in SPS control.

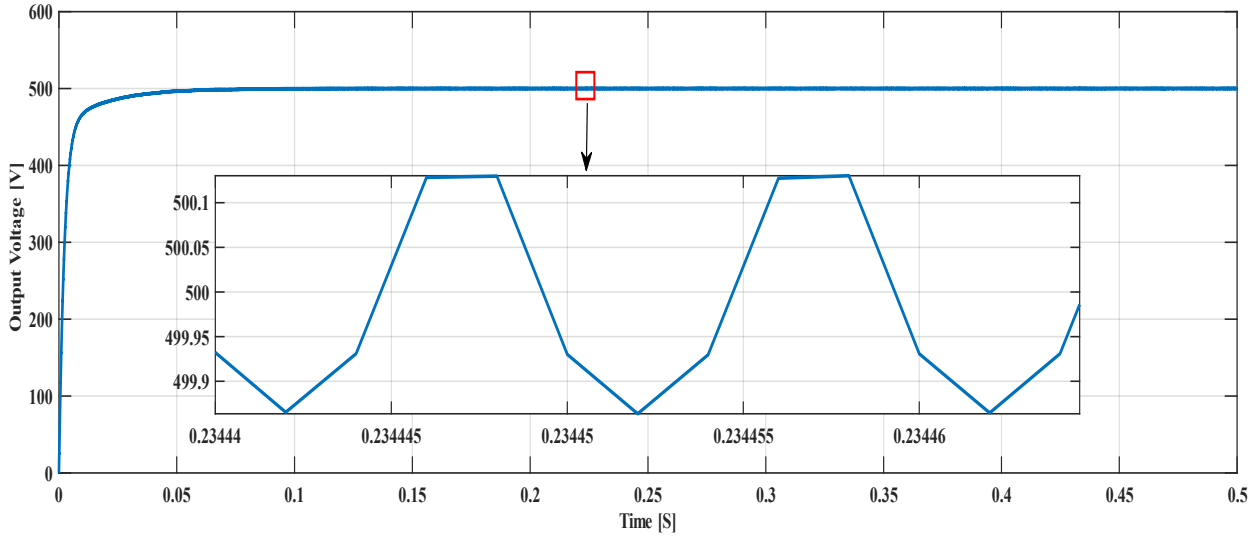

Fig.41. 500Khz sampling frequency output voltage in SPS control.

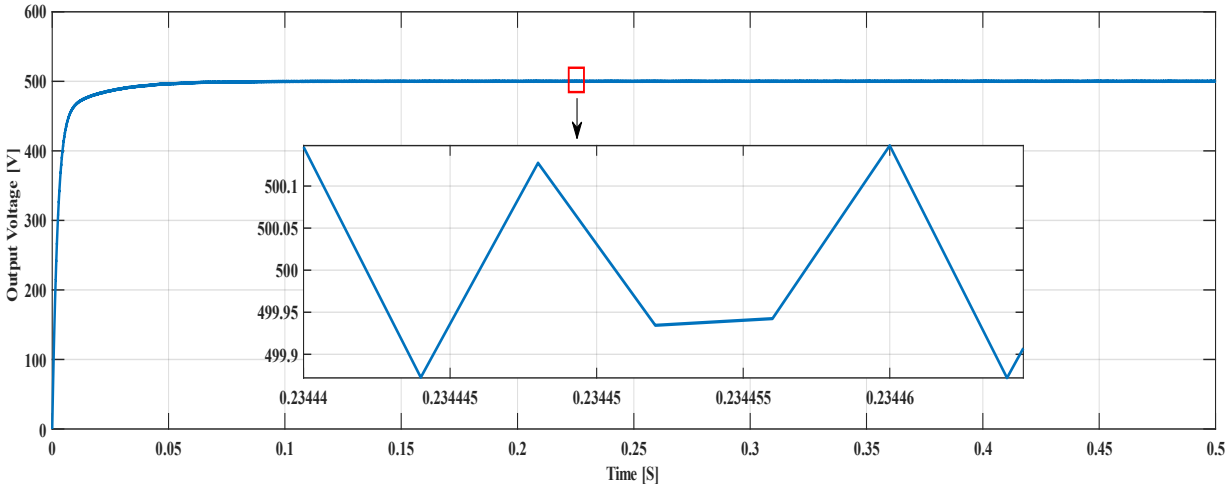

Fig.42. 250Khz sampling frequency output voltage in SPS control.

Fig 43 shows a closer picture of output voltages with different sampling frequencies. The 2MHz signal is decimated by the 2, 4, and 8 factors to match the peak values of 1MHz, 500kHz, and 250kHz signals. After decimating the signal, the calculated error is shown in fig 49.

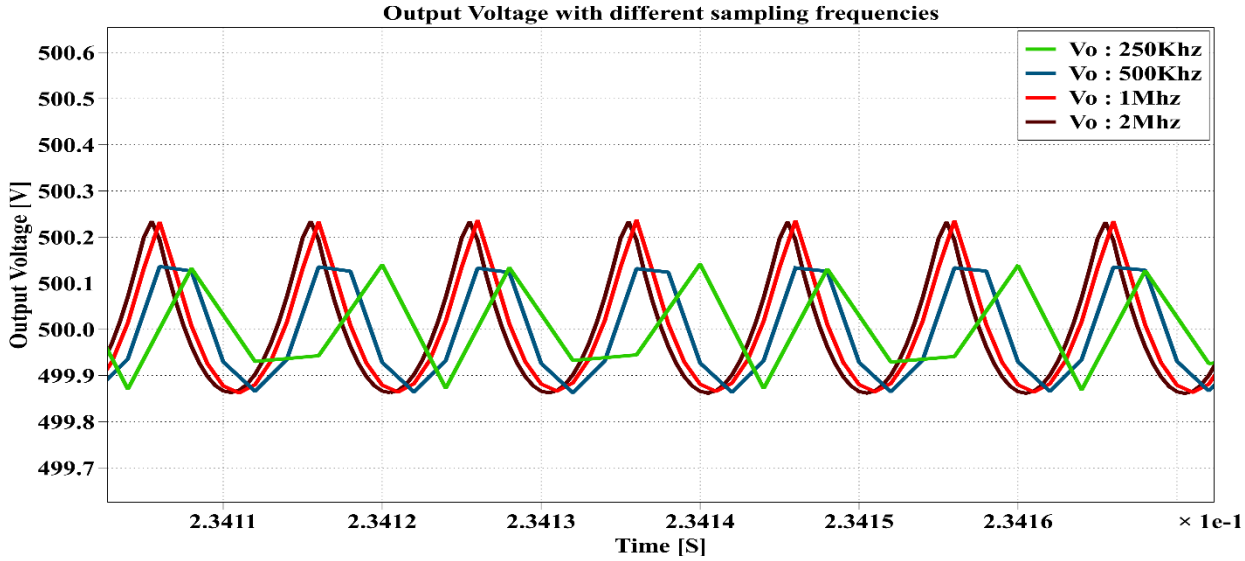

Fig. 43. Output voltage in SPS control with different sampling frequencies.

After calculating the error from fig 49, it is noticeable that there is a similarity between all considered frequencies, and the error between them is lower than 0.035%. Moreover, the offline results look precisely like the real-time simulation results, showing the same average output voltage.

4.7. Root-Mean-Square-Error Calculation in DPS control

A similar procedure is considered to calculate the similarity between the signals in the DPS control model. Fig 44, 45, 46, and 47 show the output voltage with different sampling frequencies along with their ripples.

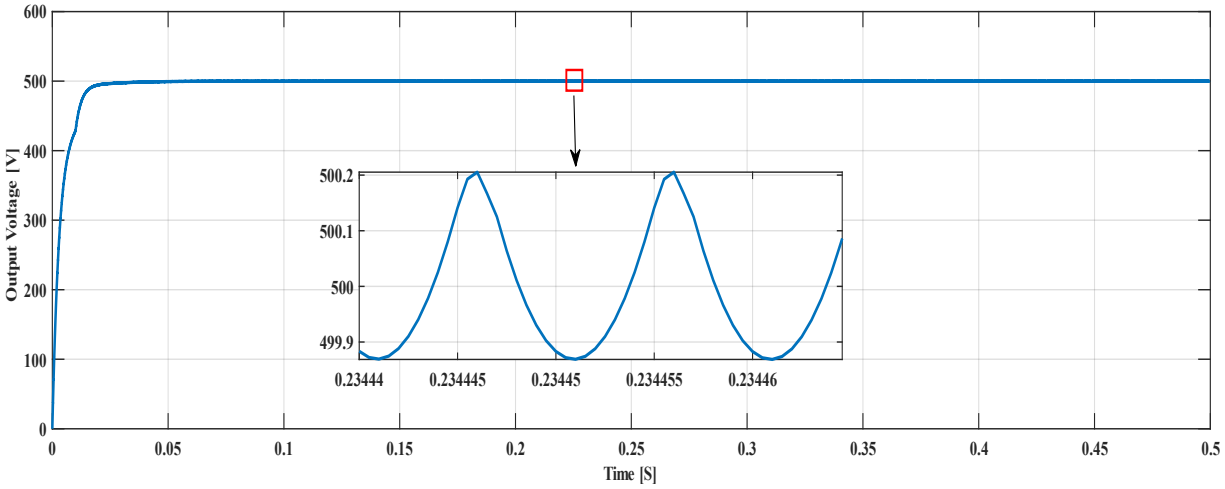

Fig. 44. 2Mhz Sampling frequency Output voltage in DPS control.

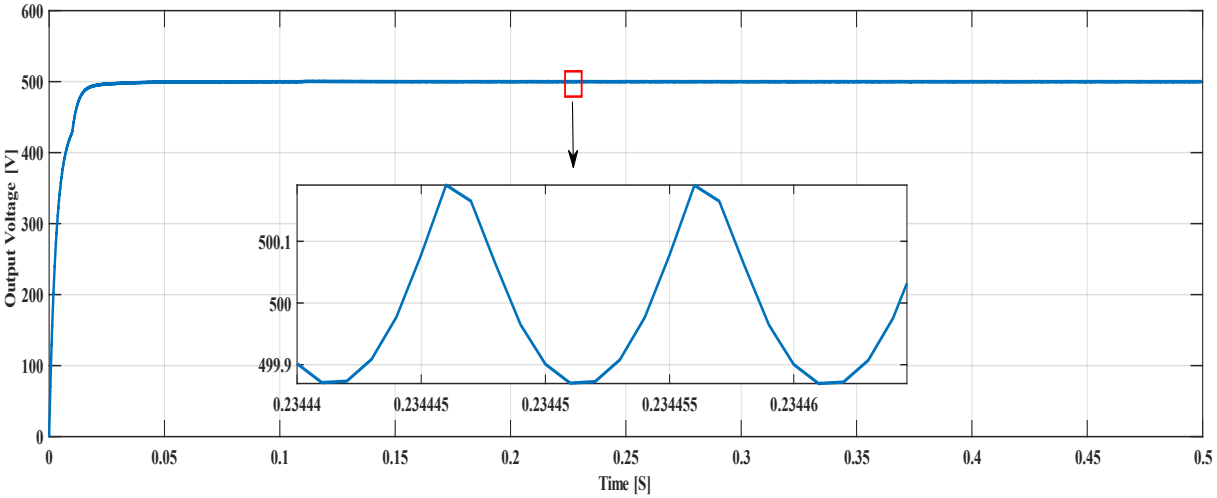

Fig.45. 1Mhz Sampling frequency Output voltage in DPS control.

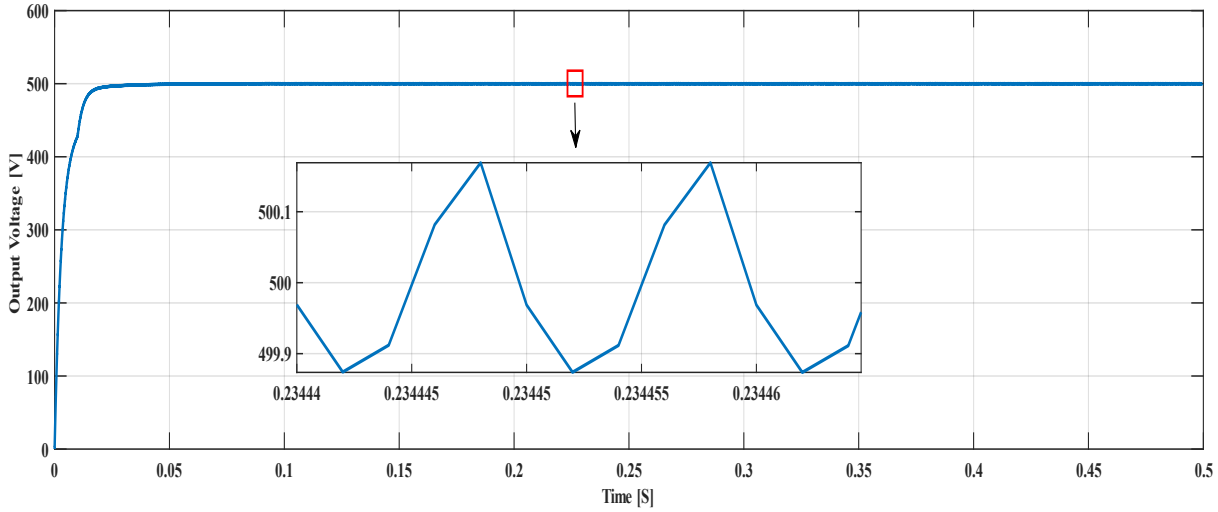

Fig. 46. 500Khz Sampling frequency Output voltage in DPS control.

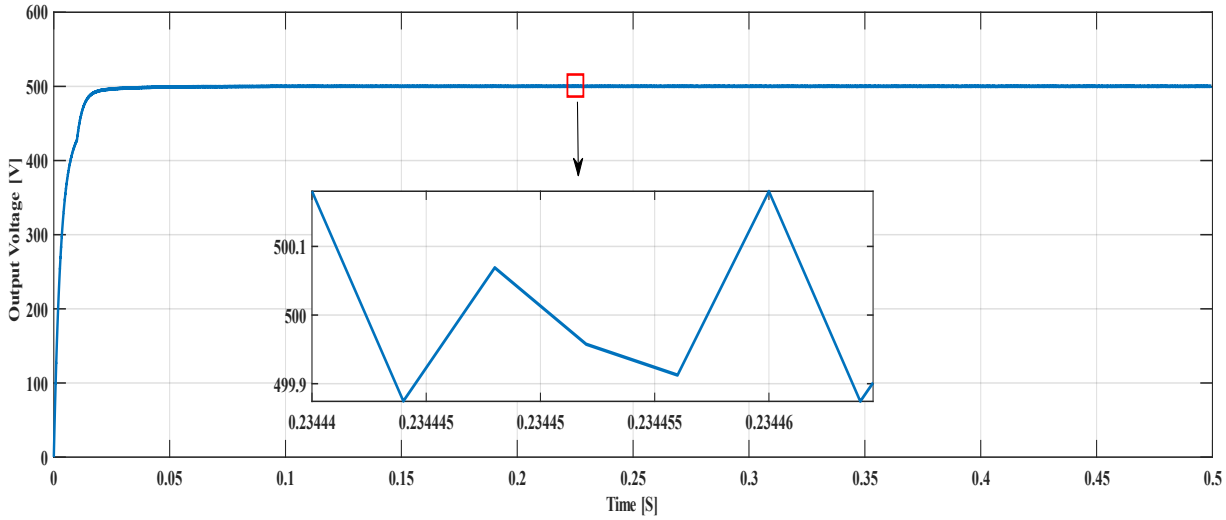

Fig.47. 250Khz Sampling frequency Output voltage in DPS control.

Fig 48 shows a closer picture of output voltages with different sampling frequencies. Same as SPS control, the 2MHz signal time samples are decimated by the 2, 4, and 8 factors to match the peak values of 1MHz, 500kHz, and 250kHz signals. After decimating the signal, the calculated error is shown in fig 49.

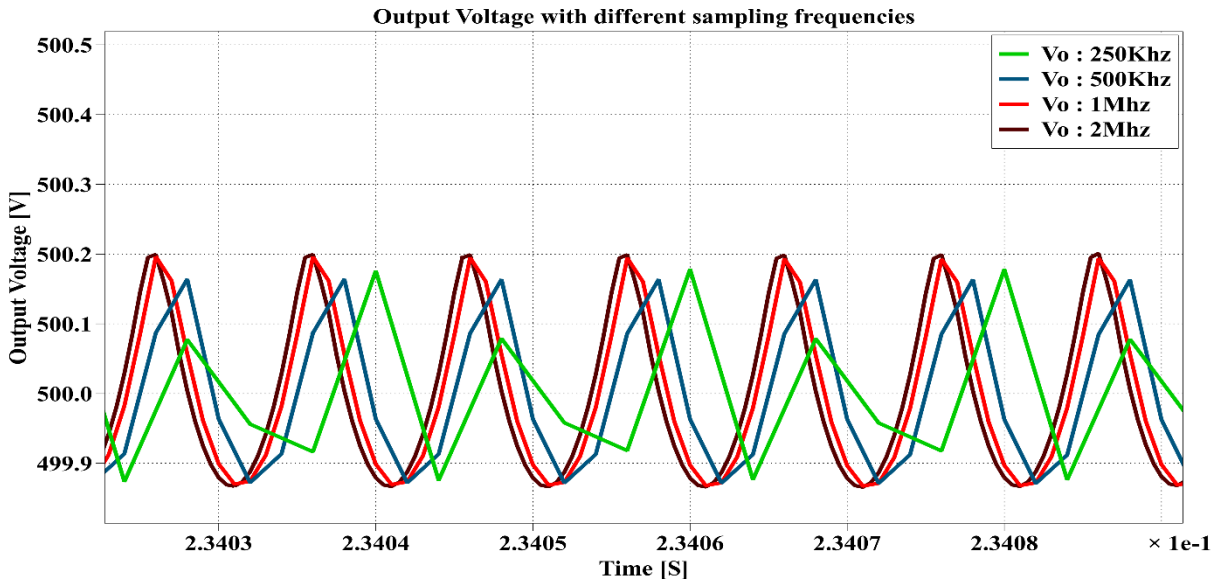

Fig. 48. Output voltage in DPS control with different sampling frequencies.

After calculating the error from fig 49, it is noticeable that there is a similarity between all considered frequencies signals, each with an approximate error < 0.035%. Moreover, as discussed in the SPS control model, the offline results look precisely like the real-time simulation results in the DPS control.

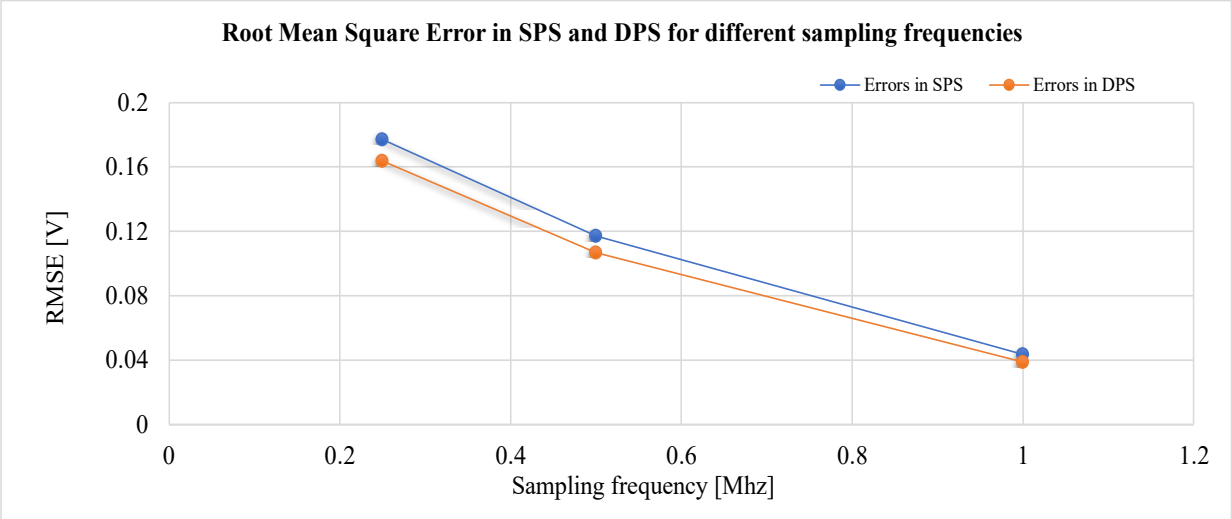

Fig.49. RMSE for different sampling frequencies in both the controls.

Note: RMSE is calculated by considering some samples in the steady-state, which means all the transients have been ignored.

From fig 49, comparing the 2Mhz signal with 1Mhz, 500Khz, and 250Khz signals, it can be observed that the number of samples increasing, the error decreases.

The offline simulation results are satisfactory from chapter 3 and achieved by using a 100kHz switching frequency. But the real-time simulation results are disappointing. In chapter 4, using Hardware-In-The-Loop, the RT box with the designed and implemented SPS and DPS control models can withstand only 50kHz switching frequency. This is due to the implementation of the converter and its controller together into a single RT box. So, to improve the real-time system efficiency, it's better to split the converter and controller into two and execute the converter into an RT box and its controller into a DSP (Digital-Signal-Processor). The new design for DSP and conclusions are discussed in chapter 5.

5. DSP Implementation

To use the DSP, installing the TI C2000 support package from the Plexim website is mandatory. This TI C2000 package supports TI2806x, TI28004x, TI2833x, TI2837xS manufactured by Texas Instruments. This experiment is conducted using a TI2806x microprocessor. TI2806x is a 32-bit microcontroller used to improve the closed-loop performance in a real-time control application. The following figure shows the Launchpad used in this experiment.

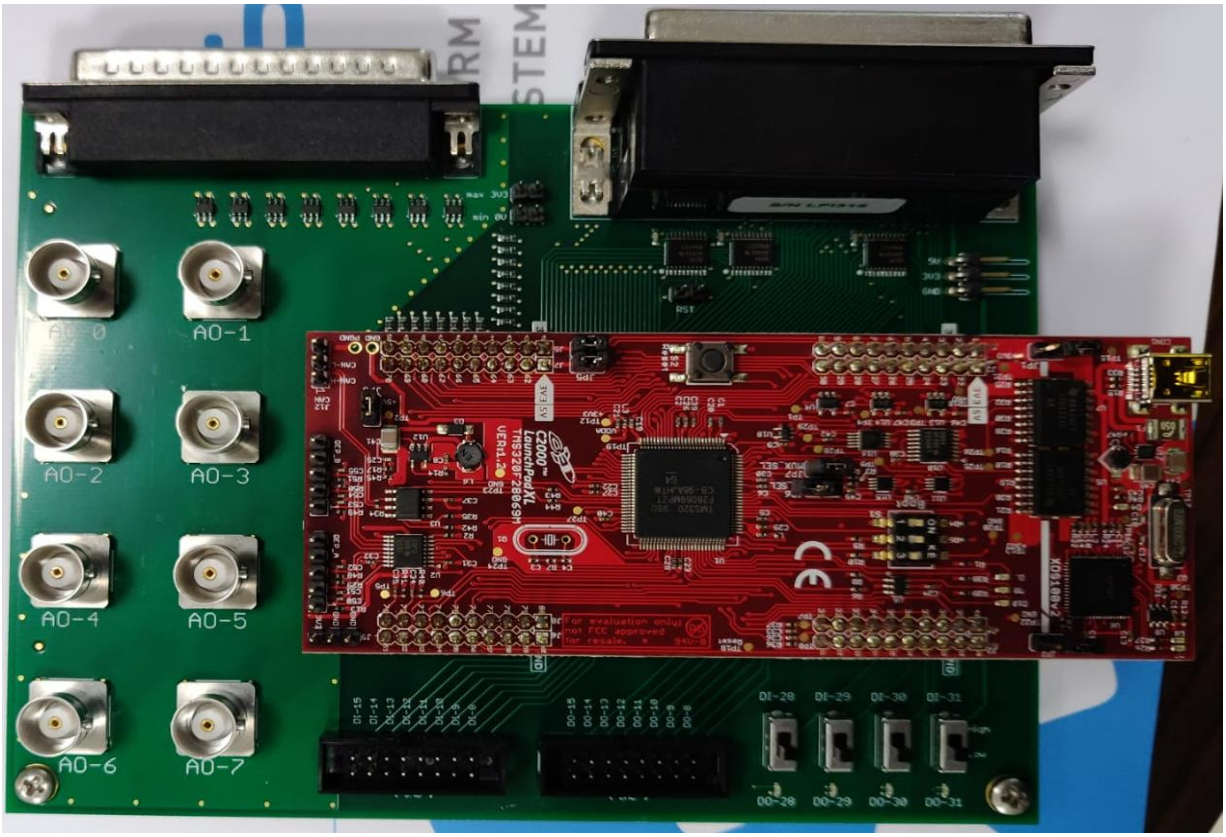

Fig. 50. TI2806x DSP.

From fig 50, it is noticeable that the red board is the TI2806x DSP, and the green board is the Plexim support board that allows communication with the RT box. After connecting the DSP with the RT box and connecting the DSP to the PC using a USB cable. Then the setup is ready to deploy the code. But the design's discussed in chapter 4 doesn't support the DSP. It is mandatory to use the new library files that support the Texas Instruments products. Hence it is advisable to change the existing design by replacing it with supporting blocks.

5.1. SPS Design

When the plant and controller are split, the discretization step size is different, and the execution time is also different from each other. Therefore, the burden on the RT box reduces and allows us to increase the switching frequency. There is no change in the plant design, and the only difference is the controller design compared to the design in chapter 4. Since DSP has been used, an Analog to Digital converter (ADC) to converter the signals and a PWM block designed primarily for DSP are needed. The figure below shows the SPS controller for DSP.

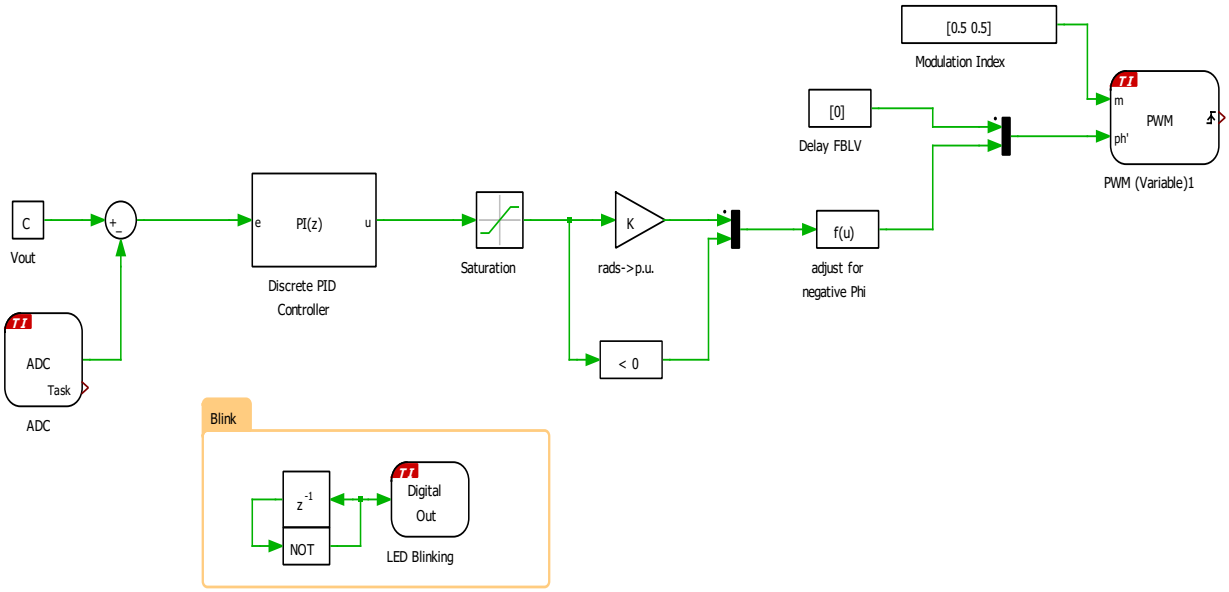

Fig. 51. SPS controller for DSP.

The ADC peripheral is configured as a single-ended input with an internal voltage reference in this block. The measured voltage at the ADC pin is represented by the ADC block output signal. The output is scalable and can be used in conjunction with an offset, with the output signal calculated as input*Scale+Offset. When the Analog input channel(s) parameter is vectorized, each input channel is measured in the order specified by the input channel vector [40].

The Trigger source parameter allows you to choose between an automatic or external ADC start-of-conversion signal, with the latter being attached to the ADC trigger port. The control task executes whenever the last ADC channel is converted if the ADC task output is a Control Task Trigger source [40]. The scaling and offset parameters are as follows:

```
% DSP Analog In Configuration
1   DSP_ADC_scale = [1/Vo_AO_scale];
2   DSP_ADC_offset = [0]
```

The scaling and offset parameters of the Analog Output block used in the plant to capture the output voltage are:

```
% Output voltage analog out
3   Vo_max = Vo*1.25;
4   Vo_AO_range = 3.3;
5   Vo_AO_scale = Vo_AO_range/Vo_max;
6   Vo_AO_offset = 0;
```

The error is fed to the PI regulator with Kp = 0.11173*0.015 and Ki = 0.11173. To avoid the negative phase values, the regulator's output is given to a function (18). Thus, a phase shift value is generated and given to the PWM block.

On a grouping of one to three PWM channels that share a common synchronization impulse, the PWM (Variable) block generates a complementary PWM pair. If the block employs more than one PWM channel, the modulation index for each channel must be provided via the input signal m, which must be a vectorized signal. The carrier begins at 0 and ranges from 0 to 1. The vectorized input signal ′ph can be used to regulate the phase shift between the carriers of the individual PWM channels. The phase delay of the PWM carrier with the same index is specified by each member of ′ph. The delay is measured in carrier period units and must be between 0 and 1 [40].

The PWM resource carriers are linked to a common synchronization signal configured in the Sync + Synchronization impulse from setting. The synchronization signal can come from the carrier zero counts of the block's first PWM resource, another PWM (Variable) block, or an external source via a GPIO pin. An External Sync block is required when an external GPIO synchronization signal is used. Each PWM (Variable) block has a synchronization output linked to other PWM (Variable) blocks. The first channel of each group of PWM generators is set to be the master, and the other channels are set to be slaves. When a synchronization impulse is received, the master sends a synchronization signal to the slaves of the same block and other PWM (Variable) blocks connected to the synchronization output signal of the block. When this occurs, the slaves' ramp generators are reset to their initial values computed from the input signal ‘ph to achieve the desired phase shift [40].

The first element of the input signal ‘ph corresponds to the master channel's phase delay and is only relevant if the synchronization source is another PWM (Variable) block or an external

GPIO. The phase delays between multiple PWM (Variable) blocks are only accurate if they share the same Carrier frequency. The PWM (Variable) block can be configured to generate independent interrupts to initiate ADC conversion and the Control Task Trigger. Interrupts occur at the carrier underflow, overflow, or underflow and overflow events and are synchronized with the master channel PWM carrier. Underflow and overflow events occur when the PWM carrier reaches the minimum and maximum values [40]. PWM carrier underflow or overflow triggers the first ADC channel's start-of-conversion signal. Until the result register of the final ADC channel is changed, the ADC channels are sampled, and the result registers are updated sequentially. This task is triggered when all ADC results are available, and the ADC conversion end-of-conversion interrupt is triggered. Using a technique known as explicit implementation, the ADC conversion starts simultaneously as PWM actuation and ensures that the ADC results registers are updated before performing the control loop [40].

In any scheme containing both ADC and PWM components, the PLECS Coder automatically selects the PWM generator with the highest control task accuracy as the ADC trigger; unless otherwise specified, this implementation method is called implicit. The CPU Timer will be used if the PWM generators cannot trigger the ADC at the exact target frequency. When the ADC conversion is complete, the control job will always be started [40]. In this experiment, the implicit method is implemented to generate the required pulses.

Following a trip event, the trip zone submodule can be used to disable the power stage. When there is an active low condition on the trip zone GPIO inputs assigned in the Power stage Protection block, trip events are detected. The PWM block protection parameters configured the trip settings for all PWM resources associated with the block. When a trip event is detected, the PWM module can either do nothing or activate a one-time trip event or a cycle-by-cycle trip event. When a trip zone is activated, a one-shot trip event latches the PWM output to the PWM safe state. Until the PWM counter reaches an underflow event, cycle-by-cycle trip events set the PWM output to the PWM safe state. If the trip zone input is no longer active, the trip condition erases when the PWM counter underflows. This event attempts to clear the trip condition once per PWM cycle using the cycle-by-cycle trip event. The Power stage Protection block allows you to configure the PWM safe state [40]. Here in this experiment, the power stage protection is not used to simplify the design.

Even the DPS control design looks similar, with some modulations. The figure shows the

designed model.

5.2. DPS Design

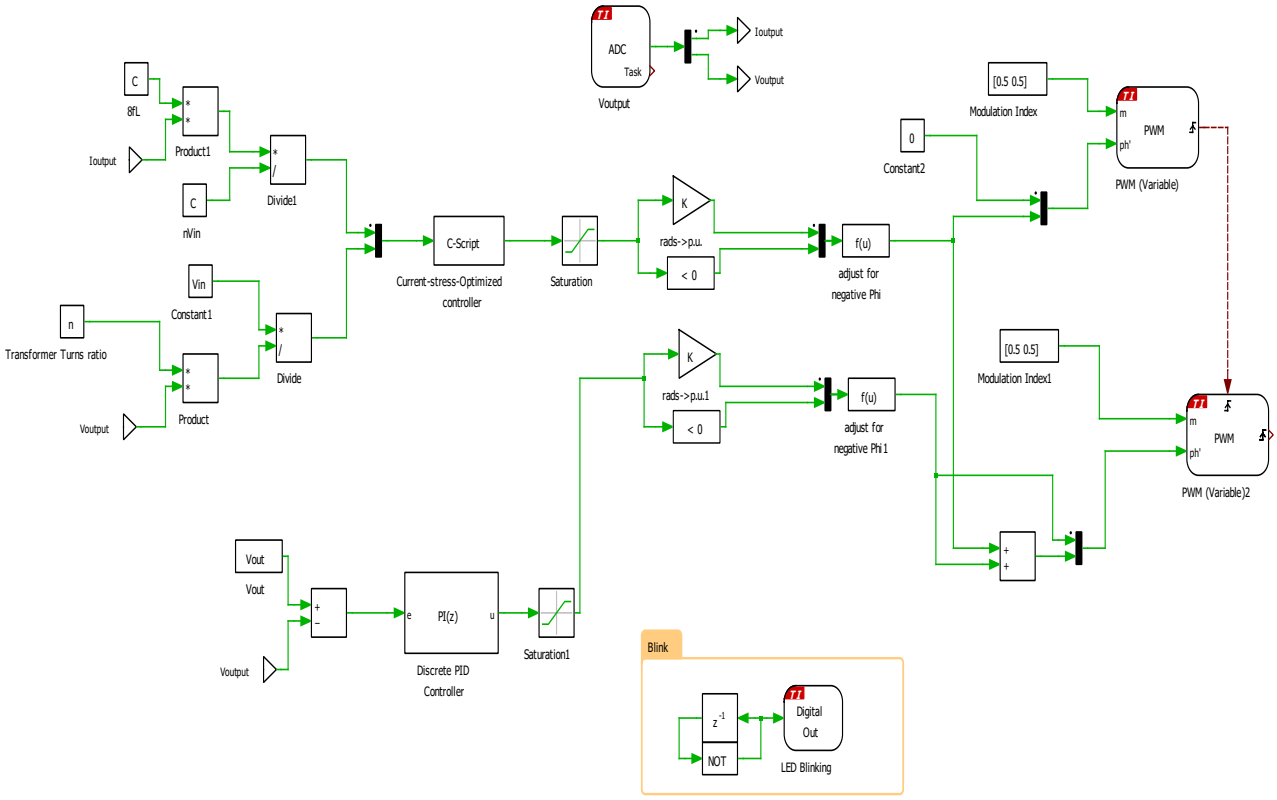

Fig. 52. DPS controller for DSP.

A single ADC block is enough to convert the two feedback signals from analog to digital by providing the two channels pins for each in the parameter section. The two feedback signals are output current and output voltage, required to generate the inner phase shift ratio and outer phase shift ratio.

As mentioned above, the PWM block generates the pulses as a pair. So to provide eight pulses to the eight switches, two PWM synchronized blocks are used. From fig 52, how phase shifts are generated can be seen. The model is designed implicitly, the same as in SPS control. Once the design is finished, the scaling and offset parameters of the ADC block should be mentioned in the initialization tab.

The scaling and offset parameters of the ADC block and the Analog Out block from the plant subsystem are as follows:

```
% Output voltage analog out
Vo_max = Vo*1.5;
Vo_AO_range = 3.3;
Vo_AO_scale = Vo_AO_range/Vo_max;
Vo_AO_offset = 0;

%Analog In\Out Configuration
I2_max = 65*1.25;
I2_AO_range = 3.3;
I2_AO_scale =I2_AO_range/2/I2_max;
I2_AO_offset = 3.3/2;

%ADC scale and offset
 DSP_ADC_scale = [1/I2_AO_scale 1/Vo_AO_scale];
DSP_ADC_offset = [-I2_AO_offset/I2_AO_scale Vo_AO_offset];
```

The PI regulator parameters are Kp = 0.11173*0.015, Ki = 0.11173. After designing the both SPS and DPS model, the DSP PINs has to be initialized. The initialization code is shown in Annexure 2 and Annexure 3 for both controllers. The parameters considered to design both SPS and DPS models are:

Table 10. Parameters to design the SPS and DPS models.

Parameter	Value
Input Voltage[V]	800
Output Voltage[V]	500
Leakage Inductance[μH]	45
Output Capacitance[μF]	320
Transformer turns ratio 'n'	1:1
Resistive Load[Ω]	26

5.3. Hardware-In-The-Loop Results

We know that the maximum step size of the RT box is 1μs. Therefore, in SPS control, the 2μs sampling time has been chosen to implement the plant into the RT box. Since the plant and the controller have been split into two, it is advisable to reduce the sampling frequency of the controller to reduce the stress on the DSP board. In general, the switching frequency of a plant can be used as a control frequency of the controller. But that's not enough to reduce the burden on the DSP. In the SPS design, the controller frequency is implemented five times lower than the switching frequency of the plant. But we make sure that the PWM block generates the pulses at the actual switching frequency. The table below shows the sampling frequency and switching frequency used in SPS control.

Table 11. Sampling and Switching frequency of SPS model.

Subsystem	Sampling frequency	Switching frequency
Plant	500kHz	100kHz
Controller	20kHz	

Since the RT box doesn't support the 1MHz sampling frequency, the 500kHz sampling frequency is used with the 100kHz switching frequency. Yes, with DSP, we can achieve a 100kHz switching frequency in the SPS control model. That's an outstanding outcome from this thesis. Fig 53 shows the output voltage of the SPS control from the real-time simulation using a 100kHz switching frequency.

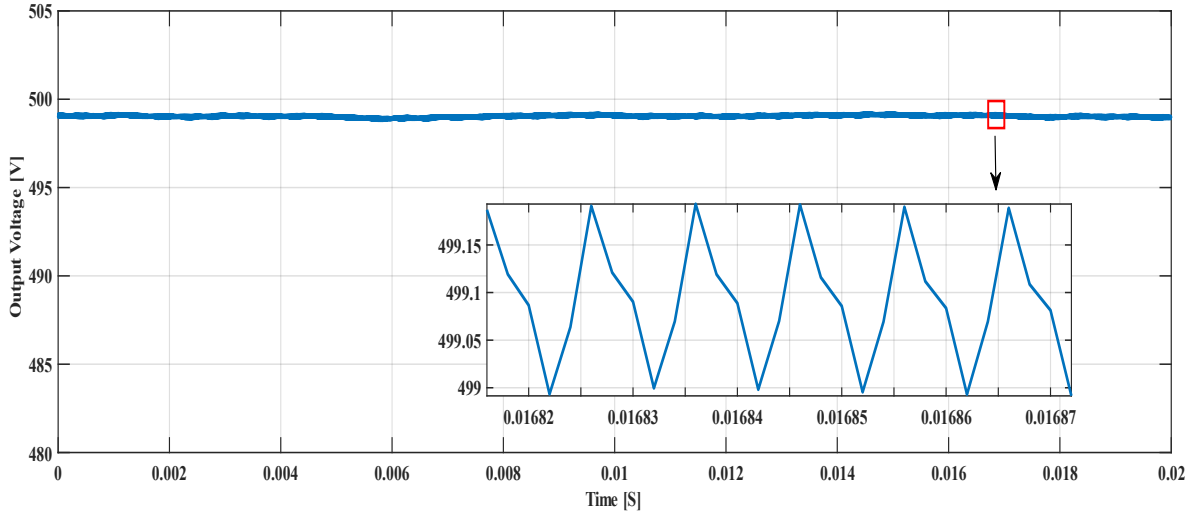

Fig. 53. The output voltage of SPS control with 100khz switching frequency.

Similarly, in the DPS model, the controller frequency is implemented five times lower than the switching frequency of the plant. Hence, the pulses are generated at the desired switching frequency, but the different discretization step sizes execute the controller. Moreover, due to the introduction of an inner phase shift ratio, the complexity of the controller has increased, making the design challenge to achieve a 100kHz switching frequency. Table 12 below shows the achievable switching and sampling frequencies for the designed model.

Table 12. Sampling and Switching frequency of DPS model.

Subsystem	Sampling frequency	Switching frequency
Plant	400kHz	80kHz
Controller	16kHz	

Due to the complexity of the DPS model, the maximum switching frequency that can be achieved without errors is 80kHz. And the sampling frequency at which the controller is executed is 16kHz. The output voltage of this model from the real-time simulation result is shown in the figure below.

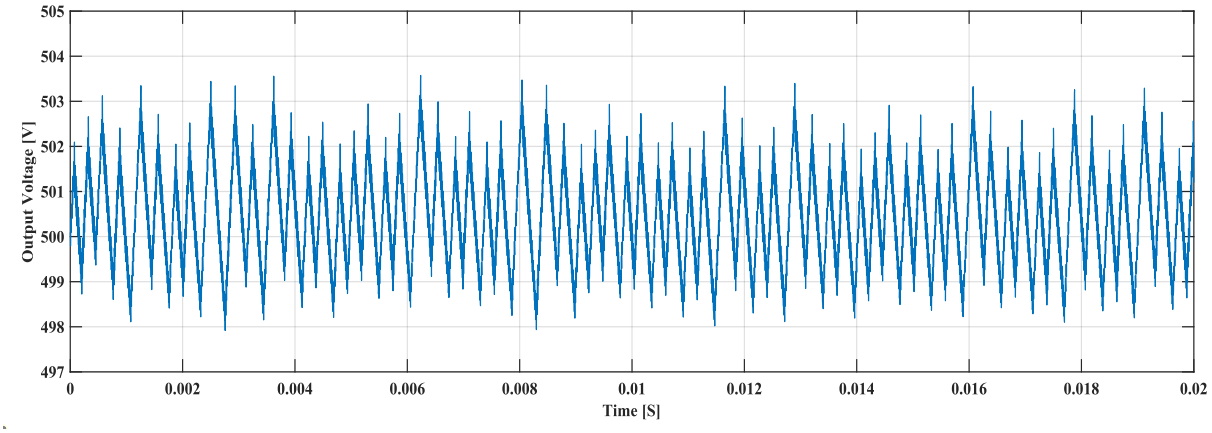

Fig. 54. The output voltage of DPS control with 80kHz switching frequency

In fig 54, the output voltage has more significant ripples than others. The output voltage with the 50kHz switching frequency also looks similar to fig 54. This could be due to many reasons; for example, using C-Script in a DSP is not feasible. But, the percentage error in the ripples is <1%, which is at an acceptable range.

Conclusion

This thesis aims to understand the different Isolated DC-DC converters used in Electric vehicle chargers. After the literature review, one topology has been selected for this work, i.e., a Dual Active Bridge converter, which allows a bidirectional power flow from vehicle to grid and grid to vehicle.

The first chapters of the thesis include studying the Dual Active Bridge converter and understanding the converter's different control schemes. The four primary control schemes are Single-phase shift, Dual-phase shift, Extended-phase shift, and Triple-phase shift control. Even though there are four control schemes, the research mainly focuses on the two first control schemes: Single-phase shift and Dual-phase shift control schemes. Chapter 3 explains the comparison between both control methods and concludes that the DPS control is better than the SPS control in some aspects like reducing circulating currents, reducing the output capacitance size, and reducing power losses. The entire simulations are carried out in PLECS (a simulation tool for power electronics). Once offline simulations are completed, the control schemes are implemented in the Hardware-In-The-Loop (HIL) to determine the converter behavior in real-time.

Chapter 4 discussed the achievable switching frequency and sampling frequency in both designs. To implement the HIL, RT-Box from Plexim has been used. The SPS and DPS models are designed to deploy the converter and its controller into the RT box. The consequences of this experiment are a bit disappointing as the designs are withstanding only a 50kHz maximum switching frequency. At the end of this chapter, using a 50kHz switching frequency in both controls proved that there exists some similarity between the output voltages with different sampling frequencies by calculating RMSE, obtained from the offline simulations

The dissatisfaction in chapter 4 leads to chapter 5. In this chapter, the converter model and controller implementation are separated: the former is executed in the RT box and the latter in a Digital Signal Processor (DSP) of Texas Instrument TI2806x. The implementation of the control in the DSP reduces the stress on the RT box, leading to a higher converter switching frequency. In particular, the SPS model results are obtained using DSP and RT box with a 100kHz switching frequency, whereas the DPS model achieved an 80kHz switching frequency. The final result of the thesis has been the study of different solutions to achieve the best performance of the real-time converter emulation and then provide the corresponding hardware in the loop results by employing both single-phase and double-phase shift.

Annexure 1

The current stress algorithm is developed in PLECS using the reference [28]**.** Taking the output current and output voltage of the converter as feedback signals, the power transmission 'P_o' (13) and voltage conversion ratio 'K ' (14) is calculated and used as the initial parameters for the C99 code, whereas D1ref is the inner phase shift ratio obtained as an output from the C script block. The code declaration and the output function code is as follows:

```
1   #include<math.h>
2   #define po InputSignal(0,0)
3   #define k InputSignal(0,1)
4   #define D1ref OutputSignal(0,0)
5   if ((0<=po) && (po<0.5))
6    {
7    if ((1<=k) && (k<3/(1+sqrt(4-6*po))))
8   {
9   D1ref= (k-1)*(sqrt(1-po))/(sqrt(2*((k-1)*(k-1)+2)))
10  }
11  else
12  {
13 D1ref=1-(sqrt((k-1)*po))/(sqrt(2*(k+3)))-(2*po)*(1/sqrt(2*(k-1)*(k+3)*po));
14  }
15  }
16  else
17   {
18    if((0.5<=po) && (po<0.67))
19    {
20    if((3/(1+sqrt(4-6*po))<=k) && (k<3))
21   {
22   D1ref=1-(sqrt((k-1)*po))/(sqrt(2*(k+3)))-(2*po)*(1/sqrt(2*(k-1)*(k+3)*po));
23    }
24  else
25  {
26  if((3<=k) && (k<3/(1-sqrt(4-6*po))))
27  {
28  D1ref=1-(sqrt((k-1)*po))/(sqrt(2*(k+3)))-(2*po)*(1/sqrt(2*(k-1)*(k+3)*po));
29   }
30   else
31  {
32  D1ref= (k-1)*(sqrt(1-po))/(sqrt(2*((k-1)*(k-1)+2)));
33   }
34   }
35  }
36  else
37  {
38  D1ref= (k-1)*(sqrt(1-po))/(sqrt(2*((k-1)*(k-1)+2)));
39   }
40   }
```

Annexure 2

Initializing the DSP PINs in the SPS control model:

```
1       type_evm = 'TI2806x';          % TI2806x Piccolo Launchpad

% Configure I/O based on processor

2       switch (type_evm)

3       case 'TI2806x'

% Configuration for TI2806x

%% RTBox settings

4       PWM_capture_1_channels = [0 1 2 3];

5       DI_RTBox_Eni = 29; % Global enable emulated by sliding switch 29

6       DO_RTBox_Eno = 4; % Global enable DO

%% DSP settings

7       DSP_ADC_channels = [7] ;  % for output voltage

8       otherwise

9       error('Unknown evaluation module selection, please choose ''TI2806x''')

10      end
```

Annexure 3

Initializing the DSP PINs in the DPS control model:

```
type_evm = 'TI2806x';       % TI2806x Piccolo Launchpad

% Configure I/O based on processor

switch (type_evm)

case 'TI2806x'

% Configuration for TI2806x

%% RTBox settings

PWM_capture_1_channels = [0 1 2 3];

PWM_capture_3_channels = [16 17 18 19];

DI_RTBox_Eni = 29; % Global enable emulated by sliding switch 29

DO_RTBox_Eno = 4; % Global enable DO

%% DSP settings

DSP_ADC_channels = [7 9]; % for output current and output voltage

Otherwise

error('Unknown evaluation module selection, please choose ''TI2806x''')

end
```

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