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Defect analysis in directionally solidified multicrystalline silicon

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Abstract

This project studies how the microstructure and the concentration of metallic impurities affect the electrical properties of multicrystalline silicon wafers, to improve the efficiency and the production yield of photovoltaic solar cells.

Dislocations and impurities in silicon act as recombination centres that reduce free carrier lifetime and thus efficiency of solar cells. Nowadays, the photovoltaic industry can improve the quality of the material by controlling the initial growth conditions and performing repeated Directional Solidifications to segregate impurities. It is known that the geometry of grain boundaries at the bottom is related to the dislocation density in the ingot, but it is not well understood how these phenomena are linked. Finding optimal starting conditions for the solidification and a threshold value for the contamination that does not compromise the device efficiency can improve the production of photovoltaic devices.

Two sets of multicrystalline p-type silicon wafers located at different heights and different lateral positions of two directionally solidified ingots, one contaminated with iron and one with aluminum, were characterized with Electron Backscatter Diffraction, Conductive Atomic Force Microscopy and Microwave Photoconductance Decay, the concentration of carriers was estimated with a Mott-Schottky analysis after evaporation of aluminum contacts, while the contamination level was estimated with the Scheil's equation.

The two ingots show similar microstructure, grain size distribution, and density of coherent grain boundaries. The top of the iron contaminated ingot has a significantly lower lifetime, as it contains more dislocation clusters decorated with segregated iron. Aluminum is less detrimental at this low concentration level and it is more homogeneously distributed along the ingot height. The electrical characterization of the Al/Si Schottky diodes, consisting in current-voltage and capacitance-voltage measurements, confirmed the p-type nature of the samples and estimated a free charge carrier concentration in agreement with the doping level used during the ingot growth. Current profiles measured across decorated grain boundaries and local I-V curves on the grain and on the boundary show that grain boundaries are a preferential path for electrical conduction compared to the grain regions. This effect is more evident if the grain boundaries are decorated with segregated impurities, in particular iron precipitates, that were seen to affect more heavily the electrical properties of the wafer compared to aluminum

precipitates. The shape of the current profile at the boundary was justified with a theoretical model that assumes a redistribution of charge density due to a Coulombic potential introduced by a spherical and positively charged precipitate, that can be identified with β-$FeSi_2$.

A structural characterization, for example through X-ray diffraction, could confirm this result, and a compositional analysis, e.g. Glow Discharge Mass Spectrometry, would complete the characterization of these set of samples by measuring the actual contamination level along the ingot height, that was just estimated with the Scheil's equation. The results from this extensive characterization clearly show that metallic contamination at grain boundaries in Si is responsible for enhanced free carrier recombination and thus photovoltaic conversion efficiency reduction in multicrystalline Si cells.

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List of Abbreviations and Symbols

A^*	Richardson's constant
AFM	Atomic Force Microscope
α	fit parameter
b	Burgers vector
β	fit parameter
c	hole density concentration parameter
C	capacitance per unit area
C_0	initial impurity concentration
C_L	impurity concentration in the liquid phase
C_S	impurity concentration in the liquid phase
C$-$AFM	Conductive Atomic Force Microscope
CCD	Charge-Couple Device
CI	Confidence Index
c$-$Si	crystalline silicon
CSL	Coincident Site Lattice
γ	fit parameter
χ_{sc}	semiconductor electron affinity
D_n	electron diffusion coefficient
D_p	hole diffusion coefficient
δ	distance from growing interface during directional solidification

DLTS	Deep Level Transient Spectroscopy
DS	Directional Solidification
e	electron charge
EBSD	Electron Backscatter Diffraction
E_C	conduction band energy
$E_{F,m}$	metal Fermi level
$E_{F,m}$	semiconductor Fermi level
E_g	energy bandgap
EPR	electron paramagnetic resonance
E_t	trap energy level
E_V	valence band energy
E_{vac}	vacuum level
ϵ_s	static dielectric constant
f	solidified fraction
F	precipitate Coulombic potential
ϕ_B	Schottky barrier
GB	Grain Boundary
GDMS	Glow Discharge Mass Spectrometry
h	Planck's constant
I	current
I_s	saturation current
j	total current density
$j_{s\rightarrow m}$	current density from semiconductor to metal
j_s	saturation current density
k_{Al}	segregation coefficient of aluminum in silicon
k_B	Boltzmann constant

k_{eff}	effective segregation coefficient
k_{eq}	equilibrium segregation coefficient
k_{Fe}	segregation coefficient of iron in silicon
m^*	effective mass
mc−Si	multicrystalline silicon
MG	Metallurgical Grade
μ_p	hole mobility
μ−PCD	Microwave Photoconductance Decay
n	ideality factor
N_D	doping donor concentration
N_t	trap states density
OIM	Orientation Image Micrograph
p	hole density
p_0	hole density inside the grain
PVC	Photovoltaic Cell
Q	precipitate charge
R	distance between tip and precipitate
R_p	precipitate radius
r_{tip}	C-AFM tip radius
RAGB	Random Angle Grain Boundary
ρ	charge density
ρ_d	dislocation density
ρ_{prec}	precipitate carrier density
SEM	Scanning Electron Microscope
Σ	character of a grain boundary
σ	charge per unit area

σ_p	hole conductivity
SMU	Source Measure Unit
SoG	Solar Grade
T	absolute temperature
t	wafer thickness
t	dislocation line
τ	average relaxation time
τ_{bulk}	bulk lifetime
τ_{eff}	effective lifetime
τ_{n_0}	electron lifetime
θ	misorientation angle in grain boundaries
v	average carrier velocity
v_g	growth velocity
v_{th}	carrier thermal velocity
V	voltage
V_{bi}	built-in potential
V_{ext}	applied external voltage
V_{sample}	potential difference between tip and sample
V_z	fluid velocity parallel to the growth direction
w	depletion layer width
W_m	metal work function
XRD	X-Ray Diffraction
1GEN	first generation

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Chapter 1

Introduction

In the recent years, first generation (1GEN) photovoltaic cell (PVC) devices have greatly improved and become one of the best sustainable source of energy, but, even if the efficiencies are reasonably high, microstructural defects and atomic impurities are still severely limiting the performance of the devices. The 1GEN covers approximately 90% of the current PVC market [1], and comprises devices based on monocrystalline silicon (c-Si) and multicrystalline silicon (mc-Si). Silicon is a good candidate for PVC production because of its abundance in the earth's crust (28%) [2], its stability and non-toxicity, and its compatibility with the Si-based microelectronics industry. The c-Si technology can reach efficiencies of the order of 26% [3], but has a high production cost, mainly because of the required high purity, high energy consumption and tightly controlled temperature conditions. On the contrary, mc-Si, that consists of small randomly oriented Si crystals, comes with several advantages compared to c-Si: less energy and less associated greenhouse effects are involved during the production.

As of 2019, the efficiency of mc-Si devices is still significantly lower, with the latest reached maximum value of 22% [3], mainly due to the presence of grain boundaries and the higher concentration of impurities. These crystal defects act as recombination center in the cell: the precipitates can straddle the p-n junction and present a short-circuit, therefore there is an incomplete carrier collection in the device that result in a lower current [4].

The microstructure of mc-Si is related to the electrical properties, because grain boundaries (GBs), given by the misorientation of the different grains, are responsible of the formation of dislocations, crystallographic defects that act as recombination centers and affect the lifetime of minority carriers. In mc-Si, dislocations clusters mainly originate from Coincident Lattice Sites (CLS) boundaries,

especially the $\Sigma 27$ boundary can originate stress concentrators, such as kinks or steps. Also, Random Angle Grain Boundaries (RAGBs) are able to better release the global thermal stress by acting like "dislocation sinks" and this could cause less dislocation nucleation and less movement. It seems it is important to study the type and density of grain boundaries, as the generation/annihilation of dislocations is related to the grain boundary geometry and to the conditions at the very beginning of the ingot growth.

Iron and aluminum are two of the most common and pervasive impurities in silicon and they can be introduced by the feedstock or by the crucible. Their presence in the silicon ingot is really detrimental to the electrical properties, as they introduce deep states in the energy bandgap, which increase the recombination rate [5, 6].

At the moment, it is possible to increase the efficiency of a mc-Si solar cell by improving the refining during the solidification process. Usually, mc-Si is solidified in a furnace with Directional Solidification (DS), a particular technique in which the silicon melt starts to solidify from the bottom, where the process of heat extraction is more rapid, to the top. An improved control of the microstructure can be obtained by favoring the initial conditions for the growth of the silicon ingot: therefore, studying the bottom of mc-Si ingots can help to improve the overall quality of the ingot [7]. Another process that occurs during the solidification is the segregation of impurities, that will tend to stay in the liquid phase, rather than in the solid one. These refining processes need to be done several times to have repeated segregations and to reach a good purity of the material, called Solar Grade silicon (SoG-Si).

This thesis presents a study of the effect of the microstructure and of the concentration of metallic impurities in multicrystalline silicon on the electrical properties of a mc-Si wafer, with the purpose of improving the quality and the efficiency of industrial photovoltaic devices.

Several different wafers coming from different heights of two industrially produced ingots, one contaminated with iron and one with aluminum, were analysed. The microstructure was studied with Electron Backscatter Diffraction (EBSD) and the impurity concentration was calculated through the Scheil's equation. The electrical properties were studied with different techniques: lifetime maps were measured with Microwave Photoconductance Decay (μ-PCD), the doping concentration was estimated with a Mott-Schottky analysis of the wafers after evaporating aluminum contacts, and the electrical activity of decorated grain boundaries was studied with Conductive Atomic Force Microscopy (C-AFM).

The thesis is structured as follows: chapter 2 contains a description of the

crystallographic defects relevant to this study (grain boundaries, dislocations and metallic impurities), the Directional Solidification, the impurity segregation mechanism according to the Scheil's model, and the metal-semiconductor junction; the characterization techniques are described in chapter 3; chapter 4 reports the main properties of the samples and the experimental details of the characterization; chapter 5 shows the experimental results and the discussion of the results.

Chapter 2

Defects in multicrystalline silicon

All real crystals contain imperfections, that introduce disorder and destroy the lattice regularity. There is a large variety of defects and they determine the electronic properties of semiconductors: some of them are responsible for carrier recombination, others trap carriers and influence the space charge that determines the carrier transport. Depending on their dimensionality, defects can be distinguished in point, line, planar, or volume defects [8]. The following sections will describe microstructural defects, such as grain boundaries, dislocations and impurities, in particular iron and aluminum. After that, segregation of impurities and Directional Solidification are described. Finally, the effect of these defects on the properties of a solar cell is explained.

2.1 Point defects

Point defects are the main class of defects that act as donors or acceptors, or, when their energy levels are farther separated from the bands, as traps or recombination centers. They are generally described by the Kröger-Vink notation [9], that takes the general form

$$M_S^C \tag{2.1}$$

where M indicates the species, that can be atoms (e.g. Si, Fe, O), vacancies (V), interstitials (I), electrons (e), holes (h); S indicates the lattice site that the species occupies; C is the electric charge of the species relative to the site that it occupies.

Many different types of points defects can be distinguished, but, for the purpose of this thesis, only impurities will be considered. Impurity atoms in a crystal

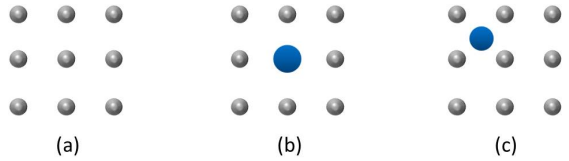

Figure 2.1: (a) parent matrix; (b) substitutional impurity; (c) interstitial impurity.

can be considered as extrinsic point defects and they affect the physical and mechanical properties of all materials. As shown in Figure 2.1, they can take two different sites in a crystal: (a) substitutional, in which an atom of the parent lattice is replaced by the impurity, and (b) interstitial, in which the impurity atom is at a non-lattice site. All the point defects produce a local distortion of the perfect crystal and the distortion depends on the size of the atoms introduced and on the space between the host atoms [8].

2.2 Grain boundaries

A grain is a three dimensional crystalline volume within a specimen that differs in crystallographic orientation from its surroundings but internally has little variation. Multicrystalline silicon is composed of randomly oriented grains separated by planar defects called grain boundaries (GBs). The atomic arrangement varies with the angle misorientation θ between the different crystals. The region of disorder is very narrow and contains only one or two atoms on each side of the boundary [8].

If there is a small difference in orientation, therefore a small angle θ, the grain boundary can be described as a set of dislocations. There exist two different type of low angle GBs, shown in Figure 2.2: in a *tilt* boundary the misorientation is around an axis parallel to the boundary, while a *twist* boundary is characterized by an angle θ around an axis normal to the boundary.

When the misorientation between two grain exceeds 10-15°, the dislocation spacing is so small that the dislocation cores overlap. *Twin boundaries* are special angle boundaries between two identical crystallites and the least disturbed boundary is that of a stacking fault. A particular type of high angle GBs, the *coincident site lattice (CSL) boundary*, has a finite ratio of lattice sites that coincide between the two lattices, resulting in a lower associated energy. A Σ-value is called character of the grain boundary and it describes the reciprocal density of the coincident

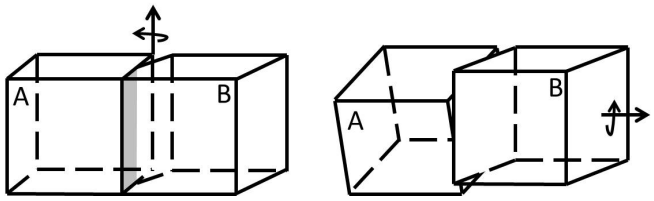

Figure 2.2: Low-angle tilt (left) and twist (right) boundary.

Σ-value	**Angle [°]**	**Axis direction**
3	60	[111]
9	38.9	[110]
27a	35.4	[210]
27b	31.5	[110]

Table 2.1: CSL boundaries parameters.

sites: for example, in a $\Sigma 3$ boundary, one out of every three sites is shared by the two lattices. Every Σ-value can be associated to a particular misorientation angle around an axis.

The CSL boundary $\Sigma 3$ is the most common GB in mc-Si, followed by other $\Sigma 3^n$ orientations, like $\Sigma 9$ or $\Sigma 27$, and Random Angle Grain Boundaries (RAGBs), without a special coincidence orientation [10]. Table 2.1 shows misorientation angle and direction of the most common CSL boundaries in mc-Si [11].

2.3 Dislocations

Dislocations are a particular type of one-dimensional line defect that was first theorized to explain the large disagreement between the theoretical shear stress and the actual shear stress that can be applied to crystals: they play a special role in the mechanical properties of a crystal, in particular the possibility to deform it plastically [8].

Dislocations act as sites of carrier recombination in semiconductors, therefore affecting the performance of a solar cell, in particular there is a degradation of the effective bulk lifetime as the dislocation density increases [12]. Additional degradation occurs when dislocations are decorated with impurities [13]. A typical parameter used to describe the microstructure of a material is the dislocation density ρ_d, defined as the number of dislocations per unit area.

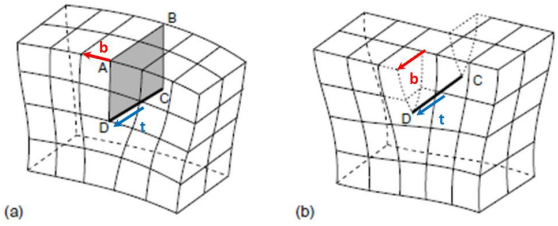

Figure 2.3: (a) Model of an edge dislocation DC, with Burgers vector **b** perpendicular to the displacement line **t**; (b) Model of a screw dislocation DC, with Burgers vector **b** parallel to the displacement line **t**. Modified from [8].

In principle, the reduction of dislocation densities from 10^6-10^8cm^{-2} to as low as 10^3-10^4cm^{-2} may lead to an improvement in the cell performance (from 13-14% to $\geq$20%) [13]. It is therefore necessary to understand the dislocation generation and motion, in order to suppress their formation during crystal growth and to remove them after the ingot growth.

Dislocations are defined by a displacement vector called Burgers vector **b**. Two types of dislocations can be distinguished: an *edge* dislocation has the Burgers vector **b** perpendicular to the dislocation line; a *screw* dislocation has **b** parallel to its dislocation line. The basic geometry of edge and screw dislocations is shown in Figure 2.3. Dislocations are more complex and usually they are a mix between edge and screw dislocations.

2.4 Metallic impurities in mc-Si

The most common contaminants in multicrystalline silicon are metals from the transition group, such as iron and aluminum. These impurity atoms diffuse through interstitial mechanism sufficiently rapidly and are extremely detrimental due to their high generation-recombination activity and their ability to form precipitates [4]. The conversion efficiency of light to electricity in solar cells is strongly affected by metal silicide precipitates with typical sizes in the range of several tens of nanometers, which decrease the minority carrier diffusion length and increase the leakage current [14]. Studying the physical properties of transition metals, their distribution in silicon ingots, and their effects on the wafer properties is fundamental to improve the efficiency of silicon-based devices.

2.4.1 Iron impurities in silicon

It is important to understand the properties of iron and its complexes in silicon, as it is one of the most pervasive metal impurities and it heavily affects the electrical properties of silicon wafers. In crystalline and multicrystalline photovoltaic devices, iron contamination results in the creation of recombination centers which reduce the minority carrier diffusion length, and consequently the solar cell efficiency. Typical iron concentrations in a mc-Si ingot are less than 0.1 ppma [15], and reducing the contamination level can be extremely expensive, therefore it is necessary to understand the mechanisms of iron contamination to find the toleration limits of iron concentration in silicon devices. An extensive summary of the fundamental physical properties of iron complexes in silicon has been published by Istratov *et al.* in 1999 [14].

Transition metals, and iron in particular, have high diffusivity in silicon: iron remains mobile at room temperature and can diffuse quickly at temperatures above 100 °C, making it difficult to establish a coherent experimental picture. Iron diffuses interstitially into silicon at high temperatures, which means that it diffuses among the interstices of the host crystal [16, 17]. This is confirmed by its donor behavior, its high diffusion coefficient and Woodbury and Ludwig's electron paramagnetic resonance (EPR) measurements in 1960 [18]. Unless vacancies are generated by irradiation or implantation, there are no convincing experimental data that suggest the existence of substitutional iron in moderately doped silicon, therefore we can consider iron point defects as just interstitial (Fe_i) [14].

The main effect of interstitial iron in silicon is the introduction of a deep energy state in the forbidden energy gap (E_V + 0.40 eV), where E_V is the valence band edge energy level, strongly affecting the minority carrier lifetime [5]. Reported values of the equilibrium segregation coefficient of iron in silicon are in the range (5-7)$\times 10^{-6}$ [19], and in this thesis an equilibrium segregation coefficient $k_{Fe} = 5 \times 10^{-6}$ is assumed [20].

Iron reach its solubility limit at high temperatures, but, during the cooling, supersaturation is not mantained and rapid interstitial diffusion occurs: atoms can either aggregate and form an intermetallic compound with silicon or be attracted to dislocations, act as a nucleation site and give rise to decorated dislocations [4]. $FeSi_2$ exists in two stable forms according to the Fe-Si phase diagram: α-$FeSi_2$ and β-$FeSi_2$. The α-$FeSi_2$ is metastable at room temperature and decompose very slowly to β-$FeSi_2$ with a transition temperature of 982°C [21]. Cubic γ-$FeSi_2$ has also been reported as a metastable phase that transform into the β phase beyond a certain size [22].

Iron-boron pairs formation At room temperature, Fe_i is predominantly positive and paired with boron in p-type silicon. When the temperatures are above 100 to 200 °C the pairs dissociate and there is an increase in the concentration of Fe_i^+, while above 600 K iron becomes mostly neutral. The available data suggest that most of the iron is neutral even at temperatures of 1100 °C [23].

Experimental evidence of pairing of iron with group III acceptor atoms, forming complexes in silicon, were first suggested by EPR measurements. Pairing between the substitutional acceptors, like (B_S^-) in p-type silicon, and the interstitial iron (Fe_i^+) is caused by the Coulombic attraction between the ionized impurities [24]. The donor energy level of the pair $(FeB)^{0/+}$ has been found at E_V + 110meV, while the acceptor level $(FeB)^-$ is in the upper half of the bandgap at E_C - 290meV, where E_C is the conduction band edge energy level [24, 25]. Both interstitial iron and FeB pairs are strong recombination centers, but the recombination activity of FeB pairs at low injection levels is about 10 times lower than of interstitial iron. Recombination takes place via the acceptor state, as it is closer to the midgap than the donor level of the pair [25].

2.4.2 Aluminum impurities in silicon

Aluminum impurities shorten the lifetime of excited carriers and therefore disturb the electric generation. Usually directional solidification has a little effect on removing Al from molten silicon, due to its high segregation coefficient, and evaporation from the melt surface is also needed for a good removal [26]. As this is one of the most common impurities in metallurgical grade silicon (MG-Si), with typical concentration levels of 0.5-2 ppma [15], in the recent years the techniques of aluminum removal have been extensively studied and significant progress have been made [26, 27, 28, 29].

Aluminum segregation coefficient is k_{Al} = 0.002 [20], which is insufficiently small to satisfy purity requirements (0.1 ppmw) after the primary directional solidification, so repeated directional solidifications are needed [28]. Aluminum features a shallow acceptor level at E_V + 0.057 eV, making it a good dopant for p-type silicon [5]. Aluminum also exhibits a deep energy level in the silicon band gap, located at E_V + (0.44 $\pm$ 0.02) eV [6].

2.5 Effect of defects on semiconductor properties

In a real semiconductor at finite temperatures, impurities, phonons and defects will contribute to scattering. There is a wide variety of factors affecting the electrical properties of mc-Si, so it is difficult to determine the recombination properties of individual defects in order to identify the most detrimental ones. In the relaxation-time approximation it is assumed that the probability for a scattering event, similar to friction, is proportional to the (average) carrier velocity. The average relaxation time τ is introduced via an additional term that sums up all the scattering events $\frac{d\mathbf{v}}{dt} = -\frac{\mathbf{v}}{\tau}$, where $\mathbf{v}$ is the average carrier velocity [30].

Semiconductors in thermodynamic non-equilibrium can have excess charges, created, for example, by the absorption of light with frequency higher than the bandgap. After the excitation is turned off, the carriers will relax to a lower energy state through a process called *recombination*.

Band-band recombination consists in the relaxation of an electron from the bottom of the conduction band E_C to the top of the valence band E_V. The band-band transitions, shown in Figure 2.4, are usually coupled with the emission or absorption of a photon of energy $h\nu$ equal to the energy bandgap E_g.

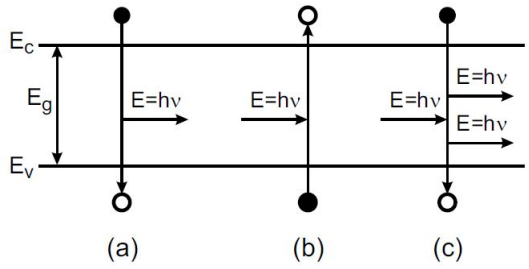

Figure 2.4: Band-band transitions from an occupied (full circle) to an unoccupied (empty circle) electron state: (a) spontaneous emission, (b) absorption, and (c) stimulated emission [30].

Another recombination mechanism in a semiconductor is linked to the presence of impurities, that introduce energy levels in the bandgap, called *electron traps* (Figure 2.5) [30]. Electron traps are defined by an energy level E_t that is related to the recombination rate of minority carriers. Capture of carriers by the trap states leads to an exponential decay of the carrier density with lifetime τ_{n_0} (for a p-type material)

$$\tau_{n_0} = (\sigma_p v_{th} N_t)^{-1} \tag{2.2}$$

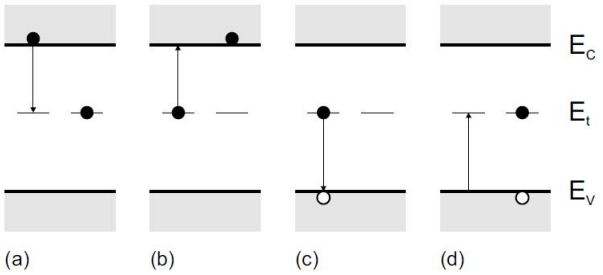

Figure 2.5: Band-impurity transitions (*left*: initial, *right*: final state): (a) electron capture from conduction band, (b) electron emission into conduction band, (c) hole capture from valence band, (d) hole emission into valence band [30].

where σ_p is the hole conductivity, v_{th} is the thermal velocity of the carriers, and N_t is the density of trap states. A recombination center is most effective when it is close to the middle of the bandgap [30].

There exist two major classes of point defects: the shallow and deep level defects. Impurities that result in shallow levels have a hydrogen-like defect level spectrum, modified only by the dielectric constant and the effective mass of the host semiconductor, that provides the key for an unambiguous identification with respect to their specific incorporation within the host lattice. Shallow defect centers play a dominant role as donors and acceptors in semiconducting devices.

Deep level centers are often closer to the center of the band gap than to one of the edges and they are created from defect centers with tight-binding potential and provide a preferred path for carrier recombination or act as deep traps. Transition metals, like iron, are highly recombination active in silicon and form carrier recombination centers in the bandgap, degrading the solar cell performance. The impurity-induced performance loss is primarily due to a reduction in the diffusion length, which is even more effective when the atoms form clusters or precipitate at the grain boundaries [19]. Each impurity shows a particular energy level or energy levels characterized by their energy, density and capture cross-sections for holes or electrons. The fraction of impurity that is electrically active varies with the metal species, so the material thermal history strongly influences the final efficiency [31]. The efficiency of a solar cell is related to the metal concentration: the curve depicted in Figure 2.6 shows the results of an analysis conducted on nearly 200 p-type wafers with a resistivity of 4 Ωcm processed into solar cells [19].

Grain Boundaries are electrically active defects that can affect the performance of solar cells, with the introduction of deep levels that act as recombination cen-

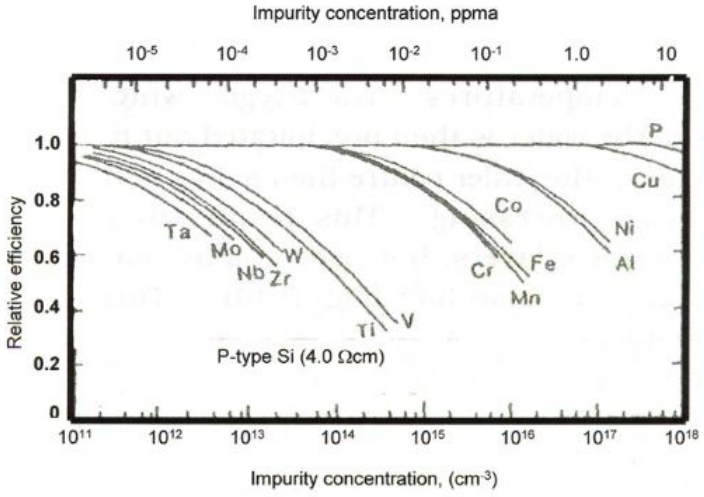

Figure 2.6: Solar cell relative efficiency versus impurity concentration for 4 Ωcm p-doped devices [19].

ters. The recombination activity depends on the character and on the coherency degree of the boundary [32]. Small angle grain boundaries also have higher recombination rates than large angle recombination boundaries [32]. Metal decoration is another factor that enhance the electrical activity of a grain boundary: single impurity atoms introduce deep levels in the bandgap [33], and the nucleation and coarsening of bigger metallic precipitates at the grain boundary introduce a metal-like density of states and an internal metal-semiconductor junction with a space charge region that determines the capture rate and recombination of the carriers.

Furthermore, dislocations clusters mainly originate in mc-Si from CSL boundaries [34]: the $\Sigma 27$ boundary is a high energy boundary that can dissociate in a $\Sigma 3$ and an asymmetric $\Sigma 9$ boundaries and it has been observed that dislocations are produced at the junction between a symmetric and asymmetric $\Sigma 9$ boundary [35]. $\Sigma 27$ can also originate stress concentrators, such as kinks or steps, which develop during crystallization and introduce more dislocations along the ingot [35].

It has also been observed that individual dislocations terminate at RAGBs between the grains, so dislocation density can decrease when the presence of these dislocation sinks increases. Also, RAGBs are able to better release the global thermal stress, rather than CSL boundaries, and this could also cause less dislocation nucleation and less movement. Recent studies have also suggested that there is

a high correlation between the ratio of densities of $\Sigma 27$ and RAGBs (dislocation source/sink) at the bottom of the wafer and the dislocation density at the top of the wafer [36].

2.6 Segregation of impurities

During crystallization the impurities tend to segregate into the liquid, leaving the solid with a higher degree of purity. Segregation of impurities is a common refining process for impurity removal in the production of photovoltaic devices. The impurity distribution is not homogeneous and depend on the conditions of crystal growth, and, since a definite amount of time is needed to reach a uniform distribution, it is not possible to reach true equilibrium in the system. It is convenient to define the equilibrium segregation coefficient, k_{eq}, that describe the segregation of impurities in silicon

$$k_{eq} = \frac{C_S}{C_L} \tag{2.3}$$

where C_S is the impurity concentration in the silicon crystal and C_L is the impurity concentration in the molten silicon [37].

If crystallization is not enough slow, the segregation of solute atoms happens at a greater rate than they can diffuse into the melt, so a concentration gradient forms ahead of the advancing crystal. This enriched region directly determines the rate of solute incorporation into the solid. BPS theory (from Burton, Prim and Slichter) provides a one-dimensional solute segregation model, by considering melt convection as a factor influencing segregation during crystal growth, and ignoring any solute transport in directions which are lateral to the crystal-melt interface [37]

In a region of the melt enough close to the crystal, the principal transport of solute away from the interface occurs by diffusion. It can be assumed that the fluid flow is laminar, given by a continual rotation of the melt during the crystallization process. Solute concentration is found to be virtually uniform in the radial direction (perpendicular to the growth direction). Since the fluid is also incompressible, the continuity equation expressing the conservation of solute atoms in the melt is

$$D\frac{d^2C}{dz^2} - V_z\frac{dC}{dz} = 0 \tag{2.4}$$

where V_z is the sum between the component of the fluid velocity parallel to the growth direction and the growth velocity v_g (positive for growth and negative for

melting).

We can then assume that beyond a distance δ from the growing interface, the concentration becomes uniformly $C(\delta) = C_L$, while within δ the flow velocity is given just by v_g. Eq. 2.4 becomes

$$D\frac{d^2C}{dz^2} - v_g\frac{dC}{dz} = 0 \tag{2.5}$$

and the new boundary condition for the concentration profile is

$$C(z = \delta) = C_L \tag{2.6}$$

The following solution results for the concentration at the crystal-melt interface

$$C_L^I = C_L + (C_L^I - C_S^I)\left(1 - e^{-\Delta}\right) \tag{2.7}$$

where $\Delta = f\delta/D$ and C_S^I and C_L^I are respectively the melt concentrations of the solid and the liquid at the interface. Equation 2.7 can be changed into

$$1 = \frac{C_L}{C_S^I} - (\frac{C_L^I}{C_S^I} - 1)\left(e^{-\Delta}\right) \tag{2.8}$$

The effective segregation coefficient is defined as $k_{eff} = \frac{C_S^I}{C_L}$ and the equilibrium segregation coefficient becomes $k_{eq} = \frac{C_S^I}{C_L^I}$, then Equation 2.8 takes the form

$$k_{eff} = \frac{k_{eq}}{k_{eq} + (1 - k_{eq})\left(e^{-\Delta}\right)} \tag{2.9}$$

The value of k_{eff} depends strongly on δ, which depends on the convection strength in the molten silicon [37].

During directional solidification growth, the liquid volume decreases while the crystallization progress. The total amount of impurities needs to stay constant and it is always equal to C_0, the starting concentration of an impurity in the molten silicon

$$\int_0^f C_S dx + (1 - f)C_L = C_0 \tag{2.10}$$

where f is the solidified fraction. Considering $C_S = k_{eff}C_L$ and differentiating with respect to f, with $C_L(f = 0) = C_0$ as boundary condition, the following equation is obtained

$$C_S = k_{eff}C_0(1 - f)^{k_{eff}-1} \tag{2.11}$$

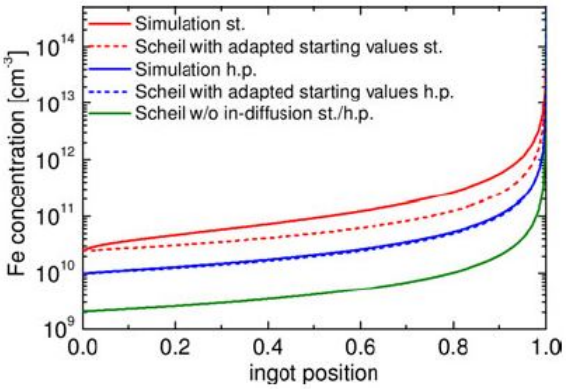

Figure 2.7: Simulation of total iron concentration in crystallized silicon ingot as a function of block height, with in-diffusion from standard crucible (red) and high purity crucible (blue). The dotted lines are profiles calculated from Scheil's equation with a starting impurity concentration that considers diffusion of iron into the melt before crystallization begins [39].

which is called Scheil equation and it describes how the impurity concentration changes along the growth direction [38].

However, even if this equation has been verified experimentally, it might lead to underestimate the concentration of impurities, especially in the case of iron. Impurities can contaminate a silicon block by entering in the melt from the crucible and the coating. This causes a continuous increase of impurity concentration with time. With the assumption of perfect stirring and infinite impurity solubility, a correction term that considers in-diffusion from crucible and coating can be introduced, by calculating the rate of atoms entering the melt per crucible area as a function of time $\mathrm{Fe}_{crucible}(t)$ [39]. Figure 2.7 shows a simulation of total iron concentration in the crystallized silicon ingot as a function of the block height. It is possible to see that the normal Scheil's distribution, without in-diffusion correction, is underestimating the iron concentration compared to the case that considers iron contamination given by a standard crucible or a high purity crucible [39].

2.7 Ingot growth

The Directional Solidification (DS) System is one of the most used methods for mc-Si ingots growth, and is suitable for the practical removal of most impuri-

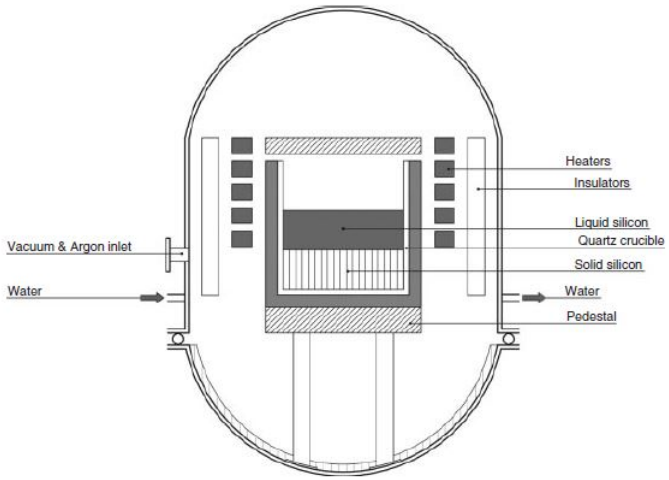

Figure 2.8: Schematic view of a directional solidification furnace [20].

ties. This technique is a lower cost alternative to the Czochralski process, used to grow monocrystalline silicon, and can ensure high-quality output, large, columnar grains parallel to the growth direction and up to 800 kg charges of virgin policrystalline silicon [20].

Figure 2.8 shows a typical commercial furnace. In this system, the production is carried out by melting a charge of high-quality policrystalline silicon in a quartz crucible with an inner coat of silicon nitride to avoid well wetting. Once the melt is homogeneized, the side insulation is moved up, while the crucible is rotating, to ensure complete symmetry in the ingots. The heat is extracted from the bottom of the crucible in order to start the solidification process, with a solidification rates that possibly never exceeds 2 cm/h [20, 40]. The temperature profile during the solidification affects the shape of the solidification interface, the segregation of impurities, the distribution of thermal stresses and the formation of defects.

Numerical simulations for this type of furnace were performed to calculate the global and local temperature distribution and the results are shown in Figure 2.9 [40]. Silicon in the lower half of the ingot is cooler at the sides than in the middle, as the heat is exchanged through radiation. As there are heat leaks from the crucible walls, the temperature gradients make the crystallization not perfectly directional. The isothermal lines change the contour throughout the height of the ingot: they are less concave during later phases of growth and can become double curved or cusped close to the top. Their shape is also related to impurities removal,

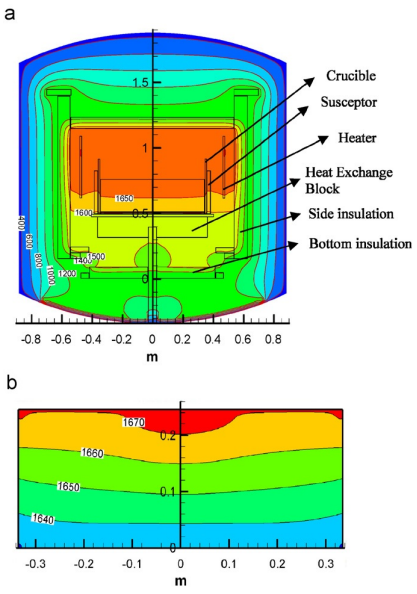

Figure 2.9: (a) Simulation results of global temperature distribution of DSS; (b) local temperature distribution of DSS ingot [40].

as during solidification they are pushed away from the crystal due to their small segregation coefficients, but some impurities can be trapped in the middle of the ingot because of the double-curved shape [40].

2.8 Metal-Semiconductor junctions

A metal is characterized by the work function $W_m = E_{vac} - E_{F,m} = -e\phi_m$, which is the difference between the vacuum level E_{vac} and the metal Fermi level $E_{F,m}$, while a semiconductor is characterized by its electron affinity χ_{sc}, where $E_{vac} - E_C = -e\chi_{sc}$ is the energy difference between the vacuum level and the conduction band edge.

The position of the semiconductor Fermi level $E_{F,s}$ relative to the vacuum level is generally different from $E_{F,m}$, but when a metal forms a contact with a semiconductor there is a flow of carriers from the semiconductor to the metal, and at the thermodynamic equilibrium the Fermi level is constant throughout the structure. When the distance between a metal and a p-type semiconductor is reduced to zero, a potential barrier, called Schottky barrier, of height $\phi_B = -\frac{E_g}{e} + \phi_m - \chi_{sc}$ forms at the interface.

Between the surface of the metal and the bulk part of the semiconductor a space-charge region due to charge accumulation is formed and there is a potential drop called built-in potential, defined as:

$$V_{bi} = \chi_{sc} + \frac{E_C - E_{F,s}}{e} - \phi_m \tag{2.12}$$

The width w of this space-charge region can be calculated making the so-called *abrupt approximation*, where the charge density ρ in the region ($0 \leq x \leq w$) is given by the doping, i.e. $\rho = eN_D$, while outside this region the semiconductor is neutral, therefore $\rho = 0$

The depletion-layer width is related to the doping concentration N_D, the built-in voltage V_{bi} and the applied external voltage across the diode V_{ext}

$$w = \left[\frac{2\epsilon_s}{eN_D} \left(V_{bi} - V_{ext} - \frac{kT}{e} \right) \right]^{1/2} \tag{2.13}$$

where ϵ_s is the static dielectric constant of the semiconductor, k_B is the Boltzmann constant, and T is the absolute temperature of the semiconductor.

The charge transport across the junction is dominated by the majority charge carriers, so holes in the case of a p-type semiconductor. At high temperatures the main transport mechanism is thermionic emission, which involves carriers with energies above the energy barrier.

The carriers need to have velocities above $(2e(V_{bi} - V_{ext})/m^*)^{1/2}$, with m^* being their effective mass, and the current density is found to be

$$j_{s \to m} = A^* T^2 exp\left(\frac{e\phi_B}{k_B T} \right) exp\left(\frac{eV_{ext}}{nk_B T} \right) \tag{2.14}$$

where n is a dimensionless parameter called ideality factor and A^* is the Richardson constant, that can be expressed as

$$A^* = \frac{4\pi e m^* k_B^2}{h^3} \tag{2.15}$$

where h is the Planck's constant.

By changing the bias, the current from semiconductor to metal increases in the forward direction, as the difference between the quasi-Fermi level and the top of the barrier is reduced and it is easier for the carriers to pass across the barrier.

The current from the metal to the semiconductor is constant, therefore the total current-voltage characteristic is:

$$j = A^* T^2 exp\left(\frac{e\phi_B}{k_B T}\right)\left[exp\left(\frac{eV_{ext}}{nk_B T}\right) - 1\right] = j_s\left[exp\left(\frac{eV_{ext}}{nk_B T}\right) - 1\right] \quad (2.16)$$

where the factor

$$j_s = A^* T^2 exp\left(\frac{e\phi_B}{k_B T}\right) \quad (2.17)$$

is called the saturation current density, from which it is possible to find the energy barrier of the junction. A metal-semiconductor junction acts as a diode that can be polarized depending on the applied bias: in forward bias the current increases exponentially, while in reverse bias it reaches a constant and small value equal to j_s.

When a voltage V_{ext} is applied across the junction, so that it is reverse biased, the metal and the semiconductor accumulate charges and the device acts as a capacitor. The total space charge σ per unit area in the semiconductor is

$$\sigma = eN_D w = \left[2eN_D\epsilon_s\left(V_{bi} - V_{ext} - \frac{k_B T}{e}\right)\right]^{1/2} \quad (2.18)$$

Therefore the capacitance per unit area $C = |dQ/dV|$ in the space charge region is

$$C = \frac{\epsilon_s}{w} = \left[\frac{eN_D\epsilon_s}{2\left(V_{bi} - V_{ext} - \frac{k_B T}{e}\right)}\right]^{1/2}. \quad (2.19)$$

Equation 2.19 can be re-written as

$$\frac{1}{C^2} = \frac{2\left(V_{bi} - V_{ext} - \frac{kT}{e}\right)}{eN_D\epsilon_s} \quad (2.20)$$

showing that, assuming a homogeneous doping concentration, the quantity $1/C^2$ is linearly dependent on the bias voltage. The doping concentration can be estimated from Equation 2.20 as

$$N_D = -\frac{2}{e\epsilon_s}\left[\frac{d}{dV_{ext}}\left(\frac{1}{C^2}\right)\right]^{-1} \quad (2.21)$$

and it is usually plotted versus the depletion layer width to understand the homogeneity of the doping concentration.

Chapter 3

Characterization Techniques

3.1 Electron Backscatter Diffraction

Grain size strongly affects the mechanical, physical, and surface properties, so measuring the grain and sub-grain structures is of great importance. Electron Backscatter Diffraction (EBSD) is a popular technique that is used to quantify microstructure parameters, like grain morphology and crystallographic texture. This technique is based on the acquisition of diffraction patterns from bulk samples in a Scanning Electron Microscope (SEM) [41]. The EBSD system (Figure 3.1) has a Charge-Couple Device (CCD) camera connected to an image processing system for pattern averaging and background subtraction. The sample is tilted at 62.5° from the horizontal, so that the backscattered electrons can reach the EBSD at its operating position. Electrons backscattered from crystalline samples show intricate intensity distributions. Individual incoherent sources produce patterns called Kikuchi patterns, that can be observed straightforward on a phosphor screen positioned close to the sample. EBSD commonly studies the geometry of the Kikuchi bands [42, 43], that is related to the crystal structure and properties such as boundary mobility and diffusivity. Once an EBSD system has been calibrated, it is possible to automatically index the diffraction patterns and calculate the crystal orientation. This is typically accomplished using the following steps:

- The diffraction pattern is transferred from the detector to the EBSD software.
- A Hough transform is used to identify the positions of the Kikuchi bands and the bands are seen as peaks in Hough space.

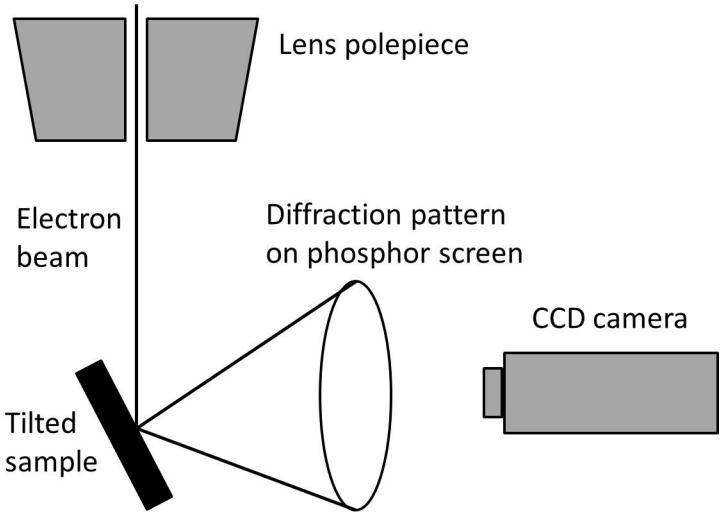

Figure 3.1: Schematic EBSD setup

- Having identified the Kikuchi band positions and from knowing the calibrated geometry, it is possible to calculate the angles between the detected bands.

- The calculated angles are compared with a list of interplanar angles for the analysed structures based on a selected number of reflecting planes (reflectors) in the reference structure.

- The possible solutions are sorted to find the best fit and the orientation matrix is calculated.

An example of indexed diffraction patterns is shown in Figure 3.2 [44].

The sample properties are studied locally and the scanned area is usually called ”orientation map” or ”EBSD map” [41]. The diffraction pattern comes from the surface layer and a good mechanical polish is sufficient in most hard materials.

An ideal scan should contain all the information like grain size, shape and size distribution, micro and macro texture: covering a large area with a larger step size gives more representative results, but small step sizes are good for grain reconstruction and data clean-up; a small scan at very high resolution is not representative of the grain size and shape distribution, and a large high resolution scan will contain all the relevant information, but can take a long time [45, 46].

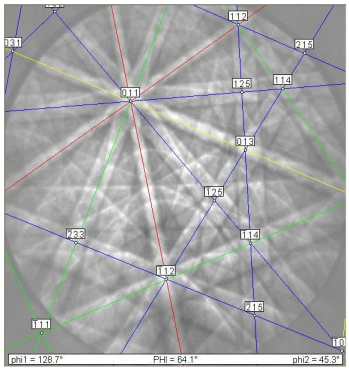

Figure 3.2: Example of EBSD pattern as it comes from the camera via the image processor and automatic indexing of the pattern made by the software [44].

3.2 Microwave Photoconductance Decay

The lifetime of mc-Si wafers is an important parameter to estimate the efficiency of a solar device. Microwave Photoconductance Decay (μ-PCD) is a technique that allows to measure with high resolution lifetime and iron distribution, using a microwave system for optical excitation and signal detection. A microwave has the necessary energy to generate electron-hole pairs close to the front surface (the penetration depth is $\approx$30 μm) and after recombination the concentration of electron-hole pairs decreases along with the conductivity. The power of the reflected microwave is proportional to the conductivity and the reflectivity decays following an exponential curve, which has as time constant the effective lifetime of the carriers.

During and immediately after the excitation, there is a redistribution of free carriers with two parallel processes: bulk recombination and carrier diffusion in the sample surface, with subsequent recombination. The second process has a large influence on the lifetime value, so quantitative measurements would need a passivation of the surface to suppress the recombination process.

As these samples were not passivated, the instrument measures an effective lifetime τ_{eff} that can be expressed as:

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_{bulk}} + D_n \left(\frac{\pi}{t}\right)^2 \tag{3.1}$$

where τ_{bulk} is the bulk lifetime without surface recombination, D_n is the diffusion coefficient and t is the wafer thickness. If the bulk lifetime is small, the first

term will dominate the value of the effective lifetime. As a result, even if these measurements do not give the bulk lifetime, regions of low quality can still be recognized.

3.3 Capacitance-voltage measurements

Capacitance-voltage measurements are used to determine the doping density and other relevant electronic properties of semiconductors. The technique requires an ohmic substrate contact and a top metal contact on the sample, which forms a metal-semiconductor junction. As described in Section 2.8, the junction can behave as a capacitor if it is reverse biased, due to the accumulation of charges in the depletion region. An AC signal is applied to the junction with a function generator, and a range of DC offset voltages is applied between the top and the base contact to work in reverse bias and measure the capacitance. Usually, the sample is placed inside a metal box that acts as a Faraday cage, to shield it from electrical noise and mitigate high voltage hazards.

3.4 Conductive Atomic Force Microscopy

The atomic force microscope (AFM) measures the interaction force between a sharp tip and the sample when the distance is in the nanometric range. The tip has a radius of few nanometers and is located at the end of a cantilever and the interaction between tip and sample produces a deflection on the cantilever. This deflection is detected using an optical system consisting of a laser beam focused on the top surface of the cantilever, that drives the reflection to the center of a photodiode. If the cantilever flexes because of an interaction between tip and sample, the laser is reflected on a different spot on the photodiode: as the deflection on the photodiode is related to the force interaction, and the force depends on the distance that the tip has deflected, information on the topography of the sample can be collected. If the tip scans the surface of the sample (in the X and Y direction) it is possible to produce three-dimensional maps of the surface.

The AFM uses an electronic feedback that continuously corrects the tip-to-sample distance on the Z axis: the user can set the cantilever deflection (*setpoint*) and the feedback *gain* to control the tip-sample interaction. The movement of tip and/or sample in the X, Y, and Z directions is applied through piezoelectric actuators, and all the instrument is placed on an anti-vibration system to isolate it

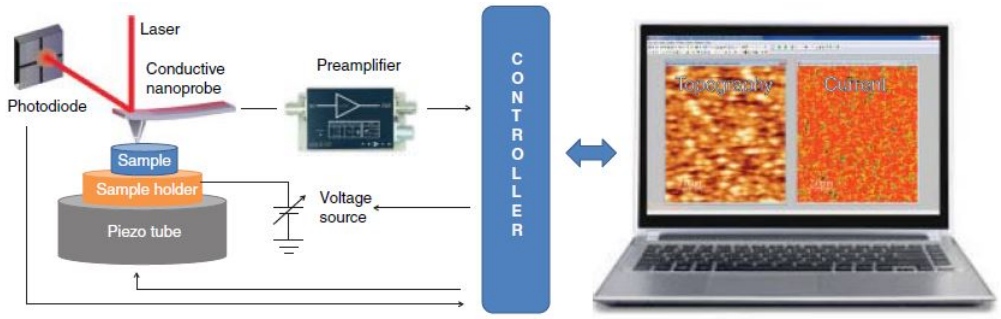

Figure 3.3: Block diagram of a conventional conductive atomic force microscope. Compared to a standard contact AFM, there are three differences: conductive tip, sample bias, and pre-amplifier [47].

from external perturbations.

There are different operation regimes, depending on the tip-sample distance during the measurements: the contact and non-contact modes. In contact mode there is a higher vertical resolution, but lateral frictions can damage the sample and/or the tip

Conductive Atomic Force Microscopy (C-AFM) is a type of contact AFM that is used to characterize simultaneously the surface topography and conductivity [47]. Figure 3.3 shows the schematic setup of a C-AFM. From the standard AFM there are three main differences: (i) the tip must be conductive, (ii) there needs to be a potential difference V_{sample} between tip and sample, and (iii) a pre-amplifier is used to convert the analogical current signal into digital voltages that can be read by the computer.

Chapter 4

Experimental details

For this project, industrial mc-Si wafers coming from different lateral positions and heights of DS ingots intentionally contaminated with iron and aluminum were analyzed. In the next sections, experimental details regarding the samples, sample preparation and characterization techniques are addressed.

4.1 Sample characteristics

Wafers from four different heights and two different lateral positions of two industrial ingots were analyzed. These ingots are representative of the current standard production and the first one was contaminated with 1000 ppb of iron, while the second one with 1000 ppb of aluminum, levels that are high enough to reduce the carrier lifetime significantly. A 20 mm thick part at the bottom of the ingots was removed before wafering, as this is a highly contaminated part that cannot be used for cell processing, called red-zone. Three wafers approximately occupy a thickness of 1 mm, and, considering that the red-zone was removed, the total height of the ingots is 360 mm. Three wafers were taken from bottom positions, one from the middle, and one from the top of both ingots: wafers 005, 024, 123, 503, and 884 from the iron contaminated ingot and wafers 005, 024, 123, 518, and 974 from the aluminum contaminated one. The numeration of the wafers starts at the bottom of the ingot with wafer 001.

The ingots are of size G5 (5×5 blocks of lateral area 156×156 mm^2) and the iron contaminated wafers were located in the corner, while the aluminum contaminated wafers were in the middle. An overview of the sample properties is given in Table 4.1, where the given sample names say the type of impurities, the

Sample name	Height (mm)	Lateral position
Fe005-c	21.7	corner
Fe024-c	28	corner
Fe123-c	61	corner
Fe503-c	187.7	corner
Fe884-c	314.7	corner
Al005-m	21.7	middle
Al024-m	28	middle
Al123-m	61	middle
Al518-m	192.7	middle
Al974-m	344.7	middle

Table 4.1: Overview of sample positions.

wafer number, starting from the bottom of the ingot, and the lateral position in the ingot (*c* for corner and *m* for middle).

From each 156 $\times$ 156 mm^2 wafer, a squared sample of dimensions 3 $\times$ 3 cm^2 was cut with laser scribing and then polished for EBSD and C-AFM measurements using sandpaper with a grit size of 9, 3, and 1 micrometers for a time of 30 s for each step.

4.2 Grain characterization

An area of approximately 23 $\times$ 14 mm^2 was analyzed in every sample. The measurements were performed using a JEOL JSM 840A Scanning Electron Microscope, equipped with a TSL MSC-2200 unit for beam control, TSL OIM software for data acquisition and analysis and a NORDIF Phosphor detector, at an accelerating voltage of 20.0 kV, tilt angle of 62.5° and a working distance of 30 mm. For this large mapped area the Comboscan technique was used, so the area of interest was divided in smaller regions, that are scanned sequentially by automatically moving the sample stage, stored and stitched back together. The stage movement is time consuming, so a low magnification of 27$\times$ and a beam step size of 50 microns were used to have more efficient measurements.

4.3 Electrical characterization

Microwave Photoconductance Decay The lifetime measurements were performed with a Semilab WT-2000PVN lifetime tester equipped with a 904 nm laser for excitation and a Wintau32 software for data acquisition and analysis. To have more representative results, the whole 156 $\times$ 156 mm^2 area of the wafers was scanned, with head height of 1.5 mm and raster 500 μm.

Al/Si diode characterization The aluminum contacts were thermally evaporated on the sample Fe005-c with an Edwards Evaporator. The source for the evaporation is 161 mg of aluminum, previously cleaned with an ultrasonic bath in acetone (10 minutes) and isopropanol (10 minutes). After placing it on an aluminum filament inside the vacuum chamber of the evaporator, an initial pressure of 6×10^{-6} mbar was reached. The power on the filament was increased of +2.5% (arbitrary unit of the instrument) every 30 s, and from a power of 25% it was increased of +2.5% every 60 s. The maximum power was reached at 27.5% and at a current of 15 A, with no formation of aluminum droplets and direct sublimation. The final pressure of the system was 5×10^{-6} mbar.

Stable ohmic contacts are mandatory to carry on reliable current-voltage and capacitance-voltage measurements. Different combinations of copper tape, silver paste and a mixture of indium and gallium were used, to achieve the best working conditions.

All the measurements were performed in the dark, inside a metallic box that acts as a Faraday cage, that shield noise and mitigate high voltage hazards. A first set of measurements was taken with probes contained in micromanipulators that can be moved with high precision with three screws, and connected with triaxial cables to two independent channels of a Keithley B2614B source measure unit (SMU). In this case the probes touched directly the silicon sample and the aluminum contact. In other measurements phosphorous bronze clamps were used on the aluminum contact and on the silicon sample to fix the diode to a copper holder. Copper wires were soldered with lead to the clamps and were connected to the SMU.

For $C - V$ measurements, the diode was connected to a Keithley LCZ-meter 3330, which generated an AC signal of 10 kHz frequency, while a Boonton 7200 capacitance meter, connected to the LCZ-meter with a GPIB connection, generated an offset DC voltage to polarize the junction. The applied bias ranged from 0 V to -2 V, with a step of 0.1 V.

Conductive Atomic Force Microscopy C-AFM measurements were performed on the samples Fe005-c and Al005-m with a Park NX10 AFM, placed on an active vibration isolation table and controlled by a PC with the NX10 Software. The tip used in the experiment was a Rocky Mountain 25Pt300B, a platinum tip with spring constant 18 N/m and tip radius below 20 nm. The sample was fixed onto a magnetic sample holder with biadhesive tape and the electrical contact was made with silver paste. All the scans were made at a rate of 0.30 Hz, the setpoint of the Z-feedback is 449.055 nN, and the gain 0.500. The sample was biased at -10.0V and the amplifier gain is 10^9. Local current-voltage measurements were made on the silicon grains and on the grain boundaries.

Chapter 5

Results and discussion

The efficiency of multicrystalline silicon wafers used in the photovoltaic industry is greatly affected by the microstructure and by the presence of metallic impurities. Analysing and understanding the effects of different types of defects is necessary to increase the quality of mc-Si based devices. The link between grain boundaries and electrical properties has become of great interest for the photovoltaic industry, in order to improve the processing and the efficiency of solar cells [48, 49].

Iron and aluminum are two of the most common and detrimental impurities in mc-Si and they can be introduced by the feedstock, by the crucible or by the Si_3N_4 coating. The quartz used in the feedstock and the coating are not the only impurity source, as impurities are also introduced during the silicon refinement process and during the fabrication of ingots. Dissolved iron is thought to be the most probable candidate for the carrier lifetime limitation in the bottom and side regions of mc-Si ingots, while the carrier lifetime in the silicon bulk is limited just by interstitial iron atoms [50, 51]. The high Fe concentration of a standard crucible acts as an infinite impurity source, causing an in-diffusion profile to the ingot, while high purity crucibles act as a sink to Fe atoms diffusing from the coating [51]. The two ingots that were characterized had a feedstock contamination of 1000 ppb of iron and aluminum, respectively: considering all the other impurity sources, the contamination is thought to be high enough to affect significantly the electrical properties of the wafers (high purity solar grade silicon contains iron in the parts per 10^9 range [52]). In this study, only one type of impurity was considered to avoid non-linear effects due to the interaction between the different impurity atoms. While many papers describe the characterization of wafers at different heights in the ingot, fewer papers focused also on the changes in the microstructure at different lateral positions (for example [36, 53]).

5.1 Microstructural characterization

The microstructural characterization was performed by means of Electron Backscatter Diffraction, as explained in paragraph 3.1, to study the grain size distribution and the character of the grain boundaries. The OIM software recognizes the different grain orientations from the interference patterns and identifies points with the same orientation as an individual grain, which is colored with a unique color. The resulting maps, called orientation image micrographs (OIM), are shown Figure 5.1 and the samples are labelled following Table 4.1.

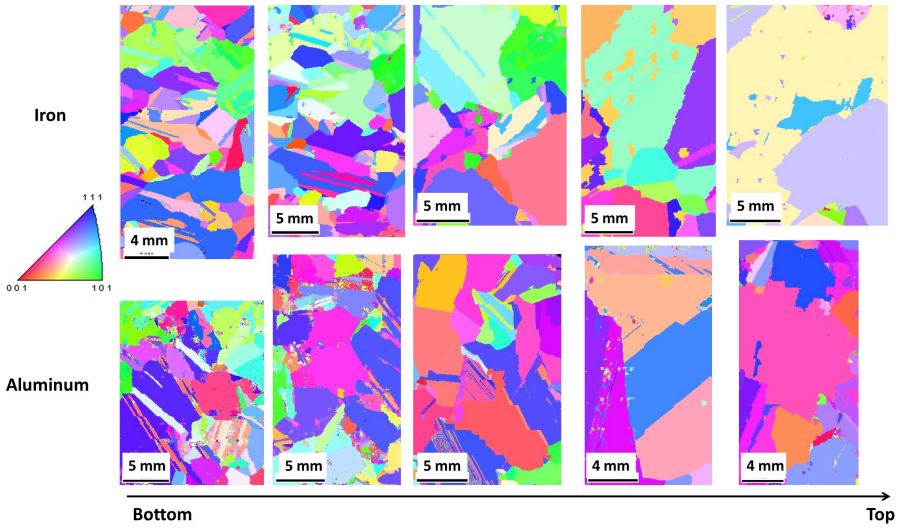

Figure 5.1: Orientation image micrographs (OIM) of the samples. Top row contains wafers Fe005-c, Fe024-c, Fe123-c, Fe503-c, Fe884-c; bottom row contains wafers Al005-m, Al024-m, Al123-m, Al518-m, Al974-m.

An important parameter of these measurements is the Confidence Index (CI), which is calculated during the automated indexing of the diffraction pattern. The diffraction bands detected during the image analysis can be given by different grain orientations, so the software compares the possible solutions and assigns to each pixel a value from 0 to 1 (CI): the grain orientation with a higher CI has a better agreement with the produced diffraction pattern and the pixel is given the corresponding color. If the software cannot recognize the diffraction pattern, for example because there is one zone axis in the middle of the diffraction pattern, or there are variations in the pattern over time and the pattern becomes saturated in the middle, a CI of -1 is assigned. An example of this effect was observed in

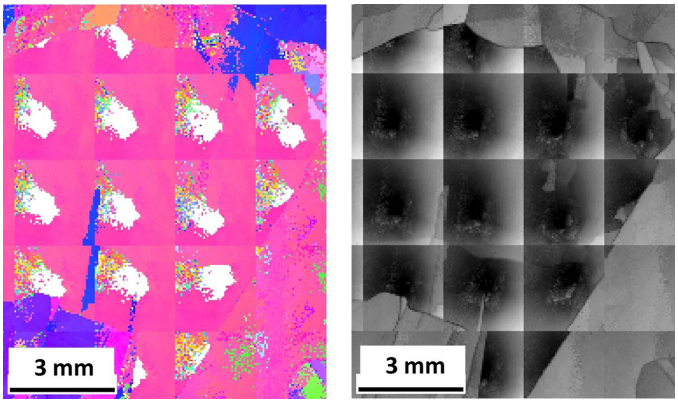

Figure 5.2: Example of grain from sample Al974-m with low confidence index (CI): orientation image micrographs (left) and CI map (right).

the sample Al974-m and it is shown in Figure 5.2: the picture on the left is the OIM map and the white spots have no solution; the picture on the right shows the confidence index of the recognized patterns on a gray scale, where a darker shade means lower CI and a black pixel means that the CI is -1. This is clearly an artifact in the measurement, given by the particular generated diffraction pattern: this area would be a single grain, but each pixel with a different color is recognized by the software as a separate grain, introducing large errors in the measurement of the grain size distribution and of the grain boundary density. To avoid this, all the pixels with a CI lower than 0.1 were selected and were given the orientation of the neighboring pixel with higher CI: in this way the signal was cleaned up and all the considered area was calculated as a single grain.

The Comboscan technique scans sequentially small rectangular regions and stitches the scans together. This is an undesirable pattern, that is again shown in Figure 5.2 and can also affect the measurement of the grain boundary density: to avoid this, the maps were cleaned up by coloring every grain with the average grain orientation.

It can be seen qualitatively that there is an increase in the grain size distribution, which can be quantified by plotting the average grain size of the different wafers (Figure 5.3).

Looking at the average grain size distribution, one can see a small average grain size in the bottom, that increases going to the top. This trend was seen in numerous previous works (e.g. [48]) and it is thought to be related to the conditions of nucleation. At the bottom of the ingot there are a large number of nucle-

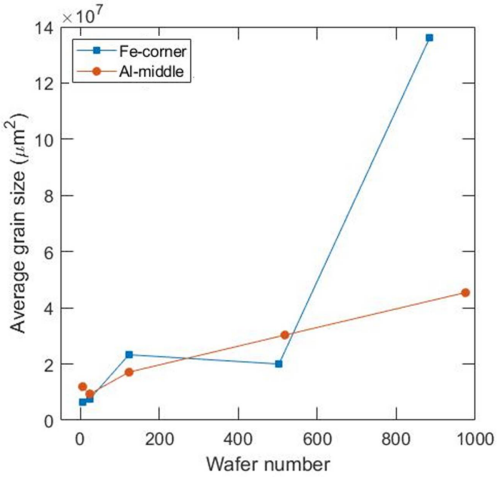

Figure 5.3: Average grain size in the iron (blue) and aluminum (red) contaminated wafers.

ation sites, both because it is at the beginning of the crystallisation, so nucleation is initiated by a high super-cooling, but it is also due to the diffusion of impurities from the crucible and the coating, that act as additional nucleation sites. During the crystal growth the smaller grains reorganise and increase in size.

An interesting feature of these wafers is the distribution of the Grain Boundaries orientations, in particular the coherent boundaries $\Sigma 3^n$. The software recognizes a grain boundaries if two points in the scan have a misorientation higher than 15°. Then, it is possible to colour the different boundaries by giving the software the information on the misorientation angle and rotation axis, as described in Table 2.1. Figure 5.4 shows how the grain boundaries are colored by the software in the CI maps.

Another quantification of the grain size is simply the total density of boundaries, since the EBSD analysis software disregards boundaries with a misorientation below 15°, the vast majority of sub-grain boundaries in silicon. The GB density is the grain boundary length normed by the considered wafer area, and it is plotted for the different samples in Figure 5.5. In agreement with other studies [36], the total density of High Angle GBs decreases along the ingot height because of the higher grain size, in both ingots. The GB density is almost halved from the bottom to the middle of the ingot, while going from the middle to the top the density becomes more stable, with no noticeable differences. It is also interesting to note that the wafers at the corner of the ingot have a GB density

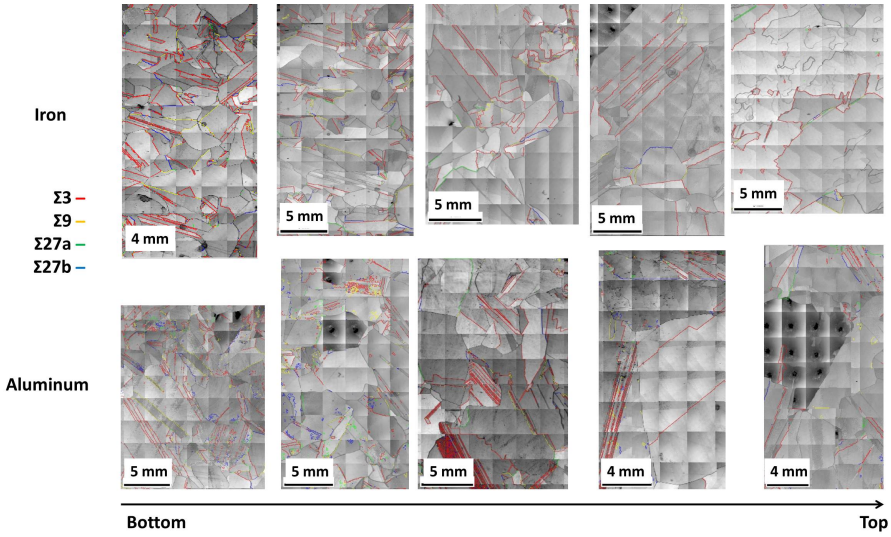

Figure 5.4: Coherent grain boundaries maps: $\Sigma 3$ (red), $\Sigma 9$ (yellow), $\Sigma 27$a (green), $\Sigma 27$b (blue). Top row contains wafers Fe005-c, Fe024-c, Fe123-c, Fe503-c, Fe884-c; bottom row contains wafers Al005-m, Al024-m, Al123-m, Al518-m, Al974-m.

lower than wafers at the center of the ingot [36]. The good correlation between decreasing GB density and increasing average grain size shown in Figure 5.6 is again something already observed (e.g. [55]).

As already seen in literature, the $\Sigma 3^n$ boundaries are the most common coherent boundary in mc-Si [35]. The density of $\Sigma 3$, $\Sigma 9$, and $\Sigma 27$ (Figure 5.7) decreases along the ingot height, with only sample Al123-m showing a deviating behaviour, as it is dominated by a few grains with profound multiple twinning. Other CSL boundaries with a non-$\Sigma 3^n$ character, such as $\Sigma 5$ and $\Sigma 11$, exist in a very small density compared to the $\Sigma 3^n$, so their density roughly corresponds to the total density of random angle grain boundaries (RAGB) [36]. Also the RAGB density is decreasing (Figure 5.8), even if this trend is not as clear as the total GB density, probably because the cleanup processes on the maps altered the count of the RAGB in the scan.

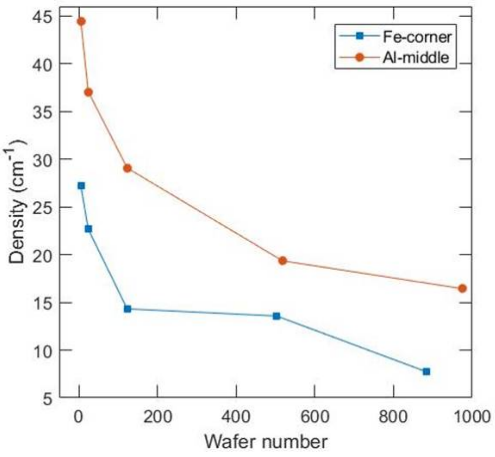

Figure 5.5: Total density of grain boundaries with misorientation angle higher than 15°.

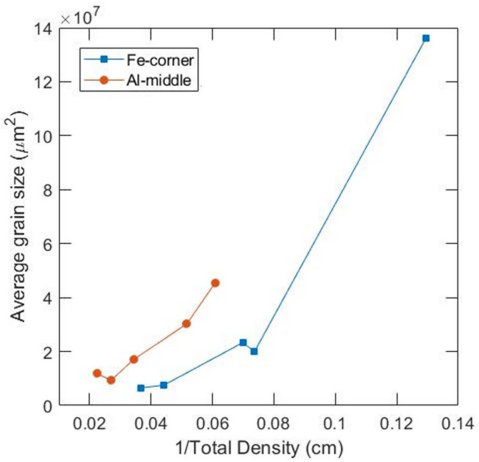

Figure 5.6: Correlation between the increasing average grain size and the decreasing value of total grain boundary density.

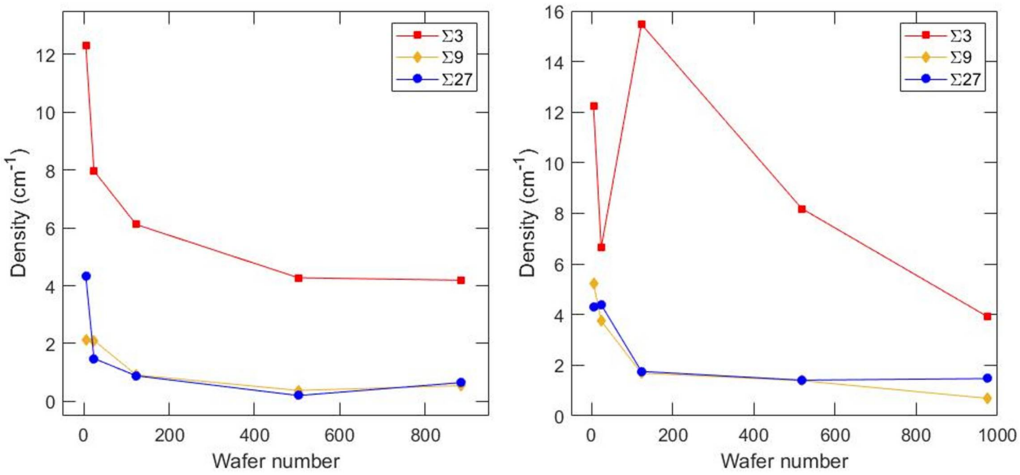

Figure 5.7: Density of Σ3 (red), Σ9 (yellow), Σ27 (blue) versus wafer number, for iron (left) and aluminum (right) contaminated wafers.

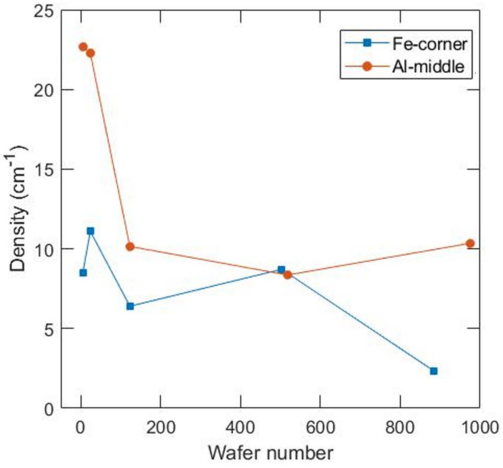

Figure 5.8: Density of RAGB versus wafer number, for iron (blue) and aluminum (red) contaminated wafers.

5.2 Impurity concentration

The initial contamination level C_0 for both ingots is 1000 ppb, a concentration considered to be high enough to affect the electrical properties. As discussed in the previous chapters, the impurities segregate during the directional solidification: their distribution along the ingot height follows the Scheil equation (Equation 2.11). Figure 5.9 shows an estimation that does not consider the correction effects discussed in Section 2.6 and Table 5.1 shows the estimated impurity concentration in the wafers.

The different segregation coefficients of iron and aluminum produce different impurity concentration profiles. As the used k_{eq} for iron is so small, the wafers at the bottom have really similar contamination levels and a high fraction of impurities is segregated at the top. Aluminum has a bigger segregation coefficient and the concentration of impurities increases more rapidly at the bottom. Even if the Scheil's equation requires many approximations and assumptions, the general impurity distribution profile agrees quite well with the chemical analysis presented in other studies [52, 54]: the main deviations from the Scheil's profile are at the bottom, where the crucible and coating contamination is high, and at the top (around 85% height), where iron can start to back-diffuse [52].

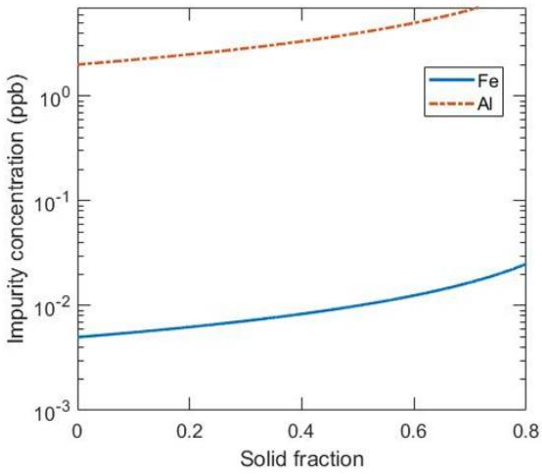

Figure 5.9: Impurity concentration profile for iron (blue) and aluminum (red) at different heights in the ingot. The segregation coefficients are k_{Fe} = 5.0 $\times$ 10^{-6} and k_{Al} = 0.002 .

Sample	Height fraction	C_S (ppb)
Fe005-c	0.060	0.0053
Fe024-c	0.078	0.0054
Fe123-c	0.169	0.0060
Fe503-c	0.521	0.0104
Fe884-c	0.874	0.0397
Al005-m	0.060	2.128
Al024-m	0.078	2.168
Al123-m	0.169	2.407
Al518-m	0.535	4.296
Al974-m	0.958	46.76

Table 5.1: Estimated impurity concentration of the different samples, using Equation 2.11.

5.3 Electrical characterization

The characterization of the electrical properties was done with different techniques: first, qualitative measurements of the lifetime were taken with Microwave Photoconductance Decay; then, aluminum contacts were evaporated on a sample in order to perform a Mott-Schottky analysis to evaluate the doping concentration, and to measure the current-voltage characteristic at different temperatures; finally, the electrical activity of decorated grain boundaries was characterized with conductive atomic force microscopy.

5.3.1 Microwave Photoconductance Decay

Figures 5.10 and 5.11 show the lifetime maps of the iron contaminated and aluminum contaminated wafers, respectively. Microwave Photoconductance Decay is a highly surface sensitive technique, and, as the wafers were not passivated, the measurements are just qualitative: the areas colored in red have lower lifetime, while the areas colored in blue have higher lifetime.

Especially the areas of good lifetime are extremely affected by bulk and surface recombination, and they are highly dependent on the surface conditions, so the analysis of the lifetime maps should be limited to the red regions with low lifetime. There is a striped pattern in most of the maps that is due to the sawing marks on the wafers: a saw damage removal step is carried out as part of the solar-cell production at a later stage, and contributes to the removal of residual surface

contamination [20]. Also, some of the wafers were cut to prepare the samples for EBSD before making the lifetime measurements, so it is possible to see were the laser cut them.

Without considering these artefacts, there are two main differences between the wafers contaminated with iron and aluminum:

- the Fe contaminated samples were located in the corner of the ingot, so it is possible to see a red zone at the top and right sides of the wafers Fe005-c, Fe024-c, Fe123-c, and Fe503-c, due to the contamination from the crucible. The side edges of any ingot show this impurity diffusion effect and this side red zone is larger towards the bottom of the ingot, showing a typical V shape [20]. The introduction of impurities from the crucible and the coating is not the same all along the ingot height, in fact the red zone gradually disappears, with no visible contamination in the Fe884-c wafer. This contamination is not present in the aluminum contaminated wafers, as they were at the centre of the ingot and far from the crucible.

- another type of low-lifetime area in the maps has a different origin, and it is related to dislocation clusters that are formed in the ingot. It is already known that the dislocation clusters increase in number while going further up in the ingot [34]. The lower lifetime in the top is mainly due to the segregation and back solid diffusion of metal impurities, as well as to the presence of precipitates and extended defects [20]. These areas are present in all the maps (both in the iron and aluminum contaminated wafers), but what happens at the top is particularly interesting, as there are far more red areas in Fe884-c than in Al974-m. This can have two different explanations: iron has a much smaller segregation coefficient than aluminum, so far more impurities are segregated at the top of the ingot (as shown in Figure 5.9) and they decorate the dislocation clusters, reducing even more the lifetime of the minority carriers; the lateral position of the wafers in the ingot can also influence the formation of dislocations.

Usually μ-PCD measures lifetime of passivated samples, but measurements on as-grown wafers showed and effective lifetime in a range between 0.1 and 2 μs, in very good agreement with the measurements presented here [56]. Bothe *et al.* studied the effective lifetime of mc-Si wafers as-cut, after saw damage removal, and after etching: as expected from literature, the carrier lifetime in the top and bottom regions is indeed smaller, compared to the centre of the ingot. This trend, already visible in the as-cut data of that study, was even more clear

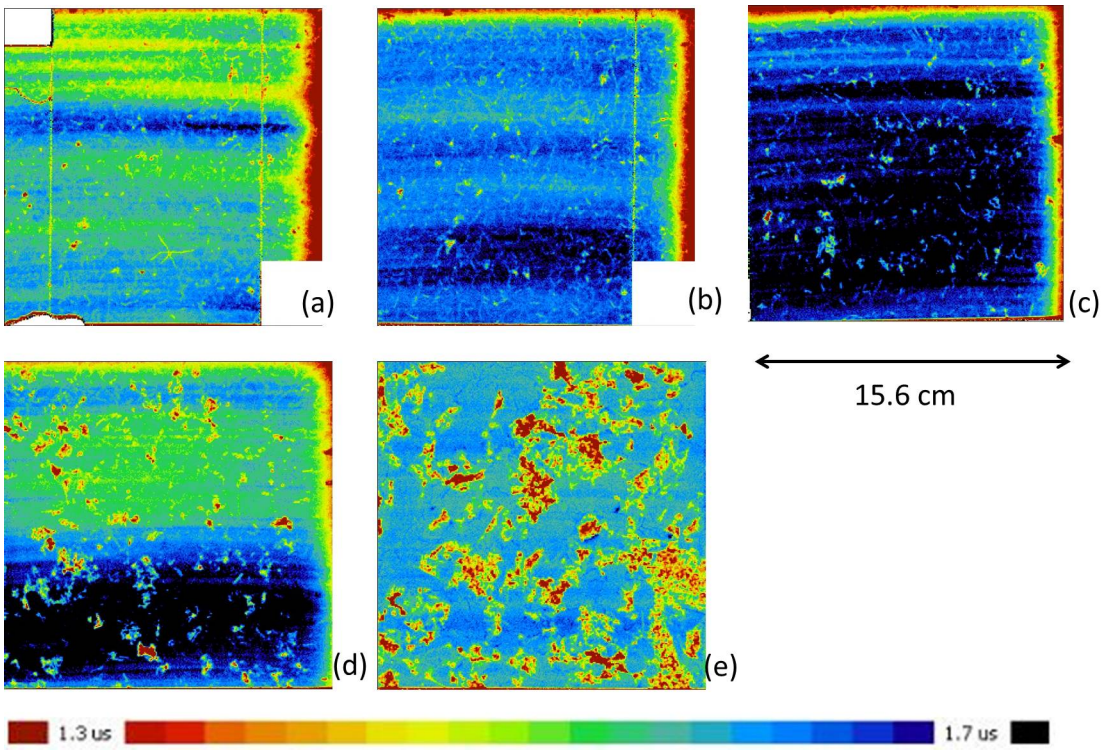

Figure 5.10: Lifetime maps obtained with μPCD for the iron contaminated wafers located in the corner of the ingot Fe005-c (a), Fe024-c (b), Fe123-c (c), Fe503-c (d), Fe884-c (e). The colored scale is the same for all the samples and it is just qualitative.

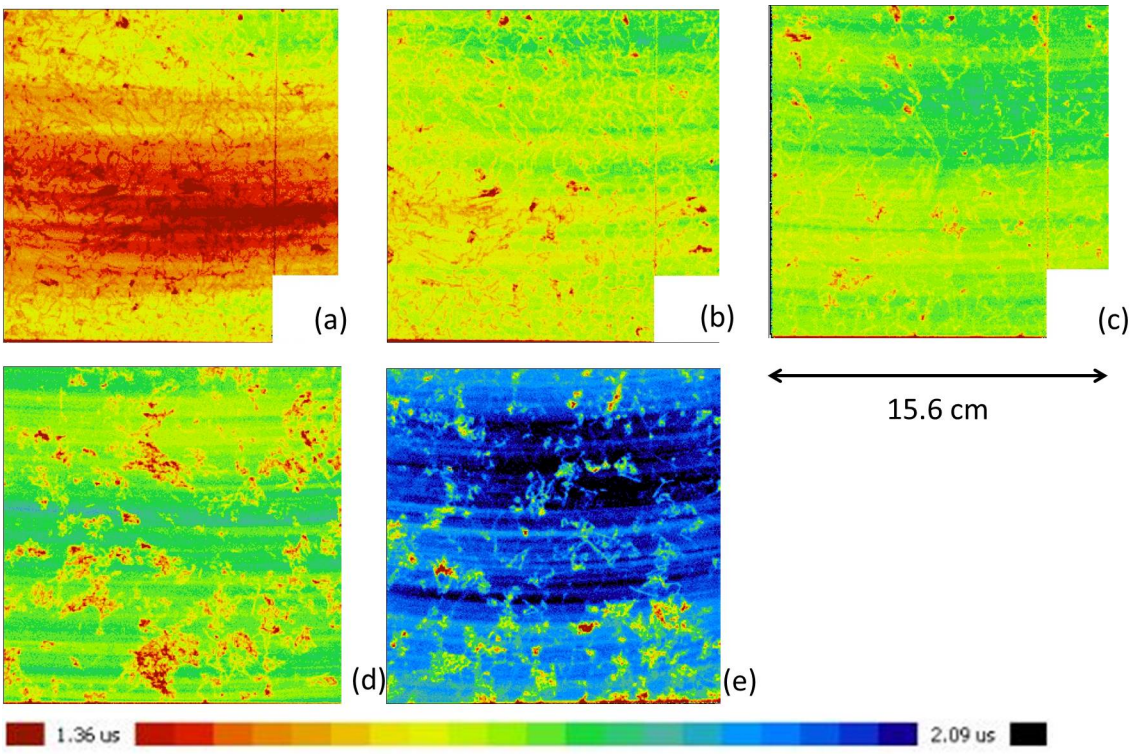

Figure 5.11: Lifetime maps obtained with μPCD for the aluminum contaminated wafers in the middle of the ingot Al005-m (a), Al024-m (b), Al123-m (c), Al518-m (d), Al974-m (e). The colored scale is the same for all the samples and it is just qualitative.

after etching and surface passivation, but the thickness of the saw damage layer critically depends on the sawing conditions [57]. Removing the sawing marks on the whole wafers studied in this project before μ-PCD measurements was not possible, because the wafers were too thin and would have broken during the polishing. It is therefore hard to identify quantitatively this trend on the lifetime maps presented here, but the reduced crucible and coating contamination and the low number of dislocation clusters in the samples Fe503-c and Al518-m might suggest a higher lifetime compared to the other samples.

A link between microstructure, impurities, and electrical properties, was already found by Buonassisi *et al.* [58]. Metal-rich precipitates are almost never detected at $\Sigma 3$ boundaries, and seldom at $\Sigma 9$: the high degree of atomic coincidence and low degree of bond distortion within lower-Σ grain boundaries, decreases the ability of metals to precipitate, possibly by suppressing precipitate nucleation and growth, and/or by retarding diffusion along the boundary.

On the other hand, higher-Σ and non-CSL boundaries, which can act as transition metal sinks, are highly undesirable, as they act as recombination-active centers or as sources of metals during high-temperature treatments. Measuring the recombination activity of the grain boundaries in these samples could be a way to see where the impurities tend to segregate at different heights.

Another study used different characterization methods to study the low-lifetime areas at the edge of directionally solidified mc-Si ingots, by comparing minority carrier lifetime-, microstructure- and dislocation density maps [53]. All samples ranging from 0 to 15 mm from the edge have a relative increase in lifetime in the region with High Angle Grain Boundaries, and a decrease in lifetime in regions dominated by twins, a trend due to internal gettering. Iron-boron pairs are the main responsible for lifetime degradation in the wafers close to the crucible, and again the concentration gradient of interstitial iron in the edge zone is explained by solid-state diffusion of iron and aluminum atoms from the crucible and the coating.

5.3.2 Al/Si diode characterization

The aim of this characterization is to find stable electrical connections for an Al/Si diode to make low temperature measurements in a cryostat. Moreover, the device should work well in reverse bias and have a low leakage current. Indeed, a low reverse current corresponds to a highly capacitive behaviour of the depletion region, ensuring a good capacitance measurement. The sample holder inside the cryostat is small, so a piece of dimensions $\approx 0.5 \times 0.5$ cm^2 was cut from the

wafer. With such small sample it was possible to evaporate only two aluminum contacts, whose area was later measured with an optical microscope and found to be $\approx$1.86 mm^2.

After the evaporation of the two aluminum contacts, the silicon sample was scratched on one side to locally increase the amount of surface defects, thus increasing the doping and therefore the conductivity. The sample was then placed on a glass substrate, using silver paste and copper tape as back contact. The diode exhibits a poorly rectifying behaviour in the range -5 V to 5 V (Figure 5.12-b): the conductive silver paste forms another Schottky junction with the sample, so the system behaves as a double Schottky junction. To avoid this effect, the conductive silver paste should not touch the sample.

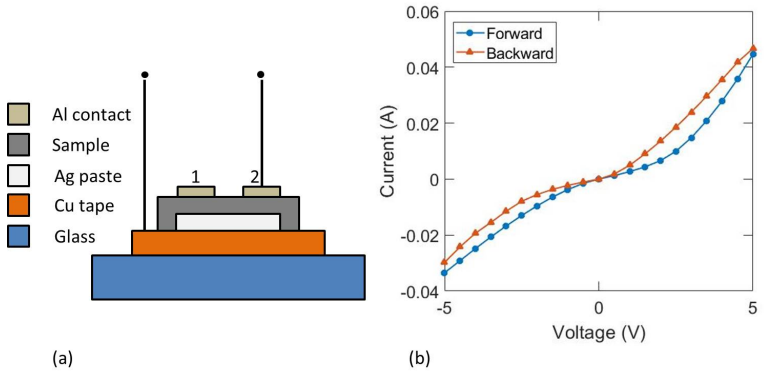

Figure 5.12: (a) Schematic configuration of the diode with silver paste back contact; (b) current-voltage measurement.

The back contact was then improved by putting a mixture of indium and gallium on the sample and then a small drop of a thicker bi-component silver paste. The ohmic contact was done on both sides of the sample to check if the surface recombination affected the current flow through the Schottky diode. From Figure 5.13 it is possible to see that the evaporation of the aluminum contacts was successful and the In/Ga paste used as a contact on silicon is a better choice than silver paste, as a rectifying $I - V$ characteristic was measured. There are several important comments that need to be done regarding the plots in Figure 5.13-b:

- the ohmic contact cannot be done on the same side as the Schottky contact. There is a higher leakage current and a low forward conduction, probably due to surface recombination. If the ohmic contact is on the back side this effect is reduced.

- one Schottky contact (labeled as 1) is worse than the other, especially in the reverse bias range. As the two aluminum contacts were evaporated simultaneously, the two junctions are expected to have the same conduction properties. This effect is probably due to inhomogeneous electrical properties of the wafer, as also seen in the lifetime measurements with μ-PCD. Therefore, it is suggested to evaporate always more than one contact, and test them all to find the one with better properties.

- The current-voltage curve was measured again on this contact after 8 minutes to check its stability. Ideally, these two measurements should be identical, but the silver paste and especially the In/Ga mixture were seen to liquefy at room temperature, therefore changing the properties of the electrical connection. This is not a desirable effect because the temperature of the device increases with high applied voltages and it is difficult to check the repeatability of the measurements. After every measurements the device was placed in an environment with lower temperature (around 4°C) to cool it down and to avoid overheating it. This problem could also be solved by improving the materials for the contacts: a bi-component silver paste is thicker and less liquefiable at room temperature; the In/Ga paste was made by manually mixing pure indium and pure gallium, but this mixture is also commercially available with added components that makes it more stable.

The diode was further improved for capacitance-voltage measurements, by using a second piece of copper tape, which was connected to the aluminum contact with a copper wire and silver paste (Figure 5.14-a). With this setup it was possible to perform $C - V$ spectroscopy with offset voltages ranging form 0 V to -2 V, so that the diode was reverse biased. A second measurement was repeated after 13 minutes from the first one, to confirm the results. Figure 5.14-b shows how the inverse square of the capacitance depends on the voltage applied across the diode. Following Equation 2.21, a linear dependence between the quantity $1/C^2$ and the applied voltage is expected: this effect is mainly seen at high negative voltages, while for smaller voltages there is a different behavior. Similarly, using Equation 2.21, the doping concentration is plotted as a function of the depletion layer width in Figure 5.14-c: N_D is expected to be constant across the sample, but there is an increase of almost one order of magnitude for small depletion layer width. Both these effects are artifacts, probably because the small negative offset voltages are not able to polarize the Schottky junction properly. However, the doping concentration is consistent between the two measurements and the estimated value is

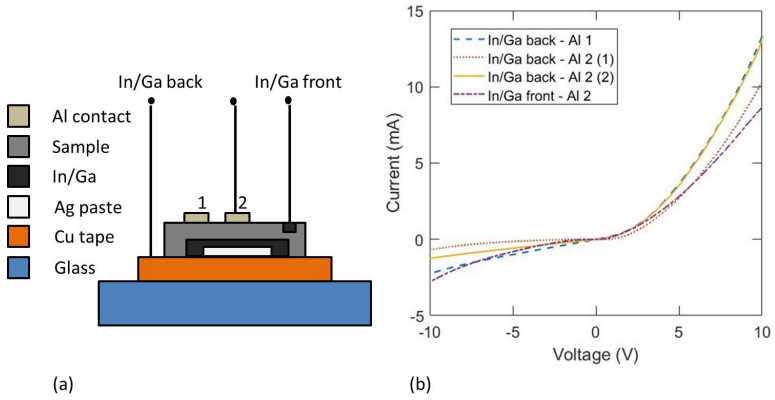

Figure 5.13: (a) Schematic configuration of the diode with In/Ga front and back contacts; (b) current-voltage measurements with four different electrical connections: back ohmic contact and first Schottky contact; back ohmic contact and second Schottky contact, repeated twice to check its stability; front ohmic contact and second Schottky contact.

between 1×10^{16} and 2×10^{16} cm^{-3}. This value was also measured with Glow Discharge Mass Spectroscopy on parallel samples, confirming a boron concentration of 10^{16} cm^{-3}.

Finally, $I-V$ curves were measured inside a cryostat at low temperatures (down to 83 K): the sample had to be placed vertically in the vacuum chamber, so the setup was changed again (Figure 5.15-a). The sample holder is made of copper and is divided in different sections that are not in electrical contact with each other. The sample is fixed with conductive carbon tape, which stays conductive and bi-adhesive also at low temperatures, and the back contact of the sample is still made of In/Ga and silver paste. Additionally, two phosphorous bronze clamps were soldered to the copper substrate with two purposes: (i) creating an electrical connection with the carbon tape for the back ohmic contact, and with the aluminum contact; (ii) exerting a mechanical force on the sample in order to keep it fixed to the holder. A first $I-V$ curve was measured at room temperature (Figure 5.15-b) using metallic tips that touch the two clamps, to check that the carbon tape and the clamps made good electrical connections. The plot shows again the typical diode behavior, with low leakage current in reverse bias. However, the logarithmic plot shows that there is one order of magnitude of difference between the current at -2 V and 2 V, which is already acceptable. Copper wires were then soldered to the clamps and the device was put inside the cryostat, which

was connected to a source measure unit with coaxial cables, and cooled down to LN_2 temperature. The measurements in Figure 5.15-c were taken at 83K, 89K, and 120K. All the electrical connections stayed stable even at very low temperatures. Also the forward current is strongly temperature dependent, and it can be seen that while the curve at 83K and 89K are really similar, a temperature of 120K is already enhancing the conductivity in the device. A final comment can be done on the current scale in Figures 5.15-b and 5.15-c: assuming that all the contacts shown in Figure 5.15-a did not change, the forward current at room temperature is expected to be much higher, but at 2 V is three orders of magnitude lower than the current measured inside the cryostat. The type of probes that are used on the contacts (metallic sharp tip or soldered wires) seems to play a major role on these kind of electrical characterization, therefore it is not meaningful to compare the absolute values of forward current if different setups are used.

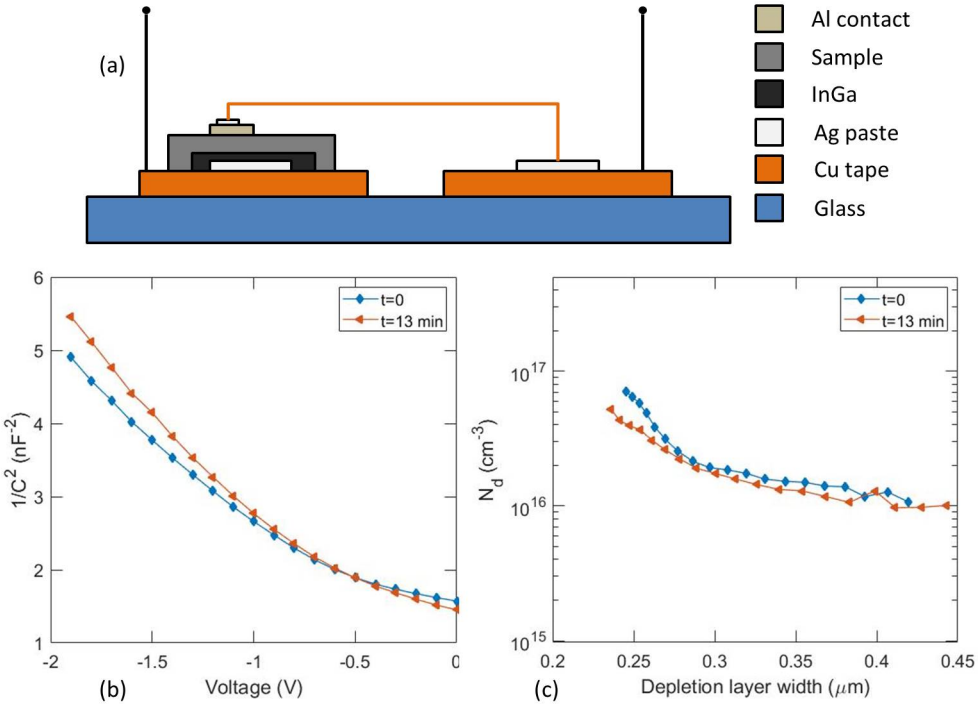

Figure 5.14: (a) Schematic configuration of the diode for $C-V$ measurements; (b) capacitance-voltage measurements; (c) doping concentration estimation as a function of depletion layer width.

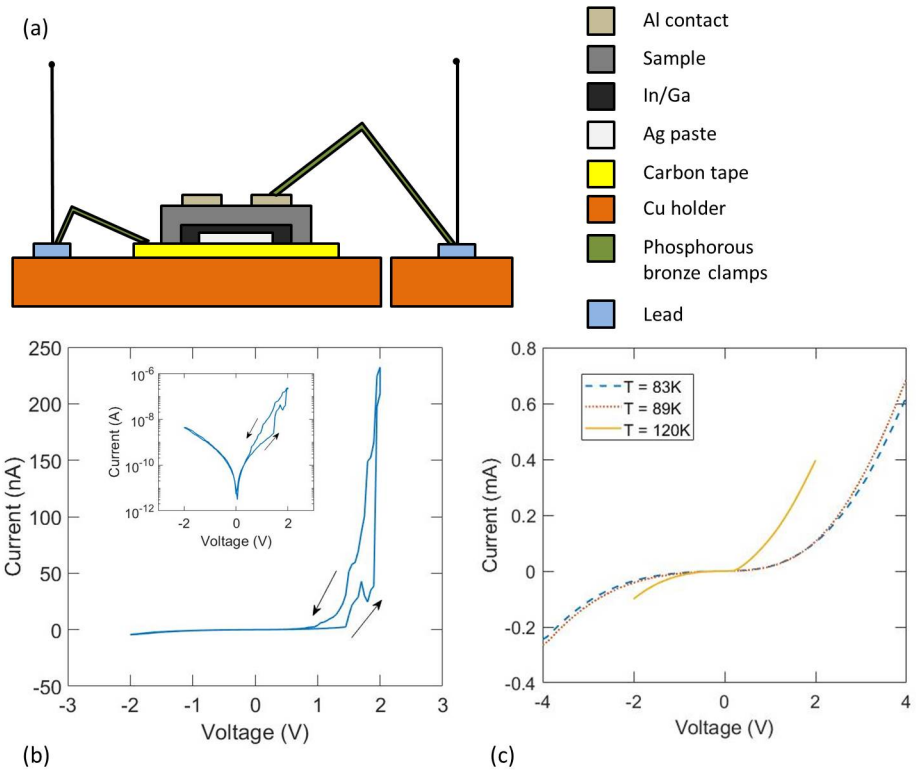

Figure 5.15: (a) Schematic configuration of the diode for temperature measurements; (b) current-voltage measurements at room temperature, with metal probe on the sample. The arrows show forward and backward sweep voltage; (c) current-voltage measurements at different temperatures.

5.3.3 Conductive Atomic Force Microscopy

C-AFM allows to study locally the electrical properties of a sample and was used to recognize electrically active grain boundaries inside the mc-Si samples, which appear as regions with a higher conductivity and no significant effect on the surface topography. In C-AFM the conductive tip is in contact with the sample and can be damaged from lateral frictions during the scan and the maximum area of a scan is $50 \times 50\ \mu m^2$. To work in a more efficient way and to limit damages to the instrument, it was chosen to study only the samples from the bottom of the ingots, Fe005-c and Al005-m, because, as seen from the EBSD maps, they have a high density of grain boundaries and it is easier to find them in the sample.

Results

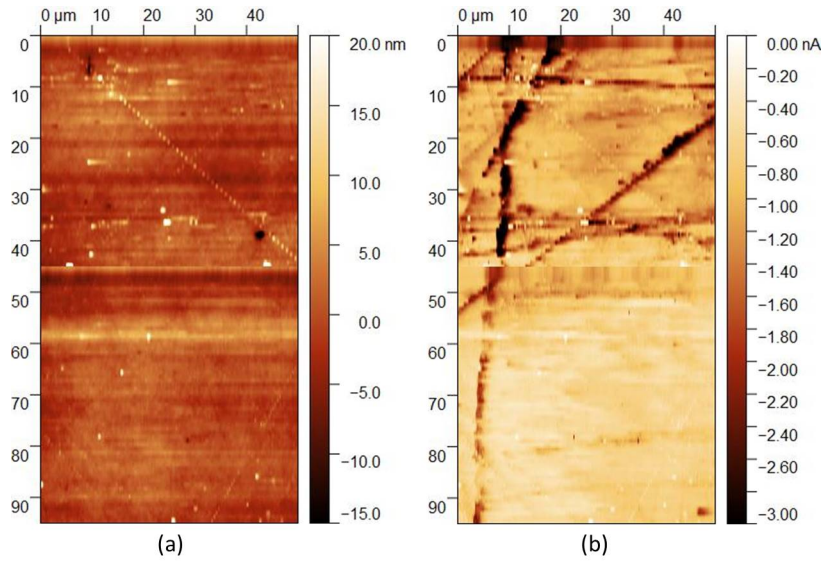

Figure 5.16: Conductive Atomic Force Microscopy (a) surface topography and (b) current maps of sample Fe005-c containing several grain boundaries.

Figure 5.16 shows the C-AFM maps, surface topography and current, of the sample Fe005-c. The maps, composed of two scans stitched together, have a total area of 50×95 μm^2 and 256×486 pixels. The current map (Figure 5.16-b) presents a constant background current and straight lines of a darker colour, which means a higher negative current, that were identified as grain boundaries. On the other hand, the topography map in Figure 5.16-a does not show any surface roughness variation that could be responsible for the enhanced current flow, apart from two diagonal lines in the top half that could be due to surface contamination. The current contrast, calculated as the difference between the average value in the grain and the minimum value reached at the boundary, is around -2 nA in the top half, and around -1.5 nA in the bottom half. As the sample was kept at a high voltage (-10 V) and the bottom half was scanned later, a charge accumulation process could explain the lower contrast. The width of the grain boundaries is between 2 and 3 μm and it is much higher than the geometric width of silicon grain boundaries, which is around 1 nm or several lattice constants. This indicates that the electrical effect of the grain boundary is detected by measuring the conductivity of the sample, and has a spatial dimension much higher than the actual geometric

dimension. This electrically relevant width is not homogeneous, suggesting that there is segregation of metallic impurities or metallic precipitates, and the decorated parts of the GBs have a stronger and wider effect on the electrical properties of the neighboring grains. It is important to note that it is not possible to compare the grains and the grain boundaries depicted here with the ones in the EBSD maps, as the scans have dimensions on a different scale: the EBSD maps have areas bigger than 1 cm^2 with a step size of 50 μm, so these maps of area 50×95 μm^2, would be as big as two pixels.

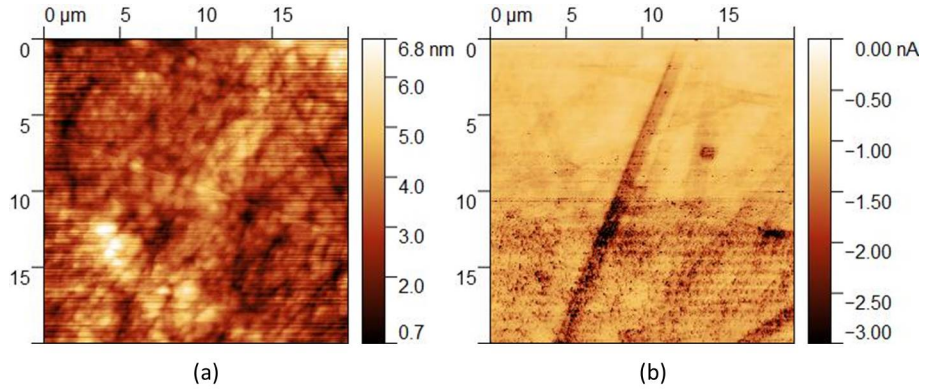

Figure 5.17: Conductive Atomic Force Microscopy (a) surface topography and (b) current maps of sample Al005-m containing a grain boundary.

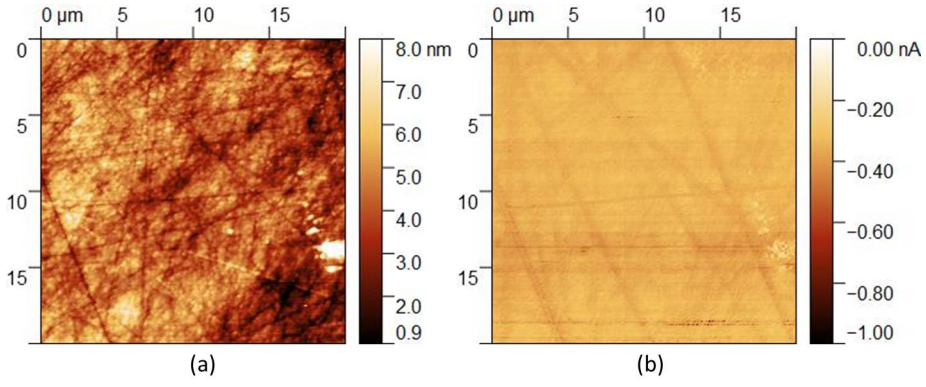

Figure 5.18: Conductive Atomic Force Microscopy (a) surface topography and (b) current maps of sample Al005-m on a single grain of silicon.

Other scans were collected from the sample Al005-m in two different positions of the surface, showing a grain boundary (Figure 5.17) and a single grain of silicon (Figure 5.18). The size of these scans is 20×20 μm^2 and 256×256 pixels. As seen in the previous scans, it is possible to distinguish the grain boundaries if there is a high current contrast and there is limited correlation with the surface topography. This is the case of Figure 5.17, that has a grain boundary with a current contrast of around -0.7 nA, while the surface scratches in Figure 5.18, are also seen in the topography map and have a current contrast less than 0.1 nA. The bottom half of the current map in Figure 5.17-b has a noise higher than the top half, which can again be explained by charge accumulation due to the high applied voltage, and is therefore not considered in the following analysis.

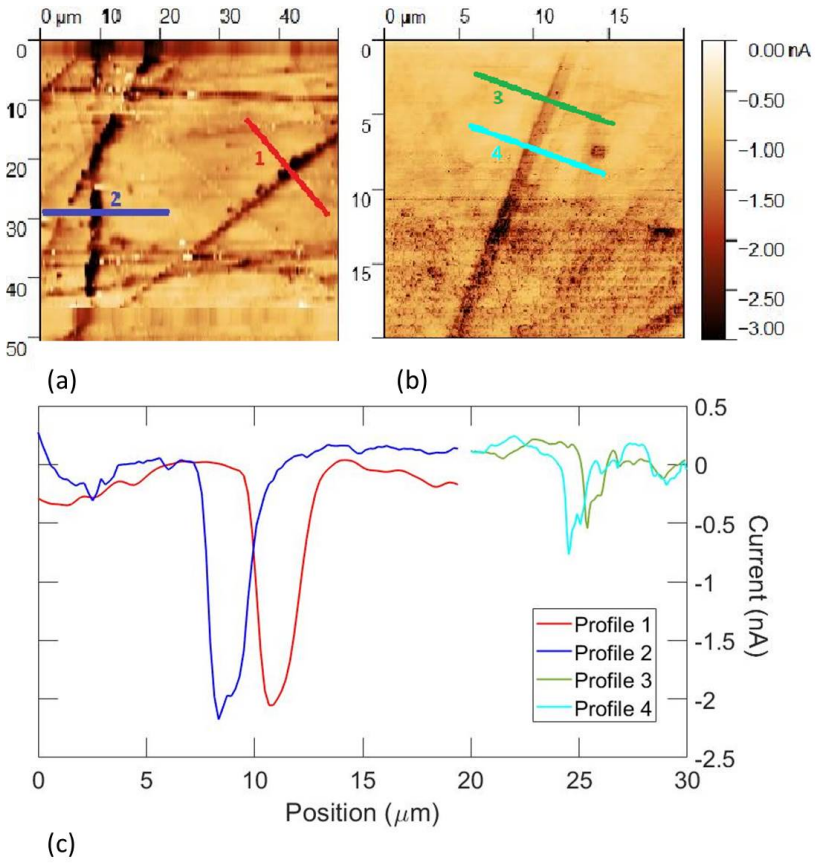

Figure 5.19: Current maps with chosen profiles in sample (a) Fe005-c and (b) Al005-m; (c) Comparison of the current profiles of the two samples.

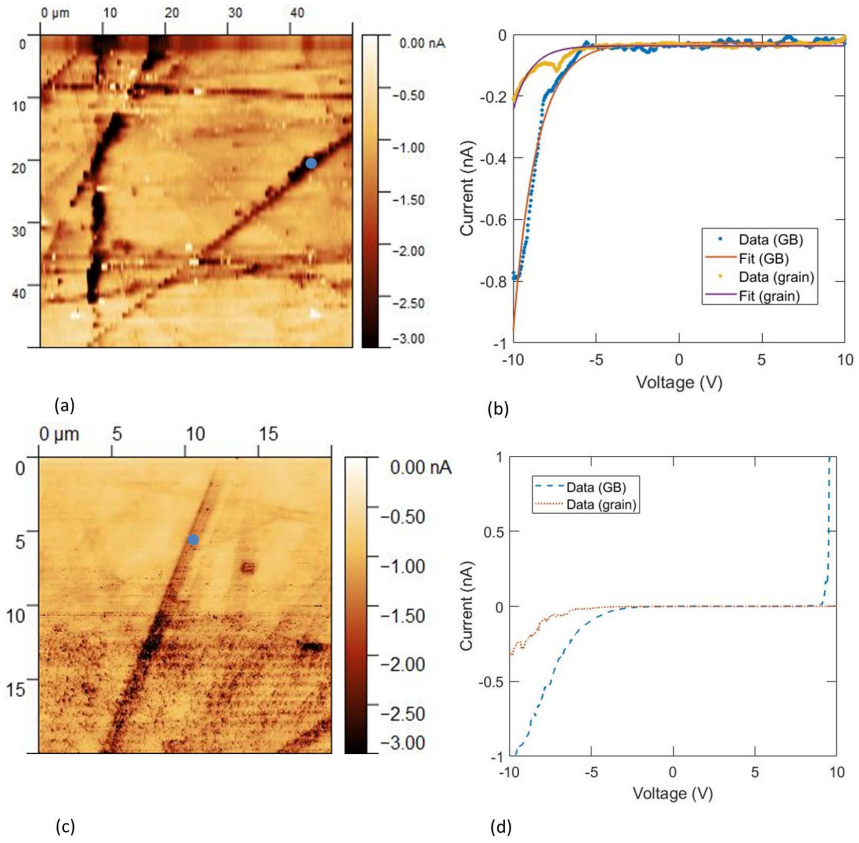

Figure 5.20: (a) (c) current map and (b) (d) current-voltage curves of samples Fe005-c and Al005-m, respectively. The measurements were taken on a grain boundary (indicated with a blue dot) and in the neighboring grains, by averaging curves taken in different positions.

Figure 5.19 shows a few current profiles extracted across the grain boundaries in the two samples. In both cases the boundaries are preferential paths for electrical conduction compared to the grain regions, but in the sample Al005-m the current contrast and the width of the boundary is lower (around 1.5 μm) and more homogeneous. This increase in conductivity at the grain boundary can be explained by a higher number of intra-gap states compared to the grain. The type of precipitates decorating the grain boundary plays a major role on the electrical properties of the sample. It is reasonable to assume that all the non-decorated grain boundaries affect the conductivity in the same way, and carbides and oxides are present with equal concentrations in both samples. Hence, the differences in

the current profiles of Figure 5.19 can be related mainly to contamination from the metallic impurities introduced in the feedstock, and iron enhances the conductivity with a higher degree compared to aluminum.

Figure 5.20 show local current-voltage measurements on the grain boundary and on the grain (averaged over 8 curves taken in different positions) for Fe and Al contaminated samples (Fe005-c and Al005-m). The Pt tip and the sample can be considered as a Schottky junction, and the resulting $I - V$ curve follows the thermionic emission model described in Equation 2.16. In both cases the tip-sample junctions are forward biased when the sample has a negative applied voltage. The forward current is higher at the grain boundaries, confirming the higher conductivity already observed in the current maps. The $I - V$ curve on the GB in Figure 5.20-d also shows an electrical breakdown voltage lower than 10 V.

The two $I - V$ curves of Figure 5.20-b were fitted with a parametric function that follows the thermionic emission model:

$$I = \alpha \left(e^{-\beta V} - 1\right) - \gamma \tag{5.1}$$

where α is the saturation current $I_S = AA^*T^2 exp\left[-\frac{q\phi_B}{k_B T}\right]$, the exponential factor β is related to the ideality factor n of the Pt/Si Schottky nano-diode, and γ is an additional current term related to the surface conduction. The barrier height ϕ_B was calculated as $\frac{k_B T}{q} ln\left(\frac{AA^*T^2}{\alpha}\right)$, using $A^* = 112$ A cm^{-2} K^{-2}, and $T = 300$ K. The area of the Schottky junction A was estimated as πr_{tip}^2, with the tip radius $r_{tip} = 20$ nm.

The barrier height values on the grain and on the grain boundary estimated from the fit are reported in Table 5.2, indicating a lowering of the potential barrier of approximately 0.1 eV at the GB, that results in a higher conductivity.

	Grain	**Grain Boundary**
ϕ_B	(0.5884 ± 0.0005) eV	(0.4883 ± 0.0002) eV

Table 5.2: Schottky barrier height on grain and on grain boundary, estimated from an exponential fit of the curves in Figure 5.20-b.

Discussion

Lal *et al.* [59] report similar values for the barrier height (0.59 eV, 0.54 eV, and 0.49 eV) from $I - V$ curves measured on similar samples as-deposited and after

annealing at 500 and 600 °C, respectively, indicating that the thermal annealing causes an increase in the interface state density, leading to a decrease in the barrier height, with the formation of stable iron disilicide β-$FeSi_2$. In other studies on a Cz low-doped ([B]=10^{14} cm^{-3}) silicon bi-crystal with a Σ25 GB, the sample face was iron plated, heat treated (1200°C for 3 hours) and then cooled. This process induced the formation of iron precipitates, giving a barrier height of 0.48 eV [60]. Similarly, the deposition of iron on n- and p-type silicon led to the formation of 18 to 35 nm thick layer of β-$FeSi_2$. Using silver paste as back contact to do $I-V$ measurements, it was found that β-$FeSi_2$ is a p-type semiconductor with high carrier density (on the order of 10^{18} cm^{-3}) [61].

The presence of this particular type of iron disilicide precipitate might explain the high current contrast between the grain and the GB. Single impurity atoms in a semiconductor introduce band-like states within the bandgap, affecting the carrier lifetime as schematically explained in Figure 2.5. On the other hand, there can be nucleation and coarsening of metallic precipitates, that have a metal-like density of states, their own Fermi level and work function. There is a formation of an internal Schottky junction with the Si matrix and a space charge region around the precipitate that determines the capture rate of the carriers.

The shape of a current profile close to the grain boundary can be justified with a theoretical model that assumes a redistribution of charge density due to a Coulombic potential introduced by a spherical and positively charged (Q) precipitate of radius R_p that is just below the oxide layer (Figure 5.21). If the precipitate is at the origin, R becomes the distance between the tip and the center of the precipitate.

The hole density profile is affected by the charged precipitate and it is assumed to have the shape $p(R) = -\frac{c}{R^2}$. The current density J is given by the usual drift term and diffusion term, but the precipitate introduces an additional electric potential $F(R)$ that modifies the drift term:

$$|J| = -eD_p\frac{dP}{dR} + e\mu_p pF(R) + e\mu_p p_0\frac{V_{sample}}{t} \tag{5.2}$$

where D_p is the hole diffusion coefficient in silicon, μ_p is the hole mobility, V_{sample} is the applied voltage, t is the thickness of the sample (≈ 180 μm) and p_0 is the hole density inside the grain.

The Coulombic potential is given by the charge Q of the precipitate and by the

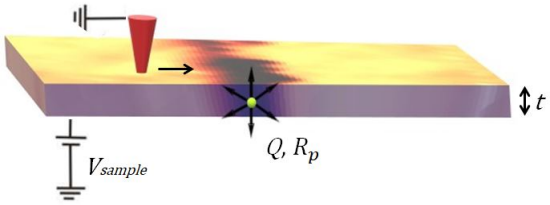

Figure 5.21: Schematic of the tip-sample system in a region close to a grain boundary. The charged iron precipitate (yellow) that decorates the grain boundary is introducing a Coulombic potential in the system, inducing a redistribution of charges that changes the current flowing between the Pt tip (red) and the sample. The sample was colored with the same color scheme of the C-AFM current maps: the darker region in the center represents the grain boundary, with higher conductivity compared to the neighboring grains.

carrier density integrated for $R > R_p$:

$$F(R) = \frac{1}{4\pi\epsilon_s R^2}\left[Q + 4\pi e\int_{R_p}^{R}(p - n - N_a)\, r^2 dr\right] \tag{5.3}$$

but, as the sample is p-type, it is possible to approximate $p - n - N_a \approx p$, so Equation 5.3 becomes

$$\begin{aligned} F(R) &= \frac{1}{4\pi\epsilon_s R^2}\left[Q + 4\pi e\int_{R_p}^{R} p(r) r^2 dR\right] \\ &= \frac{1}{4\pi\epsilon_s R^2}\left[Q - 4\pi e\int_{R_p}^{R} c dR\right] \\ &= \frac{1}{4\pi\epsilon_s R^2}\left[Q - 4\pi ec\,(R - R_p)\right] \end{aligned} \tag{5.4}$$

Combining Equations 5.2 and 5.4, the expression for the absolute value of the current density as a function of the distance R from the precipitate becomes

$$|J| = \frac{1}{R^3}\left(-2D_p ec + \frac{\mu_p e^2 c^2}{\epsilon_s}\right) - \frac{1}{R^4}\frac{\mu_p ec}{4\pi\epsilon_s}\left(Q + 4\pi ecR_p\right) + e\mu_p p_0 \frac{V_{sample}}{t} \tag{5.5}$$

Figure 5.22 shows a current profile across the grain boundary in sample Fe005-c, that was fitted with the function

$$|I| = |J|A = \left(\frac{\alpha}{R^3} + \frac{\beta}{R^4} + \gamma\right)\pi r_{tip}^2 \tag{5.6}$$

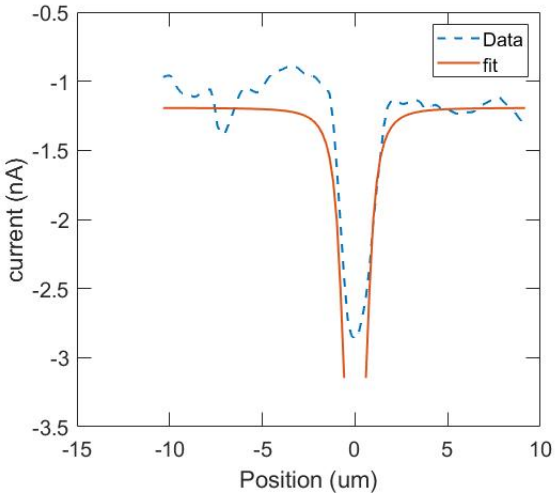

Figure 5.22: Current profile across a grain boundary and non-linear fit with Equation 5.6. The current $I(R)$ tends to a constant value for $|R| \gg 0$ (in the grain region) and is enhanced close to the precipitate at the grain boundary ($|R| \approx 0$).

where the parameters α, β, and γ can be extracted from Equation 5.5. The estimated values of the parameters are $\alpha = (1.3 \pm 0.3)$ nA μm^3, $\beta = (-0.55 \pm 0.17)$ nA μm^4, and $\gamma = (1.19 \pm 0.07)$ nA.

From these values, the shape of the hole density profile and the properties of the precipitate can be estimated. The value of α gives $c = (3.3 \pm 0.3) \times 10^8$ m^{-1}, and γ gives $p_0 = (2.37 \pm 0.14) \times 10^{15}$ cm^{-3}. The hole concentration in the grain region is one order of magnitude lower than the one estimated from the $C - V$ spectroscopy, but the grain might be depleted from the contact with the Pt tip.

From β the following expression between the charge and radius of the precipitate is found:

$$Q = 2.427 \times 10^{-16} - 6.568 \times 10^{-10} R_p \tag{5.7}$$

The profile has a resolution of ≈ 170 nm, and the tip radius is 20 nm, so it is not possible to model the current profile for $R < R_p$: the position of the tip is not precise enough to give more information on the dimension of the precipitate. It was chosen to make an assumption to simplify the relation in Equation 5.7. As it is known that the sample is contaminated with iron, it is very likely that the precipitate is a β-$FeSi_2$, a common precipitate in silicon that segregates at the grain boundaries and just below the surface oxide layer, therefore explaining the strong current contrast on the C-AFM maps. Another iron disilicide phase, α-

$FeSi_2$, is stable at temperatures between 1220 and 915°C, but at room temperature it becomes metastable and decompose very slowly to β-$FeSi_2$ with a transition temperature of 982°C [62]. The presence of a β-$FeSi_2$ also explained the barrier lowering seen with the current-voltage measurements, so it is a valid starting assumption.

The dimension of this particular precipitate was previously measured in literature: the observed β-$FeSi_2$ radii are almost constant in as-grown wafers and in low temperature annealing or phosphorous diffusion gettering treated wafers [63] and they were seen to depend on the feedstock iron contamination and on the position of the wafer in the ingot [64]. However, R_p always takes values between 5 and 30 nm, with average values of 15 to 20 nm. If this is the expected size of the precipitate, the second term in Equation 5.7 is negligible compared to the first term, giving a charge on the order of 2×10^{-16} C.

The carrier density ρ_{prec} of a spherical precipitate can be expressed as:

$$\rho_{prec} = \frac{Q/e}{\frac{4}{3}\pi R_p^3} \tag{5.8}$$

and the reported values are between 10^{18} and 10^{20} cm^{-3}. Assuming $\rho_{prec} = 3 \times 10^{19}$ cm^{-3} [65] and using Equation 5.7, the precipitate radius takes a value of $R_p \approx 22.5$ nm, and the charge is $Q \approx 2 \times 10^{-16}$ C. The chosen value of ρ_{prec} is crucial for the estimation of the radius, however, with ρ_{prec} in the range between 10^{18} cm^{-3} and 10^{20} cm^{-3}, the estimated precipitate radius ranges from 15 to 67 nm, in agreement with literature values [63, 64, 65].

Chapter 6

Conclusions

Combining microstructural analysis with an electrical characterization of the grain boundaries gives a good insight into the relevant properties of mc-Si wafers for photovoltaic applications. In this study, mc-Si wafers contaminated with iron or aluminum located at different lateral positions and height of directionally solidified ingots were investigated.

A coarsening of grains along the ingot height was observed and quantified by an increasing average grain size and a decreasing total grain boundary density. The most common Coherent Lattice Sites boundary in mc-Si identified with Electron Backscatter Diffraction is $\Sigma 3$, together with other $\Sigma 3^n$ boundaries.

Even if the samples were not passivated, it was possible to perform qualitative measurements of the lifetime of minority carriers with Microwave Photoconductance Decay, and especially detect areas of low lifetime called red zones. The samples at the corner of the ingot showed a red zone due to the crucible and coating contamination, that gradually disappeared while going to the top of the ingot. Another area of low lifetime originates from the dislocation clusters and from the segregated impurities that decorate the dislocations. Both defects (dislocation and impurities) increase in number while going to the top. The top iron contaminated sample with a lateral position at the corner of the ingot shows a higher number of low-lifetime areas with respect to the aluminum contaminated sample from the middle of the ingot.

Aluminum contacts were evaporated on a selected sample to form a Schottky diode, in order to measure current-voltage and capacitance-voltage characteristics at low temperatures inside a cryostat. From a $C - V$ spectroscopy it was possible to estimate the doping concentration of the wafer, whose value was later confirmed by Glow Discharge Mass Spectrometry measurements on parallel samples. Stable

electrical connections are necessary to make electrical measurements in a wide temperature range, meaning that the employed conductive paste should not liquefy when high voltages are applied across the diode, and all the components of the device should have a good thermal and electrical conductivity at low temperatures. A mixture of indium and gallium together with a bi-component silver paste resulted to be a good back contact, as long as the silver did not touch the silicon, otherwise the device behaved as a double Schottky junction. For low temperature measurements, conductive carbon tape and a copper sample holder were used as a substrate, with phosphorous bronze clamps used as electrical connections and to reach a good mechanical stability of the system. Two types of probes were used to connect the device to a source measure unit, metallic tips on micro-manipulators and copper wires soldered to the clamps, and the two systems strongly influenced the measured values of current.

Electrically active grain boundaries were characterized by means of Conductive Atomic Force Microscopy, showing that iron contamination is more detrimental and affects more strongly the electrical properties of the wafers, compared to aluminum contamination. The conductivity of the sample is enhanced in a region around the grain boundaries, extending up to 3 micrometers: as the geometrical width of a grain boundary is of few atomic radii, this effect is explained by the segregation of iron or iron silicide precipitates, and not to the intra-gap states introduce by the GB itself. The increasing intensity of the current flowing between the sample and the tip of the microscope at the grain boundary, as measured by C-AFM profiles, was justified by the presence of a charged spherical precipitate that introduces a Coulombic potential, inducing a redistribution of the charge density. The size and the carrier density of the precipitate estimated with this theoretical model suggest that the precipitate is a β-$FeSi_2$, a iron silicide phase that is commonly observed in multicrystalline silicon.

The results of this characterization can lead to a better understanding of the role of the iron segregating at the grain boundaries in silicon, which is one of the main cause of conversion efficiency reduction in photovoltaic cells based on mc-Si.

Further work

The characterization of these samples could be integrated with other structural and compositional techniques, such as Glow Discharge Mass Spectrometry (GDMS) and X-Ray Diffraction (XRD). With GDMS it is possible to verify the distribution of impurities along the ingot height, which was just estimated with the Scheil's

equation. XRD can determine the cristallinity and the phase composition of the samples, in particular the presence of β-$FeSi_2$ precipitates that segregate at the grain boundaries, and are assumed to introduce recombination centers that reduce the lifetime of charge carriers and increase the electrical activity of the defect. The electrical characterization could be further determined by means of Deep Level Transient Spectroscopy (DLTS), in order to identify and quantify the energy level and the density of trap states, giving an estimation of the concentration of electrically active impurities.

As the low lifetime regions in the μ-PCD maps are thought to be related to dislocation clusters, the samples could be etched in Sopori etch in order to reveal dislocations, and the dislocation density can be counted by detecting diffusely scattered light from the etch pits. The characterization of dislocations can be performed also with a Transmission Electron Microscope or with XRD.

Another possibility is to study and characterize directionally solidified mc-Si ingots, that are simultaneously contaminated with iron, aluminum, and other common impurities found in mc-Si ingots, such as carbon, oxygen and transition metals to study the non-linear effects of several combinations of contaminants. The intentional contamination should be at higher levels, for instance 1000 ppm. By using this higher level of feedstock contamination it is possible to understand better how these atoms segregate and distribute in the ingot, in order to improve the refining processes in the production of mc-Si ingots. Having higher contamination levels will also allow to easily measure the impurity concentration, which would be much above the detection limits of the techniques.

These experimental results can be compared with numerical simulations that predicts the distribution of impurities along the ingot height and in the radial direction, considering the different effective segregation coefficients and the diffusion from the coating and the crucible. Further theoretical models can be done to describe the nucleation and coarsening of the precipitates and to predict the size distribution.

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