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OFF-STATE RELIABILITY OF pGaN POWER HEMTs

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Il più grande ringraziamento va ai miei genitori. Grazie per aver creduto sempre in me e per aver appoggiato ogni mia scelta.

Thank you all,
Maurizio

Abstract

The concern for climate changes and the increase in the electricity demand turned the attention towards the production, sorting and use of electric energy through zero emission (CO_2) and highly efficient solutions (e.g. for electric vehicle), respectively. In such a scenario, power converters and/or inverters play a fundamental role, since they represent the main core of power applications. As a consequence, the need for high performance, reliable and low cost power transistors is increasing as well. The most used semiconductor materials for power transistors are three: silicon (Si), silicon carbide (SiC) and gallium nitride (GaN). Among all of them, gallium nitride, seems to be the most promising candidate for the next generation of devices for power electronics, thanks to its excellent properties and comparable cost with respect to Si counterpart. The main and most adopted GaN-based device is the high electron mobility transistor (HEMT). In particular, in the case of switching power applications, HEMTs are repeatedly switched between high current on-state and high voltage off-state operation. For both operating modes a good reliability must be guaranteed.

This thesis is focused on the reliability issues related to the off-state operation. The results have been obtained during a six months research period at *imec* (Leuven, BE) on 200V p-GaN gate AlGaN/GaN HEMTS. Different devices have been investigated, differing for gate-to-drain distance, field plates lengths, AlGaN and GaN layers properties. Time-dependent dielectric breakdown and hard breakdown tests have been performed in combination with TCAD simulations. It has been demonstrated that the gate-to-drain distance (L_{GD}) impacts the breakdown voltage and the kind of failure mechanism. If $L_{GD} \leq 3\mu m$ the breakdown occurs through the GaN channel layer due to short channel effects. In this case, by reducing the thickness of the GaN channel layer such behaviour can be attenuated, eventually leading to longer time-to-failure. If $L_{GD} \geq 4\mu m$ the breakdown occurs between the 2DEG and the source field plates, where the properties of the AlGaN barrier layer (i.e. thickness and Al concentration) and the field plates configuration play the main role on the time-to-failure.

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Chapter 1

Introduction

With increasing world population and the request for higher living standard, the demand for electricity is increasing as well. The worldwide electricity can be produced by the adoption of different sources as shown in figure 1.1, with fossil fuels representing the most adopted ones.

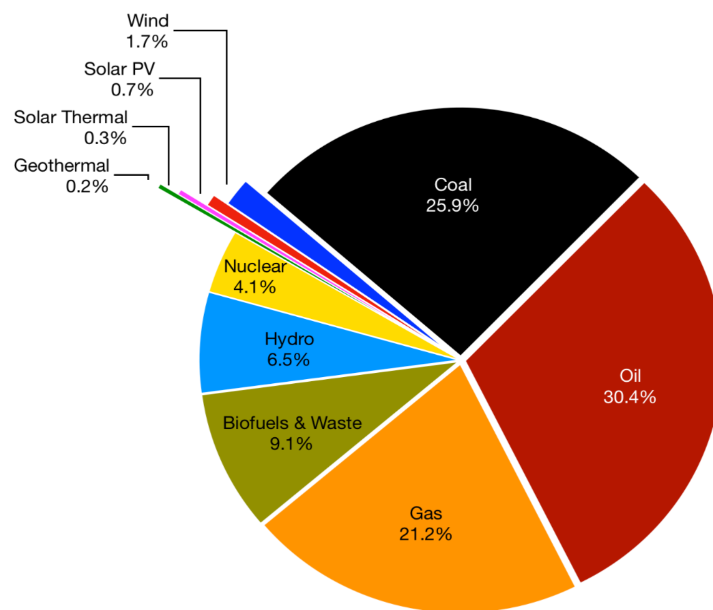


Figure 1.1: *Worldwide electricity production by various sources [1].*

The earth has large reserves of fossil fuels, however, their adoption results in waste products, which added to those produced for transport, domestic heating, etc. represent the main source of pollution that contribute

to climate change problem. To this purpose zero-emission solutions are being implemented to protect the environment (e.g. electricity production by means of renewable sources and replacement of powered fuels vehicles with electric/hybrid engines).
In this scenario, power electronics plays an important role since most of the electricity is controlled by semiconductor power devices. Today, with the advancement of technology, the size and the price of semiconductor power devices are decreasing, leading power electronics to cover a wide range of application fields such as aerospace, automotive, energy saving, industrial, commercial, smart houses, etc..

1.1 Semiconductor Power Devices Technologies

Until a few years ago, the semiconductor power devices market was completely dominated by the mature silicon (Si) technology because of the low cost and good reliability.However, with the increasing demand for lightweight, compact and evermore efficient power applications, the intrinsic limits of Si (i.e. limited switching frequency, blocking voltage and temperature capability [2]) arise the need to move towards wide bandgap semiconductors, like gallium nitride (GaN) and silicon carbide (SiC), that exhibit superior materials properties compared to silicon counterpart.

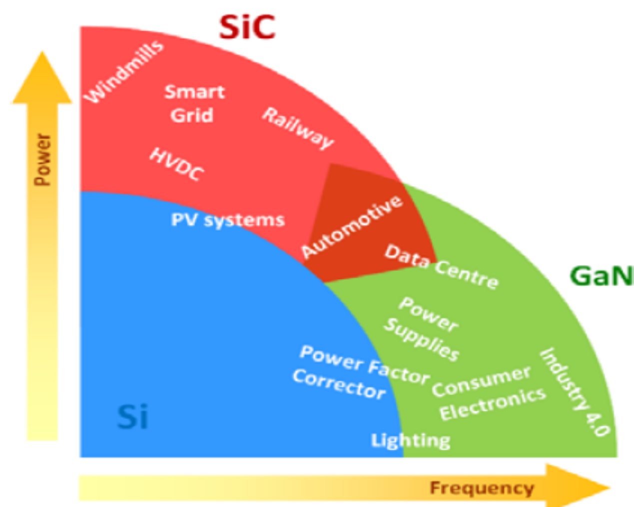


Figure 1.2: *Application fields of the different technologies (Si, SiC and GaN) as a function of operating frequency and power [3].*

In figure 1.2 the application fields of Si, SiC and GaN power devices are shown as function of the operating power and switching frequency. In particular,SiC and GaN are the best candidates for high voltage and high frequency operation, respectively, while silicon still preferred for low voltage and low frequency operation.The reason of this division will be further supported in the section 1.1.1.

1.1.1 Material Properties

The application field of Si, SiC and GaN strongly depend on their intrinsic material properties which are useful for switching power applications. In particular the most important characteristics are [4], [2]:

- bandgap: wider bandgap implies lower intrinsic carrier concentration (n_i), which is strongly dependent on the temperature and correlated to leakage current [2]. As a consequence, wider bandgap allows devices to operate at higher temperatures;
- critical electric field: higher critical field means that the impact ionization, hence the avalanche-induced breakdown, occurs at higher voltages;
- thermal conductivity: larger thermal conductivity implies that the device can withstand a higher power density;
- carrier velocity saturation: higher carrier saturation velocity implies a higher frequency of switching at higher voltages (Jhonson's FOM [4]).
- electron mobility: higher electron mobility leads to lower resistivity and conduction losses;

Table 1.1 shows the various key material parameters for power electronics of the different materials for power electronics. GaN and SiC feature a bandgap ~3 times higher than Si which lead to have higher electric breakdown field (E_C) and lower intrinsic carrier concentration useful to have negligible leakage currents at high operation temperature. Among all the materials, SiC has the highest thermal conductivity making it the best choice for high voltage and power operation, while, GaN is the best candidate for high frequency and high current operations since it has the highest electron mobility (μ) and velocity saturation (v_{sat}). Finally, for low voltage and frequency applications silicon is the best choice thanks to its low cost and reliability, even though it has less attractive features for power electronics compared to GaN and SiC.

Parameter	Units	Si	GaAs	4H-SiC	GaN
Bandgap (E_G)	eV	1.12	1.42	3.26	3.49
Intrinsic carrier concentration (n_i)	/cm^3	1.4x10^{10}	2.1x10^{-6}	8.2x10^{-9}	1.9x10^{-10}
Electric breakdown field (E_C)	MV/cm	0.23	0.4	2.2	3.3
Saturated electron velocity (v_{sat})	cm/s	1x10^7	1x10^7	2x10^7	2.5x10^7
Thermal conductivity (k)	W/cm-k	1.5	0.5	3.8	1.53
Electron mobility (μ)	cm^2/V-sec	1400	8500	950	1800
Relative dielectric constant(ϵ_r)	-	11.8	12.8	9.7	9

Table 1.1: *Comparison of material properties among different semiconductors [4].*

1.1.2 Figure Of Merit (FOM)

The choice of a semiconductor for the realization of a power device is made considering several figures of merit [5], which are related to the material properties discussed in the section 1.1.1. The Johnson's figure of merit (JFOM) [6] defines a value for the high frequency handling capability of a semiconductor being proportional to the saturation velocity and critical electric field:

$$JFOM = \frac{E_C \cdot v_{sat}}{2\pi} \tag{1.1}$$

The high power handling capability is described by Baliga's figure of merit (BFOM) [7] that quantifies the conduction losses in DC operation, which is calculated based on the relative electric permittivity (ϵ_r), electron mobility (μ) and bandgap (E_G):

$$BFOM = \epsilon_r \cdot \mu \cdot E_G^3 \tag{1.2}$$

Instead, to quantify the conduction losses in high frequency operation, and therefore, to evaluate the high power and frequency performance the Baliga's High Frequency FOM (BHFFOM) is used [5]:

$$BHFFOM = \mu \cdot E_C^2 \tag{1.3}$$

Considering these three FOMs, among the semiconductors taken into consideration, gallium nitride has the best performance although silicon carbide features similar FOMs, while, silicon and gallium arsenide have too low FOM for power applications.
SiC is the semiconductor that has the best Keyes FOM (KFOM) [5] because takes into account the thermal conductivity (k) and it describes the thermal performance of the devices during switching operation:

$$KFOM = k \cdot \sqrt{\frac{c \cdot v_{sat}}{4\pi\epsilon_r}} \tag{1.4}$$

1.1.3 Breakdown Voltage and On Resistance

For power applications the most important parameters are the breakdown voltage (V_{BD}) and the on resistance (R_{ON}) to have high blocking voltage capability and low conduction losses, respectively. In fact, their adoption is useful to compare the performance of different power device technologies and architectures by using the relationship ${V_{BD}}^2/R_{ON}$ [8]. Power devices must be able to support high voltages across a depletion region formed, in most case, at a P-N junction. Therefore, to analyze the relationship between V_{BD} and R_{ON} a simple PN junction (figure 1.3 (a)) can be considered.

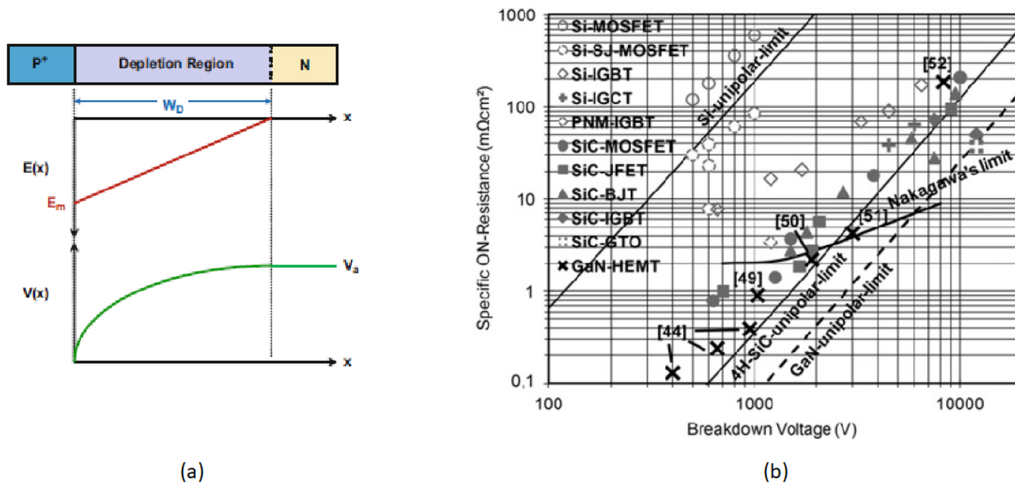


Figure 1.3: *Electric field distribution in a reverse biased P^+ /N junction [8] (a) and specific ON-Resistance versus breakdown voltage (theoretical limits) of different semiconductor (b) [9] .*

When the junction is reverse biased (positive voltage applied to the N side) the depletion region expands mainly in the N side (since the P region

is strongly doped) with the consequently generation of a strong electric field. As shown in figure 1.3 (a) the peak of the electric field occurs in the proximity of the PN junction and, according to Poisson's equation, it can be computed as follow [8]:

$$E_{max} = \frac{qN_D W_D}{\epsilon_0 \epsilon_r} \tag{1.5}$$

where N_D and W_D are the doping concentration and the maximum extension of the depletion region, while,ϵ_0 andϵ_r are the dielectric vacuum constant and the dielectric constant relative to the material, respectively.
Any electrons or holes that enter the depletion region are swept out by the electric field and as the electric field increase the mobile carriers are pushed out with a higher velocity. If the electric fields is sufficiently high, electrons and holes acquire sufficient kinetic energy to create new electron-hole pairs due to energy loss caused by interaction with the lattice. This phenomenon, namely, *impact ionization* is a multiplicative mechanism which produces an increasing amount of mobile charges with a consequent increase in the current through the depletion region. This latter leads to the *avalanche breakdown* that strongly depends on the applied electric field and it occurs when the E_{max} approaches to the critical electric field (E_C). The occurrence of the latter condition defines the breakdown voltage, defined as:

$$V_{BD} = \frac{1}{2} E_C W_D = \frac{1}{2} \frac{qN_D W_D^2}{\epsilon_0 \epsilon_r} \tag{1.6}$$

The specific ON resistance, which is mainly dominated by the resistive component of the N-drift region in ON-State operation is equal to:

$$R_{ON,sp} = \rho W_D = \frac{W_D}{q\mu_n N_D} \tag{1.7}$$

Replacing W_D and N_D from Eq. 1.5 and Eq. 1.6 into Eq. 1.7 it is possible notice the mutual dependence between ON-resistance and breakdown voltage::

$$R_{ON,sp} = \frac{4V_{BD}^2}{\epsilon_0 \epsilon_r \mu_n E_C^3} \tag{1.8}$$

Being R_{ON} and V_{BD} dependent from the intrinsic properties of the materials, it is possible to analytically calculate the theoretical limits for each semiconductor-based technology, as shown in figure 1.3 (b). By observing Fig. 1.3(b), it is worth noting that the theoretical limits are computed considering only the ON resistance of the drift region, which dominant but not the only one, devices are far away from their theoretical limits. Moreover, in

the case of GaN-devices this difference can be even larger since the breakdown voltage during OFF-state operation can be caused by additional failure mechanisms (detailed in the next chapter), anticipating the breakdown induced by impact ionization.

Chapter 2

III-N materials and devices

Gallium nitride and its related alloys (e.g. $Al_xGa_{1-x}N$) are promising candidates for the next generation of high power and high frequency devices due to their excellent material properties. As already mentioned, the wide band gap of these materials leads to have a low intrinsic concentration and, consequently, a low leakage current that allows high temperature operation. Another important feature of GaN is the high breakdown voltage which results in the possibility to fabricate smaller devices, hence characterized by lower on resistance and lower parasitics (mainly capacitances) which can be detrimental for both static and dynamic operation operation mode. Compared to their silicon counterparts, GaN-based devices have a higher switching frequency due to combined effect of higher carriers velocity saturation and smaller area, and a lower resistance due to the high mobility of the two dimension electron gas (2DEG) that appears in the AlGaN/GaN heterostructure [10],[11]. The AlGaN/GaN heterostructure is the main core of the GaN transistors, namely high electron mobility transistor (HEMT), where the electron current flows through the 2DEG from source to drain contacts.
Producing an emerging micro-scaled semiconductor device, the control and mastering of thin film techniques are essential. This includes metallization, dielectric layers, passivation layers or high quality crystalline functional layers. The crystalline layers are deposited by epitaxy starting from the substrate. Usually, the substrate and the crystalline layer are made of different materials characterized by different lattice constants and thermal expansion coefficients. This situation is usually called heteroepitaxy that leads to consequences like the formation of threading dislocation, buildup of strain, and reliability issues. These physical consequences, that involve reliability problems for the devices, could be reduced using homoepitaxy (epitaxy with same materials) but, unfortunately, nature does not provide GaN bulk crystal. Although some GaN wafers grown with HVPE [12] showed extremely low

residual impurity concentration , the challenges of high cost and small wafer diameter remain open. Moreover, homoepitaxy has a lot of mismatch issues due to the different growth processes of the GaN layer. The only alternative is to look for foreign materials for substrates that have lattice parameters and crystal structures and orientation close to GaN material. Native substrates are mandatory only for some specific applications who claim high reliability (like in the case of blue and ultraviolet semiconductor lasers) since optimizing the design of the devices it is possible to achieve a good reliability [13].
Despite its incredible characteristics, gallium nitride has many issues as the presence of nitrogen or the lack of a native substrate that will be discussed in along this chapter.

2.1 Substrates for III-N Epitaxy

The choice of substrate and material for GaN-based devices strongly depends on the field of application. Today, GaN wafers can be manufactured, but, have high costs and are only avaiable with limited wafer diameters, maximum 2 inch. GaN is very difficult to growth as a single crystal since it is strongly covalent bonded and contain nitrogen (N) that cannot be melted due to its high melting point above 2000°C and high equilibrium pressure around 60 kbar; moreover, the solubility of nitrogen in a pure gallium melt is very low [14]. This makes it impossible to grow a GaN crystal with classical melt-based methods like Czochralski pulling, vertical gradient freeze technique, etc. Today, the GaN wafers (expensive and size-limited) are manufactured with solution growth methods (addition of solvent to improve the solubility) and the GaN is crystalized from the vapor phase with two main methods: HVPE (hydride vapor phase epitaxy) and OVPE (oxide vapor phase epitaxy).
To overcome these limitations and to reduce the overall device costs, GaN devices are currently and mainly grown on foreign substrates.
For optoelectronics, sapphire is the best choice since it has a good match to GaN in terms of lattice constants and thermal expansion coefficient. Furthermore, sapphire substrates are transparent, cheap and they have the same threading dislocation densities as the Si and SiC substrates (2.1). As disadvantages, sapphire has low thermal conductivity and insulating properties, making it less attractive for power electronic applications in order to prevent overheating and premature device failure [15]. Sapphire wafers exist in large diameters, but layers growth on large area is challenging due to the wafer bowing and/or cracking after cooling because of tensile stress for between epitaxial layers.

	Sapphire	SiC	Si	GaN
Lattice mismatch (percentage)	16	3.1	-17	0
Linear thermal expansion coefficient (x10^{-6} K^{-1})	7.5	4.4	2.6	5.6
Thermal conductivity (W cm^{-1} K^{-1})	0.25	4.9	1.6	2.3
Cost	Low	High	Very Low	Very High

Table 2.1: *Properties for different substrates for GaN epitaxy [14], [16].*

Among the three foreign substrates reported in table 2.1, SiC is the one with the best matched mechanical properties with GaN. It is available both as n-type and semi-insulating material and it has high thermal conductivity which makes it the best candidate for electronic applications with high power densities. As drawbacks, it has very high costs of fabrication and and the largest available wafer diameters are 6 inch.
For GaN heteroepitaxy, the most used material for the substrates is silicon because of its lowe cost and compatibility with CMOS technology. Epitaxial growth of GaN directly on Si substrates is more challenging than heteroepitaxy on sapphire or silicon carbide due to large lattice and thermal mismatches that results in large strain accumulation in the upper III-N epilayers. This problem, if not properly monitored, leads to wafer deformation, cracking up to breakage, threading dislocations, etc. However, the advantages of a low substrate cost, large substrate diameter availability (up to 12 inches), reasonable thermal conductivity and the possibilities of the co-integration with Si-CMOS electronics, make Si substrate the preferred choice for a large set of power electronics (mostly medium range voltage) [17].

2.2 III-N Crystal Structures and Polarization Effects

Group III nitrides compound (III-N) exist in different crystal forms like zincblende, rocksalt and wurtzite structures [11]. Among these forms the wurtzite crystal structure features the highest thermo-dynamical stability. Wurtzite-type GaN is composed of two hexagonal lattices of N and Ga as shown in figure 2.1, where c-axis is the most preferred growth direction. GaN

can be grown with two different polarities, i.e. Ga-face and N-face shown in Fig. 2.1.

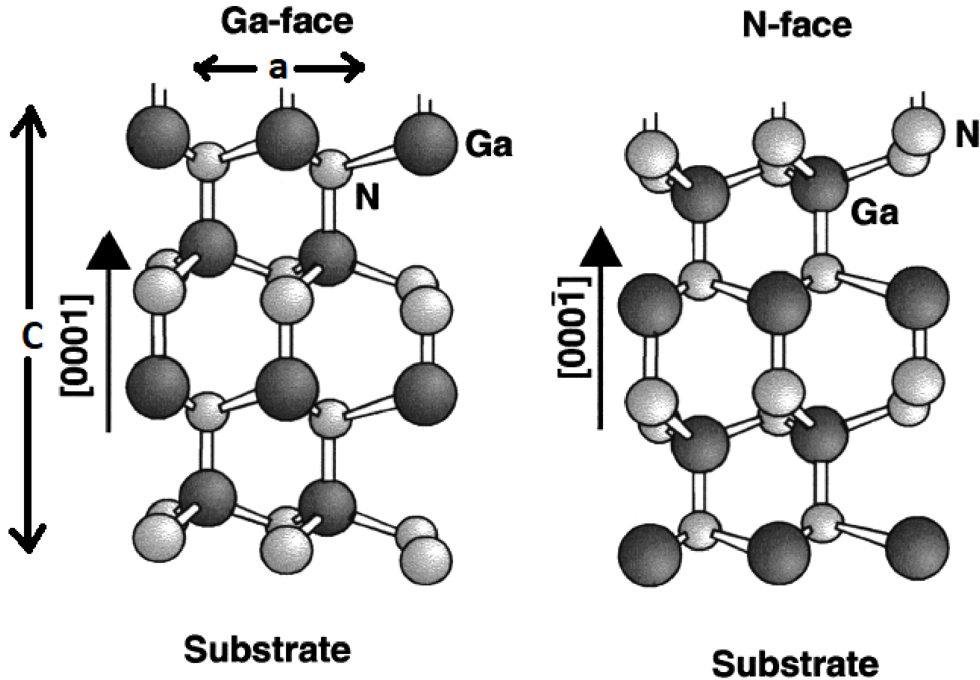


Figure 2.1: *Crystal structure of wurtzite Ga-face and N-face GaN [11]* .

In the case of Ga-face, the bonds along the [0001] direction are directed from Ga to N atoms, while, for N-face GaN the bonds along the [000$\bar{1}$] direction are from N to Ga atoms. The growth of Ga-face GaN is usually carried out using Metal Organic Chemical Vapor Deposition, while N-face GaN can be grown by Molecular Beam Epitaxy [13]. Both N-face GaN and Ga-face GaN possess spontaneous polarization (P_{SP}) properties along c-axis due to charge transfer between atoms with different electronegativity, as in the case of Ga (lower) and N (higher) [10], [11].
The III-nitride materials cover a very large range of bandgap energies, starting from infrared (InN with a bandgap of 0.7 eV) up to the extreme ultraviolet (with AlN having a bandgap of 6.2 eV), as shown in figure 2.2. This is possible by varying the concentrations of the group-III elements (Al, Ga, In) in the crystal alloy with a composition $Al_xIn_yGa_{1-x-y}N$ with x,y and x+y between 0 and 1.

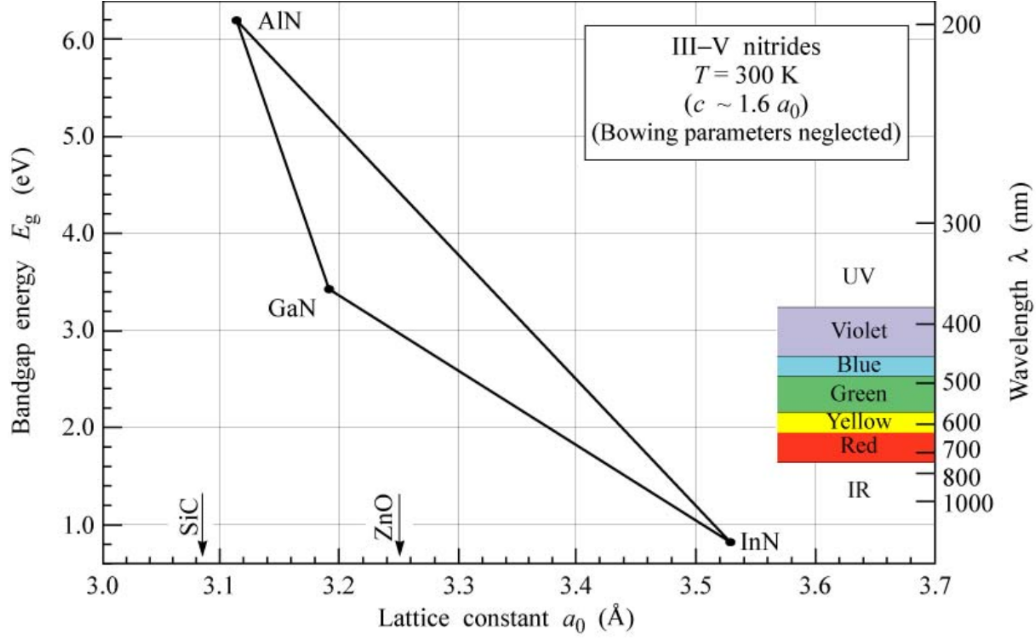


Figure 2.2: *Bandgap versus lattice constant of III-N materials [18].*

In GaN-based devices is common to find heterostructures with different lattice constant, for instance AlGaN/GaN heterojunction in HEMTs. When the AlGaN is grown on the GaN layer the different lattice constant leads to a mechanical stress causing a new type of polarization along c-axis, namely piezoelectric polarization. The latter is due to the lattice constant adjustment of the thinner material (AlGaN in this case). The amount of piezoelectric polarization is given by [10], [11]:

$$P_{PE} = 2\frac{a - a_0}{a_0}(e_{31} - e_{33}\frac{C_{13}}{C_{33}}) \tag{2.1}$$

where e_{31} and e_{33} are piezoelectric constants, C_{13} and C_{33} are the elastic deformation constants, a_0 and a are the horizontal lattice constant before and after the mechanical stress, respectively. The orientation of the spontaneous polarization is defined positive from Ga (cation) to nearest nitrogen atom (anion) along the c-axis, whereas the piezoelectric polarization is assumed negative for tensile and positive for compressed strained AlGaN barriers. Therefore, both polarizations are parallel in the case of tensile strain, while antiparallel in the case of compress strain of the AlGaN barrier. In the case of the AlGaN/GaN heterostructures, where the AlGaN barrier is grown on GaN layer, both polarizations point in the same direction and the value of total polarization is the sum of the piezoelectric and spontaneous polarization.

The presence of these polarizations lead to creation of a channel of electrons at the AlGaN/GaN interface, namely two dimensional electron gas (2DEG), without the application of external biases. Further details on the 2DEG formation are reported in the subsection 2.3.3.

2.3 Metal-Organic Vapor Phase Deposition for III-Nitride Epilayer Deposition on Si

The most suited technique for III-N epilayer deposition is the metal-organic chemical vapor deposition (MOCVD), also called metal-organic vapor phase epitaxy (MOVPE). By using this technique, the elements of the growing material are introduced in a reactor chamber in gaseous form, transported by a carrier gas like nitrogen (N_2) or hydrogen (H_2) or a mixture of both. Indeed, the atoms of a given material are introduced in the chamber as precursor, that, for the III elements are a combination of the III group metals with organic elements. The source compounds for gallium are typically trimethylgallium $(CH_3)_3Ga$ and triethylgallium $(C_2H_5)_3Ga$, while, the precursor for nitrogen is ammonia (NH_3) where the nitrogen atom is directly bonded to hydrogen atoms. These molecules are first thermally decomposed and then they react, in the gas phase, on the substrate's surface or on another III-N semiconductor layer. The epitaxial growth process is monitored thermodynamically, i.e., by setting temperature and pressure of both the substrate and ambient for the gas in the reactor. The difference between the two energies can provide etching of the below layer or growth of the semiconductor on the surface. Usually, for GaN growth the temperature of the process is around 1000^oC and the reactor pressure between 10 mbar and 200 mbar. It is important that there is always equilibrium between the gas phase composition and the vapor pressure of the molecules of the solid phase to avoid contamination, since any contamination in the gas phase induces contamination of the solid semiconductor material. The contaminants atoms, such as carbon and hydrogen, could come from the metal-organic precursor themselves and it requires a good control of the vapor pressure to reduce inclusion of this atoms in the solid phase. [19]
The residual impurities, formed during the MOCVD processes, can play an important role in the layer's conductivity since they can have donor or acceptor dopant behavior. Through MOCVD, a further intentional doping can be obtained by introducing other precursor in the initial gas mixture. The best choice for the p-type doping in GaN is the magnesium and, it is provided by the precursor biscyclopentadienyl magnesium (Cp_2Mg) [20]. While, the

n-type doping is obtained by silicon via addition of silane (SiH_4) or disilane in the chamber(Si_2H_6) [21]. In the GaN based HEMTs the active part of the devices don't need any doping, but, doping can be used for increase the resistivity of a given layer (e.g. buffer), to decrease the gate ohmic contact resistance (n-type doping) or to compensate the intrinsic n-type behavior of III-nitrides (p-type doping).

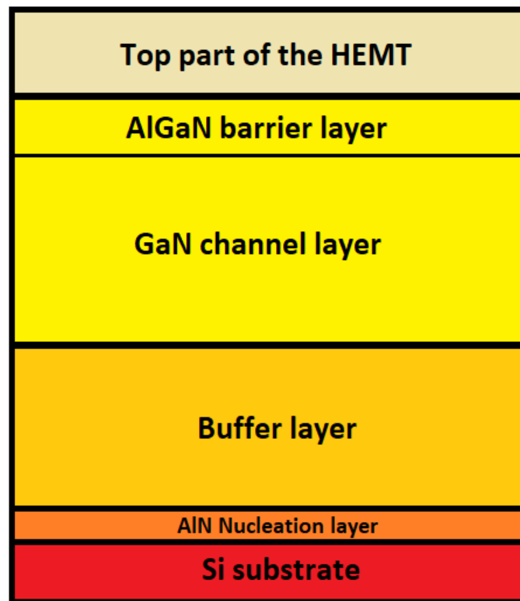


Figure 2.3: *General structure for an AlGaN/GaN HEMT device on Si.*

In the following subsections will be described, layer-by-layer, the structure of the GaN based later HEMTs on Si substrate, as shown in figure 2.3. The main parts are the following:

1. A nucleation layer to initiate the epitaxial growth on the foreign Si substrate.

2. A buffer stack to compensate mechanical differences between Si and GaN.

3. The AlGaN/GaN heterostructure with the final capping to protect the surface, also called passivation layer.

2.3.1 The Nucleation Layer

As discussed in the previous sections, there are many issues related to growing a high quality GaN crystal on Si substrate due to thermal and lattice mismatch. Monocrystalline silicon and GaN have a cubic and hexagonal crystal structure, respectively. This difference may lead to a roughness GaN/Si interface and consequent lower quality of the buffer microstructure [22]. Furthermore, at high temperature gallium easily diffuse into silicon substrate leading to gallium silicide formation. This phenomenon is called gallium melt-back etching and, to prevent it, the best solution is to deposit an AlN layer on the substrate [19].
The growth conditions and properties of the nucleation layer can influence the final GaN film quality and the breakdown voltage in HEMTs. Many studies reported that the electrical breakdown does not occur laterally but vertically [23]. This effect is attributed to vertical path for electron from ohmic drain contact to substrate due to multiple threading dislocations, a lateral conduction along the AlN/Si interface followed by another vertical conduction between substrate and source trough dislocations/defects. AlN layer thickness is the most important key parameter to improve the breakdown voltage and the crack densities into the upper III-N layers [24].

2.3.2 The Buffer Layer for Mechanical Stress Management

The nucleation layer is not sufficient to prevent cracking in the GaN channel layer or wafer bow during cool down of the wafer and, for this reason, it is necessary a buffer stack between AlN layer and the GaN channel for strain management. The growth of GaN directly on AlN showed some circular defects, probably due to silicon outdiffusion from substrate, that could act as stress concentrators and initiate the cracking [22]. One of the first adopted solutions was based on the interposition of a single AlGaN layer with a gradual decrease of Al concentration from the top to the bottom, as shown in figure 2.4 (a). This latter shows some circular defects close to the edge of the wafer very similar to those seen growing GaN directly on relatively thick AlN layer.
Another approach consists in the fabrication of a multiple layer buffer with a gradual relaxing of the strain due to the differences in lattice constants of the materials. One of the best method is called step-graded buffer [25] and consist in growing AlGaN layers with different Al concentrations, gradually lower from AlN to GaN , shown in figure 2.4 (b). This procedure is repeated from two to five times until finally a smooth and free-crack GaN layer can be

grown. This procedure leads to a gradually increase in the lattice constant and the quality of the final GaN layer improves by increasing the number of the AlGaN layers.

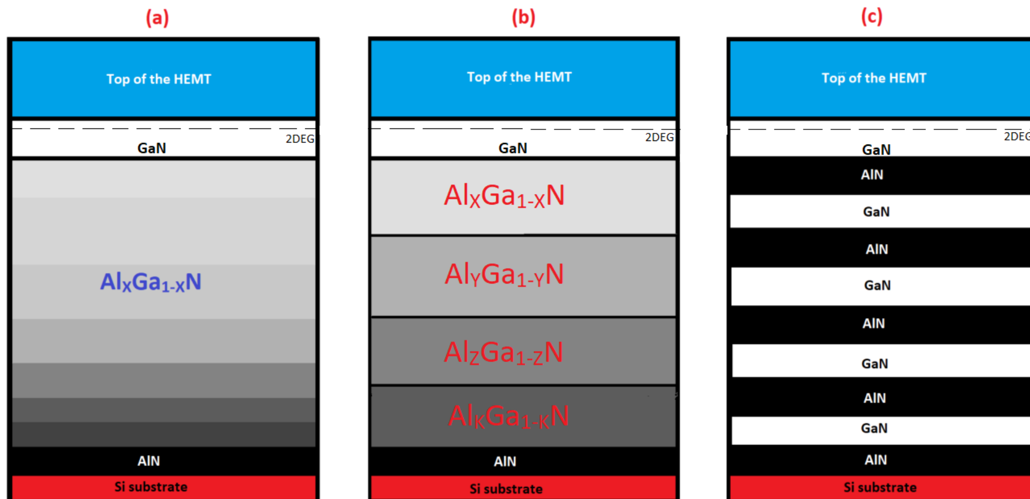


Figure 2.4: *Structure of HEMTs with different buffer stack on Si substrate: (a) graded AlGaN layer, (b) multiple step-graded AlGaN layers where $x<y<z<k$, (c) AlN/GaN superlattice buffer.*

Besides the step-graded buffer, the most commonly used approach is the superlattice buffer, as shown in figure 2.4 (c). The superlattice stack is manufactured alternating dozens of relative thin GaN and AlN layers [26]. Also in this case, by increasing the number of interlayers the final GaN crystal quality increases as well, meaning that there is a higher probability that vertically propagating threading dislocation eventually annihilate at the surfaces between the multiple layers.
Finally, after the buffer for strain management a final layer of carbon doped GaN is added (not showed in figure 2.4). The latter serves to increase the vertical breakdown voltage, to suppress punch-through in the off-state operation and to improve the normally-off operation without changes in the ON-resistance. More details can be found in [27] and [28].

2.3.3 AlGaN/GaN Heterostructure and 2DEG Formation

GaN electronics are mostly based on the HEMT structure, with the active part is composed by an AlGaN/GaN heterostructure. After nucleation layer and strain management buffer a GaN channel layer followed by a thinner

AlGaN barrier layer are deposited. Since there is lattice mismatch between the two materials, it is necessary to reduce the thickness of the AlGaN layer with increasing the Al content in order to prevent cracking.

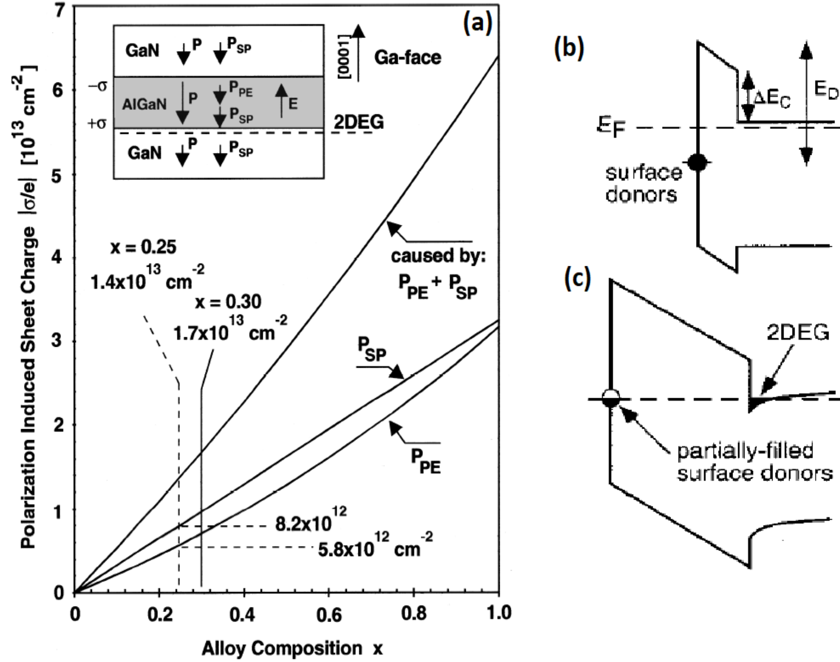


Figure 2.5: *Polarization induced sheet charge versus Al content(a). Inset (a): drawing of polarization induced sheet charge density and directions of the spontaneous and piezoelectric polarization in a GaN/AlGaN/GaN structure. Schematic band diagram illustrating the surface donor model with the undoped AlGaN barrier thickness (b) less than, and (c) greater than the critical thickness for the formation of the 2DEG [29].*

As anticipated in section 2.2, the AlGaN/GaN heterostructure has an incredible ability to form a two-dimensional electron gas (2DEG) at the interface of the two layers, and for a Ga-face structure GaN/AlGaN/GaN the sheet of electrons appears in the lower GaN layer(inset figure 2.5(a)). The 2DEG is a sheet of electrons confined in two dimensions with concentration n_s, representing the channel of the GaN HEMT. Understanding the cause of the 2DEG formation is very important in order to improve the performance of electrical characteristics of the devices. This accumulation of electrons is the result of a charge compensation, but, the origin of this charge is still a topic of discussion.

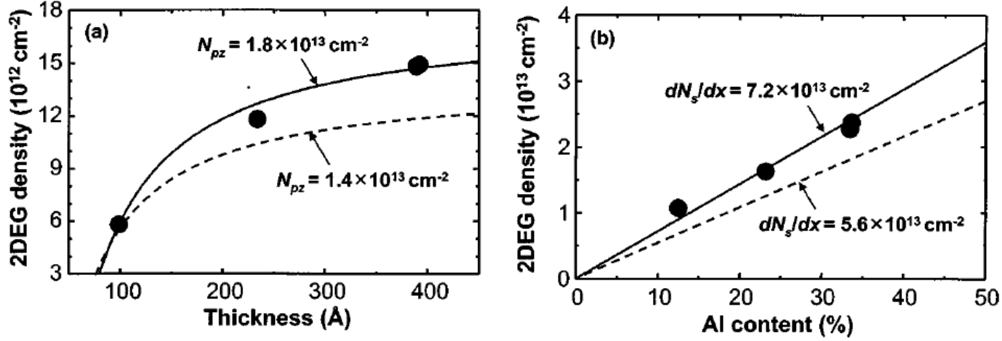


Figure 2.6: *2DEG densities in AlGaN/GaN heterostructure as functions of (a) AlGaN thickness with fixed Al percentage and (b) Al content with fixed AlGaN and GaN thickness. Solid lines are fits of the experimental data [30].*

Many studies [10],[11] associate the 2DEG formation to the amount of spontaneous and piezoelectric polarization. Since the spontaneous polarization and the piezoelectric constants (e_{31} and e_{33}) increase with increasing Al concentration, the total polarization of a strained AlGaN layer is larger than that of a relaxed GaN layer, shown in figure 2.5 (a). For this reason, the decompensation of charge is associated to the gradient of polarization in space.
Other studies, associate the 2DEG phenomenon to the presence of donor-like states in the AlGaN barrier [29]. In this case, the key parameters for the sheet charges formation and densities are the AlGaN layer thickness and the aluminum percentage. Until a certain thickness, called critical barrier thickness, the donor energy is not enough to make able the electron to transfer itself from occupied state to empty conduction band state at the surface, as shown in figure 2.5 (b). As soon as, the barrier thickness reaches the critical value the donor-like states are able to give up electrons for the 2DEG (figure 2.5 (c)), leaving behind positive surface charge. As shown in figure 2.6 the features of the AlGaN barrier layer have a strong impact in the 2DEG density and, hence, play a key role for the performance of the GaN-based devices and in particular on the threshold voltage and ON-resistance.

2.3.4 Top Part of HEMT: from Capping to Surface Passivation Layers

After AlGaN/GaN heterostructure, in many cases, a further GaN cap layer on the AlGaN barrier layer is deposited in order to improve the HEMTs performance from forward and reverse leakage point of view. By adding a

thin cap layer of GaN, the piezoelectric effect is exploited in order to increase the Schottky barrier height and, therefore, to improve the gate leakage [31].

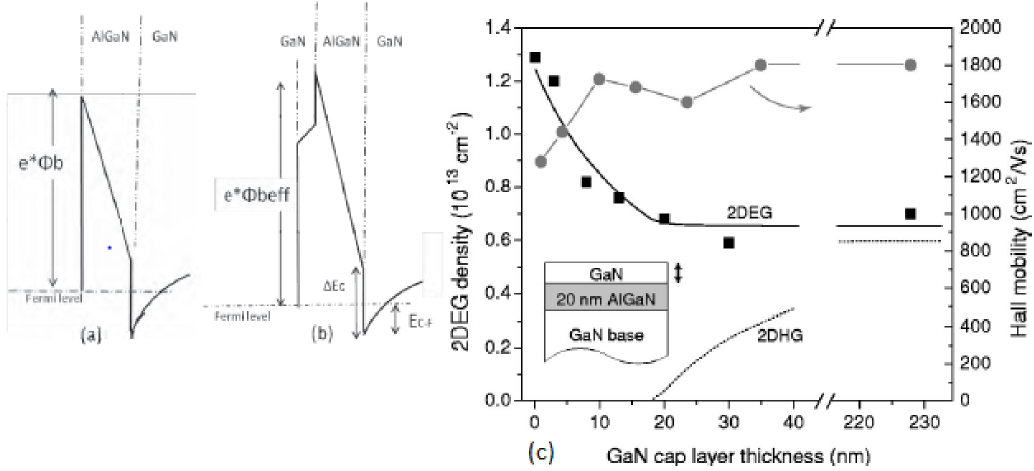


Figure 2.7: *Schematic band diagram for the structure without (a) and with (b) cap layer [32]. 2DEG density and Hall mobility versus GaN cap layer thickness for a GaN/AlGaN/GaN heterostructure with AlGaN thickness fixed (c) [33].*

As shown in figure 2.7 (a), without GaN cap the height of the Schottky barrier is relatively low and this means that electrons could penetrate the barrier for tunneling effect. By increasing the height of the barrier (figure 2.7 (b)) with the cap layer, the tunneling effect can be reduced. Furthermore, adding the cap layer introduces a negative polarization at the upper heterointerface causing increase of the electric field in the AlGaN and the 2DEG density decrease with increasing GaN cap layer thickness (illustrated in figure 2.7(c)) [33]. With a further increase of the cap thickness there is a saturation in the 2DEG density due to the complete formation of 2DHG at the upper GaN/AlGaN interface. More information are available in [33].
Since the 2DEG is determined by polarization and conduction band engineering, it follows that it is very sensitive to the surface charge of the structure which is responsible of a small depletion of the 2DEG [31]. So, for a further improvement in AlGaN/GaN HEMTS, a SiN passivation layer is added. This latter can mitigate dispersion effects, since, the Si atoms can compensate the surface change almost eliminating the 2DEG depletion under the gate [34]. A relatively thin SiN layer on the top can protect the lower layers during the growth and, furthermore, it can prevent the grooves caused by the outdiffusion of the gallium during cooldown after epitaxial growth.

The SiN passivation and the GaN cap are used only for depletion-mode devices that will be discussed in the following section.

2.4 Lateral GaN Devices for Power Application

In the previous section, the layer-by-layer description of the HEMTs has been interrupted because the top part of the devices depends on the various device designs and operation modes. One of the bigger issue of the GaN/AlGaN devices, with the structure previously described, is that the 2DEG is present also without bias and it leads to have normally-ON devices, also called depletion-mode (D-mode) devices. However, in the case of power applications, it is always preferable to have normally-OFF (enhancement-mode) devices for the following reasons:

- safety: the normally-on device is always turned on;
- power consumption: to turn off the normally-on device it is necessary to apply negative gate voltages;
- costs: driver mature technology already exists for normally-OFF silicon-based MOSFET and it can be expensive to invest money in research for new drivers.

Today, the most adopted and commercially available solutions for a normally-OFF GaN devices are: (1) using a cascode configuration by combining a low-voltage Si-MOSFET with a high-voltage D-mode GaN HEMT and (2) E-mode HV GaN HEMT by changing the design of the device.

2.4.1 Cascode Configuration: GaN + Si

One approach to achieve normally-OFF operation for GaN device is the combination of a high-voltage D-mode GaN HEMT with a low-voltage Si-MOSFET (figure 2.8)[35]. When the Si-FET is turned on by the driver system, V_{GS} of the HV HEMT is slightly negative and , therefore, the D-mode GaN device is also turned on since it has a high negative threshold voltage. When the Si-FET is turned off by the drivers its V_{DS} is really high and, consequently, the V_{GS} of the HV HEMT is sufficiently negative to turn it off, sustaining a high voltage. The advantage of this technique is to use a reliable driver for MOSFET already available on the market without any need to redesign another one. Another advantage is that the high OFF-state

blocking voltage of the HEMT is exploited. The advantage of this technique is to use a reliable driver for MOSFET already available on the market without any need to redesign another one. Another advantage is that the high OFF-state blocking voltage of the HEMT is exploited.

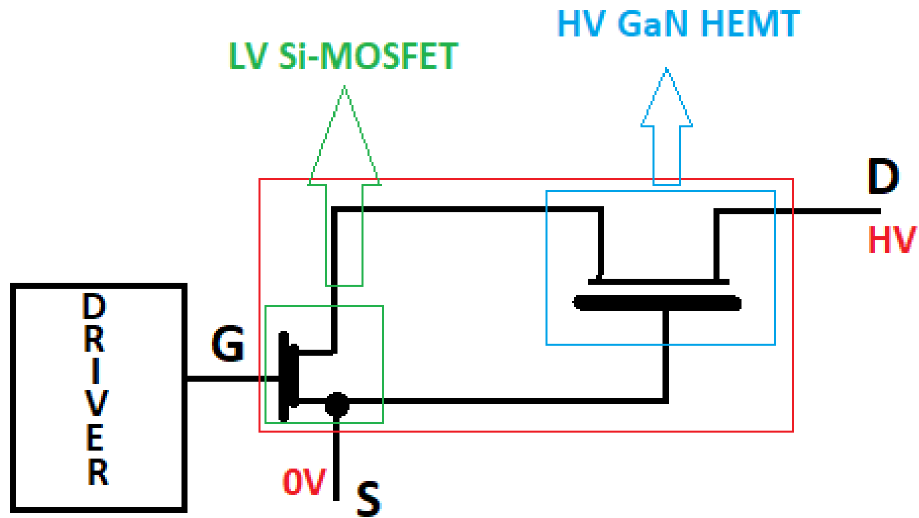


Figure 2.8: *Cascode method operation to achieve normally-OFF operation.*

The main disadvantages are two: (1) the high frequency at which the GaN-based transistor can work is not exploited since the whole circuit is controlled on the Si-FET that operates at lower frequency and (2) by using two devices the dimensions and complexity of the packaging increases and, furthermore, the connections can introduce parasitic effects that leads to a lower performance in switching operation [36].

2.4.2 E-mode GaN-based Transistor

In order to obtain normally-off GaN HEMTs devices the gate region need to be modified.
One of the first approach proposed was the "recessed-gate" HEMT [37], which corresponds to positively shift V_{th} by etching the AlGaN barrier layer under the gate. Once the remaining AlGaN thickness is thinner than critical AlGaN thickness, the 2DEG is no longer able to form under the gate, making the device normally-off.
Another solution can be the "fluorine-gate" HEMT [38], which consists in the introduction of negatively charged fluorine ions in the AlGaN layer below the gate, leading to a positive shift of V_{th} without etching the barrier as in

the "recessed-gate" technique.
It is possible to obtain normally-off HEMTs also combing the two approaches just described [39]. All these solutions have shown to be good from the point of view of the gate leakage in both reverse and forward bias but there are difficulties regarding the precision in AlGaN etching and in the right amount of fluorine implanted since they both play a key role in the threshold voltage shift.
The most used approaches for normally-off GaN-based HEMTs are the "p-GaN gate" and the "recessed gate hybrid MISHEMT" discussed in the following subsections.

p-GaN gate HEMT

Interposing a layer of p-GaN between the gate metal and the AlGaN barrier (figure 2.9 (a)) it is possible to deplete the 2DEG under the gate leading the GaN-based HEMTs to a normally-off operation as a result of raising the GaN conduction band in the channel above the Fermi level, due to a depletion effect of a PN junction. In this scenario the features of the AlGaN and p-GaN layer or the kind of metal gate play an important role for an efficient threshold voltage positive shift.
As already discussed in the subsection *2.3.3*, n_s increases with the AlGaN barrier thickness and Al concentration, leading to a lower R_{ON} but, as reported in [40], a lower V_{th} is attained due to an inefficient depletion of the 2DEG at zero bias. As a result, it is important to find the right trade off between the ON-resistance and the threshold voltage. For GaN the p-type dopant is the Magnesium and the key parameter to improve V_{th} is the Mg electrical activation and out-diffusion that strongly depend on the growth parameters and annealing conditions [41].
Many works report about the importance of the metal work-function on the threshold voltage and gate leakage. In [42] V_{th} between 1.7V and 2.1V have demonstrate with the gate metal made by Ni/Au or Ti/Au, while, it has been reported a threshold voltage around 2.1V with the Schottky gate contact, instead of an Ohmic contac, made of TiN [41] or WSiN [43]. This latter works showed also that the gate leakage current can be reduced. As result there is a metal/p-GaN Schottky diode in series with a p-GaN/AlGaN/n-GaN junction 2.9 (b). The gate leakage is reduced since under positive gate voltages the metal/p-GaN diode is reverse-biased blocking the current and, similarly acts the p-GaN/n-GaN/AlGaN under negative gate bias.
Despite the reliability issues still under investigation, the normally-off HEMT with the p-GaN gate is still the only commercially GaN-based device for power applications [44], [45] and [46].

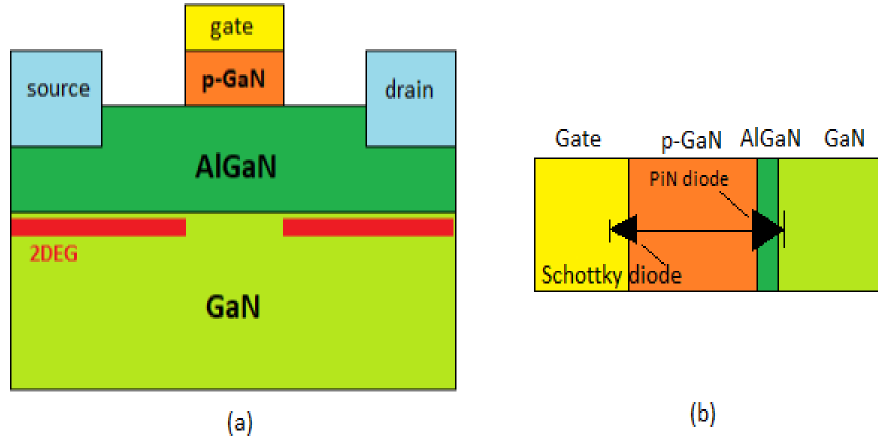


Figure 2.9: *Schematic of a normally-OFF HEMT with a p-GaN gate (a) and back-to back diode for gate leakage reduction (b).*

Metal-Insulator-Semiconductor HEMT

The other promising way to have E-mode GaN transistors is the recessed gate MISHEMT. The depletion of the 2DEG is obtained by etching the AlGaN barrier and part of the GaN channel layer (where the 2DEG is located) under the gate electrode and deposing a dielectric layer before the gate metal. The characteristics and the performances of MISHEMT are unstable since the repeatability and precision in the etching depth and in the thin dielectric layer deposition have many difficulties.
In particular the gate length, the surface and deep traps present at dielectric/GaN interface, the roughness of the etched area and the quality of the dielectric have an important impact on channel mobility, V_{th} and R_{ON} stability [36].
Regarding the dielectric layer, the most used materials are: (1) Al_2O_3 deposited by Atomic layer deposition (ALD) with a reported threshold voltage of 3.5V in [47] (2) SiO_2, processed by plasma-enhanced chemical vapor deposition (PECVD), that seems the one with the higher V_{th} (around 3.7V) [48] and, finally, (3) SiN also deposited with PECVD [49]. More details can be found in [47]-[49].
From figure 2.10 (b), in comparison with the p-GaN HEMTs, recessed gate MISHEMTs showed lower gate leakage current and larger forward gate swing due to the gate dielectric but, as reported in [50], MISHEMTs showed a large hysteresis after applying forward gate bias, probably due to the defects at the dielectric/GaN interface.

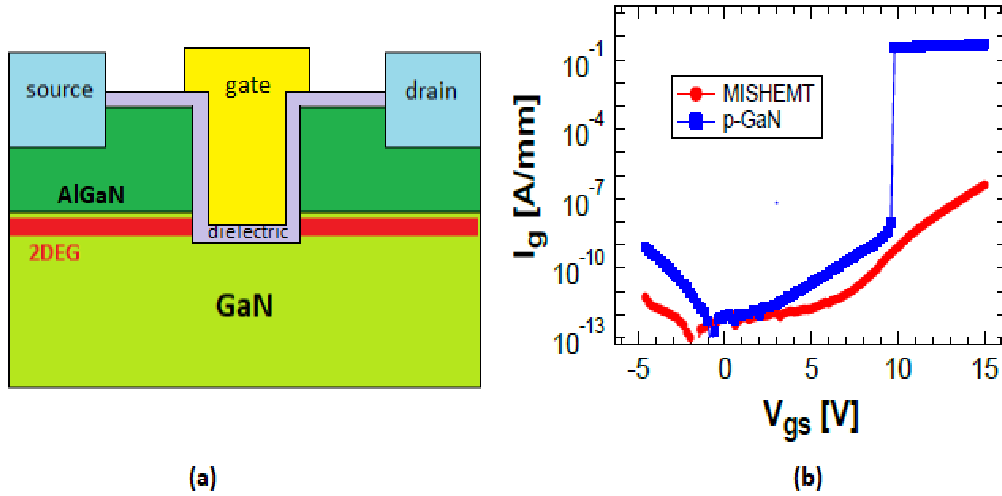


Figure 2.10: *Schematic cross section of a normally-OFF GaN-based MISHEMT(a) and (b) comparison of the forward bias gate leakage characteristics between p-GaN HEMT and MISHEMT [50].*

Summary

In this chapter the layer-by-layer description of the GaN HEMT has been discussed. So strong is the desire, so difficult is to have GaN substrates in terms of costs and wafer diameters. Despite all the difficulties, the heteroepitaxy on foreign substrates has led to promising results. In particular, especially thanks to the nucleation layer and the buffer for the strain management, GaN-on-Si devices are commercially available with good performance and reliability. The most suitable growth technique for the epilayers is the metal-organic chemical vapour deposition (MOCVD). The correct use of MOCVD has a strong impact on the quality of the deposited crystal and, hence, on the device characteristics.

In this chapter, furthermore, the gallium nitride crystal structure and materials features have been described in order to understand why GaN is the best wide band-gap material for certain applications. In particular, the presence of an AlGaN/GaN heterostructure leads to the two dimensional electron gas (2DEG) that is the heart of GaN-based HEMTs. The problem is that the 2DEG is present also with zero bias and for this reason, in the last few years many solutions are adopted to achieve normally-OFF operating devices (Enhancement-mode). A particular importance has been given to the

p-GaN gate HEMTs and recessed gate MISHEMTs, though, the p-GaN gate solution is the only one commercially available since MISHEMTs have some problem in terms of stability and repeatability in the process.

Chapter 3

GaN Reliability Issues

In addition to excellent performance at reduced cost, a semiconductor power device must guarantee a good level of reliability before making it available on the electronic market. Despite GaN power transistors demonstrated impressive performance at comparable costs with respect to Si-counterparts, the long-term reliability is still an issue not to be underestimated. GaN-based HEMTs are usually adopted in switching power applications, where their state is continuously switched, at relatively high frequencies, between high voltage off-state and high current on-state operation. In such conditions, devices can be subjected to different kinds of degradation mechanisms limiting their long-term reliability. Furthermore, during the switching phases the devices might be simultaneously subjected, for a short period of time, to both high-drain voltage and current. This regime is called semi-on-state operation and can lead to additional degradation mechanisms.
In general, the time-dependent degradation of GaN-based transistors may be triggered by many factors,, widely classified in [51] as follow:

1. Material origin: crystalline defects and lack of uniformity in the deposited epilayer;

2. Metallurgy: ohmic contact and passivation degradation, hydrogen contamination, etc.;

3. Electrical behavior: reduction in drain current (current collapse), increasing in power consumption (power drift), breakdown walkout, etc.;

Beside the aforementioned failure mechanisms, this chapter will focus with particular attention on trapping defects and self-heating problems.
The key to better understand how reliable a device is, or which failure mechanism leads to the degradation, resides in the thermo-electrical stress and characterization of the devices.

3.1 Trapping effects

Trapping effects are the main cause of power GaN HEMTs degradation. The term *traps* refers to the defects deriving as a consequence of crystal imperfections, threading dislocation or impurities, etc. The traps can introduce energy states in the bandgap of the semiconductor. These states can be: i) acceptor-like, i.e neutral when empty and negatively charged when occupied; ii) donor-like, i.e neutral when empty and positively charged when occupied. [52]

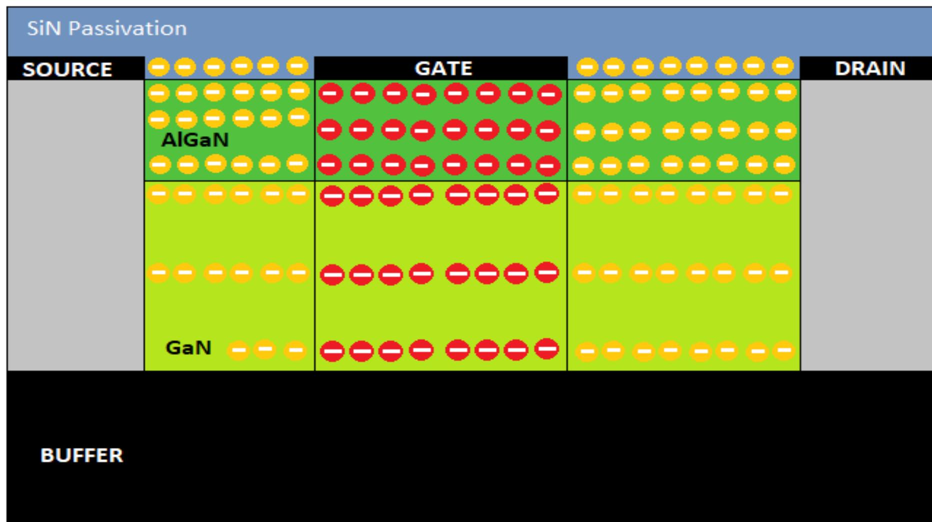


Figure 3.1: *Traps localization in GaN HEMTs.*

As shown in figure 3.1, there are several possible trap locations. The most relevant ones are the follow:

- At the AlGaN surface: their existence has been confirmed by Vetury *et al.* [53] with OFF-state measurements (high drain voltage and floating gate). During these experiments the occupation of the electrons in donor-like neutralizing his positive charge with a consequent reduction of the 2DEG density (the resistance increase).
- In the AlGaN layer: due to the carbon and oxygen concentration that has been found to be higher than in GaN or due to nitrogen vacancies, etc. [54].

- In the GaN layer: as seen in the previous chapter, a carbon doped GaN buffer is required to suppress the current leakage. Still, the doping introduces acceptor-like impurities [52], [55].

- At the interfaces between layers of different materials: these traps can be related to threading dislocation caused by lattice constants and thermal expansion coefficients between adopted epi-materials [56], [57].

- In the buffer (not shown in Fig. 3.1): this kind of traps are localized in the stack between the GaN channel layer and the substrate due to lattice mismatch between the various epilayer made of different materials.

To determine a specific degradation mechanism, it is necessary to understand how the traps behave and what energy levels they are related to, where they are physically localized and what trapping/de-trapping time constants do they have. To do this, various trap characterization experiments, such as Current-Transient measurements [58], frequency dependent capacitance and conductance measurements [59] and capacitance-voltage (C-V) have been employed.
Based on their localization, each kind of trap can impact a different parameter. In particular, the traps localized in the region under the gate (in red in figure 3.1) have a dominant impact on the threshold voltage, while all the other impurities (in yellow in figure 3.1) could lead to a change in the transconductance due to resistivity increase of the gate-drain and gate-source access regions [60].

3.2 On-State Degradation Mechanisms

In on-state condition the GaN devices are submitted to a low drain voltage, but normally-off devices operate with positives gate biases that lead to further degradation mechanisms. The reliability issues for MISHEMTs and p-GaN gate HEMTs are different because of the different gate stack.
As already said in the section *2.4*, MISHEMTs suffer of threshold voltage instability due to defect states at the dielectric/AlGaN interface. Lagger et al. [61] explained V_{th} degradation with a schematic band diagram (Fig. 3.2). In particular, by increasing the gate bias (V_G), the electrons barrier height between 2DEG and dielectric/AlGaN interface decreases, favoring electron injection. A further increase in V_G pushes the AlGaN conduction band (Fig. 3.2(c)) at the interface with the dielectric below the Fermi level, with a consequent formation of a second channel. As a result, the V_{th} shifts depends

on the amount of charge trapped at the dielectric/AlGaN interface and it can be improved by using different materials and deposition processes of the dielectric.

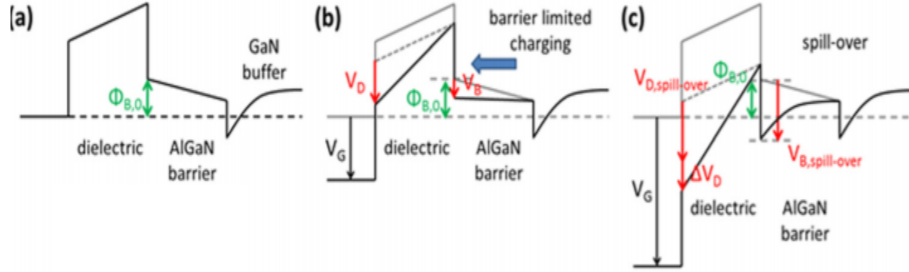


Figure 3.2: *Band diagram variation for MISHEMT with different positive gate bias levels: (a) thermal equilibrium, (b) low positive gate voltage, (c) high positive gate voltage [61].*

Regarding the p-GaN gate HEMTs, the gate breakdown phenomenon could be explained by avalanche multiplication in the depleted region of the Schottky metal/p-GaN junction [62]. As shown in Fig. 3.3 (a), under thermal equilibrium conditions the depleted region of Schottky junction has a width of 50nm. Under forward gate bias the metal/p-GaN junction is reversed biased, depletion region is further extended and AlGaN barrier height is lowered (figure 3.3 (b)).

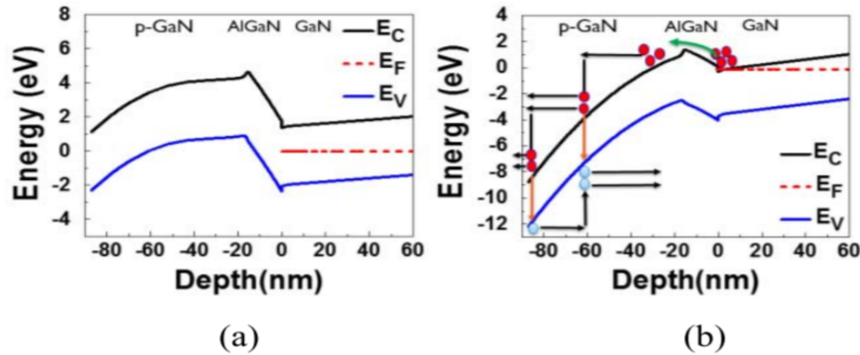


Figure 3.3: *Band diagram variation for p-GaN gate HEMT in (a) thermal equilibrium and (b) positive gate voltage [63].*

In such condition, the electrons from the channel are injected in the p-GaN and, once they reach the depletion region, they are accelerated by the

electric field promoting avalanche breakdown.
Tallarico et al. [64] demonstrated that the p-GaN layer plays a fundamental role on the gate failure, ascribing the breakdown mechanism to the creation of a percolation path in the depletion region of the Schottky junction (interface between gate metal and pGaN) due to the high electric field.
The effect of pGaN doping and gate metal work function are the key parameters in order to achieve a gate bias operating range and a performance stability as wide as possible. In particular, Mg doped p-GaN layer growth conditions and doping concentration have significant impact on the p-GaN gate HEMT device performance and reliability (more details in [41], [65] and [66]).

3.3 Semi-On-State Degradation Mechanisms

Between on- and off-state there is a third operation regime, namely semi-on-state. When the device switches from off- to on-state and viceversa, for few tens of ns, the drain current starts to increase while the drain voltage still relatively high. The simultaneous presence of high current and high voltage on the drain may favour hot electrons degradation effects, limiting the performance and the lifetime of the device due to charge trapping processes.

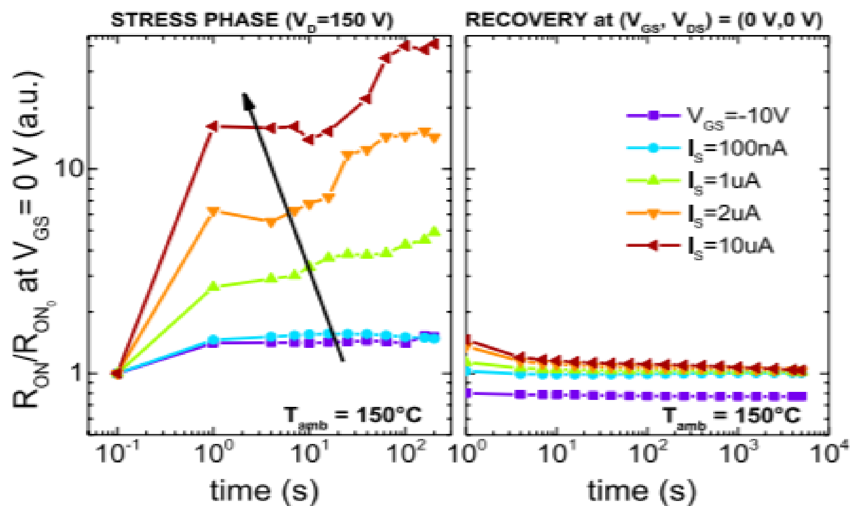


Figure 3.4: *Variation of the on resistance measured during (a) the 200s of stress and (b) 5000s of recovery (the R_{ON} values are normalized with a sample stressed with HTRB stress at VGS = -10 V) [62].*

In particular, is such regime, electrons injected from the source are accelerated by the high longitudinal electric field toward the drain, acquiring enough kinetic energy to create new defects and/or to be trapped in pre-existing ones, [67]. The most affected parameter is the on-resistance, and in order to investigate the hot electrons role in the degradation, high temperature source current (HTSC) stress tests are performed. Here, the devices are stressed for a long period of time with constant current injection from the source and with a high drain voltage. In figure 3.4 (a), it is possible to notice that the R_{ON} increases with both the current and time, but, on the other hand, the hot electrons induced degradation is recoverable as result of trapping in the gate-drain access region. By increasing the temperature, the on-resistance degradation decreases because the mean energy of the hot electrons is reduced by the scattering with the lattice. Still, these scattering could produce unrecoverable damage [62].

3.4 Off-State Degradation Mechanisms

During Off-state operation, the devices are submitted to a high drain voltage having their bulk, source and gate contacts grounded.

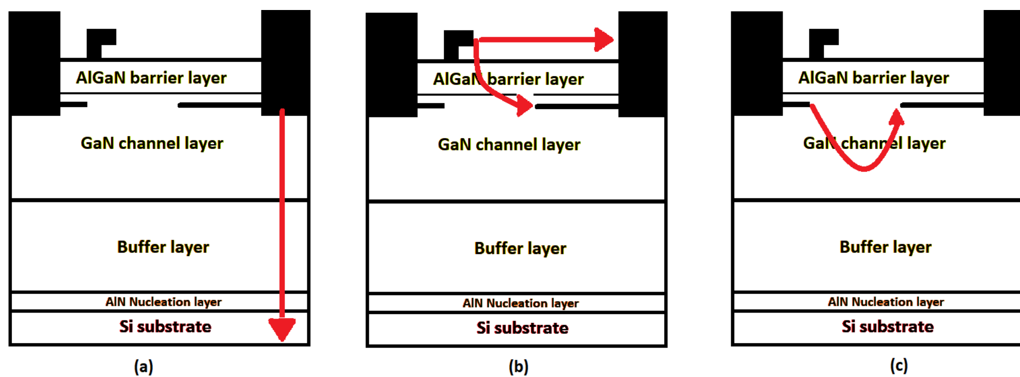


Figure 3.5: *Different off-state breakdown mechanisms namely: (a) drain to substrate breakdown, (b) drain to gate breakdown and (c) drain to source breakdown*

This operation mode can lead to an unrecoverable breakdown that is time-dependent, a situation that also occurs at drain voltages lower than the breakdown voltage evaluated by a dc sweep. The off-state breakdown mechanism can be summarized in:

1. Vertical drain to substrate breakdown of the buffer (Fig. 3.5 (a));

2. Later breakdown of the gate-drain region of the Schottky junction and the passivation layer (Fig. 3.5 (b));
3. Drain to source lateral breakdown of the GaN channel (Fig. 3.5 (c)).

3.4.1 Vertical Leakage/Breakdown

It is well known that the buffer and transition layers between GaN channel and the Si substrate are not intrinsic semi-insulating materials. So, in order to compensate the background donor doping (by residual impurities as silicon or oxygen) of the buffer/transition layer, intentionally or unintentionally deep acceptors (such as carbon or iron) are introduced to increase its resistivity, obtaining lower off-state leakage current and suppressed punch-through mechanism that can induce a premature breakdown in AlGaN/GaN HEMTs. When high drain bias is applied, the high vertical electric field strongly interacts with both acceptor and donor deep levels in the buffer [68].

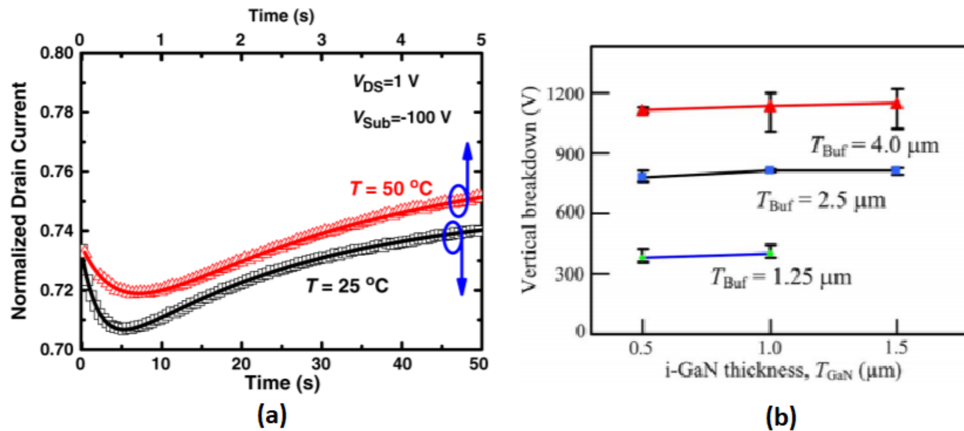


Figure 3.6: *(a)Temperature dependent transient normalized drain current at V_{DS}=1 Vm and V_{SUB}=-100 V drain to substrate breakdown [68], (b) vertical breakdown as a function buffer and GaN layer thickness [69].*

As shown in Fig. 3.6 (a), by performing a transient current test, the drain current decreases and then increases with a behaviour depending on both temperature and time. Marso et al. [70] demonstrated with the back-gating measurements (sweep test with substrate from -100V to 0V, while drain, gate and source grounded in order to suppress the surface traps effects) that the decrease in drain current is to be attributed to the generation of negative space charges in the GaN buffer/transition layer by the ionization

of acceptor traps, which depletes the 2DEG, and that the increase in drain current is caused by the ionization of donor traps, which generates positive space charges. Fig. 3.6 (b) shows the trend of the vertical breakdown by varying the buffer thickness (T_{Buf}) and the GaN layer thickness (T_{GaN}). In particular, it can be seen that the breakdown voltage is slightly affected by T_{GaN}, while T_{Buf} plays a more important role [69].
Many studies have investigated the responsible factors of the vertical conduction, proposing some solutions such as the use of a highly resistive silicon substrate [71] or the insertion of a p-type region [72] due to the fact that the voltage drop on the GaN buffer is mitigated by the partial depletion of the substrate.

3.4.2 Lateral Breakdown in the Gate-Drain Region

The other region affected by degradation/breakdown is the one between drain and gate. In particular, the breakdown can occur at the Schottky junction and/or at the passivation layer, and it is caused by the high electric field due to high voltage between gate and drain, V_{GD}. Regarding the Schottky junction, the real cause is a high peak of the electric field at the gate edge on the drain side, as it can trigger the following mechanisms:

- Inverse piezoelectric effect: as it is well known, the AlGaN barrier layer is subject to a tensile stress due to the lattice mismatch with the GaN channel layer. This can produce crystallographic defects resulting in the degradation of the electrical characteristics due to trapping/detrapping effects. Ancona et al. [73] demonstrated with an electromechanical analysis that the piezoelectric effect alone is not sufficient to generate a crack in the AlGaN layer, but the combination of the high electric field, gate leakage current and high temperature together lead to the breakage. The role of the AlGaN barrier properties is very important and by reducing the Al content the mechanical stress with the GaN layer is reduced, though, the performance (such as the R_{ON} since the 2DEG has a lower density) will be worse.

- Electrochemical degradation: by etching the passivation and the metallization from the device (without damaging the AlGaN or the GaN surface) Makaram et al. [74] showed the presence of grooves and particles. They also demonstrated that with the increase of the electric field in off-state conditions, the number of the particles and the depth of the grooves increased at the drain-side of the gate edge. These phenomena are related to an electrochemical reaction consisting in the oxidation of GaN or AlGaN, with formation of Ga_2O_3 and Al_2O_3 [75]. The main

issue is that the grooves and the particles can charge the device surface, forming a virtual gate responsible of drain current collapse and gate leakage current increase [76].

- Percolation processes: high electric field is also responsible for an increase in the amount of defects in the AlGaN barrier layer (demonstrated by electroluminescence measurements [77]). This can create a percolation multistep tunnelling path. The number of defects creating a percolation path is voltage and time dependent, as they lead to an increase of the gate leakage current (until the permanent breakdown) and a shift of I-V curves measured after constant voltage stress [78].

It emerges that the main issues for the gate-drain region are the high electric field peaks and the impurities in the epilayers. Both of them may produce current collapse, which consists in a drastic reduction of the drain current (I_D) after the application of a high drain voltage (V_D) [79]. The current collapse is caused by acceptor-like traps in both AlGaN/GaN layers and the passivation/AlGaN interface: this leads to trapping mechanism of the 2DEG electrons accelerated by the high electric field [52].

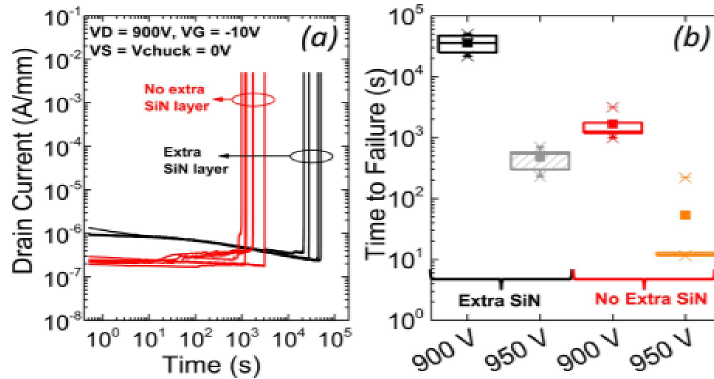


Figure 3.7: *(a) Constant voltage test at V_D = 900 V, demonstrating that the extra nitride layer increases time to failure by one order of magnitude. (b) Box chart showing the measured time to failure in devices with and without extra SiN layer stressed at V_D = 900 V and V_D = 950 V [80].*

One of the adopted solutions to suppress trapping effects (in particular the ones about the surface traps) was SiN_X passivation (as mentioned in the subsection *2.3.4*). Although, during a constant voltage off-state stress, the electric field peaks at the gate edge on the drain side, reaching a value comparable to the one of the breakdown electric strength of the SiN (6 MV/cm)

[80]. In particular, in [80], an improvement has been found by adding an extra SiN layer above the already present one. The electric field peak has been reduced, resulting in one order of magnitude increase of the time to failure/breakdown with respect to the devices without the extra SiN layer, shown in Fig. 3.7.
Another way to increase the breakdown voltage is by reducing the electric field (close to gate edge) with the adoption of the field plates. As shown in Fig. 3.8, this approach consists in depositing three metal layers, two linked to the source and one to the gate, all of them separated by oxide layers. In particular, the longer the field plates, the lower the electric fields. However, it is worth noting that a too long field plate (e.g. S-FP2 in Fig. 1.5) could lead to a lower breakdown voltage due to short distance between field plate and drain contact. As a result, the right trade-off must be achieved.

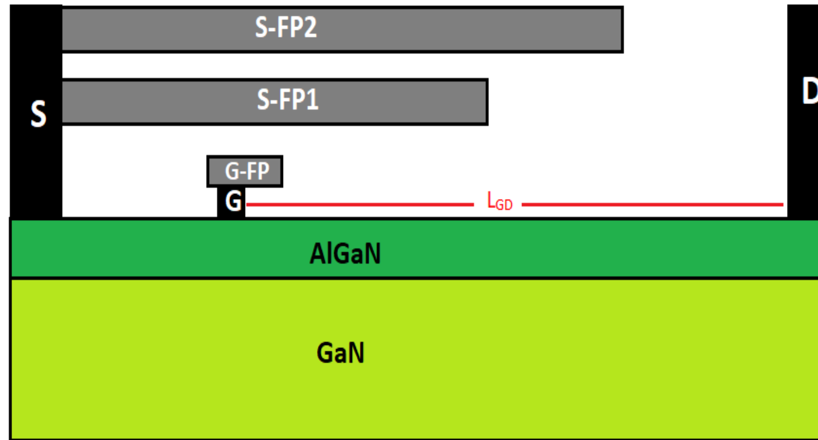


Figure 3.8: *Cross-section of a GaN HEMT with double source field plates (S-FP1 and S-FP2) and single gate field plate (G-FP).*

3.4.3 Lateral Breakdown between Source and Drain

Finally, the last breakdown mechanism with regards to the off-state condition, is the one involving th GaN channel layer. This breakdown is due to an increase in the drain-source leakage current, linked to the punch-through effects. If the region of the GaN channel under the gate is not well depleted, the high drain voltage allows a current flow through the GaN layer in a deeper position respect to the AlGaN/GaN interface and strongly depends on the gate length [81]. As shown in Fig. 3.9 (a) , the higher the negative V_{GS}, the higher the punch-through voltage,, since the GaN channel under the gate is

more depleted in the vertical direction (towards the buffer).

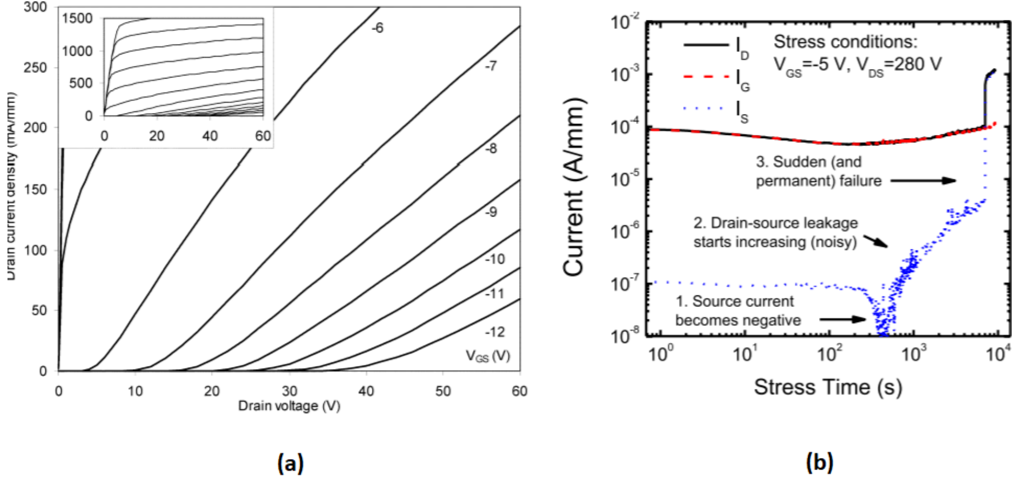


Figure 3.9: *Drain current as function of the drain voltage at different negative gate bias (V_{GS}) (a) [81]. Gate, Drain and source current during constant voltage stress in off-state condition (b) [82].*

In [82], the time-dependency of drain-source degradation has been proven and it has been attributed to positive charges originating under the gate. In particular, in Fig. 3.9 (b) it can be noticed that, with a high drain bias, the main contribute to the drain current is initially given by the gate leakage, while, increasing the stress time, the source current become negative, meaning that the current flows out of the source. When the device approaches to the breakdown, the main component of the drain current is the source one, since the gate current shows no changes.
In order to prevent this issue, a double structure AlGaN/GaN/AlGaN is used. The introduction of an AlGaN layer below the GaN channel layer leads to a better confinement of 2DEG electrons and prevents punch-through with a consequent reduction in the off-state drain leakage current [83].

Summary

Overall, gallium nitride-based HEMTs for power electronic applications are very promising devices with higher breakdown voltages, lower on-resistance and higher switching capability compared to silicon counterparts. However, being an emerging technology, further efforts in terms of optimization are required to ensure high levels of reliability in all operation regimes discussed

in this chapter, i.e. (1) on-state, (2) semi-on-state, (3) off-state. The next chapter reports an experimental activity aimed at investigating the off-state reliability of power GaN HEMTs with p-type gate fabricated on 200 mm silicon substrates by imec.

Chapter 4

Investigation of the Off-State Reliability on 200V pGaN HEMTs

In this chapter an Off-state reliability study is presented performed on 200 V p-GaN HEMTs featuring different structural configurations summarized in section 1.1.1. In particular, time-dependent dielectric breakdown and hard breakdown experimental tests have been performed in combination with TCAD simulations. Thanks to this approach, the root causes limiting the off-state device reliability have been identified, highlighting the role and the importance of structural parameters, which are fundamental for guiding device optimization.

4.1 Experimental Details

Off-state electrical stress and measurements have been carried out by means of a MPI-TS2000-HP probe station connected to KEYSIGHT B1505A parameter analyser equipped with high power, high voltage and ground source measure units (SMUs). In particular, the devices under test are connected as follows:

- Source contact: connected to high power SMU (HPSMU1);
- Drain contact: connected to high voltage SMU (HVSMU);
- Gate contact: connected to high power SMU (HPSMU2);
- Substrate contact: connected to ground SMU (GNDSMU);

During Off-state stress, the gate, source and bulk contacts are forced to 0 V while, the drain voltage is sweeped up to stress voltage and/or breakdown voltage. All contacts currents are monitored. Usually, accelerated stress tests are performed at 150 ^oC but, in this case, a temperature of 210 ^oC has been adopted to limit the stress voltage (< 500 V) and time-to-failure (< 10^5 s). Devices with different geometry parameters such as gate-drain distance (L_{GD}) and the field plates lengths have been adopted. The role of the AlGaN barrier thickness (T_{AlGaN}), Al content, and GaN channel thickness (T_{GaN}) on the off-state degradation has been also investigated.

4.1.1 Device Under Test

P-GaN gate HEMTs grown on 200mm Si(111) wafers by *imec* (Belgium) with a class voltage of 200 V are considered in this study. The epi-stack grown on top of silicon (Fig. 4.1(a)) features a 3.3 um thick superlattice buffer, 200 or 400 nm thick GaN channel, 12.5, 14 or 16 nm thick AlGaN barrier. Then, a Al_2O_3 passivation is deposited on the access regions, whereas the gate is composed by 80nm of p-GaN (doped with Mg) followed by 30nm of titanium nitride (TiN). The structure features three field plates namely gate metal (linked to the gate), source ohm metal and source metal1 (both linked to the source) field plates. For the sake of simplicity, in this chapter, the field plates will be named first field plate (FP1) for the gate field plate and second and third field plate (FP2 and FP3) for the source ohm metal and source metal1 field plates, respectively. More details on the device architecture can be found in [84].

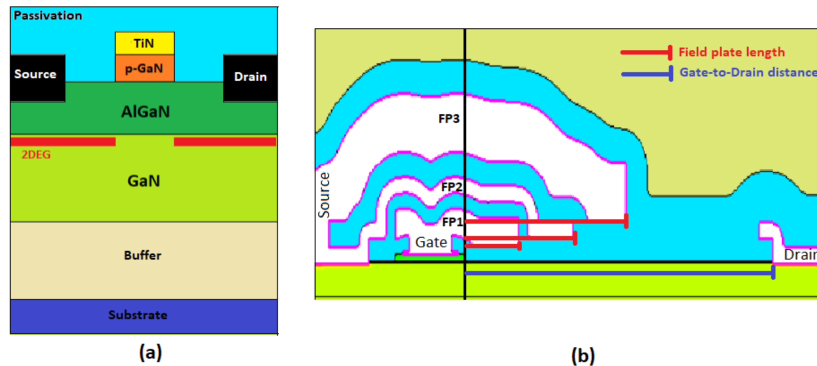


Figure 4.1: *Schematic cross section of p-GaN HEMT (a) and TAD simulator output (b).*

In table 4.1 the devices under investigation are summarized. In particular,

each device differs for gate-drain distance and field plate length configuration.

Device name	L_{GD} (μm)	FP1 (μm)	FP2 (μm)	FP3 (μm)
Device1	3	0.35	0.65	1
Device2	4	0.65	1.35	2
Device3	5	1	2	3
Device4	6	1	2	3

Table 4.1: *Overview of the devices under test.*

4.1.2 Hard Breakdown

Hard breakdown measurements consist in sweeping the drain voltage from 0V up to breakdown voltage, as shown in Fig. 4.2. During the measurements gate, source and substrate contacts are grounded and their currents are monitored.
The breakdown voltage is defined as the voltage at which the drain current suddenly increases without control (see Fig. 4.2). Hard breakdown tests performed on different devices are helpful to provide an preliminary indication on the performance, reliability, variability of the process, etc. Moreover, such tests provide an average value of the off-state breakdown voltage, which is of paramount importance to choose the stress conditions for time-dependent dielectric breakdown tests.

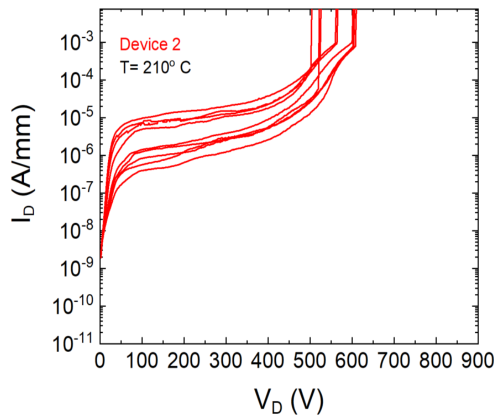


Figure 4.2: *Hard breakdown test performed on eight nominally identical devices.*

4.1.3 Time-Dependent Dielectric Breakdown (TDDB)

Time-dependent dielectric breakdown has been studied for the first time in thin oxide films [85] and [86], due to their importance in silicon CMOS integrated circuits. Regarding GaN devices, the situation is slightly different since the time-dependent breakdown can occur in different regions/materials, i.e. passivation layers (SiO_2, AlO_2, SiN, etc.), or semiconductor layers (GaN, AlGaN, etc.) [87], [80], [88] . The most commonly used test for the investigation of TDDB behavior is "constant stress". Such stress can be applied in form of constant voltage stress (CVS) or constant current stress (CCS). In the case of CVS test adopted for off-state reliability of GaN devices, a voltage is applied to the drain, while its leakage current is being monitored up to failure.

Time-to-Breakdown

In [85], [86] it has been suggested that the time-to-breakdown is a consequence of traps located in random positions in the oxide, even in a fresh device. When the oxide is submitted to a relatively high electric field new traps are generated. The amount of traps increases with time causing one or more percolation paths with a sudden increase in the current (in the case of CVS), which means that the breakdown occurred (show in Fig. 4.3).

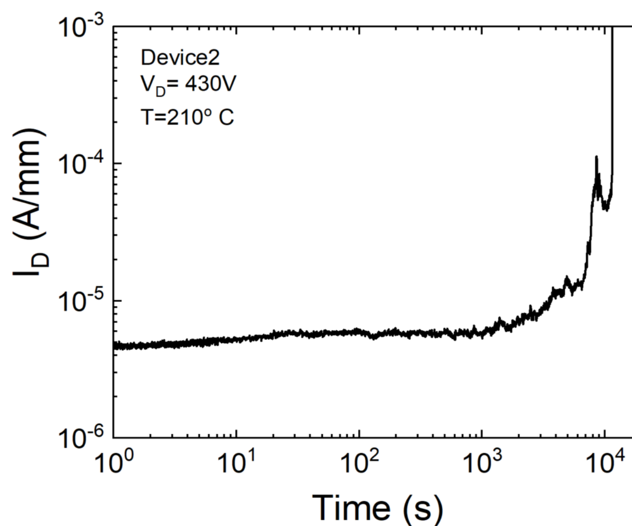


Figure 4.3: *Current monitoring during a constant voltage stress in off-state condition with V_D=430V.*

In the case of a CVS, the time-to-breakdown (t_{BD}), also called time-to-failure (TTF), corresponds to the time when the current (the drain current in the case illustrated in Fig. 4.3) increase beyond a defined current value.

Statistical Analysis

When TDDB stress is applied on several devices with same geometry, different times-to-breakdown occur because of non-ideality of devices, process, etc. Actually, the t_{BD} is a statistical distributed parameter with cumulative failure distribution function F(t), which can be calculated from a fitting of the cumulative distribution of the t_{BD} values. The t_{BD} values in [85], [86] have been shown to be distributed according to Weibull statistic distribution function defined as:

$$F(t) = 1 - exp[-(\frac{t-\gamma}{\eta})^{\beta}] \tag{4.1}$$

where β is the shape parameter, η is the scale factor (or the time in which the 63.2% of the devices fail) and γ is the time delay. Assuming γ=0 the eq. 4.1 can be rewritten as:

$$ln[-ln(1 - F(t))] = \beta ln(t) - \beta ln(\eta) \tag{4.2}$$

The analysis procedure for the TDDB experiments can be summarized as follow [85], [86]:

1. Extraction of t_{BD} values from the recorded measurements during CVS test (Fig. 4.4(a));

2. Ordering the obtained t_{BD} values from the smallest to the biggest and extraction of F(t_{BD-i}) (Fig. 4.4(b)) by the Bernard formula of the median ranking approximation:

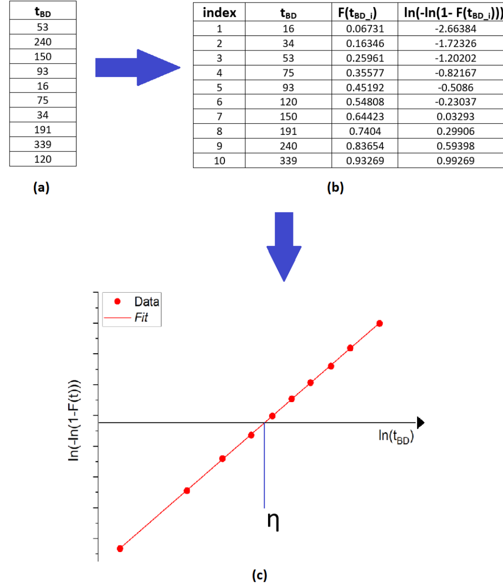
$$F(t_{BD-i}) = \frac{i - 0.3}{n + 0.4} \tag{4.3}$$

   where i is the number of the i-th failed device, and n is the total number of failed devices;

3. Plot the F(t_{BD-i}) data in a Weibull plot (ln[-ln(1-F(t_{BD-i}))] vs. ln(t_{BD-i}))) and apply a linear fit (Fig. 4.4(c)).

Finally, from the Weibull plot it is possible to extract the value of β and η. The shape parameter β of the Weibull distribution represents the slope of F(t) function and it can give information about the reliability. In

particular, β>1 indicates a smaller spread on the data which means that the time-to-breakdown is induced by a single degradation mechanism (intrinsic breakdown). When β<1, the presence of different degradation mechanisms or the poor quality of the device process is the root cause for TDDB (extrinsic breakdown).



t_{BD}
53
240
150
93
16
75
34
191
339
120

(a)

index	t_{BD}	$F(t_{BD_i})$	$ln(-ln(1- F(t_{BD_i})))$
1	16	0.06731	-2.66384
2	34	0.16346	-1.72326
3	53	0.25961	-1.20202
4	75	0.35577	-0.82167
5	93	0.45192	-0.5086
6	120	0.54808	-0.23037
7	150	0.64423	0.03293
8	191	0.7404	0.29906
9	240	0.83654	0.59398
10	339	0.93269	0.99269

(b)

Figure 4.4: *Example of analysis for a TDDB experiment:(a) t_{BD} values are extracted from the measurements, (b) the obtained t_{BD} values are ordered (from the smallest to the biggest) and then the $F(t_{BD-i})$ is calculate using the Bernard formula. Finally (c) from the plot of ln[-ln(1-F(t_{BD-i}))] vs. ln(t_{BD-i}) the values of η and β can be extrapolated.*

The scale factor η strongly depends on the applied voltage and the area of the devices. Since the percolation paths could be formed randomly in the device area, a larger area implies a higher failure probability (lower η). Based on TDDB theory,the F(t) of different areas with the same dielectric thickness follows the area scaling law [85]. In particular, the Weibull function of devices with area A_1 (F_{A1}(t)) can be expressed as a function of the the same F(t) of devices with area A_2 (F_{A2}(t)) as follows:

$$ln[-ln(1 - F_{A1}(t))] = ln(\frac{A_2}{A_1}) + ln[-ln(1 - F_{A2}(t))] \quad (4.4)$$

Replacing the Eq. 4.2 in 4.4:

$$ln(\frac{A_2}{A_1}) + \beta ln(t) - \beta ln(\eta_2) = \beta ln(t) - \beta ln(\eta_1) \tag{4.5}$$

where:

$$\eta_1 = \eta_2(\frac{A_2}{A_1})^{\frac{1}{\beta}} \tag{4.6}$$

The area scaling produce a time-shift by $(A_2/A_1)^{\frac{1}{\beta}}$ of the Weibull plot with an alignment of the two straight lines only in case of homogenous stress and degradation (same β for the Weibull plots related to A_1 and A_2). On the other hand, if the failure (forming of percolation path) occurs in a very localized spot (e.g. at a corner), the area is not responsible of a η shift and the Eq. 4.6 can not be applied [89].

Lifetime extrapolation

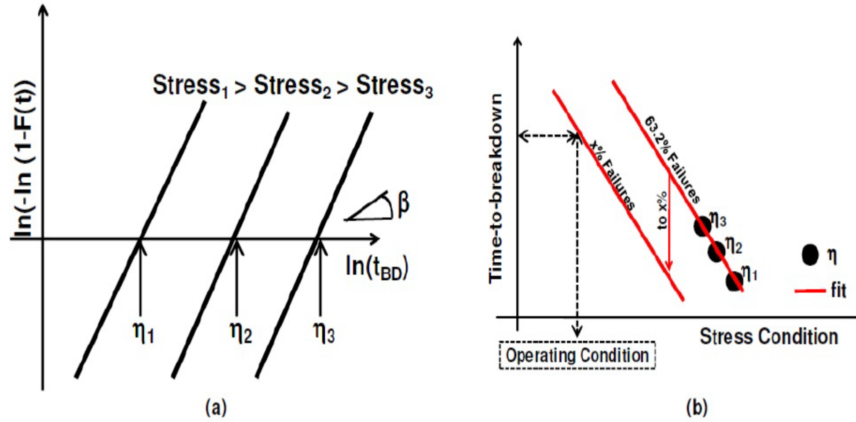


Figure 4.5: *Example of lifetime extrapolation:(a) Weibull plot associated with TDDB experiments under 3 different stress condition, (b) lifetime prediction from the values of* η_1*,* η_2 *and* η_3 *[89].*

As mentioned above, the Weibull parameter η depends on the applied voltage (in the case of CVS), indeed, a larger voltage means a lower value of η. By performing TDDB experiments at different stress conditions (voltage or current) the resulting failure distributions F(t) are parallel to each other (same β) and only shifted by the η factor as shown in Fig. 4.5 (a). To extrapolate the lifetime it is necessary to plot the different η values versus

the stress conditions and, by fitting this relation with an exponential law, it is possible to predict when the 63.2% of the devices fail under a certain operating voltage (shown in Fig. 4.5 (b)). Additionally, it is possible to extract the time corresponding to the failure of an arbitrary percentage x% and determine the guaranteed operating conditions [89]. Note that the stress conditions are always higher than the operating condition in order to obtain the failure in a reasonable time.

4.2 Results and Discussion

Fig. 4.6 shows the results of the hard breakdown measurements are performed on the four device configurations (summarized in table 4.1) featuring GaN channel and AlGaN thickness of 400 nm and 14 nm, respectively, and an aluminum content of 25%. By observing Fig. 4.6, it is possible to note that i) the source current is perfectly the same as the drain current until the breakdown. In particular, after the breakdown the source current suddenly increases whereas the gate and the substrate (not shown) currents remain low, excluding the vertical breakdown between drain and substrate.

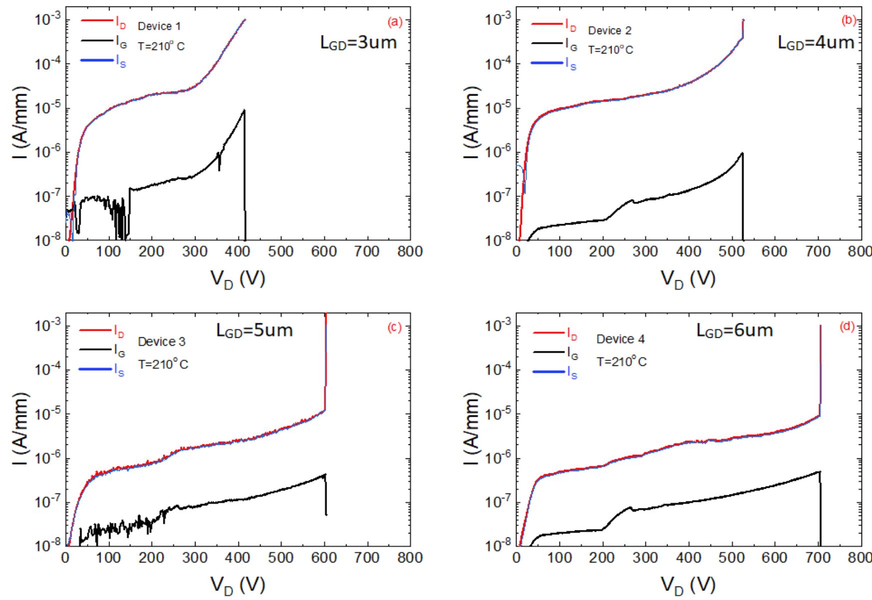


Figure 4.6: *Drain, gate and source current monitored during hard breakdown test for: (a) Device1, (b) Device2, (c) Device3 and (d) Device4. The devices feature 400nm thick of GaN channel layer and 14nm thick AlGaN barrier layer with 25% of aluminium content.*

ii) the Device1, with L_{GD}=3μm, shows a different drain/source leakage dynamic for $V_{DS} > 300$ V. This can be explained by the longitudinal electric field in the GaN channel layer, which increases by reducing L_{GD}, possibly promoting additional leakage mechanisms. Further elements will be discussed later.
In order to choose the stress voltage for the TDDB experiments, the hard breakdown test has been performed on ten samples for each kind of device. Fig. 4.7 (a) shows the breakdown voltage extrapolated from the hard breakdown measurements shown in Fig. 1.8b. In particular, it is possible to note that the longer the L_{GD}, the higher the breakdown voltage. This is due to lower longitudinal electric field in the GaN channel layer, which increases by reducing L_{GD}, reaching earlier the critical electric field causing breakdown.

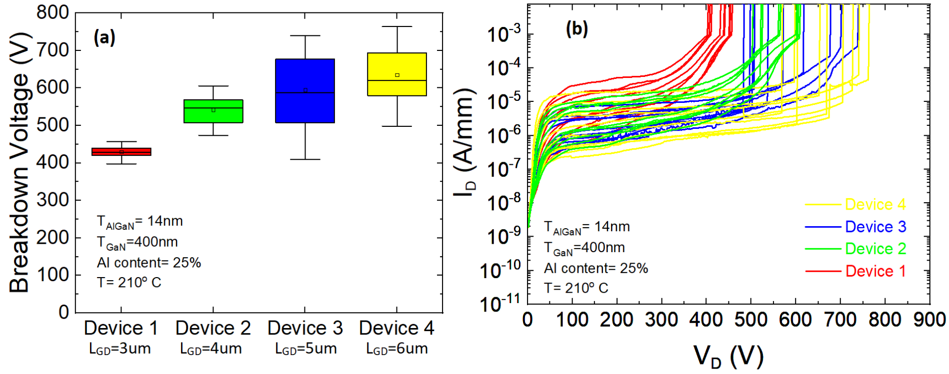


Figure 4.7: *(a) Breakdown voltage range for the devices summarized in 4.1. (b) I_D-V_D plot for the Hard breakdown test performed on ten nominally identical samples for each kind of device.*

Fig. 4.8 shows a representative case of TDDB stress with V_D=460V and T=210° C applied on Device2, 3, and 4. It is worth noting that Device1 has not been considered since the adopted stress voltage (460 V) is higher than its breakdown voltage (see Fig. 4.7), therefore TDDB tests cannot be applied. Device1 will be discussed in detail in paragraph 4.2.2.
As for the hard breakdown tests (Fig. 4.6), the breakdown during TDDB tests occurs between drain and source, since the latter increases after the failure (Fig. 4.8), excluding the vertical breakdown between drain and substrate. As a consequence, the failure might occur (a) through the depletion region of the GaN channel , (b) directly between the drain metal and the source field plate (FP2) or (c) between the 2DEG (close to drain) and the source field plates, as shown in Fig. 4.9.

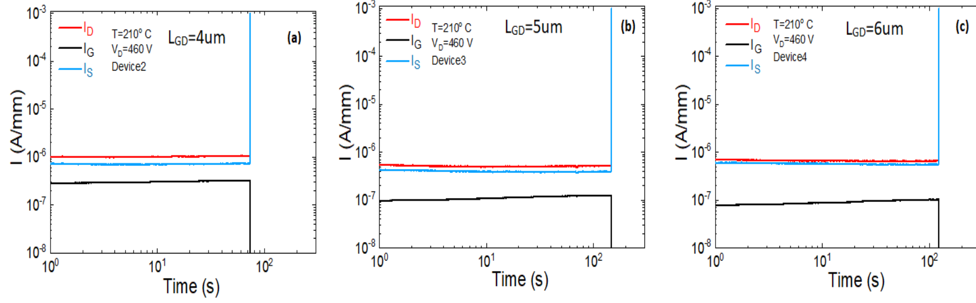


Figure 4.8: *Drain, gate and source current monitored during CVS test for: (a) Device2, (b) Device3 and (c) Device4. The devices feature 400nm thick of GaN channel layer and 14nm thick AlGaN barrier layer with 25% of aluminium content.*

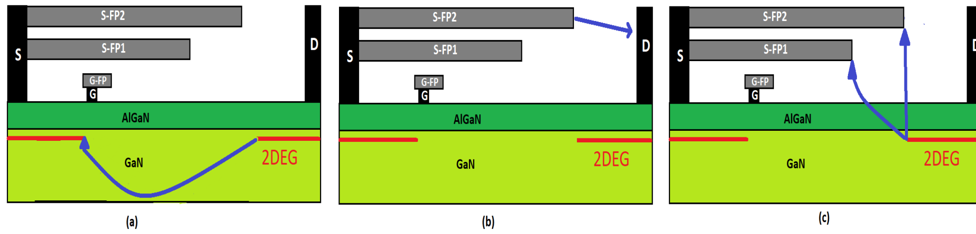


Figure 4.9: *Possible breakdown mechanisms regarding the source: (a) through the GaN channel layer, (b) between the drain metal and the source field plate (FP2) and (c) between the 2DEG and the source field plates*

To determine the location of failure, TDDB tests have been performed on samples with variation in GaN channel thickness, i.e. 400 nm and 200nm as shown in Fig. 4.10 (a) and (b), respectively. By observing Fig.4.10, it is possible to note that Device2, 3 and 4 show the same TTF independent of the GaN channel thickness, suggesting that breakdown is not occurring along the GaN channel (Fig. 4.9 (a)) since no dependency between initial drain leakage current under stress and TTF has been found (see section 4.2.2 for more detail). Moreover, the Device2 feature a longer TTF than Device3 and 4. This exclude the failure between the drain metal and the source field plate since Device2 and 3 have the same distance, which is 1 um shorter than that of Device4. Therefore, the latter should be the most robust one. Overall, it can be concluded that on Device2, 3 and 4 the breakdown is occurring between the 2DEG and the field plates (Fig. 4.9 (c)).

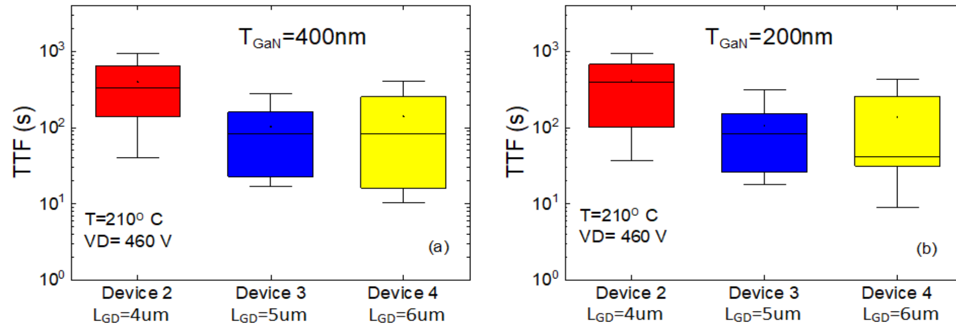


Figure 4.10: *Time to failure distribution for the Device2 (red), Device3 (blu) and Device4 (yellow) with (a) T_{GaN}=400nm and (b) T_{GaN}=200nm. For both cases T_{AlGaN} is 14m with th 25% of aluminum. The TTF values are carried out from constant voltage stress tests at 210° C with V_D=460V.*

To understand the reason why Device2 features a longer TTF compared to Device3 and 4, TCAD simulations have been performed to monitor the electric field distribution in the region below the field plates, i.e. the region interested by the failure during off-state stress. Fig. 4.11 shows the electric field distribution at V_D= 460 V for the 3 devices with different L_{GD} and field plates lengths summarized in table 4.1. In particular, although the differences in L_{GD} and field plate lengths, the electric field is more or less similar in all devices (see Fig. 4.12) whereas the area exposed to high electric field is smaller in Device2 (are below FP2 and FP3) because of the shorter field plates. As a result, similar electric field across a larger area produces a shorter time-to-failure, since TTF (or TTB) is strongly area-dependent.

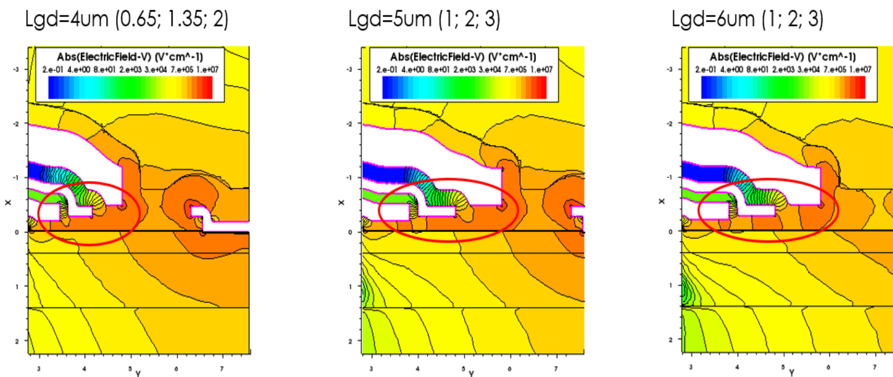


Figure 4.11: *TCAD electric field simulations for the Device2, Device3 and Device4.*

In conclusion, with longer gate-to-drain distance it is possible to obtain higher breakdown voltages (Fig. 4.6), however, it is not a good solution to improve the off-state reliability since, as shown in Fig. 4.10, there is no significant TFF difference between Device 3 and 4 (same field plate configuration and different L_{GD}). On the contrary, by optimizing the field plates geometry, the lifetime can be significantly improved, allowing to reduce L_{GD}, thus reducing the drain-to-source resistance during on-state operation.
So, it is worth noticing that for shorter L_{GD} the breakdown voltage is reduced (around 550V) but, it is enough to be above the operating voltage (200V).

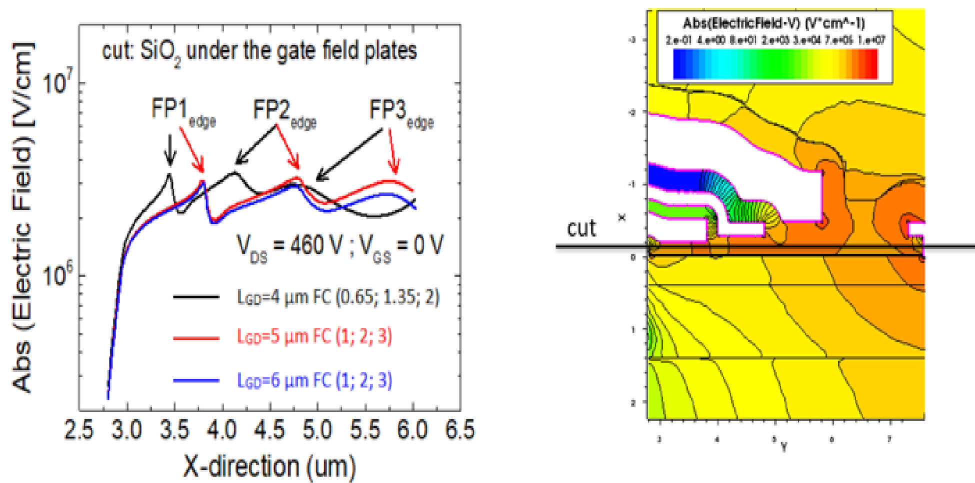


Figure 4.12: *Electric field distribution closer the FP1 and FP2 extrapolated by TCAD simulations for the Device2, Device3 and Device4 with* V_D*=460V.*

4.2.1 Role of the AlGaN on off-state reliability.

Established the location of the failure on device with $L_{GD} \geq 4\mu$m, i.e. between the 2DEG and the source field plates (FP2 and/or FP3), the material layers in between (e.g. the AlGaN barrier) could play a fundamental role on the TTF. Consequently, a off-state reliability analysis has been performed on devices featuring different AlGaN properties. It is worth noting that, because of its higher robustness, only Device2 have been adopted for such investigation.
Fig. 4.13 shows the Weibull plots, carried out from CVS tests, for three different T_{AlGaN} values: 12.5nm (Fig. 4.13(a)), 14nm (Fig. 4.13(b)) and 16nm (Fig. 4.13(c)). The GaN channel layer thickness is 400nm and the Al content in AlGaN layer is 25%. For all the three thickness the TTF values are Weibull distributed with a slope (β) around 1.3, meaning that TTF is

induced by the same degradation mechanism.

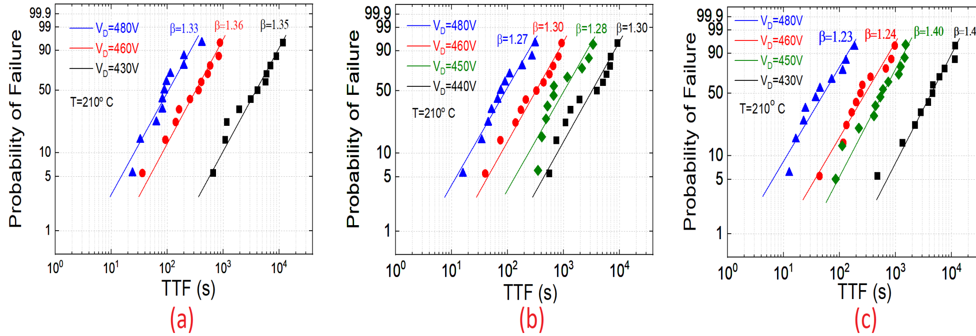


Figure 4.13: *Weibull plots of the constant voltage stress for the Device2, at different AlGaN barrier layer thickness: (a) 12.5nm, (b) 14nm and (c) 16nm.*

From the data presented in Fig. 4.13, the lifetime has been extrapolated for the devices with different AlGaN thickness, as shown in Fig. 4.14 (a) and 4.14 (b). The failure criterion is 1% at 210° C. In particular, by observing Fig. 4.14 (a) it is possible to note that the thicker the AlGaN, the longer the TTF, confirming on more time the failure location, i.e. between 2DEG and source field plates.

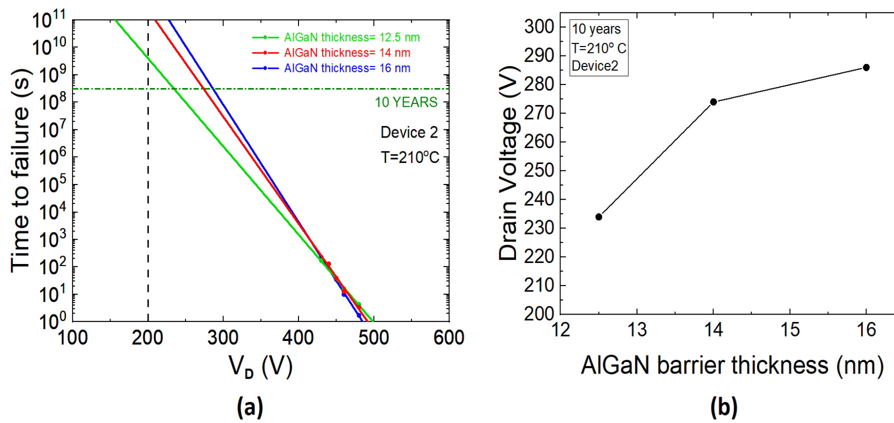


Figure 4.14: *Lifetime plot of the constant voltage stress for different AlGaN barrier layer thickness (a). Drain voltage for ten years of lifetime versus the AlGaN barrier thickness.*

In particular, with a thicker AlGaN barrier two possible situations can occur: i) if the voltage drop across the barrier does not change, the electric

field is reduced; ii) if the electric field is the same (different voltage drop) more defects must be created to form a percolation path because the thicker barrier. In both cases the robustness of the AlGaN layer is improved. By considering a lifetime of 10 years at 210° C, the maximum V$_D$s are 234V, 274V and 286V for devices with 12.5nm, 14nm and 16nm thick AlGaN barrier layer, respectively.
A similar analysis has been performed by changing the aluminum concentration in the AlGaN barrier. In particular devices with the same AlGaN barrier thickness (16nm), same GaN Channel thickness (400nm) and different Al content (25% and 22.5%) have been adopted. Also in this case the TTF values are Weibull distributed with similar β compared with the the case of 25% of Al content (see figures 4.13(c) and 4.15 (a)).

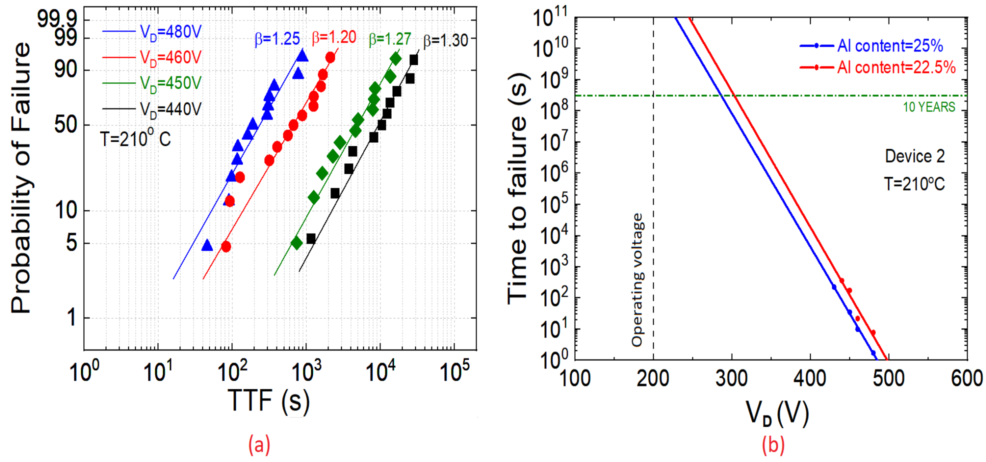


Figure 4.15: *Weibull plot of the constant voltage stress for the Device2, with 16nm thick AlGaN barrier, 22.5% of aluminium and 400nm thick GaN channel (a). Lifetime comparison for different aluminum content (b).*

By comparing the lifetime in the two cases Fig. 4.15 (b), it can be noted that a lower Al content results in an improved lifetime. The drain voltage for the case of Al=22.5% is 305V considering 10 years lifetime, which is 20 V higher with respect to devices with Al=25%. This improvement is related to the piezoelectric effect between the AlGaN barrier and the GaN channel layers. In particular, by increasing the Al content a larger lattice constant mismatch between AlGaN and GaN occurs, possibly facilitating the creation of structural defects. In particular, with increasing Al content, the atomic bonds in the AlGaN are subject to a stronger mechanical strain, consequently, less external energy may be needed to cause a bond to break (defect creation).

It is worth noting that, in order to have failure between 2DEG and source field plate the percolation path must be created in both AlGaN barrier layer and passivation layer. Further analyses are needed to understand who is failing earlier.

4.2.2 From surface to bulk failure

Fig. 4.16 shows the monitored drain current during CVS test for the Device1 with different T_{GaN} and T_{AlGaN}. In particular, in Fig. 4.16 (a) it is shown that decreasing the GaN channel layer thickness, the drain leakage current is lower and the TTF is higher. The same behaviour can be observed by increasing the AlGaN layer thickness Fig. 4.16 (b).

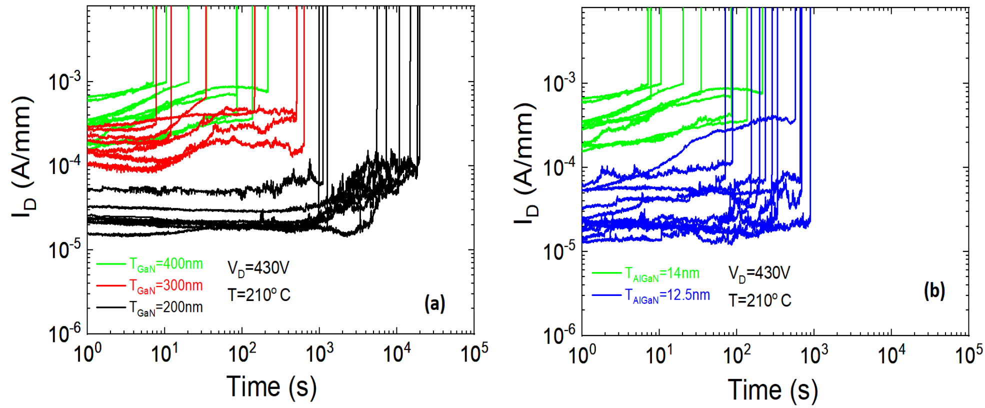


Figure 4.16: *Drain current of the Device1 (L_{GD}=3μm) during CVS tests for different T_{GaN} with the same T_{AlGaN} (14nm) and Al content (25%) (a) and for different T_{AlGaN} with the same T_{GaN} (400nm) and Al content (25%) (b).*

Since, Device1 has the shortest gate-to-drain distance (L_{GD} = 3μm), the motivation of such behaviour can be related to short channel effects, such as punch-through or drain induced barrier lowering (DIBL). Therefore, unlike devices with $L_{GD} \geq$ 4um, Device1 can be affected by breakdown occurring in the GaN channel. In this case, the depletion of the GaN channel layer can play a fundamental role. If the GaN channel layer under the gate is partially depleted, the drain leakage subjected to high longitudinal electric field is higher, promoting the creation of defects hence of the breakdown. In Fig. 4.17 the TTF versus the inverse of the initial drain leakage during the stress is shown. A strong dependency is observed for different GaN (4.17 (a))

and AlGaN thicknesses (4.17 (b)).
In particular, by increasing the AlGaN thickness the 2DEG density increases as well because of the higher spontaneous polarization. As a result, the higher the 2DEG density, the greater the difficulty to deplete such charge. Consequently, the extension of the related depletion region is limited, promoting higher drain leakage, thus shorter TTF. This phenomenon is attenuated by decreasing T_{GaN} since the undepleted GaN layer is reduced.

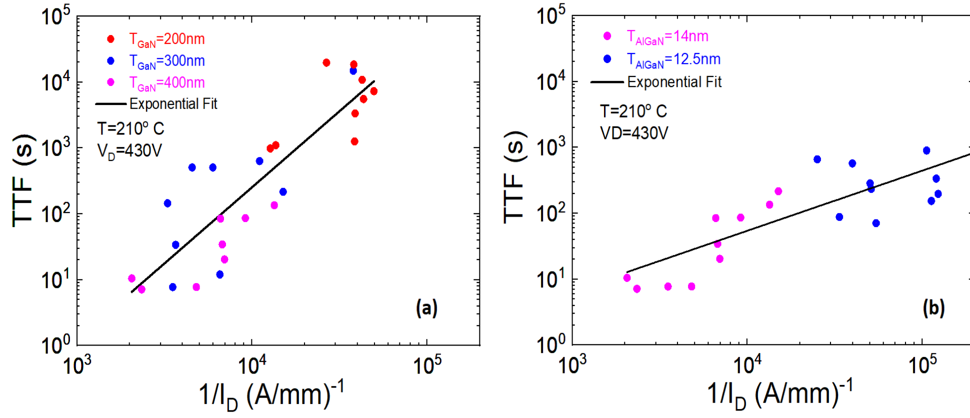


Figure 4.17: *Correlation between the drain leakage current (I_D), monitored at the beginning of the stress, for different T_{GaN} with the same T_{AlGaN} (14nm) and Al content (25%) (a) and for different T_{AlGaN} with the same T_{GaN} (400nm) and Al content (25%) (b), for the Device1.*

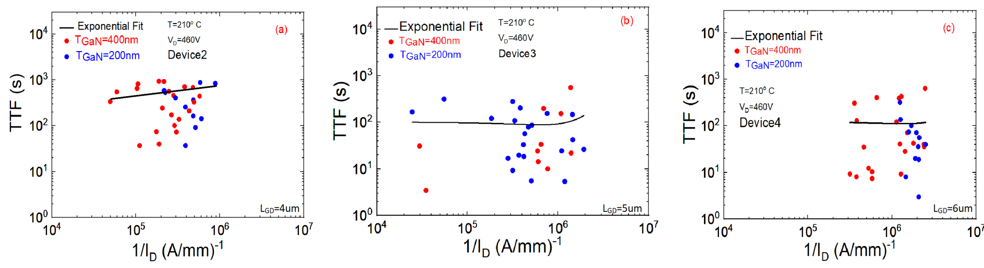


Figure 4.18: *Correlation between the drain leakage current (I_D), monitored at the beginning of the stress, and the time-to-failure for the Device2 (a), Device3 (b) and Device4 (c).*

To further demonstrate the occurrence of the breakdown in the GaN channel layer in the case of devices with L_{GD}=3μm, a similar investigation

has been provided for Device2, 3 and 4. In particular, in Fig. 4.18, the lack of TTF dependency on the initial drain leakage during the stress is shown. In particular, unlike the Device1, by changing the GaN channel thickness no dependency is shown. This confirm that: i) if the L_{GD} is shorter than 4μm the breakdown occurs in the GaN channel (400nm); ii) if longer than 4μm the failure occurs at the surface between 2DEG and source field plates.
Fig. 4.19 shows the time-to-failure distribution by varying T_{GaN} (4.19 (a)) and T_{AlGaN} (4.19 (b)). Note that two different TTF scales are adopted for the two figures. However, as already discussed, the thinner the AlGaN barrier and the GaN channel layers, the longer the TTF. Finally, the lifetime has been evaluated for the two device groups marked by the red boxes, i.e. (1) T_{GaN}=200nm and T_{AlGaN}=14nm, (2) T_{GaN}=400nm and T_{AlGaN}=12.5nm.

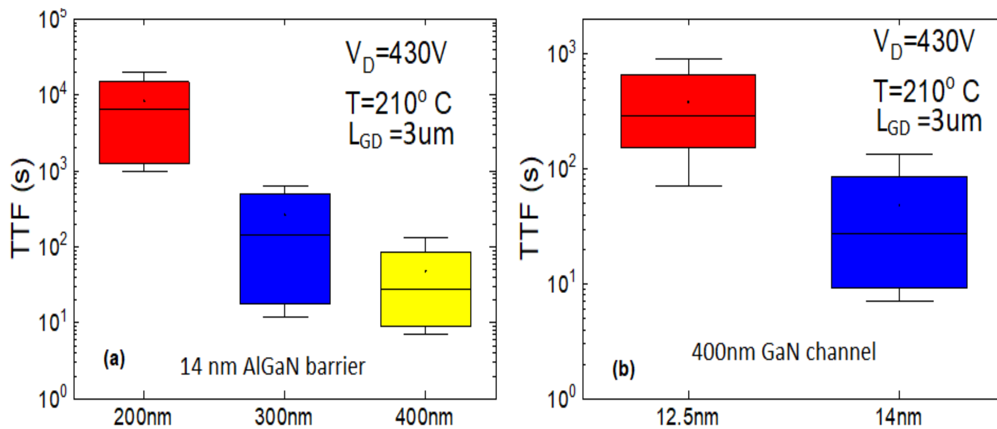


Figure 4.19: *Time to failure distribution for the Device1 for different T_{GaN} with the same T_{AlGaN} (14nm) and Al content (25%) (a) and for different T_{AlGaN} with the same T_{GaN} (400nm) and Al content (25%) (b). The TTF values are carried out from constant voltage stress tests at 210° C with V_D=430V, for the Device1.*

In the first case by performing CVS test at four different voltages, the TTF values are Weibull distributed with $\beta\sim$1.4, as shown in Fig. 4.20 (a). Although, the TTF are Weibull distributed, the lifetime at 1% of failure does not respect the target of 200V for ten years (4.20 (b)).
A strong improvement is noticed for the second case (Fig. 4.21). In particular, the extrapolated maximum drain voltage which guarantees a lifetime of 10 years at 210° C, considering 1% as failure criterion, is 262 V. The latter is higher than devices operating voltage (200 V). This means that by decreasing the GaN channel layer thickness the short channel effect, causing a

premature failure, can be suppressed.

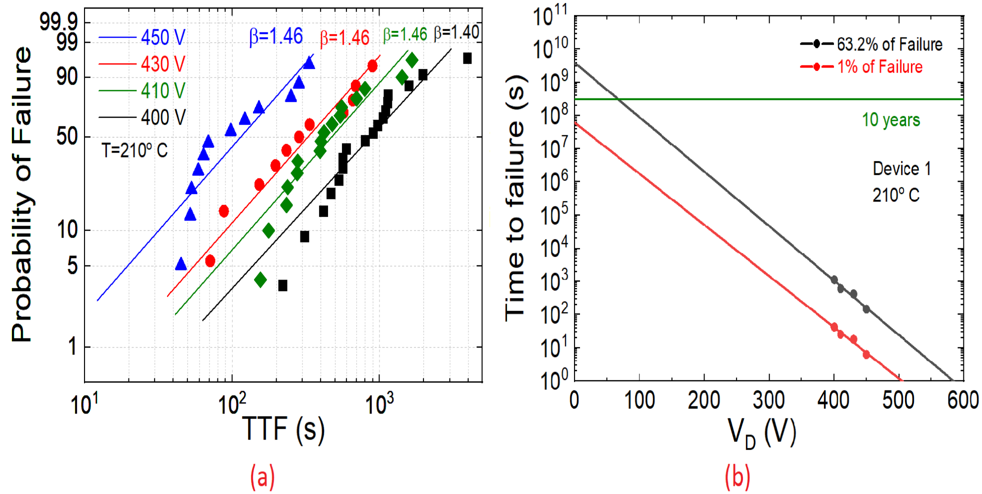


Figure 4.20: *Weibull plot of the constant voltage stress for the Device1, with 12.5nm thick AlGaN barrier, 25% of aluminium and 400nm thick GaN channel (a). (b) Extrapolated lifetime from (a).*

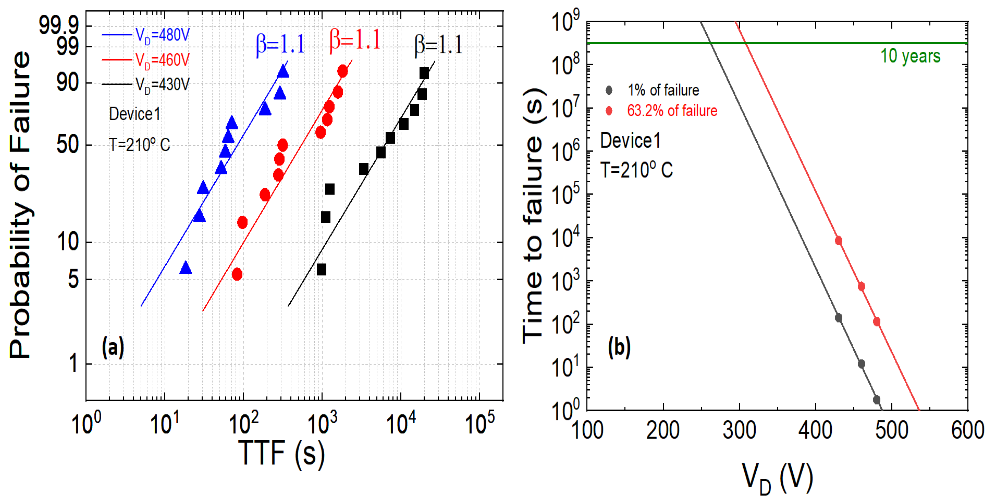


Figure 4.21: *Weibull plot of the constant voltage stress for the Device1, with 14nm thick AlGaN barrier, 25% of aluminium and 200nm thick GaN channel (a). (b) Extrapolated lifetime from (a).*

In table 4.2, the extrapolated lifetime, shown in this chapter, are summarized.

Device	L_{GD} (μm)	T_{GaN} (μm)	T_{AlGaN} (μm)	Al content (%)	V_D for a lifetime of 10 years (V)
1	3	200	14	25	262
		400	12.5	25	<<100V
2	4	400	12.5	25	236
			14	25	274
			16	25	286
				22.5	305

Table 4.2: *Extrapolated lifetime comparison.*

Conclusion

The Off-state reliability of GaN-based power HEMTs with p-type gate has been investigated by means of CVS tests, supported by TCAD simulations, on devices featuring different geometry and structural parameters. Thanks to this approach, several aspects have emerged:

1. the longer the drain-to-gate distance, the higher the breakdown voltage during hard breakdown tests. This is explained by the higher and localized electric field peaks at high drain voltages, which increase by reducing L_{GD}. Such localized electric field peaks are not detrimental for long-term reliability, which is strongly area-dependent;

2. depending on the L_{GD}, two different breakdown mechanisms can occur during CVS tests. In particular, if L_{GD}=3μm the breakdown occurs in the GaN channel (400nm) layer between drain and source (bulk breakdown), whereas if $L_{GD} \geq 4\mu$m the failure occurs between the 2DEG (channel) and the source field plates (surface breakdown);

3. in the case of surface breakdown, the L_{GD} and the GaN layer thickness have not a clear dependency on the long-term reliability. More important is the geometry configuration of the field plates. They need to be optimized to guarantee the smallest area exposed to high electric fields during off-state reliability. For such kind of surface breakdown, the material layers between the field plates and 2DEG play a fundamental role on TTF. In particular, a thicker AlGaN barrier with a lower aluminum content improve the TTF, since in both case the AlGaN barrier is more robust due to longer thickness and lower mechanical stress, respectively;

4. Finally, in the case of bulk breakdown, the GaN layer thickness play a fundamental role, i.e. the thinner the longer TTF. It can be related to effectiveness of the depletion region under the gate. If the GaN layer is partially depleted, the drain leakage subjected to high longitudinal electric field (due to short L_{GD}) is higher, promoting defects creation and shorter TTF. Similarly, by increasing the AlGaN thickness the 2DEG density is higher, limiting the extension of the depletion region. This phenomenon can be suppressed by reducing the GaN thickness.

The tested p-GaN gate HEMTs designed for 200V operation feature an extrapolated 10 years lifetime at a voltage of 234V to 305V extending the target operating voltage of 200 V (see table 4.2).

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