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A Modular Interleaved Converter for Output Current Ripple Minimization in DC Fast Chargers for Electric Vehicles

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To whom made possible this path of personal and intellectual growth.

Sommario

In questo lavoro viene presentata, progettata e testata una topologia circuitale per un caricabatterie DC off-board. Si prevede che sarà in grado di combattere l'ansia da autonomia riducendo significativamente gli attuali tempi di ricarica delle auto elettriche fino a 15-20 minuti, mantenendo contemporaneamente bassi costi di produzione, funzionamento e manutenzione. Il caricabatterie è composto da due stadi di potenza principali, i convertitori AC/DC e DC/DC. Al fine di mantenere i costi più bassi possibili, entrambe le parti sono progettate utilizzando topologie parallelizzate ed organizzate utilizzando gli stessi moduli trifase a due livelli accoppiati tramite induttori. Questa architettura consente di utilizzare i classici moduli trifase industriali sfruttando i vantaggi garantiti dalla produzione in serie e consentendo allo stesso tempo un'espansione senza sforzo grazie alla sua intrinseca modularità. Grazie alle connessioni interlacciate, è possibile raggiungere un'alta efficienza distribuendo simmetricamente corrente e potenza tra i rami. Inoltre, questa topologia può gestire flussi di potenza bidirezionali e potrebbe essere utilizzata per operare in entrambe le modalità Grid to Vehicle (G2V) e Vehicle to Grid (V2G). Al fine di ridurre le dimensioni e i costi dei componenti reattivi, viene sviluppata una strategia di controllo in grado di mantenere un ripple di corrente teoricamente nullo in qualsiasi condizione operativa. L'architettura del caricatore proposta utilizza un BUS AC di ingresso seguito da uno stadio raddrizzatore attivo. Una strategia di minimizzazione del ripple agisce sulla tensione variabile del BUS DC in accordo con il duty cycle del chopper mantenendo nullo il ripple di corrente. Nel frattempo, lo stadio DC/DC fornisce la corrente di uscita richiesta. Questa strategia coinvolge l'AC/DC con i compiti di regolare il livello di tensione del DC BUS e correggere il fattore di potenza in ingresso. Viene utilizzato un sistema di controllo model-based in grado di assicurare che la corrente di ogni ramo segua un riferimento di corrente medio. Attraverso una rete di ribilanciamento gli sbilanciamenti di corrente vengono attivamente compensati. Le simulazioni vengono eseguite utilizzando l'ambiente MATLAB Simulink e convalidate attraverso misurazioni in laboratorio su un prototipo dimensionato su scala ridotta di potenza.

Abstract

In this work, a DC off-board fast battery charger topology is presented, designed, and tested. It is expected to be able to fight the range anxiety by significantly diminish the EVs' charging times up to 15-20 minutes, meanwhile keeping low manufacturing, Operation and Maintenance (O&M) costs. The charger is made out of two main power stages the AC/DC and DC/DC converters. In order to keep the costs lower as possible, both parts are designed using interleaved topologies organized by using the same two-level three-phase modules coupled through reactors. This architecture allows to use the already well-known industrial three-phase modules taking advantage of the benefits guaranteed by mass production and at the same time permitting an effortless expansion thanks to its modularity. Thanks to the interleaved connections, it is possible to reach a high efficiency by distributing current and power evenly among the legs. Furthermore, this topology can handle bidirectional power flows, and it might be used for operating in both Grid to Vehicle (G2V) and Vehicle to Grid (V2G) modalities. In order to reduce the dimensions, and the costs of the filters, a control strategy able to keep a zero current ripple at any operative condition is developed. The proposed charger architecture uses an AC input BUS followed by an active rectifier stage. A ripple-free strategy acts on the variable DC BUS voltage according to the chopper duty cycle keeping the current ripple null. Meanwhile, DC/DC provides the requested output current. This strategy involves the AC/DC with the tasks to regulate the DC BUS voltage level and correcting the input power factor. A model-based control system ensures that every leg's current follows an average current reference signal. Legs' currents are actively rebalanced throughout a current rebalancing network. Finally, the simulation results are carried out trough MATLAB Simulink and validated with laboratory measurements on an adequately scaled prototype.

Contents

Introduction

The highly globalized society heavily underpins on transport systems. They are directly involved in the creation of market value, and their relevance in the Gross Domestic Product (GDP) computation has increased in the last decades. Transport improves the standard of life and rate of employment thanks on its capability to connect people, goods, and services. However, it has adverse effects on the environment, climate, and human health. In order to attenuate these drawbacks, a green shift towards decarbonized transport systems is necessary.

Although Europe managed to obtain a generally noticeable Greenhouse Gasses (GHGs) emissions reduction, the transport systems sector is still responsible for a quarter of them. Furthermore, it can be directly linked to the deteriorated urban areas quality of air that often does not meet standards set by European Union (EU), World Health Organization (WHO), and Environmental Protection Agency (EPA) [1].

Institutions and governments are setting multiple future targets to reduce anthropological environmental impacts. In the last decades, multiple worldwide organizations have faced this problem. United Nations (UN) Intergovernmental Panel on Climate Change (IPCC) throughout, United Nations Framework Convention on Climate Change (UNFCCC) have produced famous legally binding treaties like the Kyoto Protocol and Paris Agreement. EU's overall goal is to reduce by 85-90% GHG emissions by 2050. A gradual reduction pattern able to provide relevant outcomes without giving up current economic growth rates has been studied.

Firstly, throughout Horizon 2020 and NER300 financing programs, research and innovation are being carried out in fields like transports and low-carbon projects. Carbon dioxide removing technologies such as Land Use, Land-Use Change, and Forestry (LULUCF) and Carbon Capture and Storage (CCS) have been funded with about 2 billion euro. The 2020 main targets are to cut GHG emissions by 20% (compared to 1990 levels), having 20% of the produced energy using Renewable Energy Sources (RES) and increase by 20% the overall energy efficiency.

Secondly, in the 2030 climate-energy framework, previously cited data are expected to reach 40%, 32% and 32.5% for GHG emissions cuts, RES share, and energy efficiency improvement, respectively.

Finally, Europe plans to become the world's first major economy to go climate-neutral by 2050 [2]. In [3] European Commission (EC) have set 10 goals for reaching the 60% transport GHG emission reduction benchmark. Among them, the first goal explicitly referred to new sustainable propulsion systems able to reduce to the half the use of Internal Combustion Engine Vehicles (ICEVs) in urban transport by 2030, phase them out in cities by 2050 and lastly achieve essentially carbon-free city logistics in major urban centers by 2030. Achieving these commitments require complete decarbonization of the passenger car fleet by 2050. Meanwhile, the more

ambitious COP21 that have stipulated the Paris Agreement demands a complete decarbonization of transport to limit temperature rises to 1.5℃.

It is then apparent how a relevant part of the planned GHGs emissions reduction is expected to come from newer and cleaner road transports technologies. Transport is the only primary sector having increased its environmental impact since 1990, and a considerable effort is therefore necessary. For this reason, more efficient ICEVs are unlikely to be sufficiently compelling to achieve previously cited targets. EV is one of the most promising ways of moving toward a more sustainable transport system [1]. Although replacing ICEVs with EVs is not enough, the CO_2 emissions reduction strongly depends on the mix of primary energy sources used to generate electricity. As relevant, the RES component is as powerful the CO_2 reduction could be.

As aforementioned, EVs are expected to be a key component of the future mobility system. Moreover, cars are much easier to decarbonize if compared to other vehicle types. The market is entering a more mature stage, and comparisons at least between Alternative Fueled (AF) vehicles can be made. As visible in Figure 1, since 2016, electricity-powered vehicles have constantly outperformed gas-based solutions (Compressed Natural Gas (CNG) and Liquefied Petroleum Gas (LPG)) in terms of European new registrations AF market share. Battery Electric Vehicles (BEVs) and Plug-in Hybrid Electric Vehicles (PHEVs) comprised both around 1.2% of the new car registrations in 2018. Moreover, BEVs are expected to roughly double 2019 PHEVs' new registrations with respectively 1.9% and 1%. Fuel Cell Electric Vehicles (FCEVs) have not reached yet a satisfying Technology Readiness Level (TRL) for being widely distributed in the market. Previously stated selling considerations are performed using European Alternative Fuels Observatory (EAFO)[1] data.

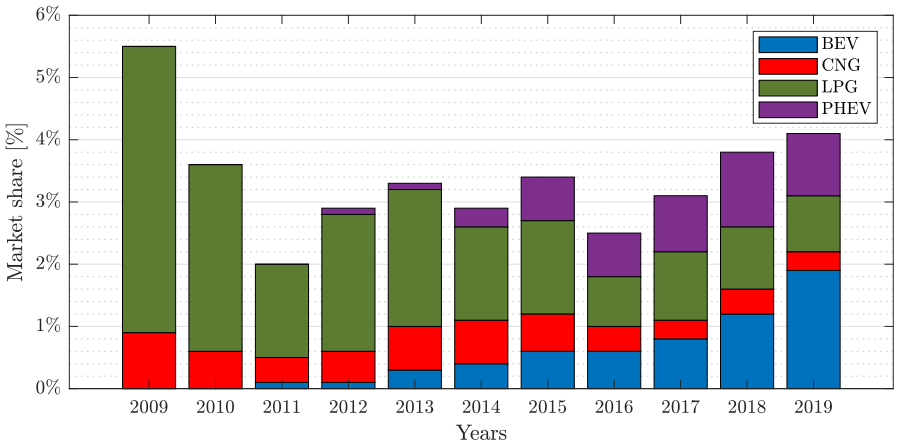


Figure 1: AF vehicles new registrations market share

Although forecasts are still unreliable most of the financial surveyors and analysts agree that break-even point between ICEVs and BEVs purchase cost should be met during the mid-2020s, with Total Cost of Ownership (TCO) lagging from two to four years [4]. The sales parity should be reached around 2037, and in 2040,

[1]More information can be found at European Alternative Fuels Observatory (EAFO) website www.eafo.eu

30% of the global fleet could be electric. Prices and diffusion of Zero-Emissions Vehicles (ZEVs) are strictly correlated with charging infrastructure diffusion. In the next decade, a relevant acceleration in BEVs diffusion is expected. However, if a comparable acceleration does not involve charging points diffusion, a relevant slow down is expected to happen during the early 2030s. Customers able to take advantage of overnight home charge are expected to be the first ongoing electric, a second customers wave is expected as soon as a reliable charging network is available. Furthermore, the current selling trend of hybrid solutions could gradually fade and become a negligible fraction of BEVs sales.

Many barriers to electric vehicles are incrementally being overcome. Batteries cost is falling, it is reaching the industrial target of 100$/kWh and in 2030 is expected to halve current prices and stabilize around 70$/kWh. This prices evolution is helping on addressing the initial cost barrier and driving to greater battery sizes. Overall the average range availability has more than doubled its value from the 160km of 2010 to about 400km of 2019. The increasing availability of electric vehicle models is attracting more prospective vehicle owners. However, the development of sufficient charging networks, is still a work in progress. Although the regular overnight home charging constitutes one of the great advantages of electric automotive technology, it does not fulfill every charging needs, and a mix of workplace charging, public charging, and fast charging is indispensable [5]. As described above, BEVs offer relevant opportunities to reduce GHGs and local air pollution, especially in the "in-use" phase of vehicle life. However, considering the whole Life Cycle Assessment (LCA) of an EV, there is the possibility to increase impacts in other areas such as human toxicity and ecosystem impacts. Focusing on vehicle design, the battery pack constitutes the most environment impacting part of the vehicle. Customers' expectations might be a key factor for future battery development. Larger batteries provide greater energy leading to a reduction of users' "cruising range anxiety". However, larger batteries require a higher quantity of raw materials and greater manufacturing energy resulting in greater environmental impacts. Furthermore, the extra weight also leads to a bigger energy requirement during BEVs usage. Those impacts cross the life cycle could be minimized if the automotive industry is encouraged to propose vehicles with modest ranges and batteries sizing but able to fully charge in a few minutes.

A huge effort is put on research around the feasibility of BEV batteries playing an active role in the electricity grid, to store excess renewable power and provide grid-stabilizing services. These services are commonly described under umbrella terms such as Vehicle to Grid (V2G), Vehicle for Grid (V4G) and Vehicle to Home (V2H). In order to take advantage of the relevant energy stored inside BEVs, more ductile converters topologies able to withstand bidirectional power flows are necessary.

The aforementioned regulatory and design constraints must be balanced with wide charging networks with an appropriate number of outlet per stations and charging settings.

Usage statistics have pointed out how fast-charging stations play a key role thanks to their ability to guarantee excellent distance coverage and the broad charging flexibility. Data shows how fast charge outlets have been used not only for long

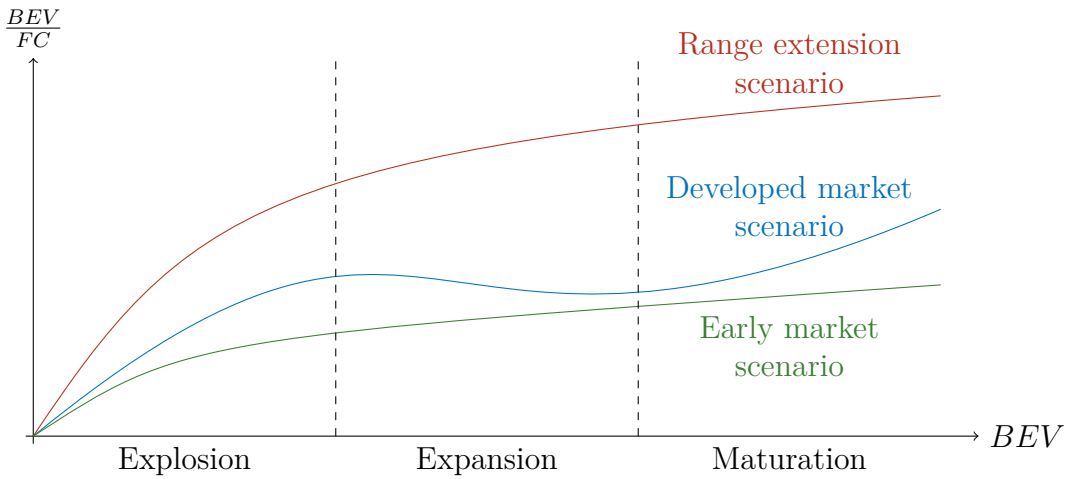


Figure 2: Possible scenarios of BEV over FC ratio in different BEVs' penetration stages

journey charging but also as a substitute for the home and the slower public charging. During the early market (green line in Figure 2), more fast chargers (FCs) per vehicle are needed to obtain sufficient geographic coverage, regardless on the market stage. As the market develops (blue line in Figure 2), less FCs per vehicle are needed as utilization increases. In a market scenario where FCs are employed for extension range only (red line in Figure 2), fast charging Electric Vehicle Supply Equipment (EVSE) are expected to have a marginal relevance if compared with the previously cited scenarios once the market have reached a considerable expansion. On the other hand, only a limited range of models are already able to take advantage of the full available power. An economically speaking feasible way for achieving these targets is to implement low cost and modular convert topologies able to guarantee a wide multi-column stations diffusion and aposteriori power scaling capability. Moreover, a discrete fast charging power deploying by mean modules based paradigm permits to effectively response to the different market stimulations in terms of FCs' diffusion and absolute power capability. Charging infrastructure is the most significant long-term challenge for EV, and comprehensive, user-friendly urban and long-distance fast-charging stations are a precondition to the growth of the market.

When new technologies start to grow multiple standards appear on the market. Every Operation and Maintenance (O&M) try to impose its own standard in order to gain market share and customers loyalty. For what it concerns EV standards, two main areas should be considered, charging plugs and charging levels standards.

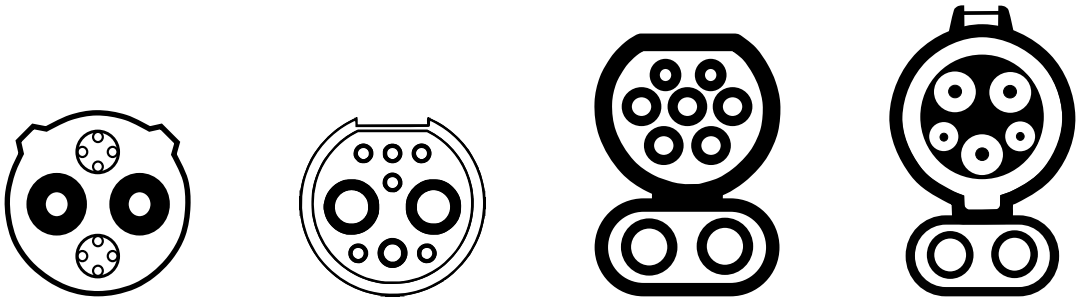
When it comes to speak about charging plugs, there are mainly four main standards, each of one well settled in a particular market and geographical area. Moreover, depending on what kind of charging is carried out, plugs can carry AC or DC for respectively onboard and offboard chargers. In this thesis, offboard DC fast charging is considered. Combined Charging System (CCS) type 2 (also known as Combo 2) (Figure 3c) has been introduced as a common DC charging plug for all the European market. It shares most of the connection available in the AC Type 2 connector. However, it adds two power pins able to carry DC. Similarly, CCS type 1 (Figure 3d) is mainly employed in the North America market. One of the most

used standard is the Chinese Guobiao Standard (GB/T) (Figure 3b) charging plug that shares most of the features present in other standards [6]. One of the oldest DC charging plug is the so-called CHArge de MOve (CHAdeMO). It is mainly employed in the Japanese market, although, it has initially diffused in North America and Europe it is rapidly being overcome from CCS standards. All the connectors have in common the presence of power connectors and a communication link between the offboard power converter and the internal Battery Management System (BMS). Tesla motors have introduced in the North America market a property standard able to carry DC power over a regular Type 1 AC plug. Most of them have been described inside IEC 62196 and SAE J1772 standards [7], [8]. In Table 1, DC charging plug features are collected.

Table 1: DC charging plugs standards

Denomination	Region	Typical power	Maximum power	Standard
CHAdeMO	Japan	$50kW$	$400kW$	IEC 62196
CCS Type 1	America	$50kW$	$400kW$	IEC 62196
CCS Type 2	Europe	$50kW$	$400kW$	IEC 62196
GB/T	China	$50kW$	$240kW$	GB/T 20234
Tesla	America	$125kW$	$145kW$	Proprietary

For what it concerns charging power, multiple denominations have been introduced during the time. A first classification based on the power rating is known as charging level. Level 1 is considered the slowest charging rate, and it is usually employed in nations where the grid phase voltage is $120V$ AC for no more than 11kW. Level 2, is considerably faster than Level 1 because able to reach $22kW$, it employs AC $230V$ grids. The charging rate considered in this thesis is Level 3 (also known as Fast Charging). It employs DC voltages up to $1000V$ and powers than start from $50kW$ and reaches $400kW$ in the latest installations.



(a) CHAdeMO (b) GB/T (c) CCS Type 2 (d) CCS Type 1

Figure 3: DC charging plugs

Depending on what type of connection and on the safety devices used, charging modes are defined. Mode 1 does not require any protection device or communication channel between EV and charger. Mode 2, it employs a communicating channel called pilot function, and a protective circuit breaker is required. Mode 3 differs from Mode 2 for the requirement to have one cable terminal hardwired to the EVSE. Moreover, Mode 4 adds a continuous bidirectional communication between EV's BMS and the EVSE. This communication can be made throughout different

technologies depending on what plug is used. For instance, CCS and CHAdeMO plugs, respectively employ Power Line Communication (PLC) and Controller Area Network (CAN) bus.

Overall, EVSEs equipped with modular highly standardizes bidirectional modules are expected to be one of the key part in the transport electrification in the near future. Moreover, power converters are expected to successfully follow market and political scenarios. Charging power availability must be tuned according to the EV diffusion. Generally, charging times should be guarantee as lower as possible, ensuring an EVs charging experience more similar to the common ICEVs refueling. For the above mentioned reasons, a battery charger topology able to ensure modularity, upgrade capability, low cost and fast charging is introduced in next chapters.

Chapter 1

Proposed Topology

Many converter topologies and modulation strategies have been introduced in the literature. Speaking about inverters (DC/AC converters), most of the research activities are oriented to the multilevel topologies such as Neutral Point Clamped (NPC) [9], [10], Level Doubling Network (LDN) [11], Modular Multi-level Converter (MMC) [12], Flying Capacitor (FC) and cascaded H-bridge [13]. Despite the improvement of the performances in terms of harmonic content and ripple amplitude of the output current and voltage, they all require more components if compared with the standard two-level three-phase converter. In the field of rectifiers, the academic interest has passed from passive diodes-based solutions like 6 and 12 pulses rectifiers to active rectifiers, based on power switches solutions such as Vienna [14], Swiss [15], [16], and Totem Pole rectifier (also simply known in literature as Active Rectifier (AR)) [17], [18]. However, it can be seen that by considering a three-phase system the Totem Pole topology becomes like a three-phase inverter used in the opposite direction, having also a Power Factor Correction (PFC) capability. Concerning bidirectional DC/DC voltage lowering stage, the most widely studied topology is the synchronous buck converter and its multi-phase version called synchronous multiphase Buck Converter (BC) [18]. It can be noticed that if the number of considered phases is set to three the topology coincides to three full legs with the poles coupled with an interleaved connection. It can be then concluded how every power stage (regardless if it is an active rectifier, inverter or chopper) can be implemented by means of two-level three-phase modules with the connections properly handled in order to achieve the desired tasks (Figure 1.1). Despite it is not the best solution when speaking about harmonics and ripple amplitude, it can be certainly concluded that it constitutes the most standardized solution among all the proposed topologies presented in the literature.

By mean of a proper routing of these simple blocks, it is possible achieving improvements in terms of ripple and efficiency. Interleaved configurations are one of the most suitable topologies for charging EVs since they are able to ensure modular design approaches. The best performances can be achieved for level 4 DC fast charging rates thanks to the possibility to evenly share the great involved power. As visible in Table 1.1, most of the EVSE power electronic producers have currently in their portfolio at least one series of products that implements somehow the modularity paradigm explained before [19]–[24].

It is possible to make either AC/DC and DC/DC based on multiple standardized bidirectional two-level three-phase block (Figure 1.1). Interleaved version of AR and

Table 1.1: Overview of DC modular fast charger commercially available

Producer	Denomination	Base unit	Power module	Available ratings
ABB	Terra HP	N/A	175kW	175/350kW
Watt&Well	BMPU-11	11kW	N/A	150/300kW
Alpitronic	Hypercharger	N/A	75kW	75/150/225/300kW
ChargePoint	Express Plus	31.25kW	156kW	156/312/468/500kW
Signet	FC100K	N/A	N/A	50/100kW
Efacec	HV175	N/A	163kW	163/326kW
BTC Power	HPCT	N/A	50kW	100/150/200kW
Tesla	Supercharger	11.5kW	N/A	120/150kW

the BBC are know respectively as Interleaved Active Rectifier (IAR) and Interleaved Buck Converter (IBC). The main idea is to share current equally (and therefore power) on multiple legs, regardless of what task the block is doing (AC/DC or DC/DC operations) and on the power flow direction. This inherent capability to carry bidirectional power flows makes it particularly suitable for storage management application like BEVs charging and V2G services.

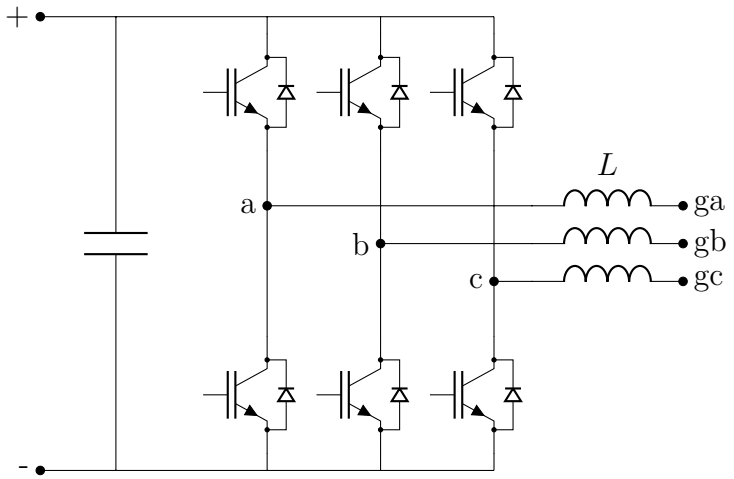


Figure 1.1: Two-level three-phase base block

In order to share current that usually would flow into a single leg among multiple legs is necessary to interleave them using properly sized reactors (visible in Figure 1.1 as L) [25]–[27].

1.1 Back to Back AC/DC Interleaved Converter

The interleaving fast charger topology shown in Figure 1.2 is considered in this thesis. It must respect all the design and economic constraints mentioned before. The proposed topology can be connected to a low voltage grid and provide an output voltage range suitable for battery charging purposes.

Firstly, a modular configuration able to use the same block of Figure 1.1 in both AC and DC side has to be considered. Thanks to this technical solution it facilitates a future power scaling by simply stacking more blocks in parallel to the

Table 1.2: Proposed system parameters

Parameter	Symbol	Value	Unit
Rated power	P	150	kW
Base block rated power	P_b	50	kW
Number of block per side	M_s	3	
Total number of block	M	6	
Number of legs per base block	N_b	3	
Number of legs per side	N	9	
Line to line RMS voltage	V_g	400	V
Grid frequency	f	50	Hz
Maximum DC link voltage	V_{DCM}	800	V
Minimum DC link voltage	V_{DCm}	600	V
Maximum output voltage	V_{oM}	800	V
Minimum output voltage	V_{om}	200	V
Switching frequency	f_{sw}	16	kHz
Reactors inductance	L	0.5	mH
Reactors resistance	R	20	$m\Omega$
DC link capacitance	C	1	mF

already present one without oversizing the system and keeping initial deployment cost as lower as possible. A further benefit is the possibility to operate with a smaller power rating in case of faults or programmed maintenance. It is possible to freely keep out blocks without shutting completely down the converter. Underload conditions can be avoided implementing the classic, $N+1$ redundancy. Overall, the system becomes more fault resilient and at the same time "low cost".

Secondly, each module is a replica of the others. Moreover, the three-phase two-level module is by far the most common power block thanks to its broad commercialization and ductility. These considerations ensure to take advantage of mass production economic benefits keeping production and therefore replacement and expansion costs as small as possible. Despite being "low cost" blocks, they have reached a high level of standardization and can ensure optimization in terms of Electromagnetic Interference (EMI) [28], [29], thermal layout, protection devices, and driving units.

Finally, this redundancy adds a further degree of freedom on the firing timing of each leg. Thanks to proper handling of the driving signal, it is possible to automatically reduce ripple in every part of the converter (I/O currents and DC link voltage) [30]–[35]. Reactive components sizing constraints are therefore less strict and in general, smaller components are needed. Inductors and capacitors are usually the bulkier components in a power converter. It is then possible space and weight saving leading to a more efficient room utilization. When it comes to speak about bus DC capacitor, it is known that ripple is one of the most degrading agent in electrolytic capacitors [36], [37].

In this thesis a symmetrical scheme (Figure 1.2) with nine legs and therefore three blocks for either the AR/inverter stage and the chopper has been developed.

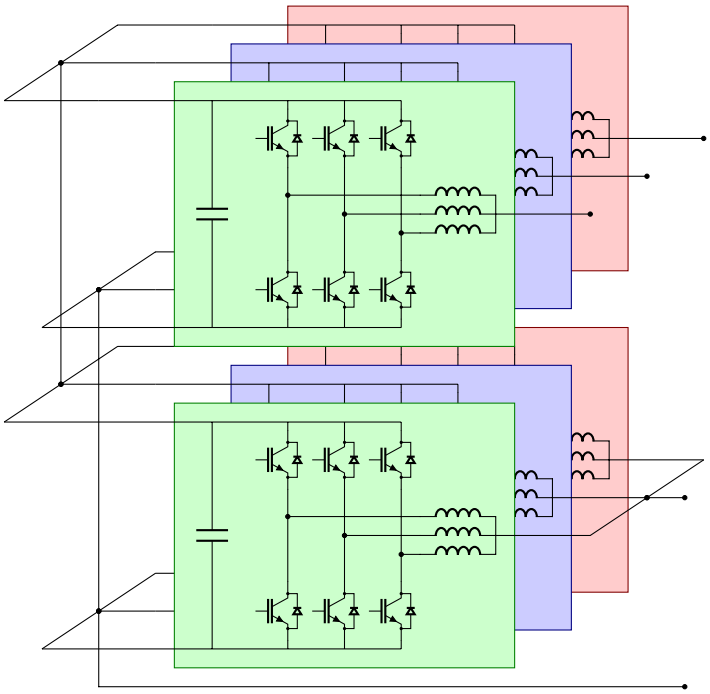


Figure 1.2: Battery charger topology

In Table 1.2 design parameters are summarized.

1.1.1 Active Rectifier Power Stage

As visible in Figure 1.3 the AC/DC stage (suitable for both active rectifier and inverter purposes) takes advantage of three legs per phase. As explained above the power can be evenly shared among them, making therefore possible using small size low-cost power switches. As shown in [33], [35], [38], DC link and input current ripple decrease when each leg of each phase is driven by mean of uniformly shifted carriers (Figure 1.4) [18], [39]–[42]. In each power block, there are N_b carriers, and each one has been shifted by t_{sw}/N_b. When it comes to speak about the modulating

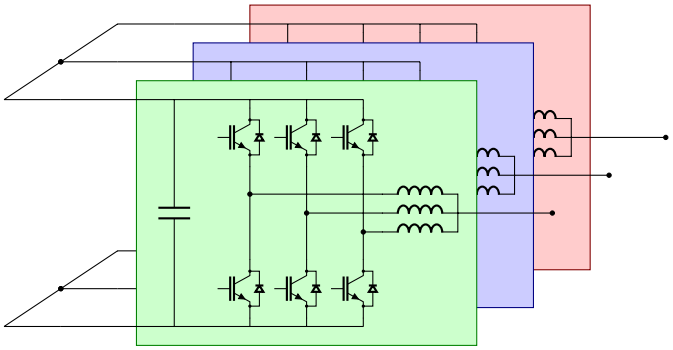


Figure 1.3: Interleaved active rectifier topology

signal generation it is necessary to operate on a synchronous framework able to take into account the parallelized design property of each phase. Despite what it has been done in section 1.2.2, inductors' ohmic component has been taken into account. For the sake of completeness, a generic analysis on N_b legs is carried out.

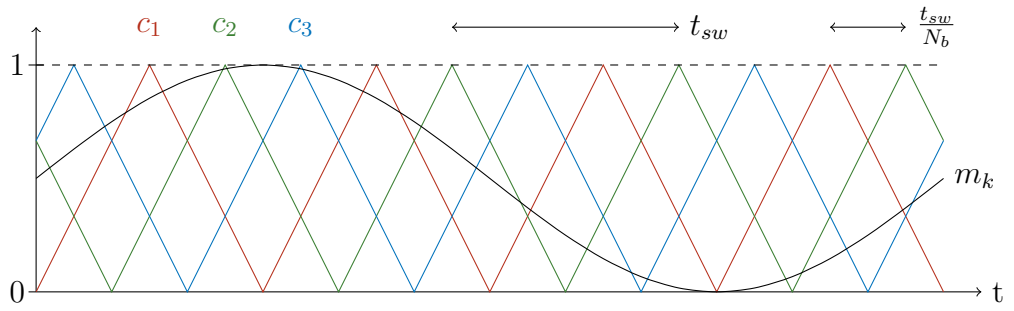


Figure 1.4: Drawing that shows $N_b = 3$ shifted carriers (c_1, c_2, and c_3) and a generic modulating signal m_k (SPWM)

As visible in Figure 1.5 each phase leg can be averaged on a switching period leading the whole phase power block to a simplified single branch equivalent system (Figure 1.6) [43]. The resultant system is equivalent to a standard two-level inverter driven with a switching frequency N_b-fold times higher (same finding shown in 1.2.2) and equivalent line parameter N_b times lower (Figure 1.7). An equivalent circuit based on computations made on the Staimnetz domain is found (Figure 1.9).

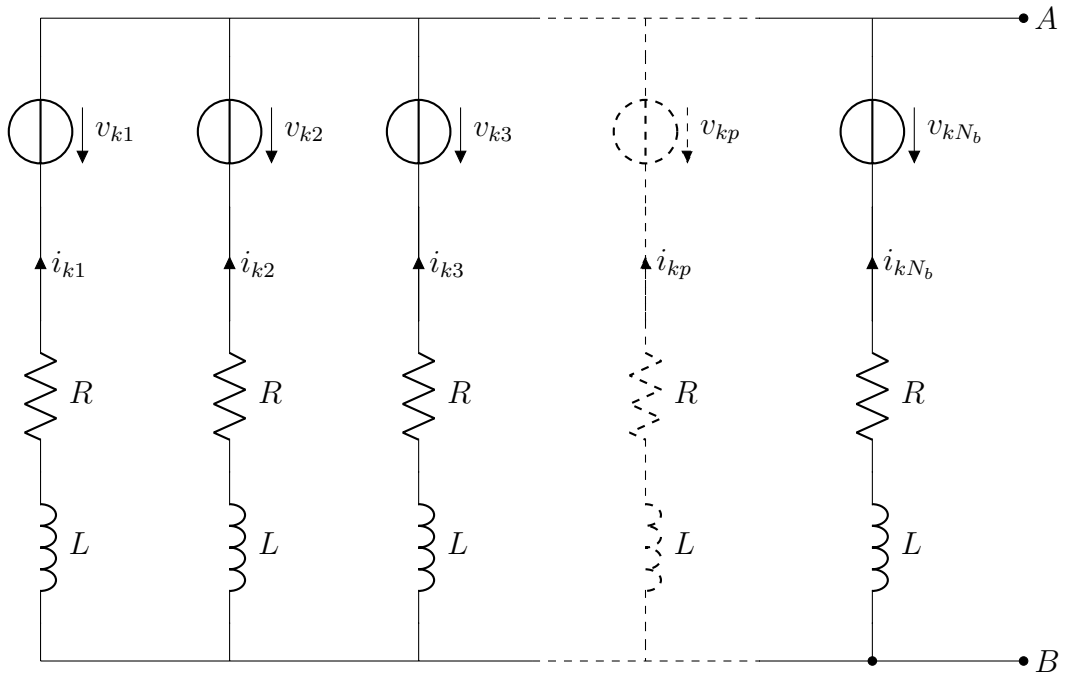


Figure 1.5: Generic phase block legs averaged on a switching period

Driving PWM signals generation is not done having as a primary task the pole voltages generation but the DC link voltage stabilization. For the sake of simplicity, conduction and commutation losses are neglected. As visible in Figure 1.7, capacitor's current depends on either load (i_{IBC}) and line currents (by mean of i_{DC}). Each phase current is combination of legs' current joining the same point of common coupling.

$$i_k = \sum_{p=1}^{N_b} i_{kp} \tag{1.1}$$

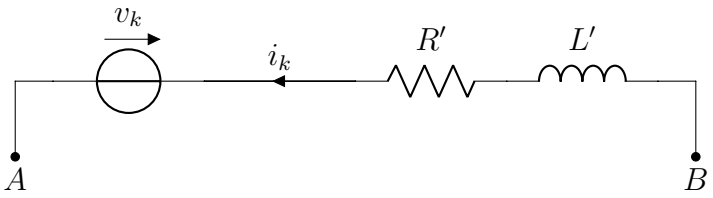


Figure 1.6: Generic phase block averaged on a switching period

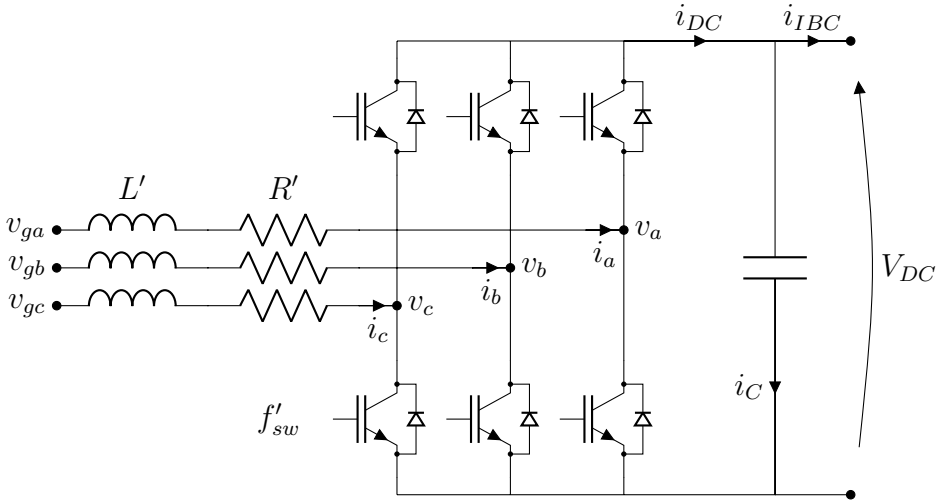


Figure 1.7: Equivalent three phase inverter

each leg inside the same power block is driven using the same modulating signal. It is then possible consider each pole voltage equal if averaged on a switching period t_{sw}. Therefore it is possible state that:

$$v_k = v_{k1} = v_{k2} = v_{k3} = v_{kp} \tag{1.2}$$

Being $v_k = m_k V_{DC}$, (1.2) can be rewritten as:

$$m_k = m_{k1} = m_{k2} = m_{k3} \tag{1.3}$$

What state above can be easily seen by mean of the folowing power balance:

$$P_{IAR} = \sum_{k=a}^{c} \sum_{p=1}^{3} v_{kp} i_{kp} = \sum_{k=a}^{c} v_k i_k = V_{DC} i_{DC} = V_{DC}(i_C + i_{IBC}) = P_C + P_{IBC} \tag{1.4}$$

deviding each term by V_{DC}:

$$\sum_{k=a}^{c} m_k i_k = i_{DC} = i_C + i_{IBC} \tag{1.5}$$

where v_{kp} are pole voltages, v_k phase block equivalent pole voltages, i_k line currents and i_{kp} legs currents. Moreover, m_k blocks' duty cycle, V_{DC} bus DC voltage, i_C capacitor's current and finally i_{IBC} buck power stage input current. Letters k and p are respectively referring to phases denomination a, b and c and legs numbering 1, 2 and 3.

Instead of finding a proper PWM able to generate i_{DC}, the control criteria is to keep constant (on a switching period base) V_{DC}. Having a constant DC link voltage is equivalent to state that i_C and P_C are both nulls. Indeed:

$$P_C = \frac{\mathrm{d}W_C}{\mathrm{d}t} = \frac{\mathrm{d}}{\mathrm{d}t}(\frac{1}{2}CV_{DC}^2) = \frac{1}{2}CV_{DC}\frac{\mathrm{d}V_{DC}}{\mathrm{d}t} \tag{1.6}$$

Condition (1.6) ensures the maximum transfer of power between IAR and IBC. Neglecting losses it can be written as:

$$P_{IAR} = P_{IBC} \tag{1.7}$$

Voltage Oriented Control

The actual control is carried out on a synchronous system (Park's framework) [44]–[46]. However, to compute needed space vectors, an equivalent circuit for each phase is necessary. Taking advantage of (1.2) it is possible to replace each leg pole voltage with an independent voltage source equal to v_k. In this way, one could immediately see that each phase power block can be decoupled from the others. Indeed, following statements refer to a generic power block (N_b legs) of the generic phase k. Furthermore, being the front end side of the AR operating on a sinusoidal regime, all the quantities are treated as phasors and impedances. In Figure 1.9, the

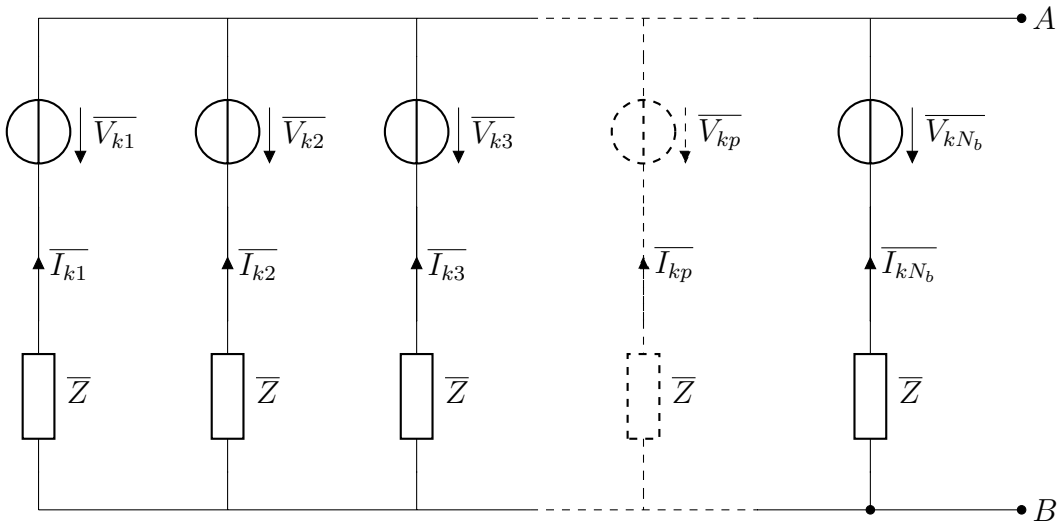


Figure 1.8: System in the Steinmetz domain

equivalent Thèvenin bipole of the circuit in Figure 1.8 has been depicted. Where:

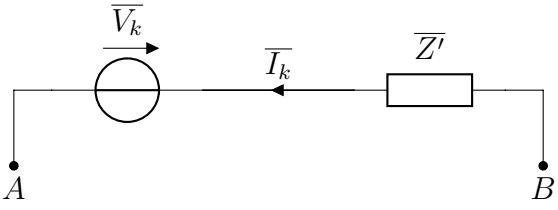


Figure 1.9: Thèvenin equivalent circuit

$$\overline{V_k} = \frac{\sum_{p=1}^{N_b} \frac{\overline{V_{kp}}}{\overline{Z}}}{\sum_{p=1}^{N_b} \frac{1}{\overline{Z}}} = \frac{1}{N} \sum_{p=1}^{N_b} \overline{V_{kp}} \tag{1.8}$$

$$\overline{Z'} = \frac{1}{\sum_{p=1}^{N_b} \frac{1}{\overline{Z}}} = \frac{\overline{Z}}{N_b} = \frac{R + j\omega L}{N_b} = R' + j\omega L' \tag{1.9}$$

That is like have a standard three-phase AR with $Z' = Z/3$, $L' = L/3$ and $R' = R/3$. It must be noticed how (1.8) provides the same equality of (1.3).

Having depicted the whole AC/DC as in Figure 1.7 makes possible use it in the same way as it would have been an inverter. Indeed, in order to keep V_{DC} constant, a three-phase set of sinusoidal voltages is computed.

By means of space vector representation, it is possible to represent the three phases quantities as vectors. Starting from (1.10), it is possible firslty get (1.11) in the Clarke's framework and then obtain (1.12) in Park's synchronous framework.

$$\frac{L}{3}\frac{\mathrm{d}i_k(t)}{\mathrm{d}t} + \frac{R}{3}i_k(t) = L'\frac{\mathrm{d}i_k(t)}{\mathrm{d}t} + R'i_k(t) = V_{gk} - v_k \tag{1.10}$$

$$L'\frac{\mathrm{d}\overline{I}^s}{\mathrm{d}t} + R'\overline{I}^s = \overline{V_g}^s - \overline{V}^s \tag{1.11}$$

$$L'\frac{\mathrm{d}\overline{I}}{\mathrm{d}t} + j\omega L'\overline{I} + R'\overline{I} = \overline{V_g} - \overline{V} \tag{1.12}$$

It is possible project (1.12) into the d and q axis, respectively real and imaginary axes of the Argand-Gauss' plane:

$$L'\frac{\mathrm{d}I_d}{\mathrm{d}t} - \omega L'I_q + R'I_d = V_{gd} - V_d \tag{1.13}$$

$$L'\frac{\mathrm{d}I_q}{\mathrm{d}t} + \omega L'I_d + R'I_q = V_{gq} - V_q \tag{1.14}$$

it must be pointed out that if the d-axis takes as reference the grid voltage space vector happens that $V_{gkq} = 0$ and therefore $|\overline{V_{gk}}| = V_{gkd}$. Introducing internal voltages u_d, and u_q.

$$u_d = L'\frac{\mathrm{d}I_d}{\mathrm{d}t} = V_{gd} + \omega L'I_q - R'I_d - V_d \tag{1.15}$$

$$u_q = L'\frac{\mathrm{d}I_q}{\mathrm{d}t} = V_{gq} - \omega L'I_d - R'I_q - V_q \tag{1.16}$$

In steady state both internal voltages are equal to zero. Neglecting voltage drop on R', it is possible to state:

$$I_d \approx \frac{V_d - V_{gd}}{\omega L'} \tag{1.17}$$

$$I_q \approx \frac{V_q - V_{gq}}{\omega L'} \tag{1.18}$$

that yields to:

$$\overline{V_g} \approx j\omega L'\overline{I} + \overline{V} \tag{1.19}$$

Complex relation (1.19) has been drawn in Figures 1.10 and 1.11 rispectivelly as vector diagram and equivalent circuit. Having defined an equivalent circuit with new

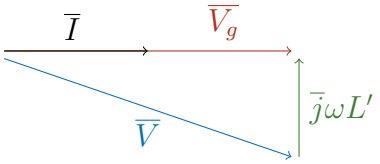


Figure 1.10: Park's framework vector diagram with unitary power factor

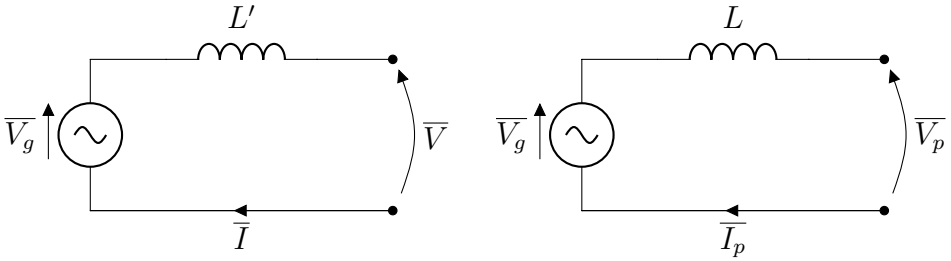


Figure 1.11: Park's framework equivalent circuits for either phases (left) and legs (right) quantities

variables (R' and L') does not provide any change on the voltage vector diagram. Moreover, writing line equations referring to each p leg (employing L, using (1.2) and setting $\overline{I_{kp}} = \overline{I_k}/3$) shows the equivalence between (1.20) and (1.19). In Figure 1.12 both voltage diagrams are depicted.

$$\overline{V_g} \approx j\omega L\overline{I_p} + \overline{V_p} = 3\frac{j\omega L'\overline{I}}{3} + \overline{V_p} = j\omega L'\overline{I} + \overline{V} \tag{1.20}$$

In order to rebalance V_{DC} voltage is necessary to drain a proper amount of grid active power. Since no reactive power is involved, it is preferable having an unitary input power factor. It is possible to demonstrate that active power P_g and reactive power Q_g are respectively proportional to I_d and I_q. Following what state above, the reference value I_q^* is set to zero. Meanwhile, I_d^* is generated with the task to provide the desired V_{DC}^*. In Figure 1.13, IAR voltage oriented control scheme is depicted. The I_d^* is computed by mean of a Proportional–Integral Controller (PI) that compensates the voltage error on the DC link. Internal voltages u_d and u_q are computed by mean of another couple of PI controllers with the task to compensate the displacements on I_d and I_q. Once u_d and u_q have been computed, (1.21) and (1.22) provide the AR front end voltage components V_d and V_q. The set of voltages V_k is ready to be used for generating the N_b modulating signals (in the current topology there are 3 modulating signals for each phase).

$$V_d = V_{gd} - u_d - R'I_d + \omega L'I_q \tag{1.21}$$

$$V_q = V_{gq} - u_q - R'I_q - \omega L'I_d \tag{1.22}$$

The system quantities used for the computation are V_{DC}, I_d, I_q, V_{gd}, and V_{gq}. Most of them are expressed in the Park's reference frame and therefore grid voltage angle θ is necessary. IAR's voltage oriented control mask depicted in Figure 1.14 have been introduced in the general scheme of Figure 1.15.

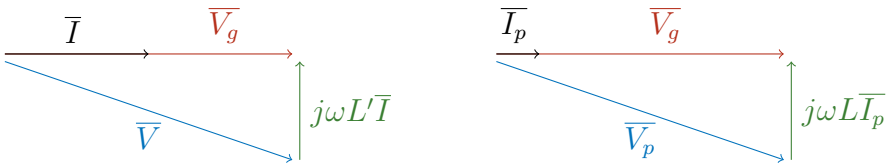


Figure 1.12: Park's framework vector diagrams for either phases (left) and legs (right) quantities

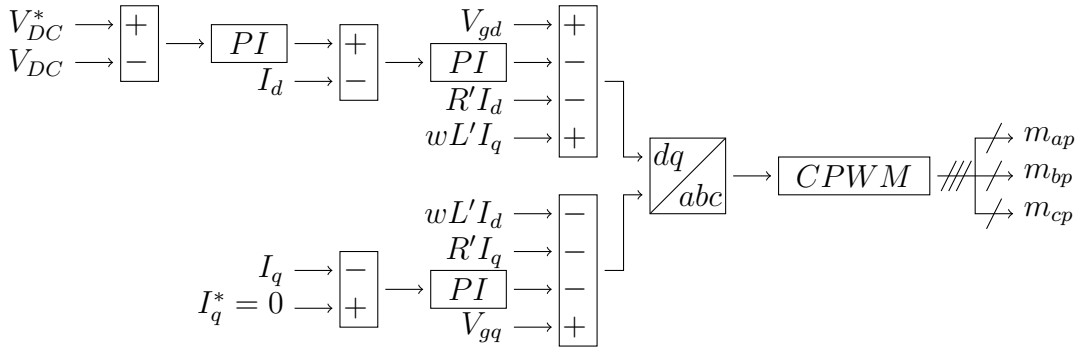


Figure 1.13: IAR voltage oriented control

Minimum DC Link Voltage Computation

In chapter 2 a control strategy able to provide V^*_{DC} is explained. However, the minimum DC bus voltage V_{DCm} depends on the grid voltage. In order to avoid the turning on of the diodes during inverter operations, it is necessary a proper value of V_{DC}. In the following, an analytical treatment is provided. In order to avoid legs' short circuits, upper and lower switches of each leg follow a complementary commutation scheme. It is then clear to notice that each upper switch of every leg can be turned on at the same time to one of the lower switches of the remaining legs without leading to short circuits. Referring to Figure 1.16, considering leg a upper switch S_1, it can be turned on when legs b or c lower switches (respectively S_5 and S_6) are turned on. In a similar way, the same criterion can be applied in the other way around considering one lower switch. The total number of not null possible commutation patterns is equal to six. Indeed, having three degrees of freedom (legs, a, b, and c) with two possible state, provides a total number of state combinations equal to $2^3 = 8$, of which two combinations are null. Are therefore necessary six systems of equations for describing the AR operations at any moment (neglecting null configurations). Moreover, it must be noticed that with the averaged method introduced above, N_b does not influence the number of possible combinations. Starting from diode turning off condition:

$$v_s \geq 0 \tag{1.23}$$

Considering commutation pattern involving S_1 and S_5 it is possible to state:

$$v_a = V_{DC} - v_{s1} \tag{1.24}$$

$$v_b = v_{s5} \tag{1.25}$$

computing the line to line pole voltage $v_{ab} = v_a - v_b$:

$$v_{ab} = V_{DC} - v_{s1} - v_{s5} \tag{1.26}$$

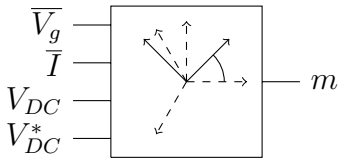


Figure 1.14: Active rectifier voltage oriented control mask

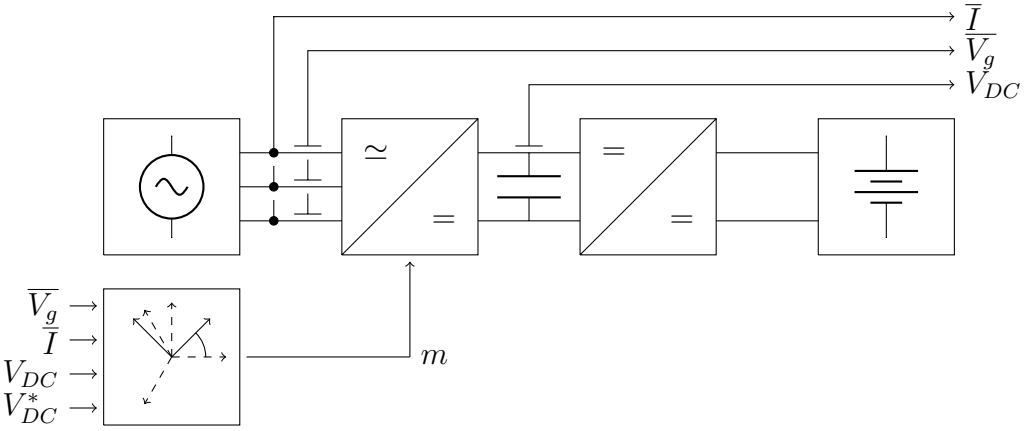


Figure 1.15: Voltage oriented control mask driving the IAR

replacing (1.26) in (1.23):

$$V_{DC} - v_{ab} = v_{s1}v_{s5} \geq 0 \tag{1.27}$$

rewriting (1.27):

$$V_{DC} \geq v_{ab} \tag{1.28}$$

in a similar way it is possible find the remaining conditions. Collecting everything together:

$$V_{DC} \geq v_{ab} \tag{1.29}$$

$$V_{DC} \geq v_{bc} \tag{1.30}$$

$$V_{DC} \geq v_{ca} \tag{1.31}$$

$$V_{DC} \leq v_{ba} \rightarrow V_{DC} \leq -v_{ab} \tag{1.32}$$

$$V_{DC} \leq v_{cb} \rightarrow V_{DC} \leq -v_{bc} \tag{1.33}$$

$$V_{DC} \leq v_{ac} \rightarrow V_{DC} \leq -v_{ca} \tag{1.34}$$

therefore, in any moment:

$$V_{DC} \geq max(|v_{ab}|, |v_{bc}|, |v_{ca}|) = 400\sqrt{2} \approx 566V \tag{1.35}$$

It must be noticed that V_{DCm} shown in Table 1.2 fully satisfy condition (1.35). Moreover, having chosen a Centered Pulse Width Modulation (CPWM) scheme, it could theoretically be possible generate sinusoidal waveform with a Root Mean Square (RMS) value of $230V$ without leading into over modulation distortion that it would have been with Sinusoidal Pulse Width Modulation (SPWM). Indeed:

$$v_{gk} = \frac{2}{\sqrt{3}}\frac{V_{DCm}}{2} = 400\sqrt{\frac{2}{3}} \approx 230V \tag{1.36}$$

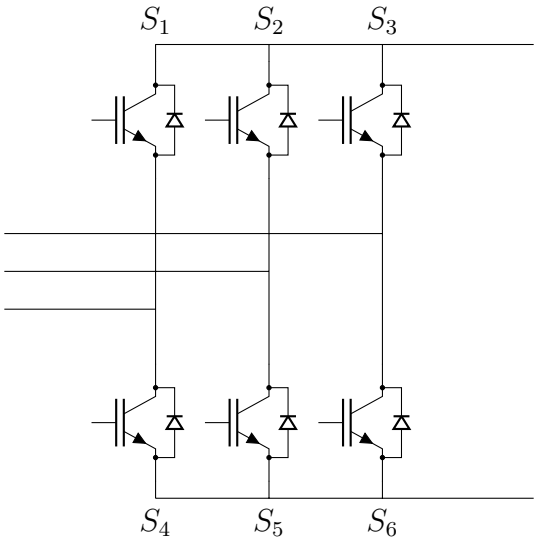


Figure 1.16: Three-phase inverter switch denomination

IAR Ripple Computation

For what it concern legs input currents ripple, it is possible compute its amplitude according to [47]:

$$\Delta i^l_{ACM} = \frac{m}{4\sqrt{3}} \frac{V_{DC}}{L f_{sw}} \tag{1.37}$$

where m is the modulating index.

From [41] it might be possible to state that a factor of about N_b reduces the total phase current ripple. Rewriting (1.37) considering the number of legs in each power block:

$$\Delta i_{ACM} \approx \frac{1}{N_b} \frac{m}{4\sqrt{3}} \frac{V_{DC}}{L f_{sw}} \tag{1.38}$$

Ripple reduction simulation introduced by IAR topology have been provided in section 4.1.

It is therefore evident that interleaving multiple legs provides an improvement on the input current ripple and can potentially bring to a reduction of the coupling reactors magnitude. From Table 1.2, it can be seen that V_{DC} ranges between $V_{DCm} = 600V$ and $V_{DCM} = 800V$. Moreover, being m inverselly proportional to the DC bus voltage, it can change during the operations according to the V_{DC} variation requested by the control strategy explained in chapter 2 [48]. Rewriting (1.37):

$$\Delta i^l_{ACM} \propto m V_{DC} \tag{1.39}$$

and being:

$$m = 2\sqrt{2} \frac{v_{gk}}{V_{DC}} \tag{1.40}$$

replacing (1.40) into (1.39):

$$\Delta i^l_{ACM} \propto 2\sqrt{2} \frac{v_{gk}}{V_{DC}} V_{DC} = 2\sqrt{2} v_{gk} \propto v_{gk} \tag{1.41}$$

it is possible to notice that the DC link voltage variation does no t directly affects Δi_{ACM}. Conversely, in chapter 2 it is possible to notice how the DC bus voltage

floatability bring relevant improvement on both IBC's inductors' and total currents. However, as shown in (1.20) and depicted in Figure 1.12, $\overline{V}$ and therefore v_{gk} depends on the current drained by the following IBC stage. Different charging profiles or State of Charge (SOC) can lead to a slightly (line parameters R and L lead to negligible voltage drops) different ripple amplitude on the AC side currents. Moreover, it is known that an active power variation meanly leads into a variation on the phase shift angle ϕ between $\overline{V}$ and $\overline{V_g}$ and a negligible variation of the $\overline{V}$ amplitude. Meanwhile, reactive power variations meanly lead to $\overline{V}$ variations. Having set $I_q^* = 0$ in section 1.1.1 leads to null steady state reactive power (steady state unitary power factor), and therefore Δi_{ACM} can be considered practically constant in any working condition. A ripple reduction is anyway introduced by the interleaving topology.

As said before, having interleaved N_b legs for each phase caused a V_{DC} pulses frequency rising of a factor N_b. It can be demonstrated that the voltage ripple on the bus DC is inversally proportional to $N_b f_{sw}$. As higher the number of power block staked together in the IAR is, as lower the voltage ripple is. A smaller capacitor voltage ripple brings to a lower Equivalent Series Resistance (ESR) energy dissipation and a longer capacitor life [30], [38].

1.1.2 Interleaved Buck Converter

The DC/DC stage take advantage of the parallelization introduced by the interleaving connection. The power is evenly shared between the N IBC's legs. As visible in Figure 1.17, proposed IBC has three power blocks having three legs each one.

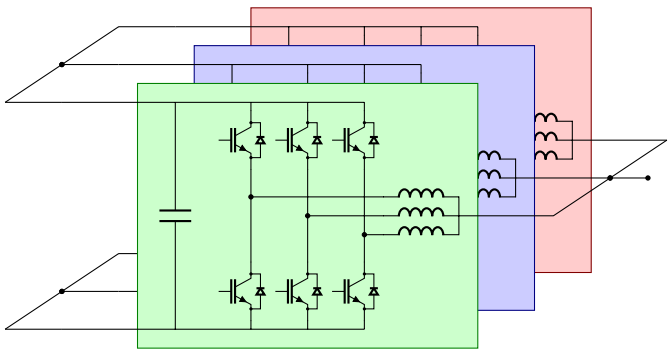


Figure 1.17: Interleaved Buck Converter

Furthermore, similarly to what emphasized in section 1.1, the usage of this configuration guarantees relevant ripple mitigation effects that are deeply discussed in the next sections [18], [31], [49].

The main task done by the IBC is to deliver at the battery the requested current or voltage. Charging procedures are carried out by means of multiple charging profiles. Each charging profile could be created by means of multiple charging methods properly scheduled. Some of the most common charging methods are:

- Constant voltage;
- constant current;
- tapper current;
- pulsed charge;

- burp charging;
- equalization charging;
- trickle charge;
- float charge;
- random charging.

and they can be carried out through multiple charging rates. Charging rates are usually classified into three main groups:

- Slow charge/Overnight;
- quick charge;
- fast charge.

Each of them has different features and may not be suitable for every batteries chemistry. Since the current proposal aims to provide fast charging rates for mainly Lithium-Ion batteries, constant voltage and current are the only methods considered in this work. However, it must be pointed out that pulse charge is getting increasing interest in the literature.

Constant Voltage (CV) and CC can be used for obtaining one of the most common charging profile, the CC-CV. It is constituted by a first charging period (bulk) where a constant current is fed inside the battery until battery voltage level reaches a cut off value. Once, the battery has reached the maximum voltage able to guarantee safe usage, the charging profiles switches from CC to CV charging method. In this last charging period where a constant voltage is provided to the battery (absorption), current decreases following a pseudo exponential profile until reaching the full charge condition. Many improvements have been introduced to previously showed charging scheme. Three-stage charging, differs from CC-CV profile, for having a further CV charging period called "floating". This new stage is able to maintain in time the full charge condition without leading to early aging and battery damages. In a similar way, four-stage charging introduces a fourth equalization stage with the task to remove chemicals products (for instance sulphation) from the battery plates surfaces, and it is mainly used for Lead-Acid chemistries.

As visible in Figure 1.18, CC bulky charging stage lasts until the battery SOC reaches a value of about 80%. The following CV stage provides the remaining 20% with times that may be comparable to the whole CC stage duration. The main task of automotive fast charging is to provide the highest quantity of charge in the shortest time possible. It is evident that (especially in a high usage scenario) the CV provides a relatively low quantity of charge in an unacceptable time. Furthermore, being the current billing politics carried out by EVSE authorities based on a "pay per charge" scheme, CV may lead to economic losses caused by a slow but time-consuming charging rate. Future politics may provide pricing tariffs made out of a mixed "charge and time" system able to encourage fast charge CC operations only.

As described in the introduction, fast charger level 4 can provide multiple hundred of kW. Being BEVs battery sizes ranging around $60/70kWh$, charging times in the tens of minutes order of magnitude are possible. It is evident that charging rates ranging from $3C$ to $6C$ (charging from 10 minutes to 20 minutes) are needed.

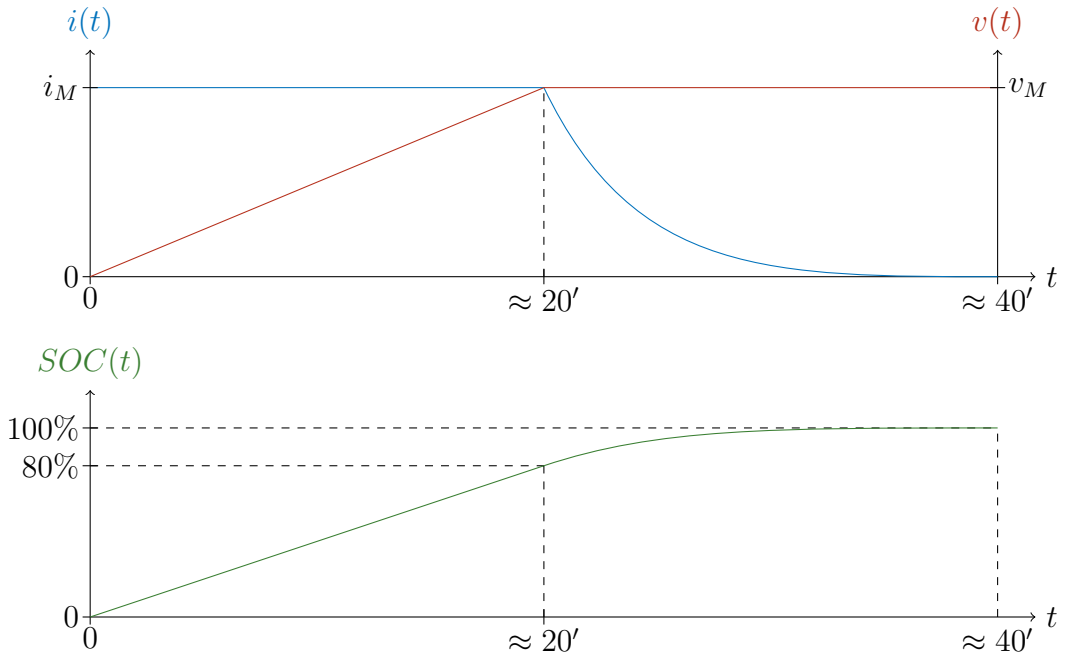


Figure 1.18: CC-CV charging profile's (level 4) voltage, current and SOC evolution

A proper control strategy is shown in chapter 3. A generic scheme showing the possible control loops with the necessary transducers is depicted in Figure 1.19. It is possible obtaining CC-CV profile either with current and voltage control loops. However, in order to have CV using a current loop is necessary in-depth knowledge of the battery model, similarly, for having CC using a voltage loop. Since charger could not know the battery status in term of SOC and State of Health (SOH), a transition from the current loop to voltage loop is usually done. In this way, a constant current can be quickly done throughout a current loop. Meanwhile, the voltage loop takes care of the constant voltage stage. Following the earlier mentioned reasons, in chapter 3 the control scheme has been implemented for a current control loop only.

In order to have an uniform power share (and therefore equal aging) among IBC's legs, it is necessary a proper current handling. Theoretically, being each leg identical to one another, the current would be evenly shared automatically. However, environmental, production, and aging conditions can lead to unbalance on legs. Unbalances could lead to an uneven current share. In order to deal with this issue, a rebalancing control system has been developed. One of the main features that the control system must have is the possibility to be easily scalable whenever a new power block is added. In chapter 3, multiple rebalancing strategy are described, and in Chapter 4 an example have been tested on one power block.

In subsection 1.2, a deep explanation of interleaved inherent ripple minimization and driving signal handling in the time domain is given. In order to further take advance of inductors size reduction in the DC/DC side, a control strategy able to provide a theoretically ripple-free condition in steady-state operations is presented in subsection 2.

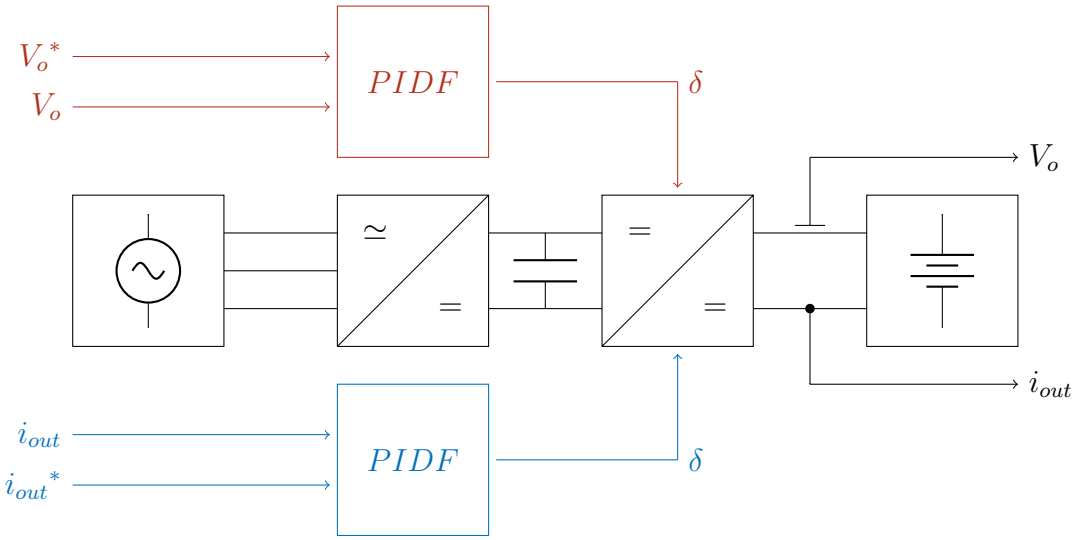


Figure 1.19: Possible voltage (red) and current (blue) control loops

1.2 IBC's Inherent Ripple Reduction

Multiple test have been done on lithium-based batteries with the target to understand the effect of high frequency components on battery aging. Chemical effects have not been fully understood. Multiple studies [50], [51] have emphasized that high frequency components does not produce appreciable battery capacity degradation. Meanwhile, low frequency components have been indicated as cause of a capacity decreasing of about 2% (especially on the early cycles). It is therefore evident that increase ripple frequency could mitigate the aging effects of this not yet fully known phenomena. However, it have also been shown that when high currents and temperatures are involved, new chemical processes might take places and provide an early battery degradation even for high frequency ripple components [52], [53].

As explained below, interleaved configurations, if properly driven, can lead to effective switching frequency increase proportional to the number of legs involved. However, ripple minimization may helps on mitigating the negative effects that an high power (high temperatures and currents involved) fast charging operations may introduce. In order to face aforementioned issues, a ripple-free strategy able to take advantage of the interleaved topology have been developed in Chapter 2. Since no battery current ripple quality constraints have been published yet, short ripple transients have been tolerated.

In section below, care have been dedicated on understanding interleaved ripple inherent minimization (and frequency multiplication) carried out by interleaved topologies. Meanwhile in Chapter 2 a general ripple cancellation strategy is introduced.

1.2.1 Current Ripple in Full Legs

Taking as a reference the full leg visible in the Figure 1.20, it can be easily seen from equation (1.42) that the inductor's voltage v_L depends on both v_p and V_o.

$$v_L = v_p - V_o \tag{1.42}$$

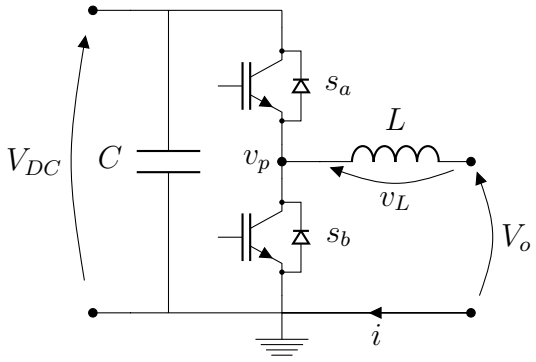


Figure 1.20: Full leg

where the pole voltage v_p can be set equal to 0 or V_{DC} and the output voltage V_o is defined as:

$$V_o = \delta V_{DC} \tag{1.43}$$

with δ known as duty cycle.

The ripple amplitude can be easily computed by means of the physical relationship (1.44) characterizing inductors. Although the following approach represents a simplification that does not take into account the resistive component of the inductor, it can be seen as a linearization of the RL exponential transient on a span comparable to the switching period t_{sw} and therefore it does not introduce any relevant error on the ripple computation [54].

$$v_L = L\frac{\mathrm{d}i(t)}{\mathrm{d}t} \tag{1.44}$$

From the theory describing the PWM technique, the current $i(t)$ flowing into the inductor can be described as the summation of two components, an average part I and a variable part $\Delta i(t)$ usually called current ripple (1.45).

$$i(t) = I + \Delta i(t) \tag{1.45}$$

The derivative of the current $i(t)$ depends on the sign of the voltage v_L. Figure 1.21 can be taken as an example. The typical sawtooth waveform is the outcome of the integration of v_L over a switching period t_{sw}. Referring to the time span ranging from 0 to δt_{sw}, where $v_p = V_{DC}$, the maximum current ripple can be easily computed with the following equation:

$$\Delta i_M = \frac{1}{2}\frac{\mathrm{d}i(t)}{\mathrm{d}t}\delta t_{sw} \tag{1.46}$$

by means of (1.42)-(1.44), equation (1.46) can be rewritten specifically showing the dependence on V_{DC}, f_{sw}, L and δ:

$$\Delta i_M = \frac{1}{2}\frac{v_L}{L}\delta t_{sw} = \frac{1}{2}\frac{V_{DC} - V_o}{L f_{sw}}\delta = \frac{1}{2}\frac{V_{DC}}{L f_{sw}}(1-\delta)\delta \tag{1.47}$$

From (1.47) it is visible how $\Delta i_M \propto (1-\delta)\delta$ and therefore for any value δ a multitude Δi_M values are expected. Furthermore, as visible in Figure 1.22, there is a geometrical symmetry for value above and below $\delta = 0.5$.

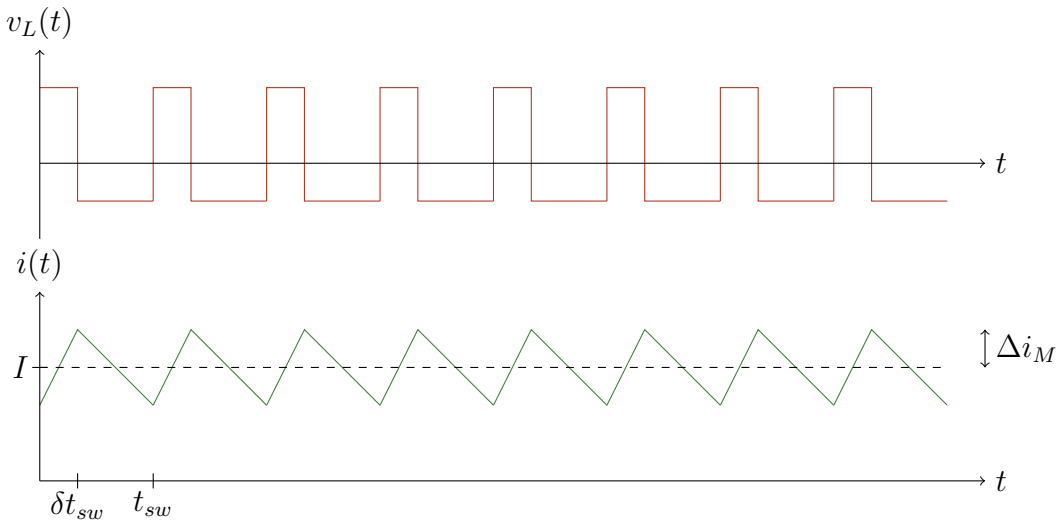


Figure 1.21: Drawing representing the ripple for $\delta = 1/3$

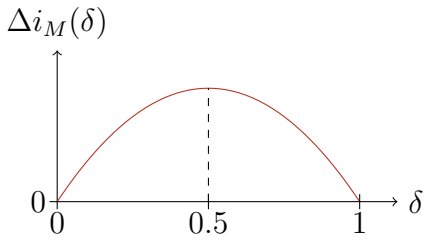


Figure 1.22: Geometrical symmetry of Δi_M among the whole δ span

1.2.2 Current Ripple in Interleaved Topologies

Interleaved topologies are built by mean of multiple full legs stacked in parallel to each other. A general case with N parallel branches has been considered (Figure 1.23).

As explained in Chapter 1, the possibility to share power among many branches by mean of proper routing of the total current through each full leg represents one of the benefits of using interleaved topologies. A further well-known advantage is the automatic ripple reduction obtained by mean of a suitable PWM carrier handling able to create a geometric total or partial compensation of the current ripple. The best choice is to evenly shift each PWM carrier by mean of a factor t_{sw}/N ($360°/N$ if considered as a phase delay). Since the total current $i(t)$ is the summation of all the branches' currents $i_k(t)$, also the output ripple $\Delta i(t)$ is the summation of all the branches' ripple currents $\Delta i_k(t)$. The previous statement can be see in (1.48)-(1.52). Figure 1.24 provides a visual representation of the aforementioned phenomena considering $\delta = 0.5$ and three branches only. Regardless from the number of parallel legs, the average output voltage V_o does not change in interleaved configurations, therefore, (1.43) is still valid.

$$i(t) = \sum_{k=1}^{N} i_k(t) \tag{1.48}$$

where each $i_k(t)$ is constituted by an average value I_k and an instantaneous ripple

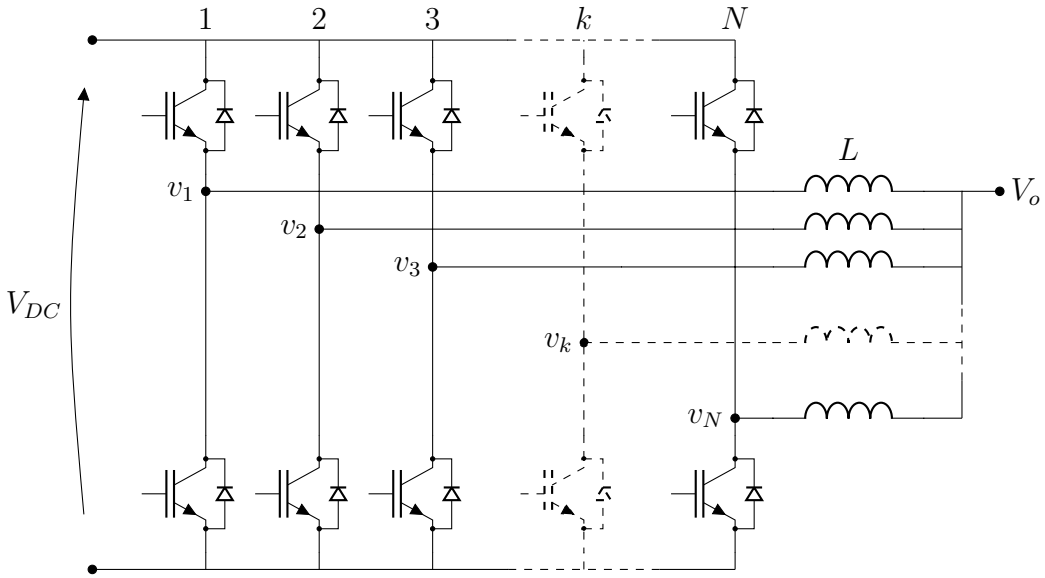


Figure 1.23: Interleaved topologies with N branches

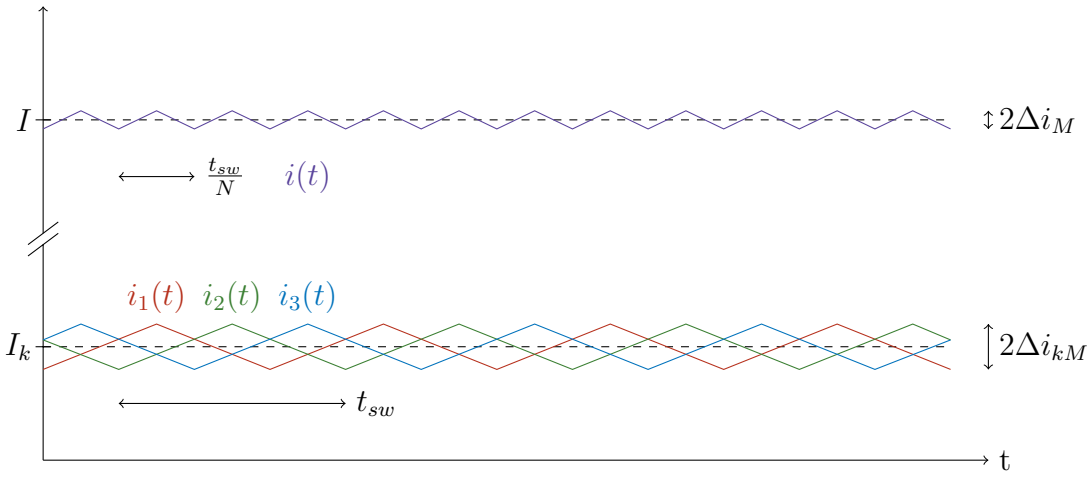


Figure 1.24: Shifted branches' currents $i_k(t)$ and total outoput current $i(t)$

component $\Delta i_k(t)$

$$i_k(t) = I_k + \Delta i_k(t) \tag{1.49}$$

and in a similar way $i(t)$:

$$i(t) = I + \Delta i(t) \tag{1.50}$$

therefore,

$$I = \sum_{k=1}^{N} I_k \tag{1.51}$$

and,

$$\Delta i(t) = \sum_{k=1}^{N} \Delta i_k(t) \tag{1.52}$$

In order to compute a formula able to describe the maximum ripple Δi_M of an interleaved connection (similar to what done in (1.47)), an equivalent circuit is necessary. Substituting each full leg by mean of an independent voltage source able to generate $v_k(t)$ and transforming the whole system on a Laplace domain (for

the sake of simplicity no energy is stored inside inductors), the following circuit is obtained:

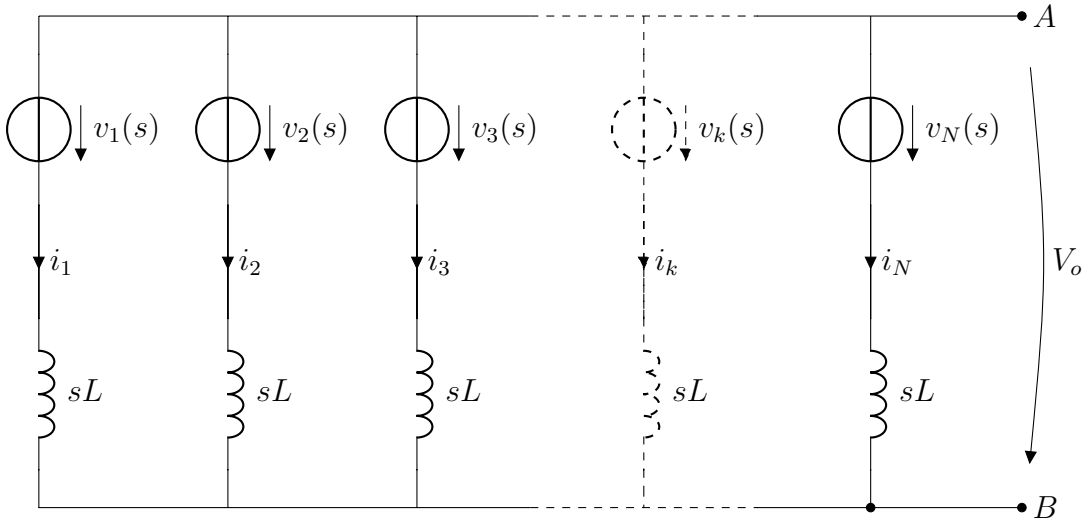


Figure 1.25: System in the Laplace domain

Thanks to Thévenin's and Millman's theorems the bi-nodal circuits can be massively simplified in a series of two elements v and Z_L.

$$v = \frac{\sum_{k=1}^{N} \frac{v_k(s)}{sL}}{\sum_{k=1}^{N} \frac{1}{sL}} = \frac{1}{N} \sum_{k=1}^{N} v_k(s) \quad \begin{matrix} \mathcal{L}^{-1} \\ \rightarrow \end{matrix} \quad v(t) = \frac{1}{N} \sum_{k=1}^{N} v_k(t) \tag{1.53}$$

$$Z_L = \frac{1}{\sum_{k=1}^{N} \frac{1}{sL}} = s\frac{L}{N} = sL' \tag{1.54}$$

Once the system have been anti-transformed back it looks like what depicted in Figure 1.26. It is worth noticing that the Thévenin's equivalent voltage (1.53) is the mean value of the instantaneous pole voltages and the equivalent impedance (1.54) is based on an inductance L' that is N times lower than L.

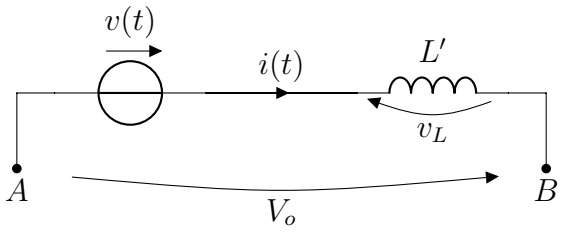


Figure 1.26: Thèvenin equivalent circuit

From the (1.43), (1.53), and knowing that each leg is fired with an even time delay of t_{sw}/N it is possible notice that the resulting v is a periodic signal of frequency Nf_{sw}. Therefore, it worth studying the system dividing the switching period t_{sw} in N time slots and introducing new conventional variables δ', L', f'_{sw} and t'_{sw}. Furthermore, since there is always a relationship between the active time t_{on} and δ (being $t_{on} = \delta t_{sw}$), it could be useful divide the duty cycle in N sectors each one identifiable by mean of a new index p. In the following subsections cases $p = 1$ (Figure 1.27), $p = 2$ (Figure 1.28), and the general case $p = p$ (Figure 1.29) are analyzed.

Case p=1, $0 \leq \delta \leq 1/N$

As visible in Figure 1.27a the active period t_{on} of a generic pole voltage v_k falls inside the first time slot. The equivalent voltage v is a rectangular wave ranging within 0 and V_{DC}/N with a period t'_{sw}, it can therefore being study with an approach similar to what done in section 1.2.1. New variables must be defined:

$$t'_{sw} = \frac{t_{sw}}{N} \quad \longleftrightarrow \quad f'_{sw} = N f_{sw} \tag{1.55}$$

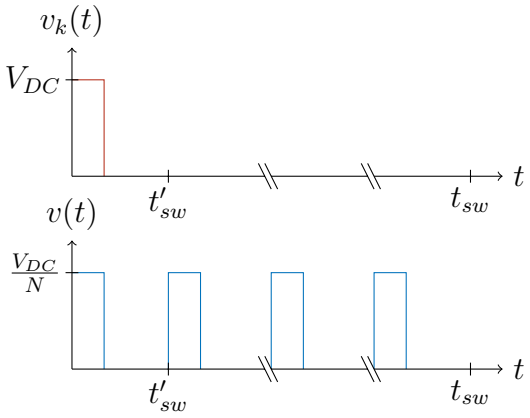
$$t'_{on} = \delta' t'_{sw} = t_{on} = \delta t_{sw} \tag{1.56}$$

and therefore:

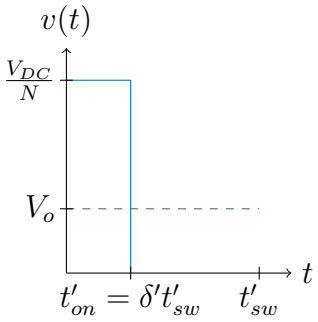
$$\delta' = \frac{t'_{on}}{t'_{sw}} = N\frac{t_{on}}{t_{sw}} = N\delta \tag{1.57}$$

$$L' = \frac{L}{N} \tag{1.58}$$

$$V_o = \frac{V_{DC}}{N}\delta' = V_{DC}\delta \tag{1.59}$$



(a) Drawing of v_k and v in the whole switching period t_{sw}



(b) Zooming on v in the whole conventional switching period t'_{sw}

Figure 1.27: Generic pole voltage v_k and equivalent voltage v for $0 \leq \delta \leq 1/N$ (sector $p = 1$)

Rewriting the (1.47) with reference to the equivalent circuit and the active period t'_{on}:

$$\Delta i_M = \frac{1}{2}\frac{\mathrm{d}i(t)}{\mathrm{d}t}\delta' t'_{sw} = \frac{1}{2}\frac{v_{L'}}{L'}\delta' t'_{sw} = \frac{1}{2}\frac{1}{L' f'_{sw}}\delta'\left(\frac{V_{DC}}{N} - V_o\right) = \frac{1}{2}\frac{V_{DC}}{L' f'_{sw}}\frac{(1-\delta')\delta'}{N} \tag{1.60}$$

It is worth noticing the direct proportionality with $(1-\delta')\delta'$ in a similar way to what previously emphasized in Figure 1.22. Substituting the new variable inside the (1.60):

$$\Delta i_M = \frac{1}{2}\frac{V_{DC}}{L f_{sw}}(1 - N\delta)\delta \tag{1.61}$$

Noticing that $(1 - N\delta) \leq (1 - \delta)$, it is already possible state that, as many legs are stacked in the converter as lower the output current ripple will be.

Case p=2, $1/N \leq \delta \leq 2/N$

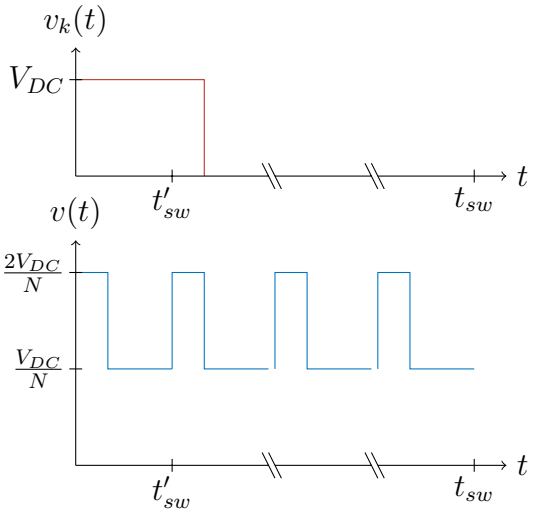
As visible in Figure 1.28a the active period t_{on} of a generic pole voltage v_k falls inside the second time slot. The equivalent voltage v is a rectangular wave ranging within V_{DC}/N and $2V_{DC}/N$ with a period t'_{sw}, it can therefore being study with an approach similar to what did in the previous case. Despite (1.55) and (1.58) are still valid, some changes are required:

$$t'_{on} = \delta' t'_{sw} = t_{on} - t'_{sw} = N\delta t'_{sw} - t'_{sw} = t'_{sw}(N\delta - 1) \tag{1.62}$$

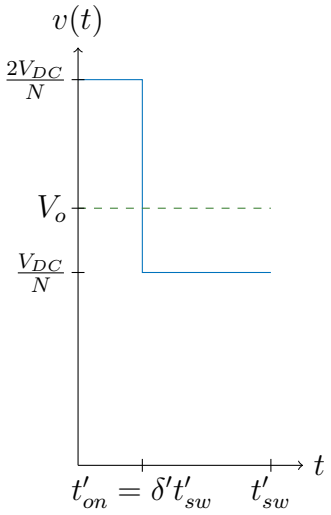
and therefore:

$$\delta' = \frac{t'_{on}}{t'_{sw}} = N(\delta - \frac{1}{N}) \tag{1.63}$$

$$V_o = \frac{V_{DC}}{N}\delta' + \frac{V_{DC}}{N} = V_{DC}(\frac{\delta'}{N} + \frac{1}{N}) = V_{DC}\delta \tag{1.64}$$



(a) Drawing of v_k and v in the whole switching period t_{sw}



(b) Zooming on v in the whole conventional switching period t'_{sw}

Figure 1.28: Generic pole voltage v_k and equivalent voltage v for $1/N \leq \delta \leq 2/N$ (sector $p = 2$)

Updating the (1.60) at the second case:

$$\Delta i_M = \frac{1}{2}\frac{1}{L' f'_{sw}}\delta'(2\frac{V_{DC}}{N} - V_o) = \frac{1}{2}\frac{1}{L' f'_{sw}}\delta'\frac{V_{DC}}{N}(2 - \delta' - 1) = \frac{1}{2}\frac{V_{DC}}{L' f'_{sw}}\frac{(1-\delta')\delta'}{N} \tag{1.65}$$

It is visible a perfect overlapping between the 1.60 and 1.65. Substituting the new variable inside the (1.65):

$$\Delta i_M = \frac{1}{2}\frac{V_{DC}}{L f_{sw}}[1 - N(\delta - \frac{1}{N})](\delta - \frac{1}{N}) \tag{1.66}$$

As expected, the 1.66 is similar to the 1.61 apart from the fact that δ have being shifted by a value $1/N$ during the passage between the first and the second case.

General case p=p, $(p-1)/N \leq \delta \leq p/N$

As visible in Figure 1.29a the active period t_{on} of a generic pole voltage v_k falls inside the generic p-th time slot. The equivalent voltage v is a rectangular wave ranging within $(p-1)V_{DC}/N$ and pV_{DC}/N with a period t'_{sw}, it can therefore being study with an approach similar to what did in the previous cases. As done before, in order to compute the general case, few changes are required:

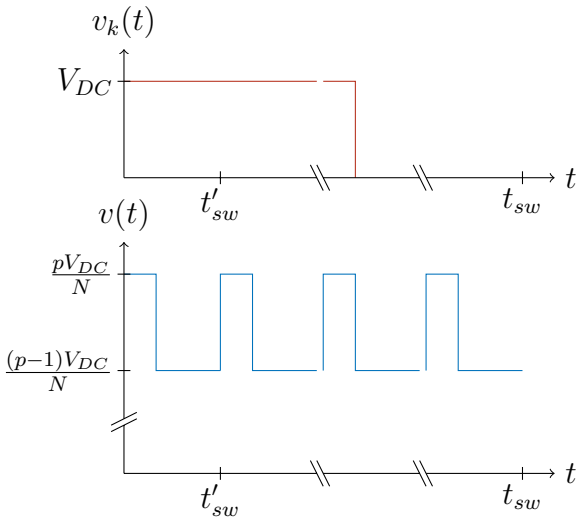
$$t'_{on} = \delta' t'_{sw} = t_{on} - (p-1)t'_{sw} = N\delta t'_{sw} - (p-1)t'_{sw} = t'_{sw}[N\delta - (p-1)] \tag{1.67}$$

and therefore:

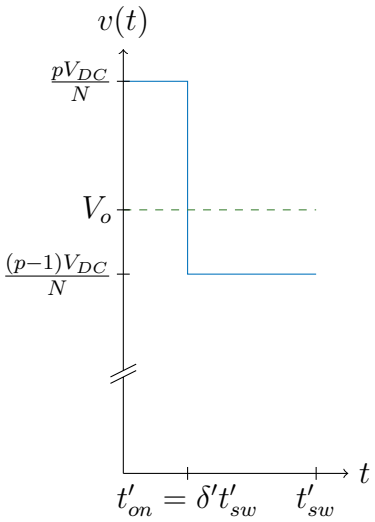
$$\delta' = \frac{t'_{on}}{t'_{sw}} = N(\delta - \frac{p-1}{N}) \tag{1.68}$$

$$V_o = \frac{V_{DC}}{N}\delta' + (p-1)\frac{V_{DC}}{N} = V_{DC}(\frac{\delta'}{N} + \frac{p-1}{N}) = V_{DC}\delta \tag{1.69}$$

Updating (1.60), and (1.65) to the general case:



(a) Drawing of v_k and v in the whole switching period t_{sw}



(b) Zooming on v in the whole conventional switching period t'_{sw}

Figure 1.29: Generic pole voltage v_k and equivalent voltage v for $(p-1)/N \leq \delta \leq p/N$ (generic sector $p = p$)

$$\Delta i_M = \frac{1}{2}\frac{1}{L' f'_{sw}}\delta'(p\frac{V_{DC}}{N} - V_o) = \frac{1}{2}\frac{V_{DC}}{L' f'_{sw}}\frac{(1-\delta')\delta'}{N} \tag{1.70}$$

Again, in the convectional reference system the general formula (1.70) perfectly matches (1.60), and (1.65). Finally, replacing the new variable inside the (1.70) the general formula (1.71) is found.

$$\Delta i_M = \frac{1}{2}\frac{V_{DC}}{L f_{sw}}[1 - N(\delta - \frac{p-1}{N})](\delta - \frac{p-1}{N}) \tag{1.71}$$

As stated in [55], [56] the current ripple is lower than what expected with a single leg and it has a repetitive simmetric parabolic behaviour among the whole δ span, the number of lobes depends on the numbers of legs N (Figure 1.30).

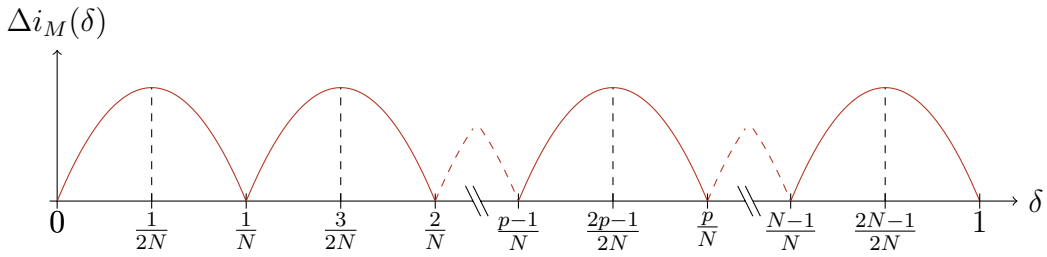


Figure 1.30: Geometrical symmetry of Δi_M among the whole δ span with a generic number N of legs

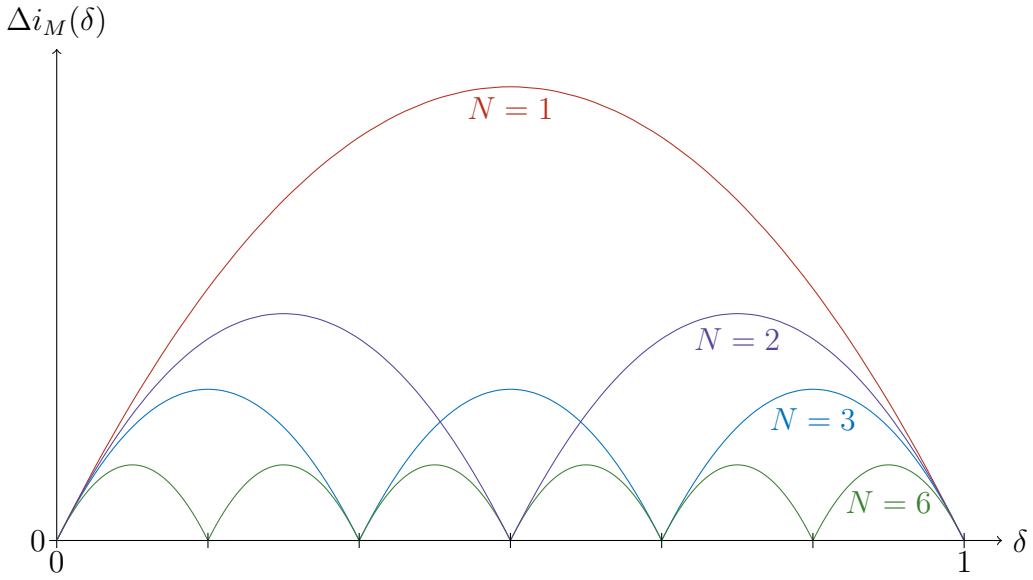


Figure 1.31: Geometrical symmetry of Δi_M among the whole δ span for $N = 1$, 2, 3, and 6

As visible in (1.70), when δ' is equal to 0.5, Δi_M reaches its maximum. Since the whole δ span is constituted by N subsectors of δ', there are always N equal global maximums and they always occur in the middle of each lobe (Figures 1.30 and 1.31). Substituting in (1.70) $\delta' = 0.5$:

$$max\Delta i_M(\delta') = \Delta i_M(0.5) = \frac{1}{8}\frac{V_{DC}}{L' f'_{sw}}\frac{1}{N} \propto \frac{1}{N} \tag{1.72}$$

In order to quantitatively estimate the effectiveness of the output ripple reduction, the ratio r is introduced (1.73). It represents the ratio between the global maximum of output and inductors current ripples. Seeing the single leg k current as the output current of an improper interleaved with $N = 1$, it is easy state that r is inversely proportional to the number of legs N.

$$r = \frac{max\Delta i_M(\delta)}{max\Delta i_{kM}(\delta)} = \frac{1}{N} \tag{1.73}$$

Referring to Figure 1.31, it worth notice that every δ/N the value of $\Delta i_M(\delta)$ is equal to zero. In other terms, the general equation (1.71) has always $N+1$ roots and they represent the following operative conditions:

$$\delta = \frac{z}{N} \tag{1.74}$$

whereas z is an integer ranging between 0 and N.

Those operative conditions could theoretically guarantee a ripple null regardless from the switching frequency and inductors magnitude. In chapter 2 an original control strategy able to guarantee a ripple null at any working point is presented.

Chapter 2

Ripple Free Strategy

As anticipated in section 1.2, high frequency ripple may lead to an early aging in battery involved in high power charging operations [52], [53]. For this purpose a ripple cancellation strategy have been developed in this chapter. It is able to take advantage of inherent ripple minimization feature that interleaved topology introduces.

2.1 Ripple Free Strategy in the Proposed Case with 9 Legs

As visible in Figure 1.31 and cited in subsection 1.2.2, working points able to nullify $\Delta i_M(\delta)$ are available. Equation (1.71) has always $N+1$ roots and they represent the operative conditions visible in (1.74). Those working points could theoretically guarantee a ripple null regardless of the switching frequency and inductors magnitude.

Equation (1.43) (rewritten in 2.1), is depicted in Figure 2.1. Meanwhile, in Figure 2.2 "no ripple" working points for the current case ($N = 9$) are highlighted.

$$V_o = \delta V_{DC} \tag{2.1}$$

In Figure 2.3, working points locus shown in equation 2.1 are depicted. Moreover, it is visible that design parameters shown in Table 1.2 limit the suitable working area between $V_{DC} = [600; 800V]$ and $V_o = [200; 800]V$. It is therefore immediate see how not all the available discrete duty cycles are suitable. Since the maximum value of the DC link V_{DCM} is $800V$ and the minimum expected output value V_{om} is $200V$ the smallest duty cycle δ_m is:

$$\delta_m = \frac{V_{om}}{V_{DCM}} = 0.25 \rightarrow 25\% \tag{2.2}$$

Meanwhile the maximum duty cycle is $\delta_M = 1$ when $V_o = V_{oM} = 800V$ and $V_{DC} = V_{DCM} = 800V$.

In the proposed DC/DC topology the number of legs N is equal to nine. Recalling the theory explained in part 1.2.2, the maximum ripple in the output current is N times lower than the single maximum ripple in each leg, indeed $r = 1/9$.

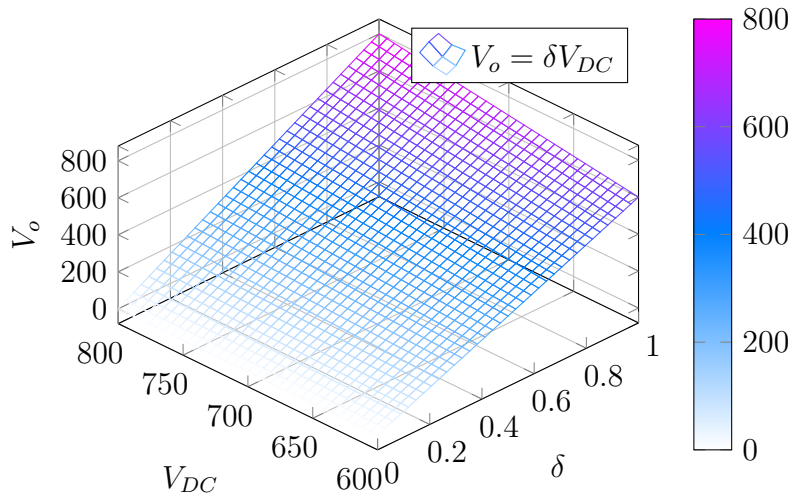


Figure 2.1: V_o as a function of δ and V_{DC}

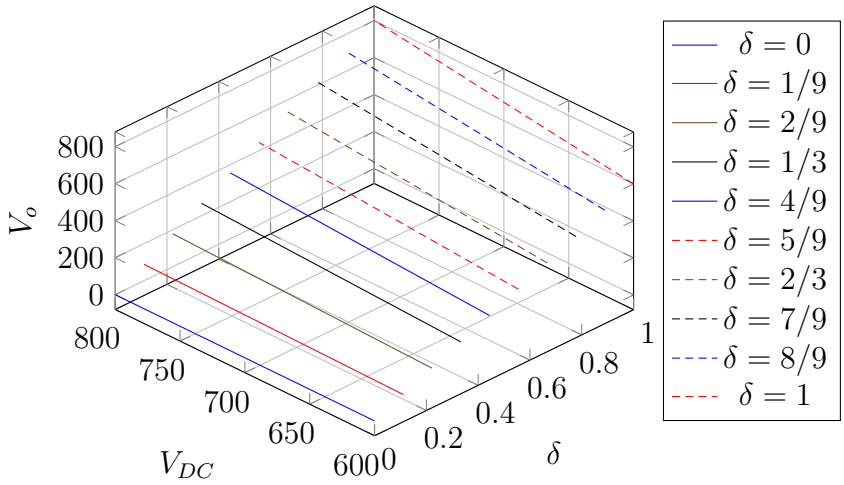


Figure 2.2: V_o as a function of "no-ripple" discrete δ and V_{DC}

The possible discrete duty cycles are the one able to fulfill the (1.74), considering over mentioned boundary conditions:

$$\delta_m \leq \frac{z}{N} \leq \delta_M \tag{2.3}$$

therefore the integer z spans between 3 and 9.

2.1.1 DC Link Voltage Variation Range

In previous paragraphs, V_{DC} range has been taken as given. However, it is not a freely settable parameter, it depends on the previous AC/DC stage capability, on the desired output voltage and the number of legs. As described in section 1.1.1, the interleaved active rectifier is tied up to the low voltage grid, and it is driven maximizing the DC BUS utilization using Interleaved Centered Pulse Width Modulation (ICPWM) (also known has Interleaved Space Vector Pulse Width Modulation (ISVPWM)) scheme. Analyzing the AC/DC stage with a positive power flow (G2V operations) it can be seen as a boost converter, and therefore the minimum DC voltage value cannot be lower than the double of the maximum value in the AC side

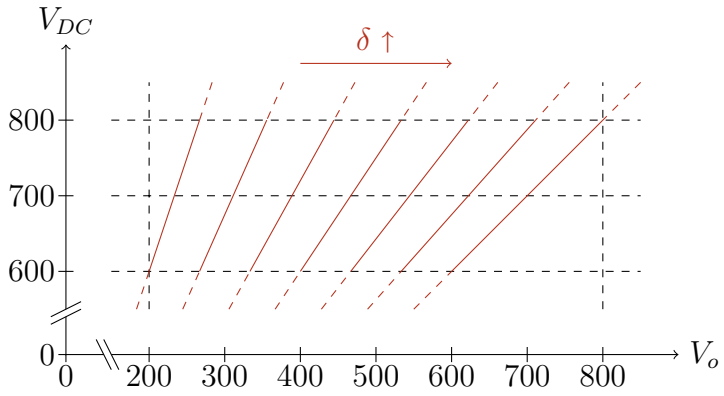


Figure 2.3: Projection of (2.1) on the plane $V_o \times V_{DC}$ with reference to the studied case

(V_{DCm} calculation discussed more in detail in part 1.1.1). Being each phase connected to the industrial voltage level (as visible in Table 1.2, European distribution grid has been considered) the line to line voltage V_g is set as $400V$. The maximum phase to ground voltage is then:

$$V_{kM} = V_g \frac{\sqrt{2}}{\sqrt{3}} \approx 327V \tag{2.4}$$

taking into account the improvement of about 15% on DC link utilization garantee by the modulation scheme. The V_{DCm} must be:

$$V_{DCm} \geq 2\frac{V_{kM}}{\frac{2}{\sqrt{3}}} = 400\sqrt{2} \approx 566V \tag{2.5}$$

as visible the chosen value $V_{DCm} = 600V$ fully respects the condition (2.5).

As can be seen in Figure 2.3, for every duty cycle δ a range of working points can be found. They are limited between a minimum value when $V_{DC} = V_{DCm}$ and a maximum value when $V_{DC} = V_{DCM}$.

Speaking about V_{DCM}, it is undoubtedly true that being $\delta = 1$ the maximum value and having set $V_{oM} = 800V$ it should be at least equal to $800V$. However, this assumption is not enough. Since δ can not freely vary, it is necessary a V_{DCM} able to guarantee a continuous range of V_o without "holes" in the dynamics. For instance, being $N = 9$, if V_{DCM} had been set equal to $750V$, it would have created a discontinuity regardless on the value of V_{oM}.

Indeed, setting $\delta = 1/3$ (minimum possible value) it would create as maximum output value:

$$V_o = 750\frac{1}{3} = 250V \tag{2.6}$$

meanwhile by setting $\delta = 4/9$ (immediately following value) it would create as minimum output value:

$$V_o = 600\frac{4}{9} \approx 267V \tag{2.7}$$

creating then a disctinuity rapresented by an hole in the V_o dynamics in the range $[250; 267]V$ (Figure 2.4).

To avoid this issue, the highest possible value (when $V_{DC} = V_{DCM}$) of each discrete duty cycle must be at least equal to the lowest possible value (when $V_{DC} =$

V_{DCm}) of the following discrete duty cycle. Nevertheless, being the slope of each line in Figure 2.3 decreasing as bigger δ becomes, this condition must be applied only for the first suitable couple of duty cycles. Satisfy this condition for the lowest suitable couple of discrete duty cycles guarantees no V_o discontinuity for the remaining couples. In the current case:

$$V_{DCM}\frac{1}{3} \geq V_{DCm}\frac{4}{9} \tag{2.8}$$

From (2.8), V_{DCM} can be easily seen as:

$$V_{DCM} \geq V_{DCm}\frac{4}{3} = 600\frac{4}{3} = 800V \tag{2.9}$$

and as visible in Table 1.2 the condition (2.9) is respected.

As demonstrated above, V_{DCM} is not known a priori, it is therefore necessary rewrite (2.2). The minimum suitable duty cycle for the studied system δ_m is described by (2.10)[1]. Generally speaking the minimum admissible duty cycle is 1/9 and can be easily found by replacing in (2.10) the minimum admissible $V_{om} = 600/9$. In part 2.2 a generalization of (2.10) is provided.

$$\delta_m = \frac{\left\lfloor 9\frac{V_{om}}{V_{DCm}} \right\rfloor}{9} = \frac{1}{3} \tag{2.10}$$

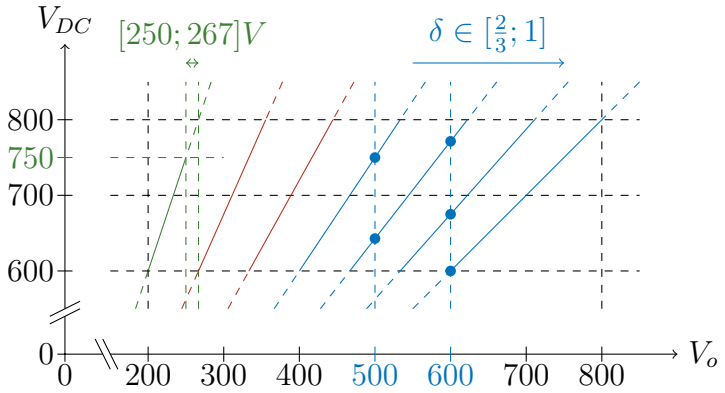


Figure 2.4: Highlighting of the V_o discontinuity in $[250; 267]V$ (green) and multiple availiable working points for $V_o = 500V$ and $V_o = 600V$ (Blue)

2.1.2 Legs Ripple Minimization Criterion

From (1.43), to span the whole V_o range with a set of discrete duty cycles, an AC/DC is needed. It must be able to vary the DC voltage level appropriately. In other words, the continuous output voltage span is made possible by a continuous variation of the DC BUS rather than a continuous variation of the duty cycle. However, it can happen that (2.1) has multiple solutions. It is then necessary to define a criterion that permits to choose the proper couple of values $[V_{DC}; V_o]$. As visible in Figure 2.4, there are multiple cases with two or even three possible solutions. The following

[1] $\lfloor x \rfloor$ represents the *floor* function

inequality able to compute what duty cycles are suitable for generating a certain output voltage V_o in a given range of V_{DC} is obtained by reverting (2.1).

$$V_{DCm} \leq \frac{V_o}{\delta} \leq V_{DCM} \tag{2.11}$$

and therefore:

$$\frac{V_o}{V_{DCM}} \leq \delta \leq \frac{V_o}{V_{DCm}} \tag{2.12}$$

For instance, replacing in (2.12) $V_o = 500V$ and $V_o = 600V$ it can been seen that δ could be either 2/3 and 7/9 or either 7/9, 8/9, and 1 respectively.

Since one of the most desirable features of power converters is having the lowest possible current ripple, the operating condition able to better guarantee this statement should be preferred. Output current ripple Δi is already minimized (theoretically totally called off) by using discrete duty cycles. However, leg's current ripple Δi_k dose not take advantage of interleaving connections.

Replacing (1.43) inside (1.46) gets:

$$\Delta i_{kM} = \frac{1}{2}\frac{V_{DC}}{Lf_{sw}}(1-\delta)\delta = \frac{1}{2}\frac{V_o}{Lf_{sw}}(1-\delta) \propto 1-\delta \tag{2.13}$$

or alternatively:

$$\Delta i_{kM} = \frac{1}{2}\frac{V_{DC}}{Lf_{sw}}(1-\delta)\delta = \frac{1}{2}\frac{V_o}{Lf_{sw}}(1-\frac{V_o}{V_{DC}}) \propto 1-\frac{V_o}{V_{DC}} \tag{2.14}$$

Both equations (2.13) and (2.14) state that for a given value of V_o having a lower DC bus voltage V_{DC} and a greater δ provide an improvement on leg's current ripples. The same finding can be graphically seen in Figure 2.5.

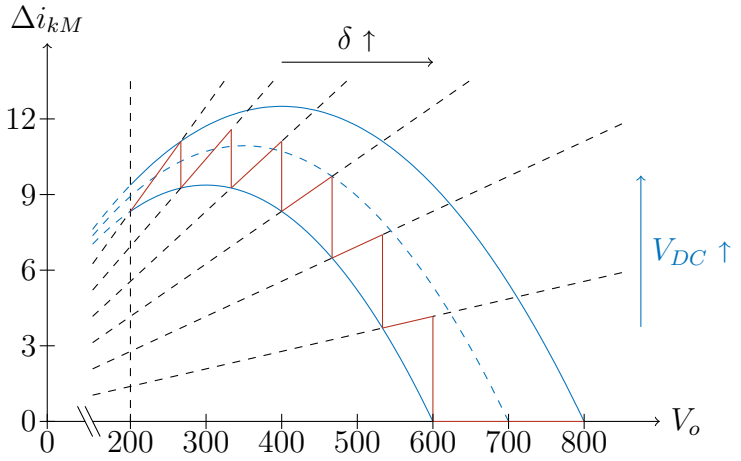


Figure 2.5: Visualization of inductor' ripple when ripple free strategy is applied

From Figure 2.5 it is worth noticing that having introduced a variable DC link voltage brings to a reduction on inductor's current ripple. As said above, although global ripple performance is improved, interleaving topology does not improve the ripple performance in each leg. This enhancement is solely ascribable to the introduction of the ripple-free strategy that permits to avoid always using the maximum

voltage V_{DCM} in the DC BUS. Furthermore, it can be notice that the maximum ripple does not necessarily occurs when V_{DCM} is selected but when (2.13) and (2.14) are maximized. In the next section 2.2 an analytical analysis of the maximum ripple is provided.

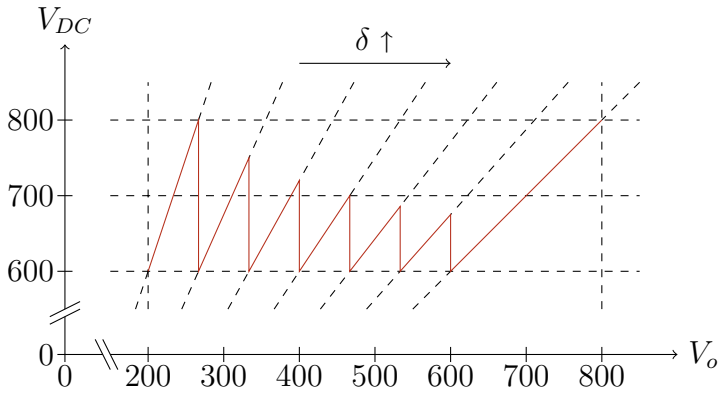


Figure 2.6: Visualization of ripple free strategy applied to the studied case

Paths visible in both Figures 2.5 and 2.6 follows what stated above. This path can be shown as a lookup table. Values V_o and δ are respectively, the input and the output of Table 2.1. DC link voltage V_{DC} is a continuous quantity depending on the wanted V_o value and the discrete δ (as visible in (2.15)). It is considered as a parameter rather than an output, and therefore it has not been inserted inside Table 2.1.

$$V_{DC} = \frac{V_o}{\delta} \tag{2.15}$$

Table 2.1: Ripple free alghorithm lookup table

Input	Output
V_o	δ
$V_{DCm} \leq V_o \leq V_{DCM}$	$\delta = 1$
$\frac{8}{9}V_{DCm} \leq V_o \leq V_{DCm}$	$\delta = \frac{8}{9}$
$\frac{7}{9}V_{DCm} \leq V_o \leq \frac{8}{9}V_{DCm}$	$\delta = \frac{7}{9}$
$\frac{6}{9}V_{DCm} \leq V_o \leq \frac{7}{9}V_{DCm}$	$\delta = \frac{2}{3}$
$\frac{5}{9}V_{DCm} \leq V_o \leq \frac{6}{9}V_{DCm}$	$\delta = \frac{5}{9}$
$\frac{4}{9}V_{DCm} \leq V_o \leq \frac{6}{9}V_{DCm}$	$\delta = \frac{4}{9}$
$\frac{3}{9}V_{DCm} \leq V_o \leq \frac{4}{9}V_{DCm}$	$\delta = \frac{1}{3}$

Table 2.1 represents a rigid and ideal algorithm that does not take into account the unavoidable transient that the BUS DC does on changing values. Figure 2.6 represent the steady-state set of ripple-free working points. In the next part, transient evaluations and consideration are performed.

2.1.3 DC Link Voltage Transients

Voltage V_{DC} can not have step variations, therefore every time that a change on the DC link voltage is required a transient outside ripple-free conditions occurs. In the following part, two types of variation are analyzed.

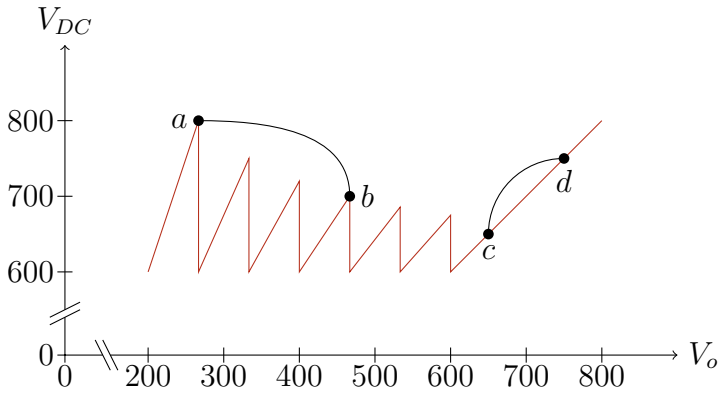


Figure 2.7: Possible type of V_{DC} variation

The first kind of variation happens when a change in V_{DC} does not require a reselection of δ. This condition is equivalent to state that the newer working point remains over one of the diagonal pieces of path visible in Figure 2.6. Moreover, it corresponds to remaining in the same row of the lookup Table 2.1. For instance the variation from point c to point d drawn in Figure 2.7.

The second typology requires a variation of both V_{DC} and δ. This variation occurs when the change on the V_o reference value is big enough for causing a crossing of at least one discontinuity zone in the path of Figure 2.6. Conversely to the previous case, this variation requires a change of row in Table 2.1. For instance the variation from point a to point b draw in Figure 2.7. As visible in Figure 2.8, δ reselection occurs.

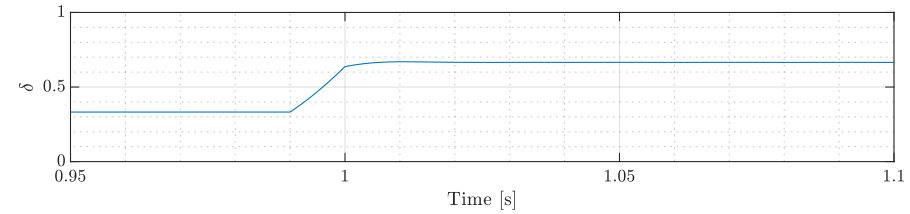
In both cases, during the transient δ loses its discrete status, and therefore the geometrical compensation of the output current ripple is missed. The new δ is expected to range around ripple-free areas taking advantage of the inherent ripple reduction capability discussed in section 1.2. An estimation of the ripple degradation during transients can be found in section 2.2.

2.2 Ripple Free Strategy in a General Case with N Legs

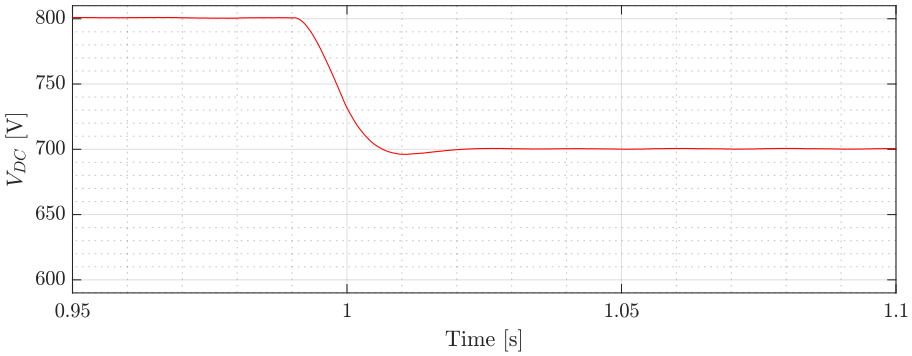
As shown in 1.2.2, as more parallel legs are staked in the converter as more effective the ripple reduction and the zero ripple points availability are. It worth study the previously shown approach in a general case with N legs.

Firstly, the number of possible discrete duty cycles is $N + 1$ of which the first one ($\delta = 0$) is always unsuitable. Without a ripple-free strategy, the maximum Δi_M would be N times smaller than the maximum ripple in each inductor.

It is immediate to verify that the the range of admissible output voltage is



(a) Evolution in time of δ



(b) Evolution in time of V_{DC}

Figure 2.8: Working point transient from point a to b depicted in Figure 2.7

provided by (2.16). Its minimum occurs when discrete δ is $1/N$ and $V_{DCm} = V_{om}N$.

$$V_{om} \geq \frac{V_{DCm}}{N} \tag{2.16}$$

Moreover, it is possible notice that as great the number of legs is, as lower V_{om} is. Having an high value of N makes the chooper more ductile.

However, δ_m might be different from $1/N$. Indeed, once V_{om} has been set, δ_m can be easily computed with equation:

$$\delta_m = \frac{\left\lfloor N \frac{V_{om}}{V_{DCm}} \right\rfloor}{N} \tag{2.17}$$

As shown above V_{DCM}, rapresents a key value for either obtaining V_{oM} and a continuos span of V_o. Equation (2.19) is a generalization of (2.9), it is able to define V_{DCM} regardlees on the value of V_{DCm} and N. Since:

$$V_{DCM}\delta_m \geq V_{DCm}(\delta_m + \frac{1}{N}) \tag{2.18}$$

V_{DCM} becomes:

$$V_{DCM} \geq \frac{V_{DCm}}{\delta_m}(\delta_m + \frac{1}{N}) = V_{DCm}(1 + \frac{1}{N\delta_m}) \tag{2.19}$$

Furthermore, defining ΔV_{DC} as the difference between V_{DCM} and V_{DCm}:

$$\Delta V_{DC} = V_{DCM} - V_{DCm} \geq V_{DCm}(1 + \frac{1}{N\delta_m}) - V_{DCm} = \frac{V_{DCm}}{N\delta_m} \tag{2.20}$$

As bigger N is, as lower the floating capability of V_{DC} necessary for correct usage of the ripple-free strategy is.

For what it concerns the maximum inductors' current ripple, it is possible to compute it once the number of legs N and the V_{DCm} have been defined. Diagonal dashed lines in Figure 2.5 are a visual rappresentation of (2.13). As visible in Table 2.1, for a given output duty cycle δ ($0 \leq \delta \leq 1$) the maximum value of the lookup table input V_o admissible is always equal to:

$$V_{oM}(\delta) = (\delta + \frac{1}{N})V_{DCm} \tag{2.21}$$

As visible in Figure 2.5 the maximum value of ΔI_{kM} for each discrete δ happens when V_o reaches the maximum admissible value before changing δ. Following what state above, replacing (2.21) inside (2.13) it is possible obtaining the general expression (2.22) able to provide ΔI_{kM} at any δ.

$$\Delta i_{kM} = \frac{1}{2}\frac{V_o}{Lf_{sw}}(1-\delta) = \frac{1}{2}\frac{V_{DCm}}{Lf_{sw}}(1-\delta)(\delta + \frac{1}{N}) \propto (1-\delta)(\delta + \frac{1}{N}) \tag{2.22}$$

computing the derivative of (2.22) it is possible finding the condition for having the global maximum of Δi_{kM}.

$$\frac{\mathrm{d}}{\mathrm{d}\delta}[(1-\delta)(\delta + \frac{1}{N})] = -2\delta - \frac{1}{N} + 1 \tag{2.23}$$

that has as roots:

$$-2\delta - \frac{1}{N} + 1 = 0 \rightarrow \delta = \frac{1}{2}(1 - \frac{1}{N}) \tag{2.24}$$

As draw in Figure 2.5, replacing in (2.24), $N = 9$ it gives that the global maximum of Δi_{kM} happens when $\delta = 4/9$ (second diagonal dashed line starting from left).

Replacing (2.24) in (2.22):

$$\Delta i_{kM} = \frac{1}{2}\frac{V_{DCm}}{Lf_{sw}}(1-\delta)(\delta + \frac{1}{N}) = \frac{1}{8}\frac{V_{DCm}}{Lf_{sw}}(1 + \frac{1}{N})^2 \tag{2.25}$$

Regardlees on the number of availiable legs, output ripple free strategy provides always a leg's ripple improvement.

2.2.1 General Algorithm

In order to provide a general algorithm suitable for any N it is not possible to use a lookup table. In the following, a range of equations provides all the relations necessary for obtaining the ripple-free strategy in closed form. Since, either reference or actual quantities have been used, the following equations can also work during transients.

$$V_{DC}^* = {V_o}^* \frac{N}{\left\lfloor \frac{N{V_o}^*}{V_{DCm}} \right\rfloor} \qquad if\ {V_o}^* \leq V_{DCm} \tag{2.26}$$

$$V_{DC}^* = {V_o}^* \qquad if\ {V_o}^* > V_{DCm} \tag{2.27}$$

The generalized procedure for computing the reference DC link voltage ${V_{DC}}^*$ once the wanted output voltage ${V_o}^*$ is defined, is shown in equations (2.26) and (2.27).

The active input rectifier adjusts the actual value V_{DC} accordingly (Figure 2.14). Going from V_{DC} to ${V_{DC}}^*$ involves a transient.

$$\delta = \frac{{V_o}^*}{V_{DC}} \tag{2.28}$$

From (2.28), δ is set considering the actual value of V_{DC} in order to always ensure ${V_o}^* \approx V_o$. As soon as ${V_{DC}}^*$ reaches V_{DC} (${V_{DC}}^* \approx V_{DC}$) the computed δ become one of the possible discrete values z/N. It is therefore obvious notice that equations (2.26)-(2.28) are able to guarantee a ripple free output current in steady state conditions. In normal operative conditions these transients are several order of magnitude lower than the charging time and the ripple degradation effects introduced is therefore acceptable. It can be seen that setting $N = 9$ and V_{DCm} as shown in Table 1.2, generate steady state δ visible in Table 2.1 and reference V_{DC} of (2.15).

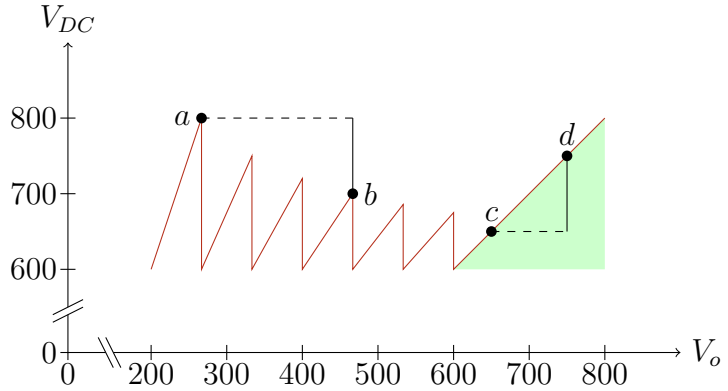


Figure 2.9: Theoretical sudden working point variation for the proposed IBC. Over-modulation area marked in green

Moreover, it must be noticed that being the actual V_o defined as δV_{DC}, (2.26)-(2.28) are theoretically able to always guarantee that $V_o = V_o^*$. Assuming to have a positive sudden change (ideally a positive step) on V_o^*, it would lead to an ideally immediate horizontal transition toward the value V_o^* (in Figure 2.9 showed as a dashed path). Furthermore, a vertical transition toward V_{DC}^*, lasting for the whole transient time completes the working point variation. However, Ripple Free strategy might not be able track all the possible working point variations. Indeed, when it comes to work with values V_o^* greater than the actual value V_{DC}, δ saturates to its maximum value and the variation cannot be accurately tracked anymore. Equation (2.29) well explains the phenomena depicted in Figure 2.9.

$$\delta = \frac{{V_o}^*}{V_{DC}} > 1 \; if \; {V_o}^* > V_{DC} \tag{2.29}$$

moreover, any sudden positive variation having has steady state value $\delta = 1$ leads to a distortion. In other words, every transient that needs to enter in the area highlighted in green (Figure 2.9) can not be generated because it requires $\delta > 1$. When it comes to work in this piece of path, working point variations must be continues and slow enough do not lead into an appreciable over-modulation. This is the only case where (2.26)-(2.28) cannot ensure that $V_o = V_o^*$.

2.2.2 Transients Maximum Output Current Ripple

As explained below, whenever δ falls outside the ripple free condition, it means that transients are occurring. As visible in Figure 1.31, even in the worst case (the medium point between discrete duty cycles) the output ripple is still N times lower then what expected without interleaved topology.

As visible in Figure 1.30 the δ's displacement effect repeats periodically and symmetrically around each point p/N. Whit (2.30)[2] is possible asses the magnitude of this variation.

$$\Delta\delta = |\delta - \frac{\lfloor N\delta \rceil}{N}| \tag{2.30}$$

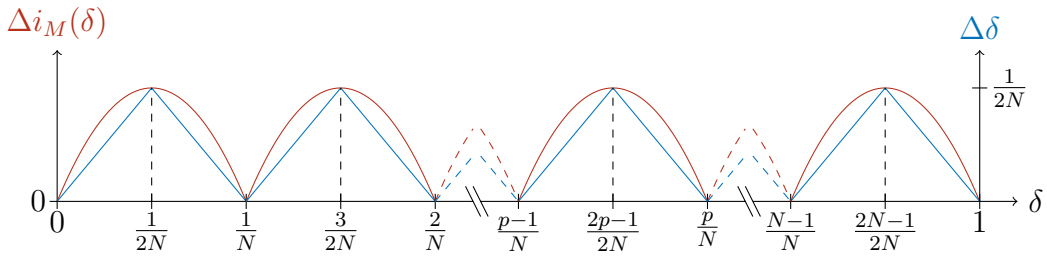


Figure 2.10: Geometrical symmetry of Δi_M and $\Delta\delta$ among the whole δ span with a generic number N of legs

In Figure 2.10 it can be seen that the maximum $\Delta\delta$ is:

$$\Delta\delta_M = \frac{1}{2N} \tag{2.31}$$

Taking advantage of the aforementioned periodicity $\Delta\delta_M$ can be easily related to the conventional duty cycle introduced in Section 1.2.2. Replacing (2.31) into (1.57) shows that the maximum δ's displacement expressed in the conventional framework is 0.5.

$$\Delta\delta'_M = N\Delta\delta_M = \frac{1}{2} \tag{2.32}$$

Moreover, replacing (2.32) into (1.60) provides the same relation found in (1.72).

$$max\Delta i_M = \frac{1}{8}\frac{V_{DC}}{L'f'_{sw}}\frac{1}{N} = \frac{1}{8}\frac{V_{DC}}{Lf_{sw}}\frac{1}{N} \tag{2.33}$$

The general case drawn in Figure 2.11 can be seen in:

$$\Delta i_M = \frac{1}{2}\frac{V_{DC}}{Lf_{sw}}\frac{(1-\Delta\delta'_M)\Delta\delta'_M}{N} \tag{2.34}$$

As soon as the transient expires the ripple-free condition restores. As visible in Figure 2.12 transients can last typically for times ranging around tenth of second, that is multiple orders of magnitude smaller than the fastest charging profile.

[2] $\lfloor x \rceil$ represents the *round* function

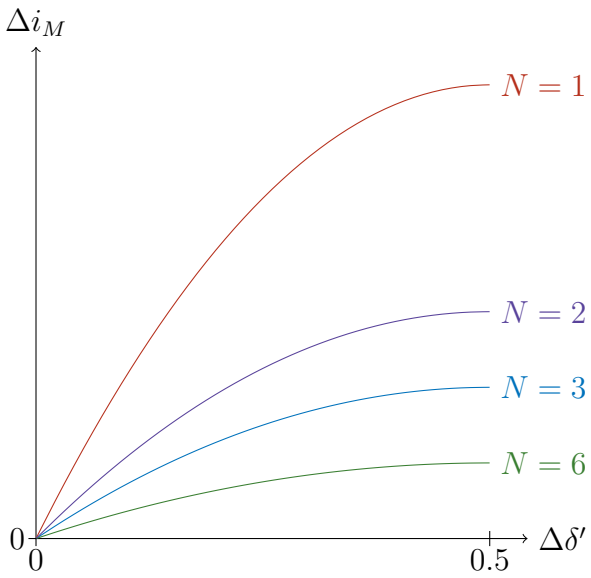
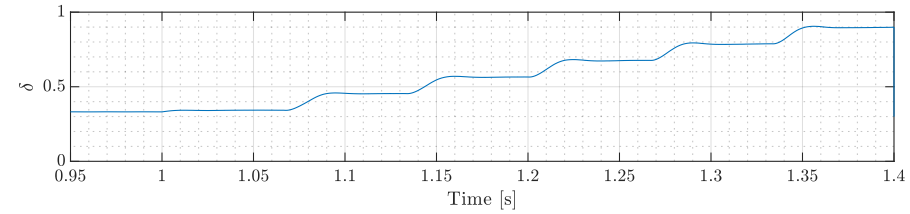


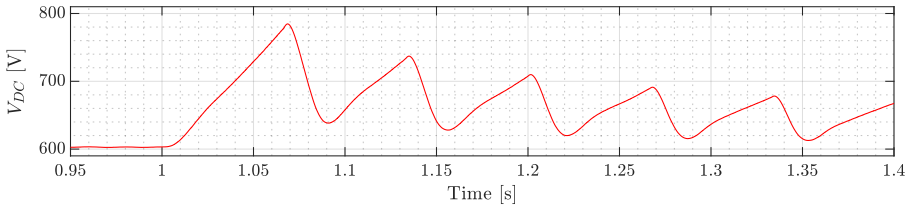
Figure 2.11: Maximum total output ripple Δi_M as a function of $\Delta\delta'$ for $N = 1$, 2, 3, and 6

Although negative ripple effects on batteries are known [50]–[53], no design requirements are already available in the literature. No tests on the aging introduced by high frequency components is yet demanded. For this reason, a steady-state only approach has been chosen.

The ripple free strategy explained in this section is carried out troughtout a control block called *"ripple free mask"* (Figure 2.13). Outer output loop controllers (for instance, voltage and current output loops) do not need to know what the actual values of V_{DC} and δ are, as soon as they are robust enough. In chapter 3, V_o^* is generated using an outer output current loop. This mask represents an interface layer between controllers and power blocks. The reference DC BUS voltage will be forwarded to the input active rectifier. Meanwhile, output IBC is driven using the computed δ (Figure 2.14).



(a) Evolution in time of δ



(b) Evolution in time of V_{DC}

Figure 2.12: Working point transient on a V_o ramp from 200 to 600V

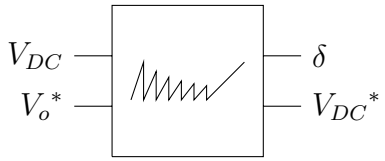


Figure 2.13: Ripple free mask

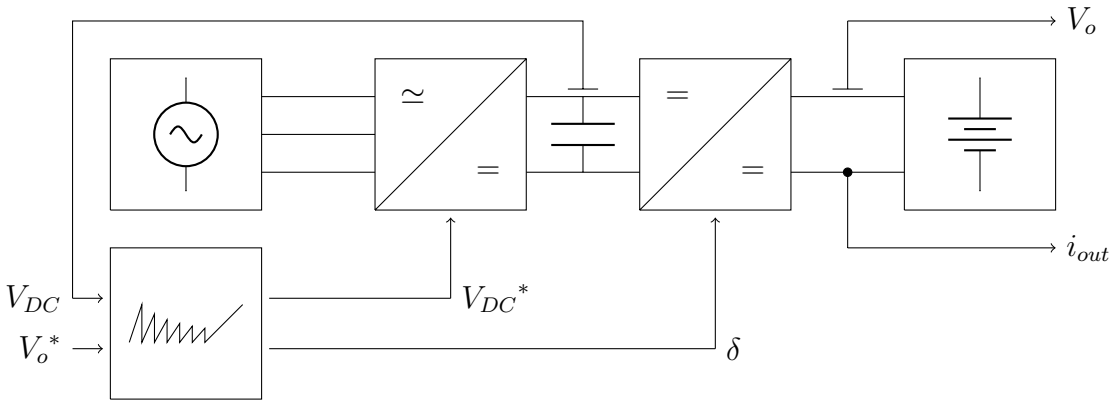


Figure 2.14: Ripple free mask driving AR and IBC

Chapter 3

General Control Strategy

As visible in Chapter 1, multiple controllers are involved. In order to deliver to the battery any desired charging profile, one or multiple control loops might be implemented. In Figure 3.1 are depicted two possible voltage, and current control loops even though only the second type have been developed. This main controller provides a proper V_o^* that the IBC must produce. However, as explained in Section 2, this signal does not directly drive the IBC but has to pass inside the ripple-free mask. The ripple mask converts main controller's output in two reference signals V_{DC}^* and δ^* able to maintain ripple-free conditions. Voltage V_{DC}^* is forwarded to the IAR that my mean of the voltage oriented control technique provides the proper PWM commutation pattern. Voltage oriented control requires three controllers able to operate on the synchronous Park framework. A first PI controller treats the IAR BUS voltage error ΔV_{DC} and computes a proper I_d. Another couple of PI controllers computes the necessary internal voltages u_d and u_q necessary for nullifying the current errors ΔI_d and ΔI_q. For what it concerns δ^* it is not directly forwarded to the IBC. It is again treated by mean of a rebalancing network in order to compensate possible unbalances inside IBC's legs. It must be noticed that a similar approach could also be applied at the front side of the charger trying to keep symmetric the IAR's front end voltages.

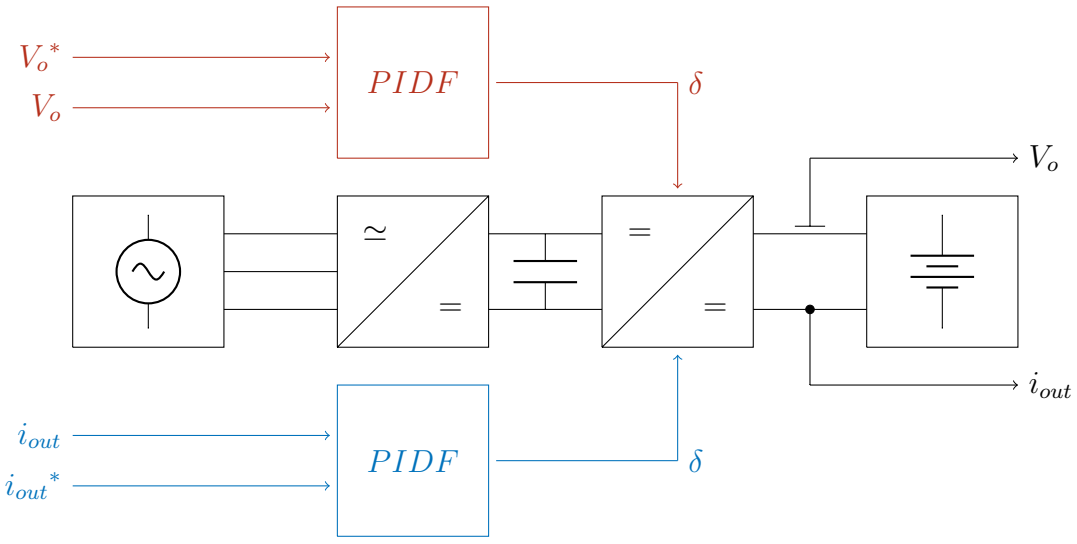


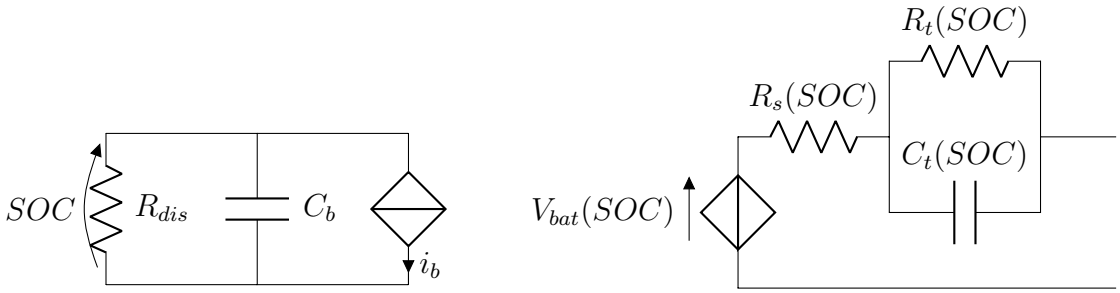
Figure 3.1: Possible voltage (red) and current (blue) control loops

Voltage oriented controllers have not been studied. In this section, much care

has been dedicated to the main controller and the rebalancing network design. For the sake of completeness, a further filtering action carried out by mean of an output capacitor have been considered. All the test have been done using a resistive load R_l for the only purpose to study the rebalancing action and the averaged approach for tuning the main controller. Further experiments may use actual loads able to introduce battery features such as open circuit Electromotive Force (EMF), and RC dynamic answers.

3.1 Averaged Main Control

One of the most used equivalent circuits for describing batteries consists in a voltage source in series to the so called Randles circuit representing electrochemical interfaces' processes [57]. As visible in Figure 3.2b, the RC parallel bipole introduces a first order dynamic answer (more complete models take into account also superior order contributes). All the involved parameters (V_{bat}, R_s, R_t and C_t) depend on



(a) SOC driving circuit (b) Electrochemical processes reppresentation

Figure 3.2: Battery equivalent circuit

the SOC level. Driving circuit visible in Figure 3.2a represents parameters SOC dependency. However, since the charge takes places in times ranging in the order of twenty minutes ($3C$ charging), one could perform a circuit linearization around a certain working point considering internal parameters as SOC invariant. As a first approximation the equivalent circuit visible in Figure 3.3 can be considered for studying and testing purposes. Where R_l represent the equivalent series resistance in a certain moment with a certain SOC. It can be shown that considering a series connection able to reach a voltage of about 500V (hundreds of cells) the equivalent R_l becomes in the order of magnitude of few Ω. For the sole purpose to study the proposed topology and the rebalancing network introduced below, the charging operation have been studied throughout equivalent IBC connected to a resistive load (Figure 3.4).

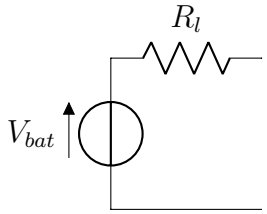


Figure 3.3: Linearized steady-state battery circuit

Assuming to represent the battery charger as a voltage source V_{IBC} it can be easily demonstrated that the charging circuit could be described by mean of one equivalent voltage source V_{eq} equal to:

$$V_{eq} = V_{IBC} - V_{bat} \tag{3.1}$$

The new system could be described as a resistive load R_l connected to an equivalent IBC that feeds V_{eq}. However, having transformed the IBC from operating on the whole battery voltage on a new system operating on the voltage drops only introduces changes on the duty cycle computation. The equivalent IBC gain is described by $V_{eq} = V_{DC}\delta$. Meanwhile the actual IBC gain is $V_{IBC} = V_{DCr}\delta_r$. Actual duty cycle δ_r depends on the computed δ and on the V_{bat}. From (3.1), one could state:

$$\delta_r = \delta\frac{V_{DC}}{V_{DCr}} + \frac{V_{bat}}{V_{DCr}} \tag{3.2}$$

Where the equivalent IBC bus voltage depends on the end of charge V_{batM} (maximum value). From (3.2) the following inequality can be done:

$$\delta_r = \delta\frac{V_{DC}}{V_{DCr}} + \frac{V_{bat}}{V_{DCr}} \leq \frac{V_{DC}}{V_{DCr}} + \frac{V_{bat}}{V_{DCr}} \leq \frac{V_{DC}}{V_{DCr}} + \frac{V_{batM}}{V_{DCr}} \leq 1 \tag{3.3}$$

Considering the worse case, it is possible compute the equivalent V_{DC}. Indeed:

$$V_{DCm} \leq V_{DCr} - V_{batM} \tag{3.4}$$

Otherwise one could employ the actual V_{bat}:

$$V_{DC} \leq V_{DCr} - V_{bat} \tag{3.5}$$

Furthermore, according to (1.47), having changed both duty cycles and DC link, currents ripples in the new equivalent IBC are different from the actual one. This transformation must be intended for average values only. As explained in Section 3.3, a proper sampling strategy able to get rid of ripple effects is employed in the control stage. It must be noticed that values V_{DC}, V_{DCM}, V_o and δ showed in this section does not corresponds to the same symbols employed in the other sections but are only referring to the controller equivalent IBC. Moreover, V_{eq} introduced above is indicated with V_o for the remaining part of the Section 3.1.

Following approach explained in [58], [59] one could estimate all the SOC varying parameters trough the charging process. An on-live controller re-tuning is necessary for reaching correct operations.

The following control has been designed considering the general equivalent IBC circuit visible on Figure 3.4 operating with a resistive load only. Computed working point δ is transferred back to the actual converter scheme (connected to an actual battery model) by mean of (3.2). Tests have been done considering three legs only. As visible below, the control can be easily scaled to $N = 9$. Since filtering branch involves the high frequency components only, it can be added directly into the equivalent IBC without leading to appreciable errors. Similarly to what did in previous chapters, it is possible to model the buck converter throughout an averaged model [43], [60]–[62]. In Figure 3.5 an averaged representation on the Laplace domain of the IBC's legs has been drawn.

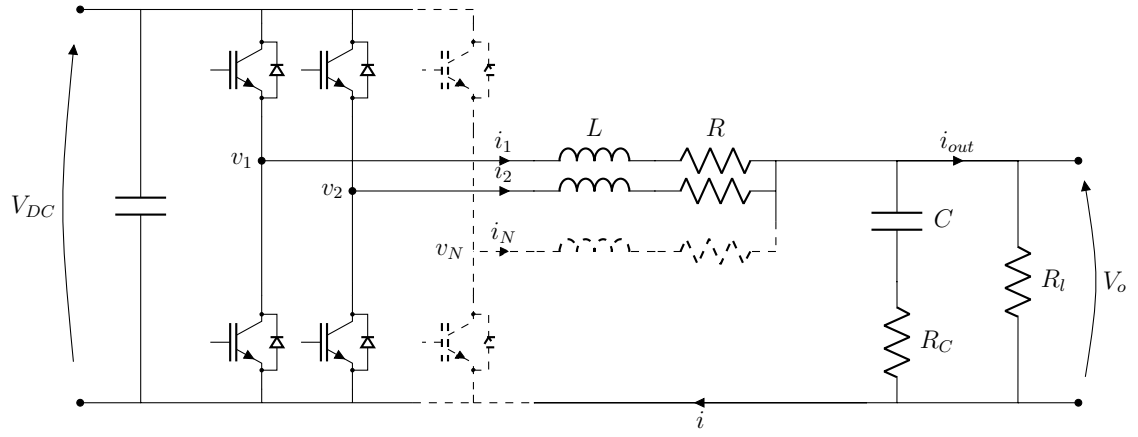


Figure 3.4: Main controller reference topology

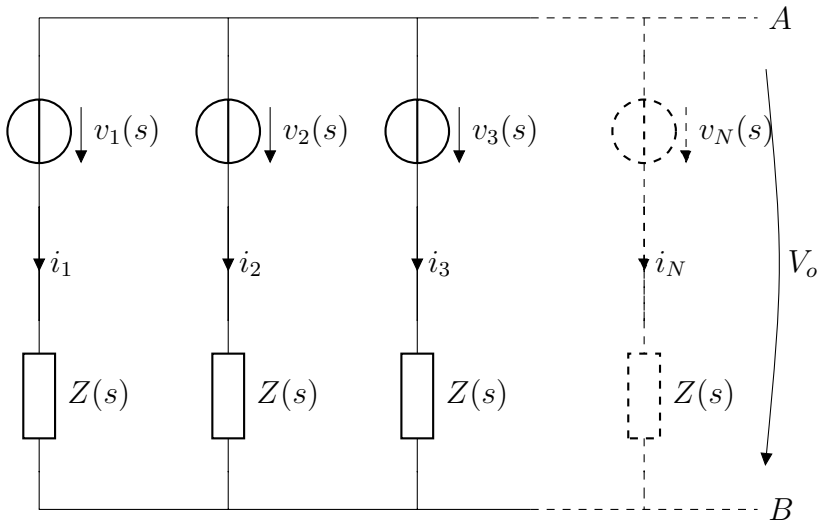


Figure 3.5: IBC's legs averaged in the Laplace domain

Describing each pole voltage as:

$$v_k(t) = \delta_k(t) V_{DC} \tag{3.6}$$

it is possible to write a voltage circuitation (Kirchhoff's law) for each leg. For the sake of semlicity each leg is considered a replica of the others. For instance, the first leg equation is:

$$v_1(t) = L\frac{\mathrm{d}i_1(t)}{\mathrm{d}t} + Ri_1(t) + V_o(t) \tag{3.7}$$

rewriting (3.7) on a generic k leg it follows that:

$$v_k(t) = L\frac{\mathrm{d}i_k(t)}{\mathrm{d}t} + Ri_k(t) + V_o(t) \rightarrow v_L(t) = v_k(t) - Ri_k(t) - V_o(t) = L\frac{\mathrm{d}i_k(t)}{\mathrm{d}t} \tag{3.8}$$

In a similar way it is possible write the a current equality for the node involving the oputput capacitor C:

$$i(t) = i_{out}(t) + C\frac{\mathrm{d}V_C(t)}{\mathrm{d}t} \rightarrow i_C(t) = i(t) - i_{out}(t) = C\frac{\mathrm{d}V_C(t)}{\mathrm{d}t} \tag{3.9}$$

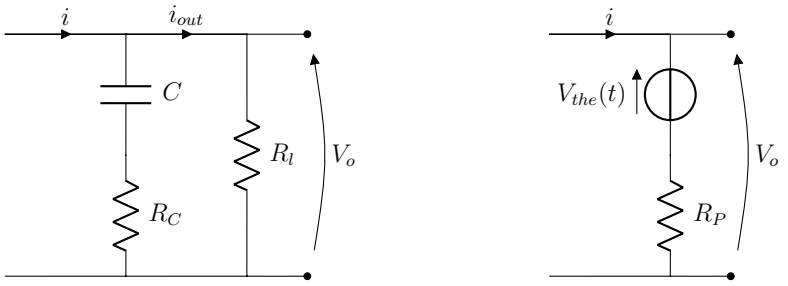


Figure 3.6: Output parallel branch before (left) and after (right) Thèvenin topological transformation

Computing a topological transformation (Figure 3.6) on the output parallel branches makes possible express $V_o(t)$ in (3.8) as a function of $V_C(t)$ and $i(t)$. Assuming to know the voltage $V_C(t)$ accros the capacitor C, thanks to the substitution theorem it is possible replace it with an independent voltage source that replicates the voltage $V_C(t)$. It is immediate verify that the Thévenin equivalent voltage is:

$$V_{the}(t) = V_C(t)\frac{R_l}{R_l + R_C} \tag{3.10}$$

and that the equivalent resistance becomes:

$$R_P = \frac{R_l R_C}{R_l + R_C} \tag{3.11}$$

and therefore $V_o(t)$ becomes:

$$V_o(t) = V_{the}(t) + R_P i(t) = V_C(t)\frac{R_l}{R_l + R_C} + R_P i(t) \tag{3.12}$$

In a similar way, replacing each inductor with a independent current source $i_k(t)$ it is possible find the Norton equivalent bipole seen from the capacitor C. It is then possible express $i_C(t)$ in (3.9) as a function involving $V_C(t)$ and $i(t)$. The Norton

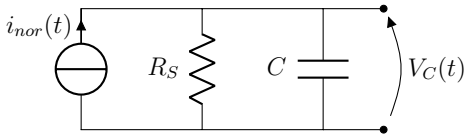


Figure 3.7: Norton topological transformation of the IBC seen from C

equivalent current is:

$$i_{nor}(t) = i(t)\frac{R_l}{R_l + R_C} \tag{3.13}$$

and the equivalent resistance becomes:

$$R_S = R_l + R_C \tag{3.14}$$

and therefore $i_C(t)$ becomes:

$$i_C(t) = i_{nor}(t) - \frac{V_C(t)}{R_S} = i(t)\frac{R_l}{R_l + R_C} - \frac{V_C(t)}{R_S} \tag{3.15}$$

Replacing (3.11) and (3.12) into (3.8) yields:

$$L\frac{\mathrm{d}i_k(t)}{\mathrm{d}t} = v_k(t) - Ri_k(t) - V_c(t)\frac{R_P}{R_C} - R_P i(t) \tag{3.16}$$

Similarly, replacing (3.14) and (3.15) into (3.9) yields:

$$C\frac{\mathrm{d}V_C(t)}{\mathrm{d}t} = i(t)\frac{R_P}{R_C} - \frac{V_C(t)}{R_S} \tag{3.17}$$

The total current $i(t)$ can be seen as the summation of all the legs currents $i_k(t)$ (Equation 3.18).

$$i(t) = \sum_{k=1}^{N} i_k(t) \tag{3.18}$$

It can be easily seen that by replacing (3.6) and (3.18) inside (3.16) and (3.17) the system could lead to the following matrix:

$$\begin{bmatrix} \frac{\mathrm{d}i_1(t)}{\mathrm{d}t} \\ \frac{\mathrm{d}i_2(t)}{\mathrm{d}t} \\ \vdots \\ \frac{\mathrm{d}i_N(t)}{\mathrm{d}t} \\ \frac{\mathrm{d}V_C(t)}{\mathrm{d}t} \end{bmatrix} = \begin{bmatrix} -\frac{R+R_P}{L} & -\frac{R_P}{L} & \cdots & -\frac{R_P}{L} & -\frac{R_P}{LR_C} \\ -\frac{R_P}{L} & -\frac{R+R_P}{L} & \cdots & -\frac{R_P}{L} & -\frac{R_P}{LR_C} \\ \vdots & \vdots & \ddots & \vdots & \vdots \\ -\frac{R_P}{L} & -\frac{R_P}{L} & \cdots & -\frac{R+R_P}{L} & -\frac{R_P}{LR_C} \\ \frac{R_P}{CR_C} & \frac{R_P}{CR_C} & \cdots & \frac{R_P}{CR_C} & -\frac{1}{CR_S} \end{bmatrix} \begin{bmatrix} i_1(t) \\ i_2(t) \\ \vdots \\ i_N(t) \\ V_C(t) \end{bmatrix} + \\ + \begin{bmatrix} \frac{V_{DC}}{L} & 0 & \cdots & 0 \\ 0 & \frac{V_{DC}}{L} & \cdots & 0 \\ \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & \cdots & \frac{V_{DC}}{L} \\ 0 & 0 & \cdots & 0 \end{bmatrix} \begin{bmatrix} \delta(t) \\ \delta(t) \\ \vdots \\ \delta_N(t) \end{bmatrix} \tag{3.19}$$

Replacing (3.18) in (3.12):

$$V_o(t) = \begin{bmatrix} R_p & R_p & \cdots & R_p & \frac{R_l}{R_l+R_C} \end{bmatrix} \begin{bmatrix} i_1(t) \\ i_2(t) \\ \vdots \\ i_N(t) \\ V_C(t) \end{bmatrix} \tag{3.20}$$

and knowign that $i_{out(t)} = V_o(t)/R_l$:

$$i_{out}(t) = \begin{bmatrix} \frac{R_p}{R_l} & \frac{R_p}{R_l} & \cdots & \frac{R_p}{R_l} & \frac{1}{R_l+R_C} \end{bmatrix} \begin{bmatrix} i_1(t) \\ i_2(t) \\ \vdots \\ i_N(t) \\ V_C(t) \end{bmatrix} \tag{3.21}$$

By attaching to (3.19) equations (3.20) and (3.21) it is possible represent the IBC in the well known state-space representation respectively having as output variable $V_o(t)$ or $i_{out}(t)$.

Having averaged the pole voltages $v_k(t)$ have made possible the creation of a continuous time-invariant system. However, it must be noticed that circuits parameters could varying in time and may differ from one another. A more rigorous representation would have used different time-varying values for legs parameters (for instance $R_k(t)$ and $L_k(t)$) leading to a more complex continuos variant representation.

Equation (3.19) represents a Multiple Inputs, Single Output (MISO) system because has N input variables $\delta_k(t)$ and one output variable. The set of currents $i_k(t)$ and $V_C(t)$ represent the state variables.

However, being the IBC's main task generate a certain $V_o(t)$ or $i_{out}(t)$ starting from a unique duty cycles δ (chapter 1), a simplyfication is necessary. Thanks to averaged δ introduced in (3.22) it is possible transform (3.19) into a Sultiple Inputs, Single Output (SISO) system.

$$\delta(t) = \frac{1}{N}\sum_{k=1}^{N}\delta_k(t) \tag{3.22}$$

As explained before, the main controller discussed in this chapter has been designed for controlling the current only. The state/space representation is therefore described by mean of (3.19) and (3.21).

Introducing (3.18) and (3.22) produces a maxive semplification on the (3.19) associate system of equations. Indeed:

$$\begin{cases} L\frac{\mathrm{d}i(t)}{\mathrm{d}t} = -R_l i(t) - NR_P i(t) - N\frac{R_p}{R_C}V_C(t) + NV_{DC}\delta(t) \\ C\frac{\mathrm{d}V_C(t)}{\mathrm{d}t} = \frac{R_P}{R_C}i(t) - \frac{1}{R_S}V_C(t) \end{cases} \tag{3.23}$$

Defining new variables $v(t) = V_{DC}\delta(t)$ $L' = L/N$ and $R' = R/N$ and replacing (3.11) and (3.14) into (3.23):

$$\begin{cases} v(t) = L'\frac{\mathrm{d}i(t)}{\mathrm{d}t} + R'_l i(t) + \frac{R_l R_C}{R_l+R_C}i(t) + \frac{R_l}{R_l+R_C}V_C(t) \\ \frac{R_l}{R_l+R_C}i(t) = C\frac{\mathrm{d}V_C(t)}{\mathrm{d}t} + \frac{1}{R_l+R_C}V_C(t) \end{cases} \tag{3.24}$$

In a similar way, replacing (3.11), (3.14) and (3.18) into (3.21) produces:

$$i_{out}(t) = \frac{V_o(t)}{R_l} = \frac{R_C}{R_l+R_C}i(t) + \frac{1}{R_l+R_C}V_C(t) \tag{3.25}$$

Replacing (3.25) into (3.24) creates (3.26).

$$\begin{cases} v(t) = L'\frac{\mathrm{d}i(t)}{\mathrm{d}t} + R'_l i(t) + V_o(t) \\ i(t) = C\frac{\mathrm{d}V_C(t)}{\mathrm{d}t} + i_{out}(t) \end{cases} \tag{3.26}$$

It must be noticed that the same outcome (3.26) could have been founded following the single branch equivalent circuit approach shown in section 1.2, (Figure 3.8).

Assuming the capacitor's ESR R_C negligible, it is possible to quikly state that $v_C(t) = v_o(t)$. System (3.26) further simplifies:

$$\begin{cases} v(t) = L'\frac{\mathrm{d}i(t)}{\mathrm{d}t} + R'_l i(t) + V_o(t) \\ i(t) = C\frac{\mathrm{d}V_o(t)}{\mathrm{d}t} + i_{out}(t) \end{cases} \tag{3.27}$$

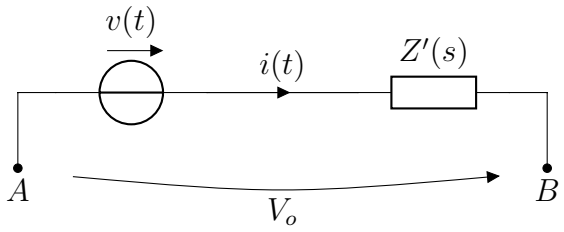


Figure 3.8: Single branch equivalent circuit on the Laplace domain

Transforming (3.27) into Laplace domain:

$$\begin{cases} v(s) = (sL' + R')i(s) + V_o(s) \\ i(s) = sCV_o(s) + i_{out}(s) \end{cases} \tag{3.28}$$

and with the same procedure

$$\delta(s) = \frac{1}{N}\sum_{k=1}^{N}\delta_k(s) = \frac{v(s)}{V_{DC}} \tag{3.29}$$

moreover it is possible state:

$$V_o(s) = R_l i_{out}(s) \tag{3.30}$$

that could be rewritten as:

$$V_o(s) = i(s)\frac{R_l}{1 + sCR_l} \tag{3.31}$$

One could find (3.32) (3.33) transfers functions.

$$G(s) = \frac{i(s)}{V(s)} = \frac{1 + sCR_l}{s^2L'CR_l + s(L' + CR_lR') + R_l + R'} \tag{3.32}$$

$$G(s)' = \frac{i_{out}(s)}{i(s)} = \frac{1}{1 + sCR_l} \tag{3.33}$$

Transfer function (3.32) can be easily expressed as a function of $\delta(s)$ by mean of (3.29):

$$G(s) = \frac{i(s)}{d(s)} = \frac{V_{DC}}{R_l + R'}\frac{1 + sCR_l}{s^2\frac{L'CR_l}{R_l+R'} + s\frac{L'+CR_lR'}{R_l+R'} + 1} \tag{3.34}$$

3.1.1 Possible Transfer Function Assumptions

Depending on information availability, multiple assumptions can be made. Since a rebalancing control is expected to be done, current transducers on each leg are present. Having all the $i_k(t)$ currents make possible compute $i(t)$. One possible choice is neglecting the capacitor effect by completely remove the terms referring to the R_CC branch. A further possibility is to assume $i(t) \approx i_{out}(t)$. Conversely one could also measure $i_{out}(t)$ and work on the whole rigorous system. It must be noticed that in any case a preliminary assumption neglecting R_C have already been made. Moreover, the resistive load consists in a massive simplification for only test purposes. In the following paragraphs, all the three possibilities are analyzed.

Table 3.1: Single module three-phase testing bench parameters

Parameter	Symbol	Value	Unit
Number of legs per side	N	3	
DC link voltage	V_{DC}	90	V
Switching frequency	f_{SW}	20	kHz
Sampling frequency	f_s	60	kHz
A/D resolution	M	12	bit
Reactors inductance	L	1	mH
Reactors resistance	R	900	$m\Omega$
Filter capacitance	C	16	μF
Filter ESR	R_C	900	$m\Omega$
Resistive load	R_l	6	Ω

It must be pointed out that in any case, the real answer of the legs has not been taken into account. Parasitic parameters such as dead times could bring to steady-state errors. More, in general, the model might lose its linearity due to switches' and inductors' coils behaviors. Circuit parameters visible in Table 3.1 have been considered.

Capacitive Branch Removal

As explained above, one of the possibility is to consider the system without the capacitive branch (Figure 3.9). The immediate effect can be seen on the lack of $V_o(t)$ smoothness, carried out by C. In most application, this assumption could introduce acceptable voltage ripples. It must be noticed that when the converters operate in the ripple-free zone, the current profile $i(t)$ is theoretically flat. This means that, in steady-state, the capacitive branch would not perform any filtering action.

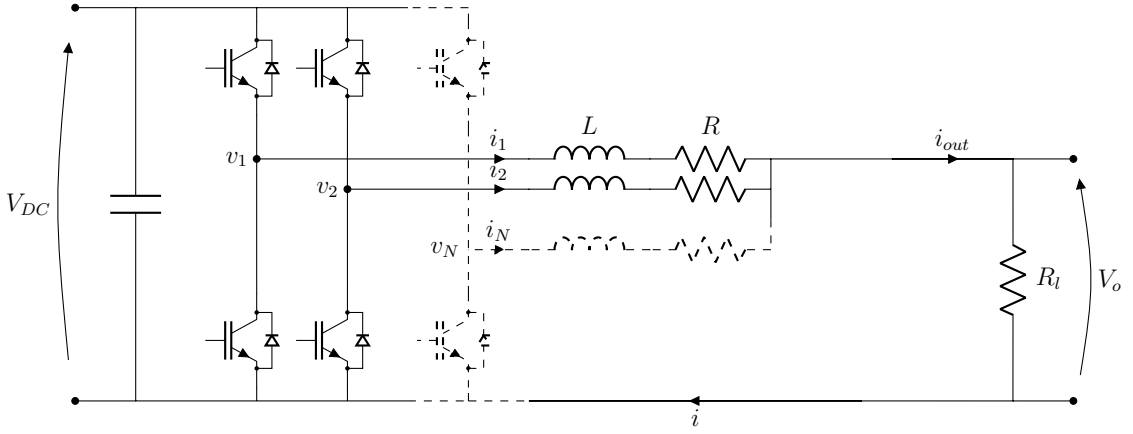


Figure 3.9: Main controller reference topology without capacitive filtering branch

Being C missing, (3.33) becomes:

$$G(s)' = \frac{i_{out}(s)}{i(s)} = 1 \tag{3.35}$$

and therefore as visible in Figure 3.9:

$$i_{out}(s) = i(s) \tag{3.36}$$

For what it concern (3.34), it can easily verify that it becomes a first-order transfer function:

$$G(s) = \frac{i(s)}{d(s)} = \frac{V_{DC}}{sL' + R_l + R'} \tag{3.37}$$

computing the total transfer function:

$$\frac{i_{out}(s)}{d(s)} = G(s)G(s)' = \frac{V_{DC}}{sL' + R_l + R'} \tag{3.38}$$

Studying the open-loop stability, the only present pole (3.39) is located on the left side of the Nyquist plane.

$$S = -\frac{R_l + R'}{L'} \tag{3.39}$$

Full removal of the capacitor C leads to V_{DC} state variable removal. All the matrix A, B and C shown in (3.19) and (3.21) must be modified accordingly. Since both vectors containing the derivative of the state variable and the state variable itself have been downsized from $N + 1$ to N, the matrix A need to be resized accordingly, becoming then NxN. Both B and C matrix have lost one dimension.

Showing the relation between $i_{out}(t)$ and legs' currents $i_k(t)$:

$$i(t) = \sum_{k=1}^{N} i_k(t) = i_{out}(t) \tag{3.40}$$

The updated state-space representation becomes:

$$\begin{bmatrix} \frac{\mathrm{d}i_1(t)}{\mathrm{d}t} \\ \frac{\mathrm{d}i_2(t)}{\mathrm{d}t} \\ \vdots \\ \frac{\mathrm{d}i_N(t)}{\mathrm{d}t} \end{bmatrix} = \begin{bmatrix} -\frac{R+R_P}{L} & -\frac{R_P}{L} & \cdots & -\frac{R_P}{L} \\ -\frac{R_P}{L} & -\frac{R+R_P}{L} & \cdots & -\frac{R_P}{L} \\ \vdots & \vdots & \ddots & \vdots \\ -\frac{R_P}{L} & -\frac{R_P}{L} & \cdots & -\frac{R+R_P}{L} \end{bmatrix} \begin{bmatrix} i_1(t) \\ i_2(t) \\ \vdots \\ i_N(t) \end{bmatrix} + \\ + \begin{bmatrix} \frac{V_{DC}}{L} & 0 & \cdots & 0 \\ 0 & \frac{V_{DC}}{L} & \cdots & 0 \\ \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & \cdots & \frac{V_{DC}}{L} \end{bmatrix} \begin{bmatrix} \delta(t) \\ \delta(t) \\ \vdots \\ \delta_N(t) \end{bmatrix} \tag{3.41}$$

$$i_{out}(t) = \begin{bmatrix} 1 & 1 & \cdots & 1 \end{bmatrix} \begin{bmatrix} i_1(t) \\ i_2(t) \\ \vdots \\ i_N(t) \end{bmatrix} \tag{3.42}$$

Output Current Assumption

As explained above, a possible solution for considering the effect of the capacitor without measuring the i_{out} is considering $i(t) \approx i_{out}(t)$. The capacitor introduces a filtering action on the system, but it is not taken into account in the model. It must be pointed out that thanks to ripple-free strategy, this action occurs only during

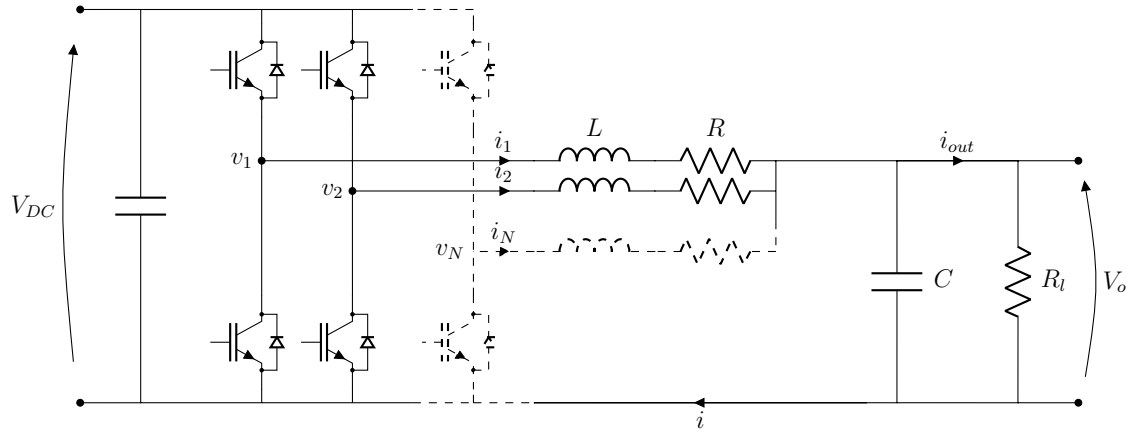


Figure 3.10: Main controller reference topology without ESR

V_{DC} transients (considering resistive loads). In Figure 3.10, topology neglecting R_C have been drawn.

Forcing $i(t) \approx i_{out}(t)$, (3.33) becomes:

$$G(s)' = \frac{i_{out}(s)}{i(s)} = 1 \tag{3.43}$$

meanwhile (3.34) does not change.

$$G(s) = \frac{i(s)}{d(s)} = \frac{V_{DC}}{R_l + R'} \frac{1 + sCR_l}{s^2 \frac{L'CR_l}{R_l+R'} + s\frac{L'+CR_lR'}{R_l+R'} + 1} \tag{3.44}$$

computing the total transfer function:

$$\frac{i_{out}(s)}{d(s)} = G(s)G(s)' = \frac{V_{DC}}{R_l + R'} \frac{1 + sCR_l}{s^2 \frac{L'CR_l}{R_l+R'} + s\frac{L'+CR_lR'}{R_l+R'} + 1} \tag{3.45}$$

Zero poles cancellation approach might lead to a better system answer.

For transducer availability reasons, in Chapter 4, $i(t)$ have been considered as main current.

Having considered (3.33) as an unitary function leads to a variation in state space reppresentation ((3.19) and (3.21)). Matrices A and B does not vary. On the other hand I_{out} does not take into account the capacitive current contribution. Having $i(t) \approx i_{out}(t)$ means:

$$i(t) = \sum_{k=1}^{N} i_k(t) \approx i_{out}(t) \tag{3.46}$$

that represents a strong variation in matrix C. Indeed the new state-space repre-

sentation becomes (R_C neglection have not been represented):

$$\begin{bmatrix} \frac{\mathrm{d}i_1(t)}{\mathrm{d}t} \\ \frac{\mathrm{d}i_2(t)}{\mathrm{d}t} \\ \vdots \\ \frac{\mathrm{d}i_N(t)}{\mathrm{d}t} \\ \frac{\mathrm{d}V_C(t)}{\mathrm{d}t} \end{bmatrix} = \begin{bmatrix} -\frac{R+R_P}{L} & -\frac{R_P}{L} & \cdots & -\frac{R_P}{L} & -\frac{R_P}{LR_C} \\ -\frac{R_P}{L} & -\frac{R+R_P}{L} & \cdots & -\frac{R_P}{L} & -\frac{R_P}{LR_C} \\ \vdots & \vdots & \ddots & \vdots & \vdots \\ -\frac{R_P}{L} & -\frac{R_P}{L} & \cdots & -\frac{R+R_P}{L} & -\frac{R_P}{LR_C} \\ \frac{R_P}{CR_C} & \frac{R_P}{CR_C} & \cdots & \frac{R_P}{CR_C} & -\frac{1}{CR_S} \end{bmatrix} \begin{bmatrix} i_1(t) \\ i_2(t) \\ \vdots \\ i_N(t) \\ V_C(t) \end{bmatrix} + \\ + \begin{bmatrix} \frac{V_{DC}}{L} & 0 & \cdots & 0 \\ 0 & \frac{V_{DC}}{L} & \cdots & 0 \\ \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & \cdots & \frac{V_{DC}}{L} \\ 0 & 0 & \cdots & 0 \end{bmatrix} \begin{bmatrix} \delta(t) \\ \delta(t) \\ \vdots \\ \delta_N(t) \end{bmatrix} \tag{3.47}$$

$$i_{out}(t) = \begin{bmatrix} 1 & 1 & \cdots & 1 & 0 \end{bmatrix} \begin{bmatrix} i_1(t) \\ i_2(t) \\ \vdots \\ i_N(t) \\ V_C(t) \end{bmatrix} \tag{3.48}$$

Rigorous Approach

Assuming to add a further current transducer on the load branch it is possible fully consider the capacitor filtering contribution. This third approach is able to deal with any load. Higher-order answers introduced from more realistic loads (rather than resistive one) could activate the capacitor C even outside the V_{DC} transients periods.

The topology of Figure 3.10 does not vary:

$$\frac{i_{out}(s)}{d(s)} = G(s)G(s)' = \frac{V_{DC}}{R_l + R'} \frac{1}{s^2 \frac{L'CR_l}{R_l+R'} + s\frac{L'+CR_lR'}{R_l+R'} + 1} \tag{3.49}$$

No changes in the state-space representations are needed.

3.1.2 Average Duty Cycle Control

The control must refer to the previously showed (Section 1.1.2) charging profile. In the first CC stage (going from SOC 0% to 80%), the current profile is mostly flat. However, pre-charge and post-charge modality should be introduced, avoiding to provide or remove the full charging current suddenly. Being the whole charging process expected to last tens of minutes adding a precharge mode does not significantly degrade the charging times. As visible in Figure 3.11, a possible solution could introduce a current ramp with a duration in the order of a few seconds. In [63] current staircase is presented as a possible pre-charging profile. In the same way, it is possible to introduce turning off post charging profiles.

A further aspect that must be taken into account is the legs faults occurrence. Once a leg or a power block occurs in a fault condition, it should be left out, and if possible, the battery charger should try to continue feeding the battery with the maximum current possible maintaining components safety conditions. In every

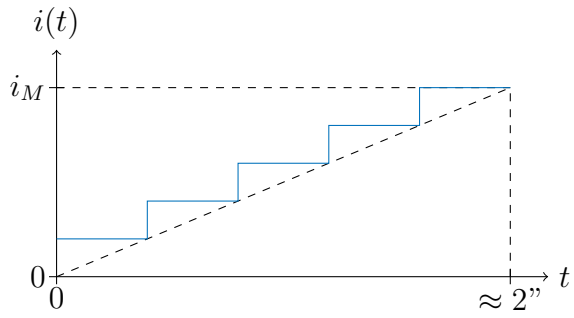


Figure 3.11: Current evolution during precharging mode

battery application involving lithium-based chemistries, a primary controlling and monitoring system (battery management system (BMS)) is always present. Every signal introduced by the BMS must be considered with the highest priority level. A fast BMS's tasks execution could prevent to SOH degradation or potentially dangerous dynamics.

Even though the charging profile is not expected to undergo in sharp parameters variation, an excellent dynamic response is still necessary during pre-charging mode, fault responses, and BMS's tasks executions.

Regardelles on what assumption have been done on the system model, every total transfer function $G(s)G(s)'$ provides $i_{out}(\delta(s))$. As shown in (3.29), δ represent the averaged duty cycle that must be used for powering the averaged single leg circuit visible in Figure 3.8 and getting a certain value of i^*_{out}. This averaged value is transfered back to the real N-legs circuit. In Figure 3.12, a proposed control scheme is introduced.

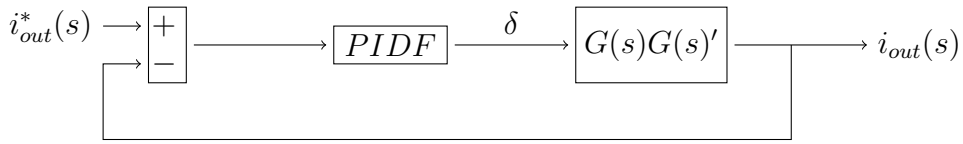


Figure 3.12: Averaged main control loop

Expected total current i^*_{out} must preliminary routed inside a saturation block that limits the maximum converter's i_{outM} accordingly to components capability. It must be pointed out that the rated output current could vary during operation. Fault detection or maintenance modules bypass (regardless if envolving the IAR or the IBC) could temporarily reduce the output current capability. Saturated output current is compared with the actual value of i_{out}. It must be noticed that in a rigorous approach (introduced in subsection 3.1.1), value i_{out} is directly provided by the load current transducer. In the remaining cases (visible in 3.1.1 and 3.1.1), i_{out} is computed by summing all the legs currents components:

$$i_{out}(t) = \sum_{k=1}^{N} i_k(t) \tag{3.50}$$

Error signal $e(s)$ enters inside a Proportional–Integral–Derivative-Filtering Controller (PIDF) stage $C(s)$ that computes the proper average δ that must feed the PWM generation block.

In the current proposal, the output current assumption has been implemented. The total transfer function $G(s)G(s)'$ have been transformed in the Z-transform domain (ensuring the compatibility in digital systems such as Digital Signal Processor (DSP) or Field-Programmable Gate Array (FPGA)). A biquadratic filter (PIDF) $C(s)$ have been tuned following the approach showed in [64]. Zero-pole cancellation and inversion formulae introduced in [65]–[70] have been used.

In order to implement the ripple-free strategy, it is necessary to convert back the computed δ into a pole voltage form by multiplying it by the V_{DC} value used in (3.6). It must be noticed that the V_{DC} employed by the averaged main control might be different from the one actually computed by the ripple-free mask.

3.2 Current Rebalancing Network

Mean duty cycle δ computed in section 3.1.2 must be transformed in the N δ_k that have to fire each IBC's legs. As explained above, legs can not be perfectly equal, and therefore the system could be unbalanced. An active current rebalancing network is needed in order to ensure the power share among each leg.

Rewriting legs' Kirchhoff voltage laws for legs 1 and k:

$$v_1(t) = L_1 \frac{\mathrm{d}i_1(t)}{\mathrm{d}t} + R_1 i_1(t) + V_o(t) \tag{3.51}$$

$$v_k(t) = L_k \frac{\mathrm{d}i_k(t)}{\mathrm{d}t} + R_k i_k(t) + V_o(t) \tag{3.52}$$

moreover, adding the averaged branch equation:

$$v(t) = L' \frac{\mathrm{d}i(t)}{\mathrm{d}t} + R'_l i(t) + V_o(t) \tag{3.53}$$

Transforming (3.51), (3.52), and (3.53) into Laplace domain:

$$v_1(s) = Z_1(s) i_1(s) + V_o(s) \tag{3.54}$$

$$v_k(s) = Z_k(s) i_k(s) + V_o(s) \tag{3.55}$$

$$v(s) = Z'(s) i(s) + V_o(s) \tag{3.56}$$

Assuming in a generic case having N legs and considering the unbalance mostly condensed in leg k. It is, therefore, possible state that:

$$Z_1(s) = Z(s) = NZ' \tag{3.57}$$

and that:

$$Z_k(s) = Z(s) + \Delta Z_k(s) = NZ' + \Delta Z_k(s) \tag{3.58}$$

furthermore:

$$i_1(s) = \frac{i(s)}{N} \tag{3.59}$$

$$i_k(s) = \frac{i(s)}{N} - \Delta i_k(s) \tag{3.60}$$

Where $\Delta i_k(s)$ is the current displacement[1] caused by the unbalance $\Delta Z_k(s)$. However, current unbalance can be also caused by other phenomena (uneven death times) that can not be summarize with an impedence variation. In the following treatmet, no referece to $\Delta Z_k(s)$ is done, all the impedences are considered equal and the error is summarize as $\delta_k(s)$ displacement.

Rebalancing network must compute the proper δ_k in order to compensate the current displacement $\Delta i_k(s)$. In the aforementioned example, legs 1 is considered perfectly balanced (3.57). Computing the current error $\Delta i_k(s)$ referring to both $i_1(s)$ and $i_k(s)$ provides the same results. However, in real condition, every leg differs from the averaged model (properly scaled by a factor N). Current errors may differ depending on what current has been taken as a comparison term. It is, therefore, necessary to define the notation in order to make it suitable for all the possibilities. When it comes to speaking about error referred to averaged $i(s)$, current displacement is defined as:

$$\Delta i_k(s) = \frac{i(s)}{N} - i_k(s) \tag{3.61}$$

meanwhile, the error in k-leg referred to a generic p-leg is defined as:

$$\Delta i_{pk}(s) = i_p(s) - i_k(s) \tag{3.62}$$

as explained above, an easier and more generic way for summarize current displacement is introducing $\delta_k(s)$ displacement in a similar way as done above for current displacement.

$$\Delta \delta_k(s) = \delta(s) - \delta_k(s) \tag{3.63}$$

meanwhile, the error in k-leg referred to a generic p-leg is defined as:

$$\Delta \delta_{pk}(s) = \delta_p(s) - \delta_k(s) \tag{3.64}$$

By simply subtracting Kirchoff's voltage law of the averaged branch (properly scaled) with the one of a generic k-leg:

$$v(s) - v_k(s) = Z(s)(\frac{i(s)}{N} - i_k(s)) \tag{3.65}$$

similarly considering p-leg and k-leg:

$$v_p(s) - v_k(s) = Z(s)(i_p(s) - i_k(s)) \tag{3.66}$$

Rewriting each pole voltage in function of the duty cycle and replacing current error definitions in (3.65) and (3.66):

$$V_{DC}\Delta\delta_k(s) = V_{DC}(\delta(s) - \delta_k(s)) = Z(s)(\Delta i_k(s)) \tag{3.67}$$

$$V_{DC}\Delta\delta_{pk}(s) = V_{DC}(\delta_p(s) - \delta_k(s)) = Z(s)(\Delta i_{pk}(s)) \tag{3.68}$$

Regardless of what is the reference current, rebalancing current controllers are necessary in order to compute the differential duty cycles needed for ensuring the even power share. Furthermore, the unbalance magnitude is totaly independent on

[1] To no be confused with current ripple

the load typology. Having considered a resistive load rather than an actual battery model dose not affect the unbalance transfer function.

Unbalance transfer functions can be then easily found:

$$D_k(s) = \frac{\Delta i_k(s)}{\Delta \delta_k(s)} = \frac{V_{DC}}{Z(s)} \tag{3.69}$$

$$D_{pk}(s) = \frac{\Delta i_{pk}(s)}{\Delta \delta_{pk}(s)} = \frac{V_{DC}}{Z(s)} \tag{3.70}$$

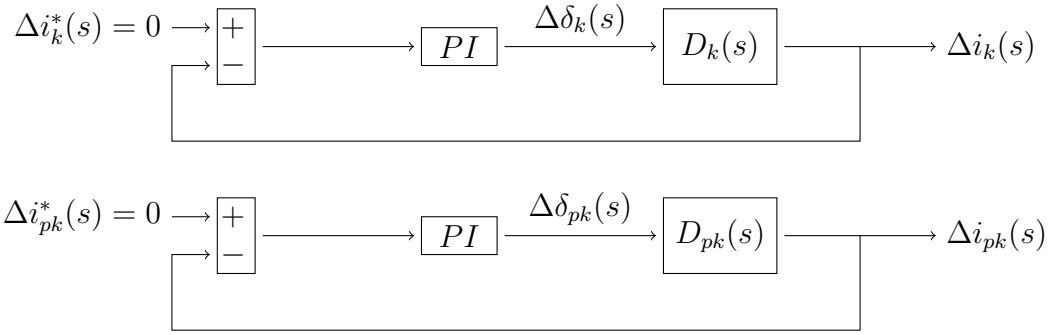


Figure 3.13: Drawing representing both kind of error rebalancing control loops

It must be noticed that regardless of what current error definition has been chosen, the unbalance transfer function is always defined as $V_{DC}/Z(s)$. Moreover, each rebalancing controllers could work with any current error, and it does not depend on loads (even an actual battery model) and main controller loop (regardless if voltage or current loops). This feature ensures high system flexibility making possible the live setting of each leg reference current. In Figure 3.13, rebalancing controllers are depicted by mean of a generic PI controller. In Figure 3.14 the rebalancing network mask have been drawn.

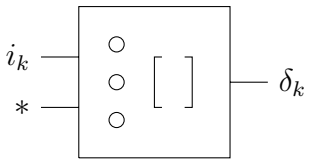


Figure 3.14: Rebalancing network mask

3.2.1 Duty Cycles Computation

Once the averaged duty cycle δ has been computed by the averaged main controller, it is necessary to attach at it duty cycle errors ($\Delta\delta_k(s)$ and/or $\Delta\delta_{pk}(s)$). Since there are N unknown δ_k, N relations are necessary for solving the system of equations. Averaged duty cycle δ provides the first equation (3.71), the remaining $N-1$ are provided by multiple current rebalancing controllers.

$$\delta(s) = \frac{1}{N}\sum_{k=1}^{N} \delta_k(s) \tag{3.71}$$

Various rebalancing network topologies can be made. In the following treatment, four noteworthy cases are exposed.

Currents Sequential Binding

It is base on the idea that each controlled current is taken as a reference current by the following rebalancing controller. In Figure 3.15 a visual representation is provided.

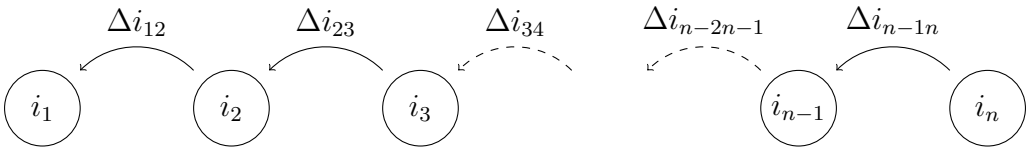


Figure 3.15: Currents sequential binding representation

Starting from the system below:

$$\begin{cases} \Delta\delta_{12}(s) = \delta_1(s) - \delta_2(s) \\ \Delta\delta_{23}(s) = \delta_2(s) - \delta_3(s) \\ \vdots \\ \Delta\delta_{n-1n}(s) = \delta_{n-1}(s) - \delta_n(s) \end{cases} \tag{3.72}$$

Attaching at the system (3.72) relation (3.71) it is possible write the following matrixs equation:

$$\begin{bmatrix} \delta(s) \\ \Delta\delta_{12}(s) \\ \Delta\delta_{23}(s) \\ \vdots \\ \Delta\delta_{n-2n-1}(s) \\ \Delta\delta_{n-1n}(s) \end{bmatrix} = \begin{bmatrix} \frac{1}{N} & \frac{1}{N} & \frac{1}{N} & \cdots & \frac{1}{N} & \frac{1}{N} \\ 1 & -1 & 0 & \cdots & 0 & 0 \\ 0 & 1 & -1 & \cdots & 0 & 0 \\ \vdots & \vdots & \vdots & \ddots & \vdots & \vdots \\ 0 & 0 & 0 & \cdots & -1 & 0 \\ 0 & 0 & 0 & \cdots & 1 & -1 \end{bmatrix} \begin{bmatrix} \delta_1(s) \\ \delta_2(s) \\ \delta_3(s) \\ \vdots \\ \delta_{n-1}(s) \\ \delta_n(s) \end{bmatrix} \tag{3.73}$$

Computing the inverse matrix:

$$\begin{bmatrix} \delta_1(s) \\ \delta_2(s) \\ \delta_3(s) \\ \vdots \\ \delta_{n-1}(s) \\ \delta_n(s) \end{bmatrix} = \begin{bmatrix} 1 & \frac{N-1}{N} & \frac{N-2}{N} & \cdots & \frac{2}{N} & \frac{1}{N} \\ 1 & -\frac{1}{N} & \frac{N-2}{N} & \cdots & \frac{2}{N} & \frac{1}{N} \\ 1 & -\frac{1}{N} & -\frac{2}{N} & \cdots & \frac{2}{N} & \frac{1}{N} \\ \vdots & \vdots & \vdots & \ddots & \vdots & \vdots \\ 1 & -\frac{1}{N} & -\frac{2}{N} & \cdots & -\frac{N-2}{N} & \frac{1}{N} \\ 1 & -\frac{1}{N} & -\frac{2}{N} & \cdots & -\frac{N-2}{N} & -\frac{N-1}{N} \end{bmatrix} \begin{bmatrix} \delta(s) \\ \Delta\delta_{12}(s) \\ \Delta\delta_{23}(s) \\ \vdots \\ \Delta\delta_{n-2n-1}(s) \\ \Delta\delta_{n-1n}(s) \end{bmatrix} \tag{3.74}$$

Current binding to k-th leg

It is base on the idea that each control takes as a reference current the k-th leg current. Assuming $k = 1$:

Starting from the system below:

$$\begin{cases} \Delta\delta_{12}(s) = \delta_1(s) - \delta_2(s) \\ \Delta\delta_{13}(s) = \delta_1(s) - \delta_3(s) \\ \vdots \\ \Delta\delta_{1n}(s) = \delta_1(s) - \delta_n(s) \end{cases} \tag{3.75}$$

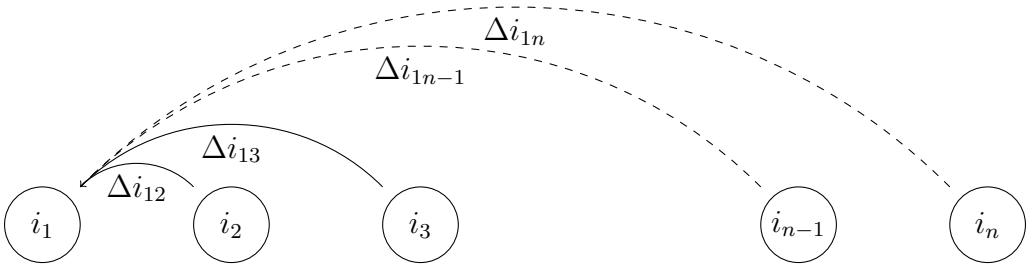


Figure 3.16: Currents binding to the first leg current

Figure 3.16 provides a visual representation of the (3.75) case.

Attaching at the system (3.75) relation (3.71) it is possible write the following matrix equation:

$$\begin{bmatrix} \delta(s) \\ \Delta\delta_{12}(s) \\ \Delta\delta_{13}(s) \\ \vdots \\ \Delta\delta_{1n-1}(s) \\ \Delta\delta_{1n}(s) \end{bmatrix} = \begin{bmatrix} \frac{1}{N} & \frac{1}{N} & \frac{1}{N} & \cdots & \frac{1}{N} & \frac{1}{N} \\ 1 & -1 & 0 & \cdots & 0 & 0 \\ 1 & 0 & -1 & \cdots & 0 & 0 \\ \vdots & \vdots & \vdots & \ddots & \vdots & \vdots \\ 1 & 0 & 0 & \cdots & -1 & 0 \\ 1 & 0 & 0 & \cdots & 0 & -1 \end{bmatrix} \begin{bmatrix} \delta_1(s) \\ \delta_2(s) \\ \delta_3(s) \\ \vdots \\ \delta_{n-1}(s) \\ \delta_n(s) \end{bmatrix} \tag{3.76}$$

Computing the inverse matrix:

$$\begin{bmatrix} \delta_1(s) \\ \delta_2(s) \\ \delta_3(s) \\ \vdots \\ \delta_{n-1}(s) \\ \delta_n(s) \end{bmatrix} = \begin{bmatrix} 1 & \frac{1}{N} & \frac{1}{N} & \cdots & \frac{1}{N} & \frac{1}{N} \\ 1 & -\frac{N-1}{N} & \frac{1}{N} & \cdots & \frac{1}{N} & \frac{1}{N} \\ 1 & \frac{1}{N} & -\frac{N-1}{N} & \cdots & \frac{1}{N} & \frac{1}{N} \\ \vdots & \vdots & \vdots & \ddots & \vdots & \vdots \\ 1 & \frac{1}{N} & \frac{1}{N} & \cdots & -\frac{N-1}{N} & \frac{1}{N} \\ 1 & \frac{1}{N} & \frac{1}{N} & \cdots & \frac{1}{N} & -\frac{N-1}{N} \end{bmatrix} \begin{bmatrix} \delta(s) \\ \Delta\delta_{12}(s) \\ \Delta\delta_{13}(s) \\ \vdots \\ \Delta\delta_{1n-1}(s) \\ \Delta\delta_{1n}(s) \end{bmatrix} \tag{3.77}$$

Current binding to Average

It is base on the idea that each control takes as a reference current the averaged branch current (properly scaled). Duty cycles error are expressed in the form $\Delta\delta_k(s)$. In order to not overpass N equations limit, one current should not be bounded with the average one (in the following, first leg current error has not been included in the system of equations).

Starting from the system below:

$$\begin{cases} \Delta\delta_2(s) = \delta(s) - \delta_2(s) = \frac{1}{N}\sum_{k=1}^{N}\delta_k(s) - \delta_2(s) \\ \Delta\delta_3(s) = \delta(s) - \delta_3(s) = \frac{1}{N}\sum_{k=1}^{N}\delta_k(s) - \delta_3(s) \\ \vdots \\ \Delta\delta_n(s) = \delta(s) - \delta_n(s) = \frac{1}{N}\sum_{k=1}^{N}\delta_k(s) - \delta_n(s) \end{cases} \tag{3.78}$$

that is equal to:

$$\begin{cases} \Delta\delta_2(s) = \frac{1}{N}\delta_1(s) - \frac{N-1}{N}\delta_2(s) + \frac{1}{N}\sum_{k=3}^{N}\delta_k(s) \\ \Delta\delta_3(s) = \frac{1}{N}\sum_{k=1}^{2}\delta_k(s) - \frac{N-1}{N}\delta_3(s) + \frac{1}{N}\sum_{k=4}^{N}\delta_k(s) \\ \vdots \\ \Delta\delta_n(s) = \frac{1}{N}\sum_{k=1}^{N-1}\delta_k(s) - \frac{N-1}{N}\delta_n(s) \end{cases} \tag{3.79}$$

Figure 3.17 provides a visual representation of the (3.78) case.

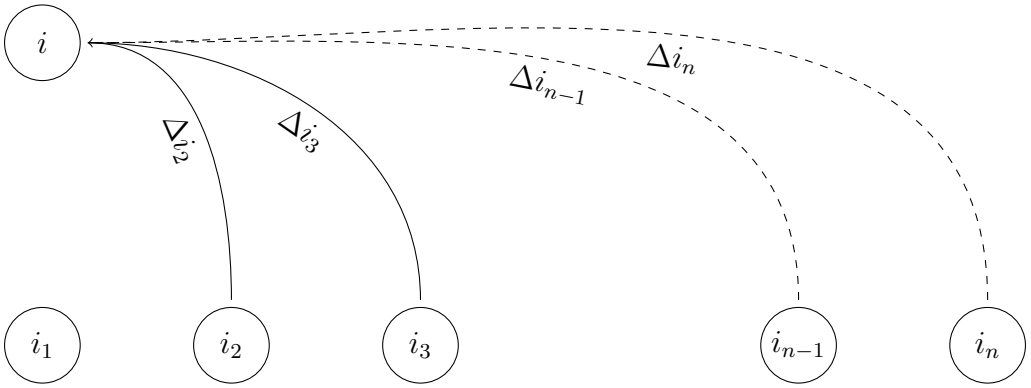


Figure 3.17: Currents binding to the averaged branch current

Attaching at the system (3.79) relation (3.71) it is possible write the following matrice equation:

$$\begin{bmatrix} \delta(s) \\ \Delta\delta_2(s) \\ \Delta\delta_3(s) \\ \vdots \\ \Delta\delta_{n-1}(s) \\ \Delta\delta_n(s) \end{bmatrix} = \begin{bmatrix} \frac{1}{N} & \frac{1}{N} & \frac{1}{N} & \cdots & \frac{1}{N} & \frac{1}{N} \\ \frac{1}{N} & -\frac{N-1}{N} & \frac{1}{N} & \cdots & \frac{1}{N} & \frac{1}{N} \\ \frac{1}{N} & \frac{1}{N} & -\frac{N-1}{N} & \cdots & \frac{1}{N} & \frac{1}{N} \\ \vdots & \vdots & \vdots & \ddots & \vdots & \vdots \\ \frac{1}{N} & \frac{1}{N} & \frac{1}{N} & \cdots & -\frac{N-1}{N} & \frac{1}{N} \\ \frac{1}{N} & \frac{1}{N} & \frac{1}{N} & \cdots & \frac{1}{N} & -\frac{N-1}{N} \end{bmatrix} \begin{bmatrix} \delta_1(s) \\ \delta_2(s) \\ \delta_3(s) \\ \vdots \\ \delta_{n-1}(s) \\ \delta_n(s) \end{bmatrix} \tag{3.80}$$

Computing the inverse matrix:

$$\begin{bmatrix} \delta_1(s) \\ \delta_2(s) \\ \delta_3(s) \\ \vdots \\ \delta_{n-1}(s) \\ \delta_n(s) \end{bmatrix} = \begin{bmatrix} 1 & 1 & 1 & \cdots & 1 & 1 \\ 1 & -1 & 0 & \cdots & 0 & 0 \\ 1 & 0 & -1 & \cdots & 0 & 0 \\ \vdots & \vdots & \vdots & \ddots & \vdots & \vdots \\ 1 & 0 & 0 & \cdots & -1 & 0 \\ 1 & 0 & 0 & \cdots & 0 & -1 \end{bmatrix} \begin{bmatrix} \delta(s) \\ \Delta\delta_2(s) \\ \Delta\delta_3(s) \\ \vdots \\ \Delta\delta_{n-1}(s) \\ \Delta\delta_n(s) \end{bmatrix} \tag{3.81}$$

Decoupled Current Approach

One could completely decouple one current from the others by exclusively assign the averaged duty cycle $\delta(s)$ to a specific leg's duty cycle $\delta_k(s)$ rather than follow the averaged approach shown in (3.71).

Considering k = 1-th leg as a reference current, one could state that:

$$\delta(s) = \delta_1(s) \tag{3.82}$$

It must be noticed that there is no needing to change the transfer function $Dpk_{pk}(s)$. Despite $D_k(s)$ has always been found following an averaged approach, it can be seen that it coincides with the single-leg transfer function in a balanced condition.

Assuming in a balanced condition that:

$$i_k(s) = \frac{i(s)}{N} \tag{3.83}$$

one could rewrite (3.56) as:

$$\begin{aligned} V_{DC}\delta(s) = Z'(s)i(s) + V_o(s) = \\ = Z(s)\frac{i(s)}{N} + V_o(s) = \\ = Z(s)i_k(s) + V_o(s) = V_{DC}\delta_k(s) \end{aligned} \tag{3.84}$$

Being leg equations (3.84) perfectly equal in both cases, also the transfer function $D_k(s)$ remains equal to $D_{pk}(s)$ regardless to what assumption (3.82) have been done.

Following the current sequential binding approach introduced in part 3.2.1, equations are slightly different.

Attaching at the still valid system of equations (3.72) relation (3.82) rebalancing network matrixs becomes:

$$\begin{bmatrix} \delta(s) \\ \Delta\delta_{12}(s) \\ \Delta\delta_{23}(s) \\ \vdots \\ \Delta\delta_{n-2n-1}(s) \\ \Delta\delta_{n-1n}(s) \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 & \cdots & 0 & 0 \\ 1 & -1 & 0 & \cdots & 0 & 0 \\ 0 & 1 & -1 & \cdots & 0 & 0 \\ \vdots & \vdots & \vdots & \ddots & \vdots & \vdots \\ 0 & 0 & 0 & \cdots & -1 & 0 \\ 0 & 0 & 0 & \cdots & 1 & -1 \end{bmatrix} \begin{bmatrix} \delta_1(s) \\ \delta_2(s) \\ \delta_3(s) \\ \vdots \\ \delta_{n-1}(s) \\ \delta_n(s) \end{bmatrix} \tag{3.85}$$

Computing the inverse matrix:

$$\begin{bmatrix} \delta_1(s) \\ \delta_2(s) \\ \delta_3(s) \\ \vdots \\ \delta_{n-1}(s) \\ \delta_n(s) \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 & \cdots & 0 & 0 \\ 1 & -1 & 0 & \cdots & 0 & 0 \\ 1 & -1 & -1 & \cdots & 0 & 0 \\ \vdots & \vdots & \vdots & \ddots & \vdots & \vdots \\ 1 & -1 & -1 & \cdots & -1 & 0 \\ 1 & -1 & -1 & \cdots & -1 & -1 \end{bmatrix} \begin{bmatrix} \delta(s) \\ \Delta\delta_{12}(s) \\ \Delta\delta_{23}(s) \\ \vdots \\ \Delta\delta_{n-2n-1}(s) \\ \Delta\delta_{n-1n}(s) \end{bmatrix} \tag{3.86}$$

It worth notice that having introduced assumption (3.82) made the two remaining approaches one equal to the other. The matrix equation used for describing these two cases becomes:

$$\begin{bmatrix} \delta(s) \\ \Delta\delta_2(s) \\ \Delta\delta_3(s) \\ \vdots \\ \Delta\delta_{n-1}(s) \\ \Delta\delta_n(s) \end{bmatrix} = \begin{bmatrix} \delta(s) \\ \Delta\delta_{12}(s) \\ \Delta\delta_{13}(s) \\ \vdots \\ \Delta\delta_{1n-1}(s) \\ \Delta\delta_{1n}(s) \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 & \cdots & 0 & 0 \\ 1 & -1 & 0 & \cdots & 0 & 0 \\ 1 & 0 & -1 & \cdots & 0 & 0 \\ \vdots & \vdots & \vdots & \ddots & \vdots & \vdots \\ 1 & 0 & 0 & \cdots & -1 & 0 \\ 1 & 0 & 0 & \cdots & 0 & -1 \end{bmatrix} \begin{bmatrix} \delta_1(s) \\ \delta_2(s) \\ \delta_3(s) \\ \vdots \\ \delta_{n-1}(s) \\ \delta_n(s) \end{bmatrix} \tag{3.87}$$

Computing the inverse matrix:

$$\begin{bmatrix} \delta_1(s) \\ \delta_2(s) \\ \delta_3(s) \\ \vdots \\ \delta_{n-1}(s) \\ \delta_n(s) \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 & \cdots & 0 & 0 \\ 1 & -1 & 0 & \cdots & 0 & 0 \\ 1 & 0 & -1 & \cdots & 0 & 0 \\ \vdots & \vdots & \vdots & \ddots & \vdots & \vdots \\ 1 & 0 & 0 & \cdots & -1 & 0 \\ 1 & 0 & 0 & \cdots & 0 & -1 \end{bmatrix} \begin{bmatrix} \delta(s) \\ \Delta\delta_{12}(s) \\ \Delta\delta_{13}(s) \\ \vdots \\ \Delta\delta_{1n-1}(s) \\ \Delta\delta_{1n}(s) \end{bmatrix} \tag{3.88}$$

Moreover, it worth notice that the system described with (3.87) and (3.88) employs an involutory matrix.

Furthermore, care must be dedicated to saturate legs' current error not to overcome power capability on trying to compensate strong unbalances or a faults. Duty cycles δ_k are a linear combination of δ and all the $\Delta\delta$. Rebalancing network may be able to guarantee the total current i even in case of legs disconnection. However, this may lead to damages and early aging on the active legs. In Chapter 4, sequential binding on a three-phase power block has been considered.

Current Subgrouping Approach

Especially in three-phase modular applications, it is possible to define multiple current subgroups and reference currents on each subgroup as first rebalancing action. Furthermore, one could introduce a secondary rebalancing action that must be able to link one another each subgroup. One could divide the N leg's current into subgroups and apply one of the approach mentioned above (even different approach in different groups). These subgroups are tied together using a secondary rebalancing action following the same approach shown before. No analytical computations are provided. In Figure 3.18, it is possible to see a drawing representing one possible grouping approach.

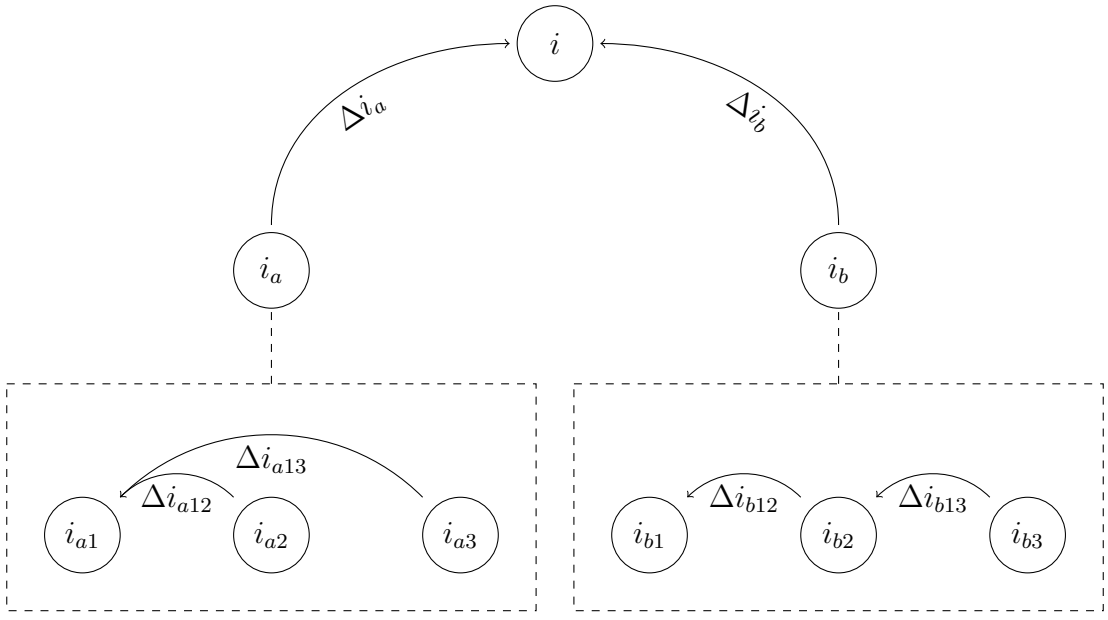


Figure 3.18: Subgroups current bounding with different involved approaches

3.2.2 Rebalancing Action and Ripple-Free Strategy

Rebalancing network could correctly work regardless of what averaged duty cycles is being provided at its input. Thanks to this ductility, one could feed the rebalancing network with δ computed by the ripple-free mask rather than the one directly computed by the averaged main controller.

However, it must be noticed that the ripple-free mask represents a SISO system. Meanwhile, the rebalancing network represents a Multiple Inputs, Multiple Outputs (MIMO) system. It is, therefore, necessarily extend ripple-free mask capability when it comes after the rebalancing network.

A possible solution is to feed (2.26) and (2.27) with $V_o^* = \delta V_{DC}$, employing, therefore, the averaged duty cycles (regardless of how it have been computed) for the V_{DC} reselection. Each actual duty cycle δ_k (provided by the rebalancing network) is used for feeding (2.28) and compute the discrete duty cycles able to guarantee ripple-free operations in steady-state.

However, having different duty cycles could make harder reaching ripple-free operations. As explained in section 2.2 any duty cycle displacement respect with the ideal discrete value is in any case minimized by the interleaving configuration. In Figures 3.19 and 3.20, two possible configuration able to join both rebalancing and ripple minimization effects are shown.

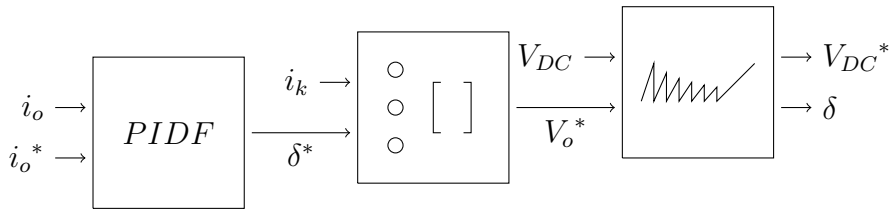


Figure 3.19: Possible joining scheme having rebalancing control network upstream the ripple free computation

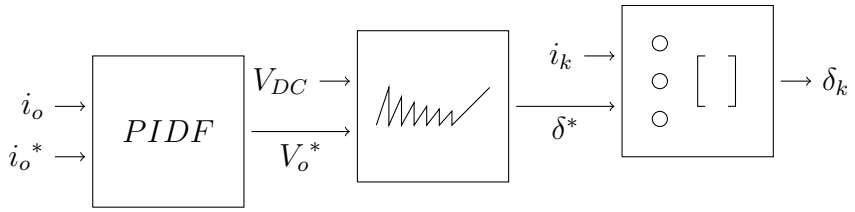


Figure 3.20: Possible joining scheme having rebalancing control network downstream the ripple free computation

The rebalancing network explained in this chapter could be used on IAR input side by computing a similar calculation on the N_b actual Park's current framework.

3.3 PWM Generation and Current Sampling

As shown in Figure 1.4, the carrier is implemented throughout multiple triangular waveforms. Utilizing a proper link between sampling time and carrier, one could

always sample the average current I in each leg. This practice always ensures a measurement without the error introduced by the ripple $\Delta I(t)$.

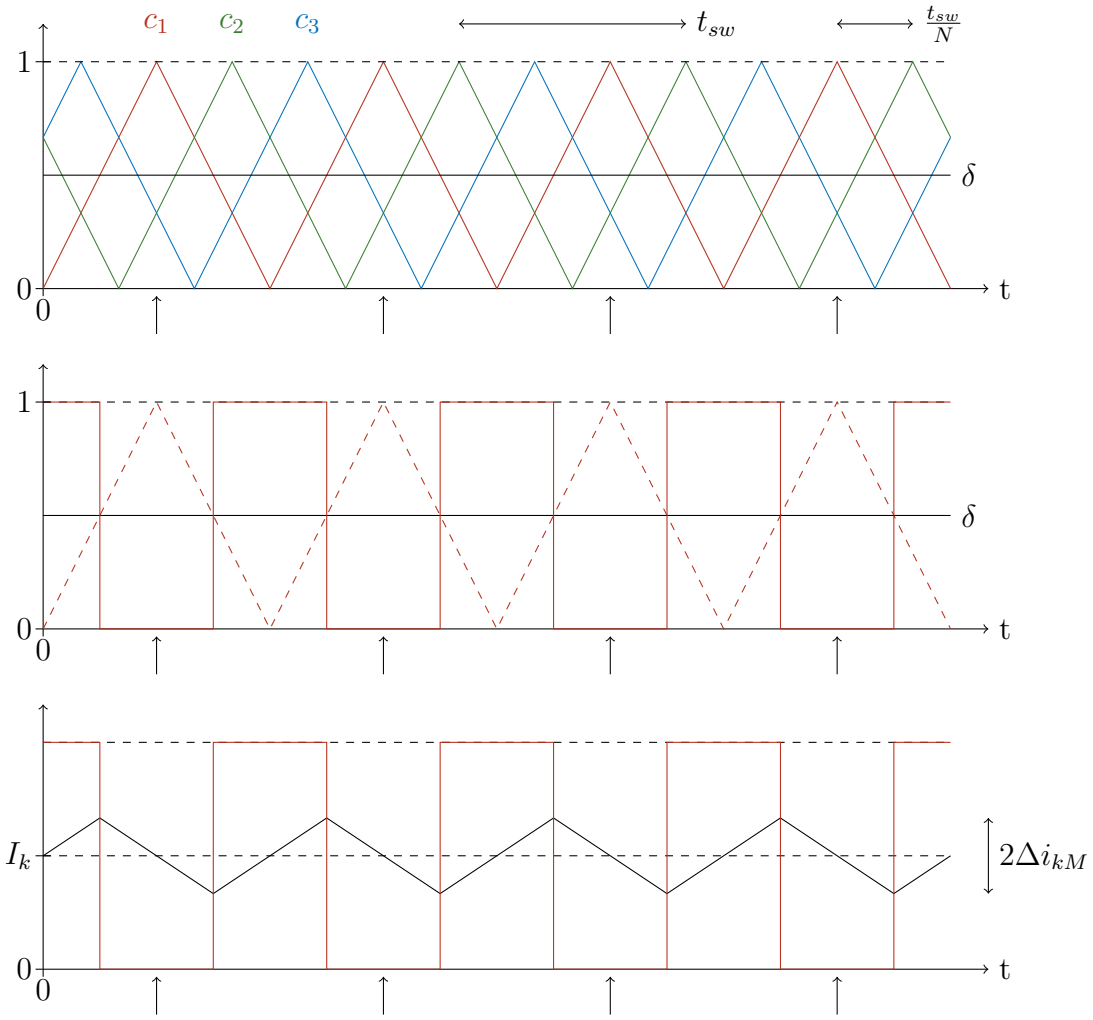


Figure 3.21: Drawing that shows $N = 3$ shifted carriers (c_1, c_2, and c_3) and the PWM generated from generic modulating signal $\delta = 0.5$. The current medium point sampling time is linked with the respective carrier.

As visible in Figures 3.21 and 3.22, sampling each current on the top or bottom carriers peaks guarantees that the sample and hold (S&H) always hits the average value I. Since carriers are evenly shifted, newer currents values are acquired every t_{sw}/N even though each leg's current is sampled every t_{sw}. In order to take advantage of the full rate of refresh, it is necessary executing the complete current control with a frequency of Nf_{sw}. New SiC based power switch solution may employ switching frequency in the order of about $100kHz$. Therefore, as the number of legs increase, as faster the digital system should be. Solution based on FPGA technology may provide the most satisfying outcomes. However, thanks to the slow varying feature of the charging dynamics, one could undersample the current and execute the whole control process with frequency even lower than f_{sw}. Furthermore, taking advantage of both carrier's peaks, it is possible to doubly the rate of update of each leg and on the whole system.

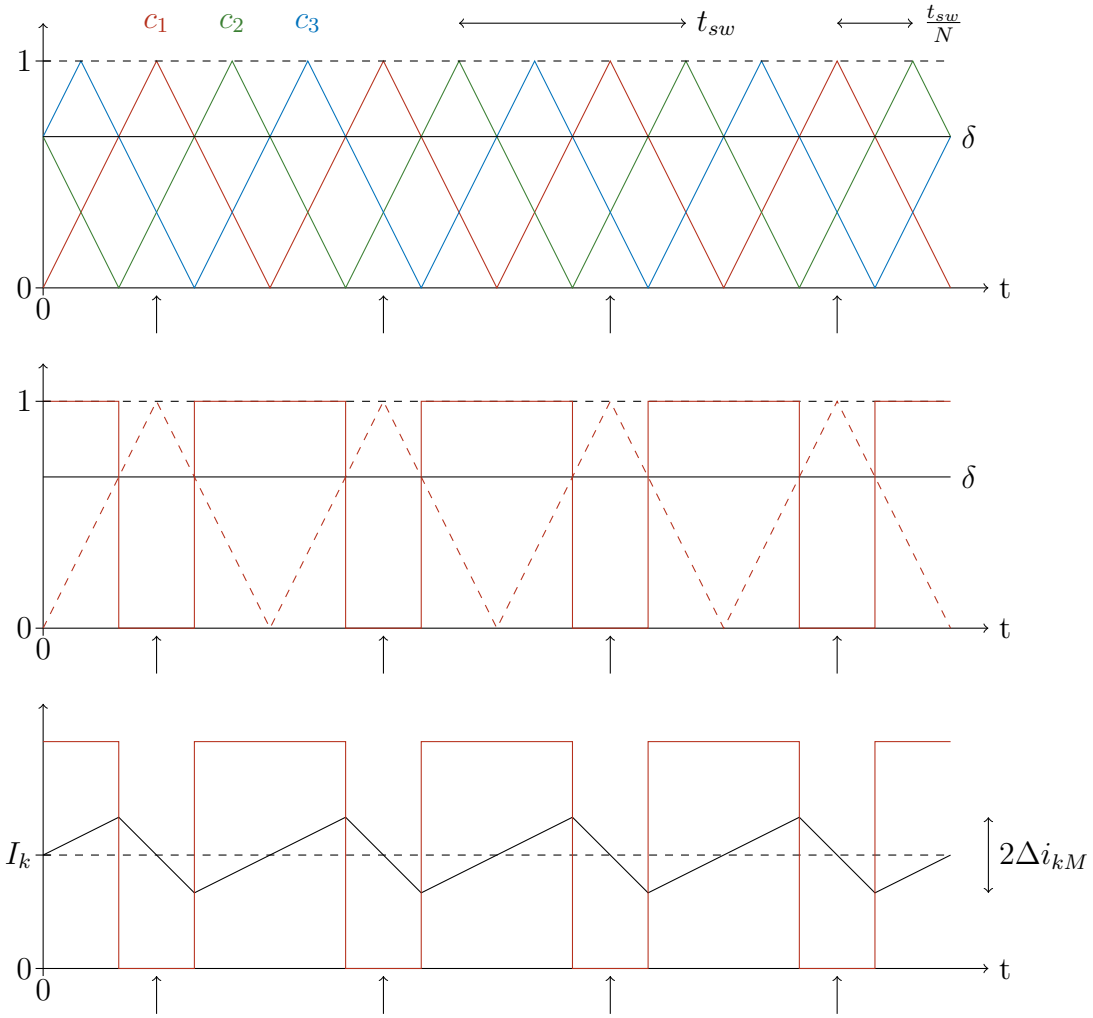


Figure 3.22: Drawing that shows $N = 3$ shifted carriers (c_1, c_2, and c_3) and the PWM generated from generic modulating signal $\delta = 2/3$. The current medium point sampling time is linked with the respective carrier.

Chapter 4

Simulations and Measurements

Multiple simulations and measurements have been done on the whole area of the proposed topology. All the assumption carried out in the previous chapter have been verified numerically. The simulation environment used is MATLAB Simulink. Experimental tests have been done in Solartronic-Lab at University of Bologna.

With reference to the simulation results, following list have been carried out:

- IAR's input currents ripple reduction;
- IBC's output current ripple reduction;
- IBC's output current ripple cancellation;
- ripple-free strategy total output current ripple cancellation;
- ripple-free transients;
- control equivalent IBC;
- mean value sampling strategy;
- precharge current staircase;
- current rebalancing network.

Concerning experimental measurements, the following tests have been performed:

- averaged main control step response;
- averaged main control robustness;
- current rebalancing network;
- current rebalancing in unbalanced system.

4.1 IAR Simulation

The simulation performed concerning IAR's variables has been carried out on the grid input current ripple measurement. Simulation parameters are listed in Table 4.1.

Table 4.1: IAR simulations parameters

Parameter	Symbol	Value	Unit
Number of legs per base block	N_b	3	
Number of block per side	M_s	3	
DC link voltage	V_{DC}	700	V
Switching frequency	f_{sw}	16	kHz
Reactors inductance	L	0.5	mH
Reactors resistance	R	20	$m\Omega$
Line to line RMS voltage	V_g	400	V
Switching frequency	f	50	Hz

The solver parameters used in the simulation are presented in Table 4.2.

Table 4.2: IAR simulations settings

Parameter	Value	Unit
Simulation time	0.2	s
Simulation type	Fixed step	
Solver	ode4 Runge-Kutta	

4.1.1 IAR's Input Currents Ripple Reduction

Figure 4.2, shows grid current ripple for a standard three-phase active rectifier.

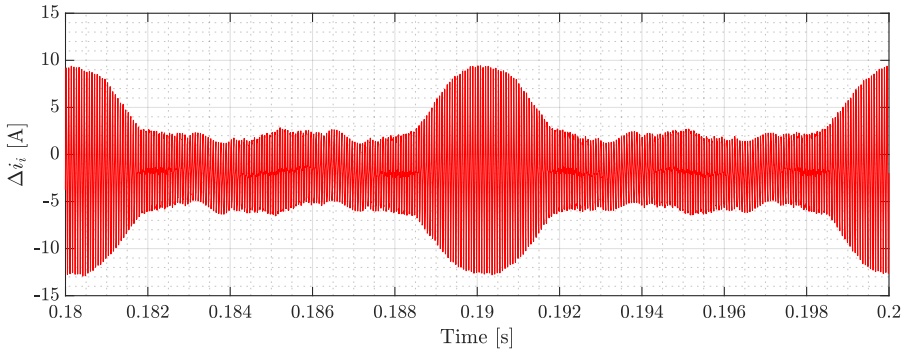


Figure 4.1: Grid current ripple without interleaving conditions

Meanwhile, Figure 4.1, shows grid current ripple due to an interleaved three-phase active rectifier with three legs per phase. As visible, interleaved topology leads to relevant ripple reduction.

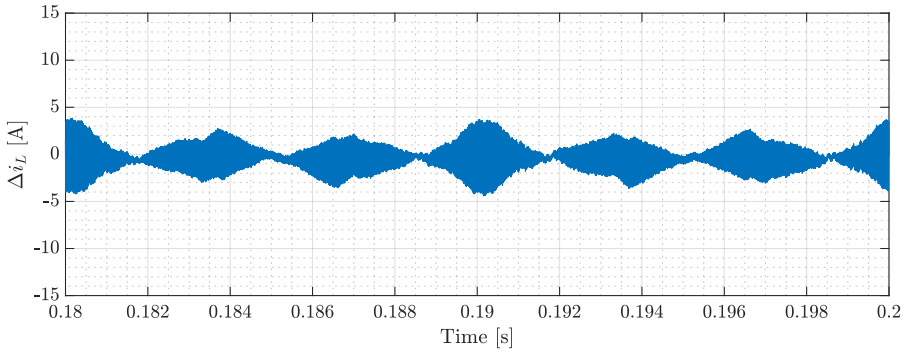


Figure 4.2: Grid current ripple in interleaving connections

4.2 IBC Simulations

Multiple simulations involving IBC's variables have been performed. Most of the simulations share the parameters listed in Table 4.3.

Table 4.3: IBC simulations parameters

Parameter	Symbol	Value	Unit
Number of legs	N	9	
DC link voltage	V_{DC}	800	V
Switching frequency	f_{sw}	16	kHz
Reactors inductance	L	0.5	mH
Reactors resistance	R	20	$m\Omega$
Resistive load	R_l	6	Ω

The solver parameters used in the simulations are presented in Table 4.4.

Table 4.4: IBC simulations settings

Parameter	Value	Unit
Simulation time	6	s
Simulation type	Fixed step	
Solver	ode3 Bogacki-Shampine	

4.2.1 IBC's Output Current Ripple Reduction

In order to emphasize ripple reduction capability, simulation have been implemented using $\delta = 7.5/9 \approx 0.83$ that is one of the worse points shown in Figure 1.30.

Computing Δi_{kM} by mean of (1.46) the expected ripple maximum is around $6.95A$. As visible in Figure 4.3, the simulation confirms this statement. The triangular waveform approximately ranges between $5.5A$ and $19.5A$, having as mean value $12.5A$.

Moreover, Figure 4.4, shows that ripple free conditions have not been reached, as expected. However,a strong ripple reduction in the $i(t)$ is introduced by mean of the interleaving topology. Furthermore, $i(t)$ repeates with a frequency $N = 9$ times higher than $i_k(t)$.

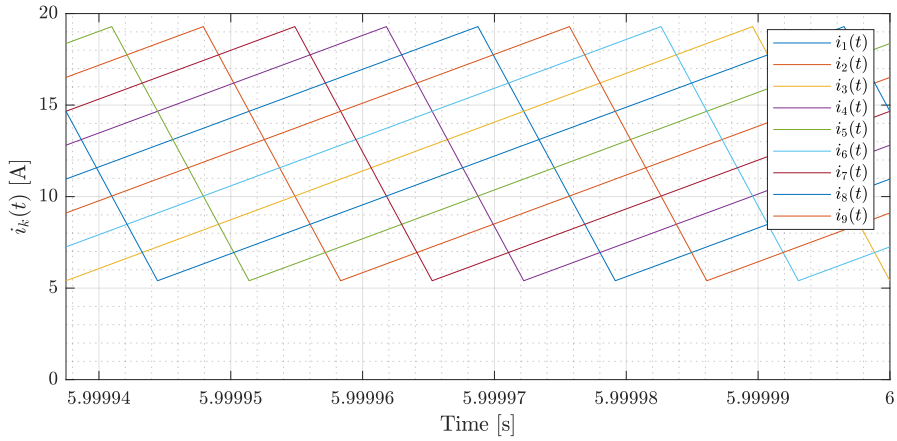


Figure 4.3: Leg's currents $i_k(t)$ in case of $\delta = 7.5/9$ (outside ripple cancellation conditions) with purely inductive coupling reactors

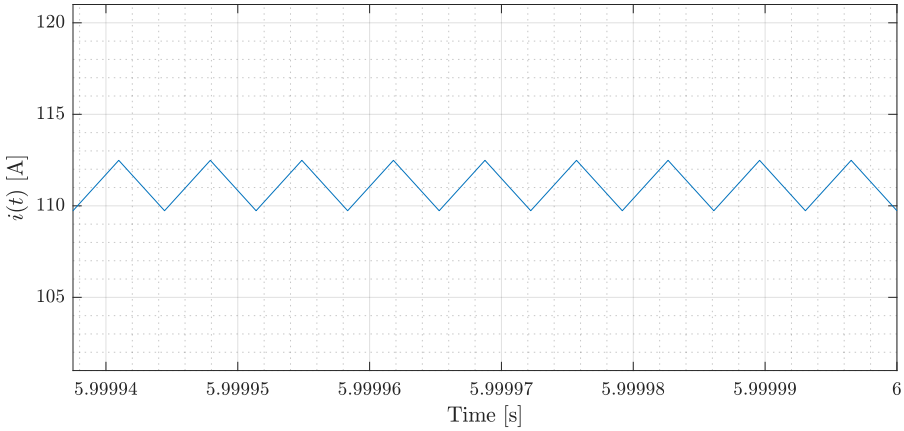


Figure 4.4: Total output current $i(t)$ in case of $\delta = 7.5/9$ (outside ripple cancellation conditions) with purely inductive coupling reactors

4.2.2 IBC's Output Current Ripple Cancellation

Simulations have been set on one of the ripple cancellation points visible in Figure 1.31. Being $N = 9$, selecting $\delta = 8/9$ guarantees the total ripple cancellation. Simulation has been done on a fully inductive model since, as shown before, no relevant errors are introduced by this assumption.

Computing Δi_{kM} by mean of (1.46) the expected ripple maximum is of around $4.9A$. As visible in Figure 4.5, the simulation confirms this statement. The triangular waveform approximately ranges between $8A$ and $18A$, having as mean value $13A$. As expected leg's ripple have been reduced if compared to previous case (subsection 4.2.1).

Moreover, Figure 4.6, shows that ripple free conditions have been reached. Conversely to what seen in Figure 4.4 current $i(t)$ has a completely flat profile.

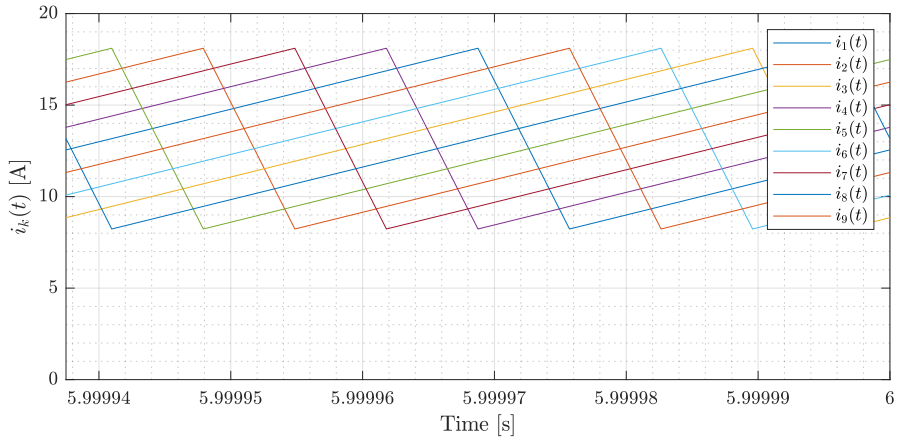


Figure 4.5: Leg's currents $i_k(t)$ in ripple cancellation conditions with purely inductive coupling reactors

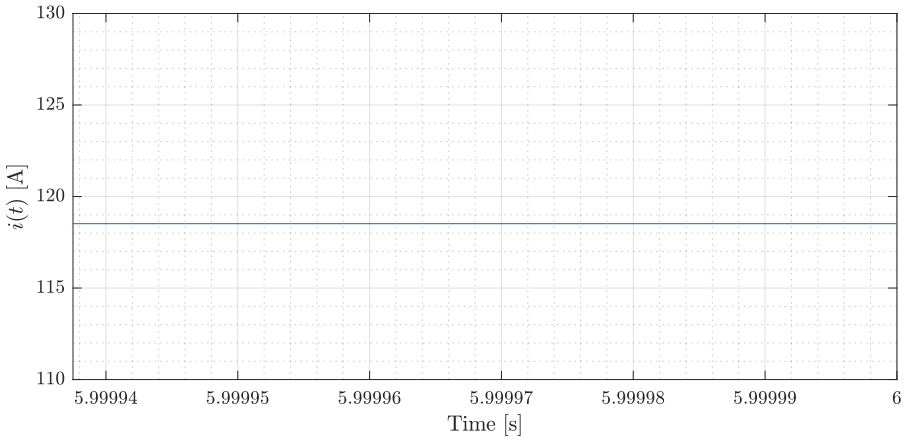


Figure 4.6: Total output current $i(t)$ ripple cancellation with purely inductive coupling reactors

4.2.3 Equivalent IBC for Control Purposes

In order to verify that the assumptions made in section 3.1 are correct, two simulation results involving the actual IBC and the equivalent IBC have been compared. In Table 4.5 simulation parameters have been collected.

It can be easily demonstrated that the actual IBC having $V_{DCr} = 1000V$, driven at $\delta_r = 1/2$ feeding a battery having $V_{bat} = 400V$ and $R_l = 5\Omega$ produces an average current:

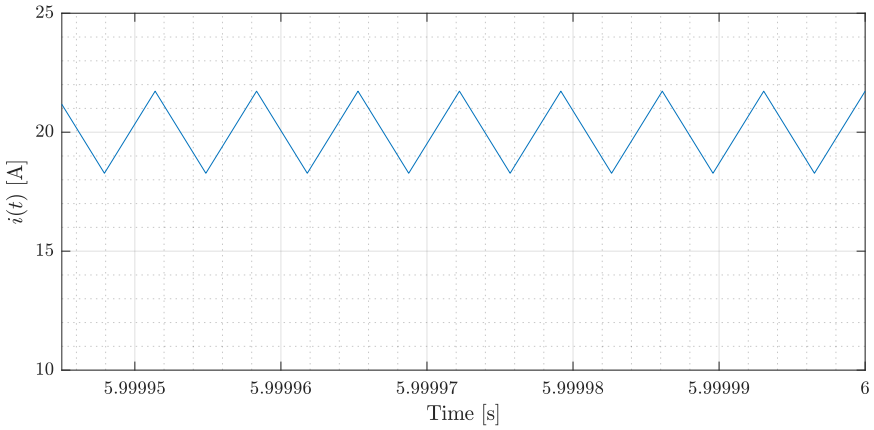
$$I = \frac{V_{DCr}\delta_r - V_{bat}}{R_l} = 20A \tag{4.1}$$

By mean of (3.3) and (3.5) it is possible set parameters for the equivalent IBC. Setting $V_{DC} = 600V$, δ becomes:

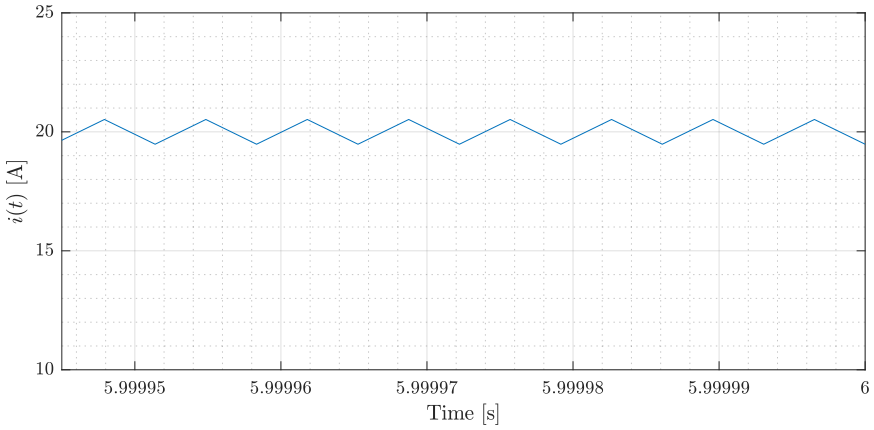
$$\delta = (\delta_r - \frac{V_{bat}}{V_{DCr}})\frac{V_{DCr}}{V_{DC}} = \frac{1}{6} \tag{4.2}$$

Table 4.5: Actual and equivalent IBC simulations settings

Parameter	Symbol	Actual IBC	Equivalent IBC	Unit
Number of legs	N	9	9	
DC link voltage	V_{DCr}, V_{DC}	1000	600	V
Duty cycle	δ_r, δ	$\frac{1}{2}$	$\frac{1}{6}$	
Switching frequency	f_{sw}	16	16	kHz
Reactors inductance	L	1	1	mH
Internal FEM	V_{bat}	400	N/A	V
Internal resistance	R_l	5	5	Ω

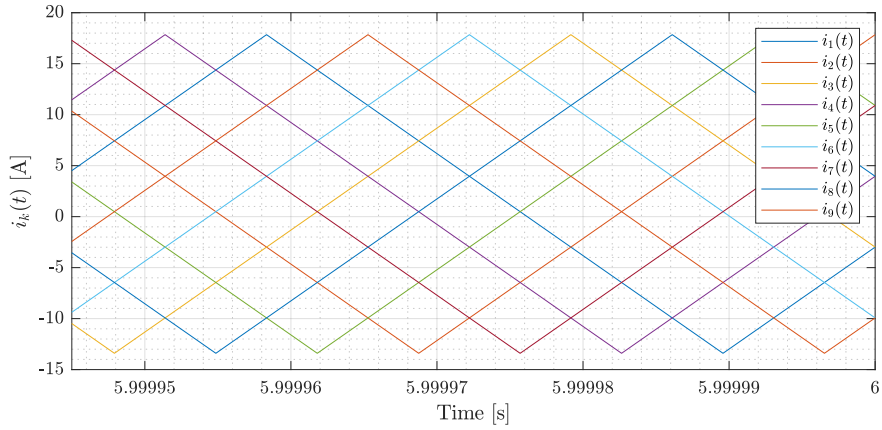


(a) Current i in the actual IBC output

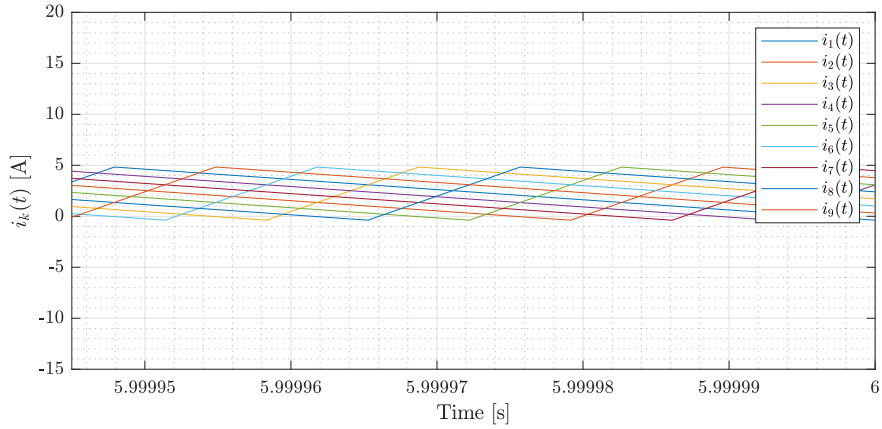


(b) Current i in the equivalent IBC output

Figure 4.7: IBCs output current comparison



(a) Actual IBC legs' currents i_k



(b) Equivalent IBC legs' currents i_k

Figure 4.8: IBCs legs' currents comparison

The current on the R_l is therefore:

$$I = \frac{V_{DC}\delta}{R_l} = 20A \tag{4.3}$$

As visible in Figure 4.7a and Figure 4.7b both currents have the same average value. However, it must be noticed that has deeply changed the IBC's parameters from the actual to the equivalent the current ripple in the branches and on the output currents are considerably different in the two cases. Figure 4.8 shows current ripple amplitude variation. As mentioned above, this equivalent IBC must be considered average current invariant only.

4.3 Ripple-Free Strategy Simulations

Multiple simulation involving IBC's under a ripple-free strategy have been performed. All the simulation share the parameters listed in Table 4.6.

Table 4.6: Ripple-free strategy simulations parameters

Parameter	Symbol	Value	Unit
Number of legs	N	9	
Minimum DC link voltage	V_{DCm}	600	V
Switching frequency	f_{sw}	16	kHz
Reactors inductance	L	0.5	mH
Resistive load	R_l	6	Ω

The solver parameters used in the simulations are presented in Table 4.7.

Table 4.7: Ripple-free strategy simulations settings

Parameter	Value	Unit
Simulation time	6.4 and 1.4	s
Simulation type	Fixed step	
Solver	ode3 Bogacki-Shampine	

4.3.1 Ripple-Free Strategy Total Output Current Ripple Cancellation

In this simulation, ideal DC-link has been assumed (no transients when V_{DC} changes) with the only purpose to test the ripple-free strategy correctness. Equations (2.26) and (2.27) have been introduced inside the ripple-free mask. The strategy is fed with a continuous ramp between $200V$ and $600V$.

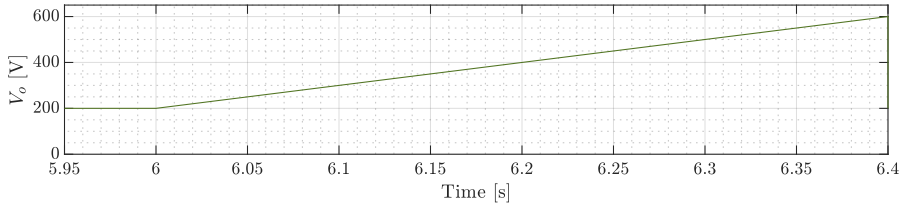
4.3.2 Ripple-Free Transients

As already shown in Section 2, during transient DC-link needs time for reaching the new value. At the same time ripple-free strategy keeps on tracking (when possible) the reference signal V_o^*. In this section, steps and ramps are performed.

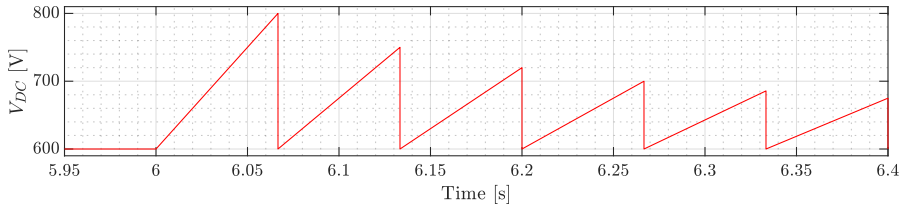
Continuous Ramp between $200V$ and $600V$

As explained in Chapter 2, when $V_o^* \geq V_{DCm}$ IBC enters in a overmodulation area where the output voltage reference can not be tracked anymore. In order to show the duty cycle recomputations, according to the V_{DC} actual value, a ramp from V_{om} to $V_o = V_{DCm}$ is performed.

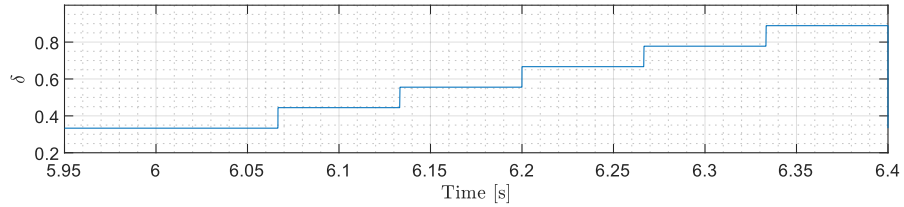
Comparing Figure 4.10 with Figure 4.9, it is possible to notice that the V_{DC} transients introduce variation on the variables. Focusing on Figure 4.10b, it is possible notice that $V_{DC}(t)$ is able to replicate the diagonal paths visible in 4.9. However, it must be pointed out that these paths last considerably less than what ideally expected. This delay passing from a path to the other depends on the V_o^*



(a) Output voltage V_o evolution

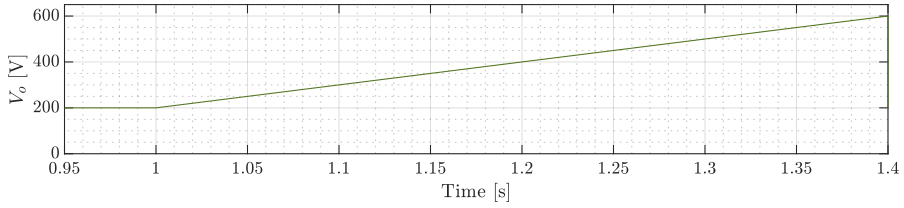


(b) DC link voltage V_{DC} evolution

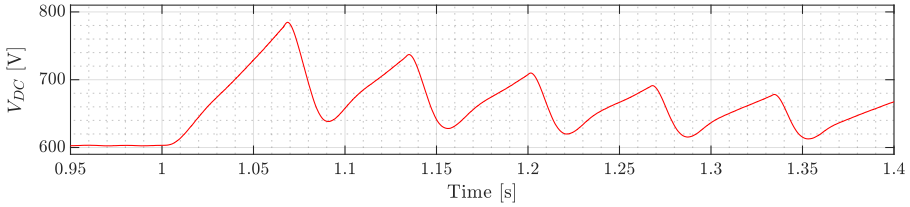


(c) Duty cycle δ evolution

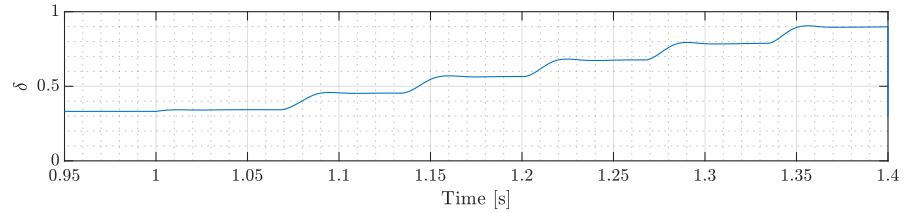
Figure 4.9: Voltage ramp ripple-free tracking variables evolution with an ideal DC link



(a) Output voltage V_o evolution



(b) DC link voltage V_{DC} evolution



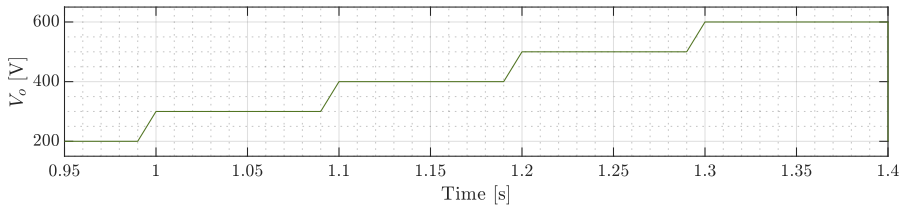
(c) Duty cycle δ evolution

Figure 4.10: Voltage ramp ripple-free tracking variables evolution

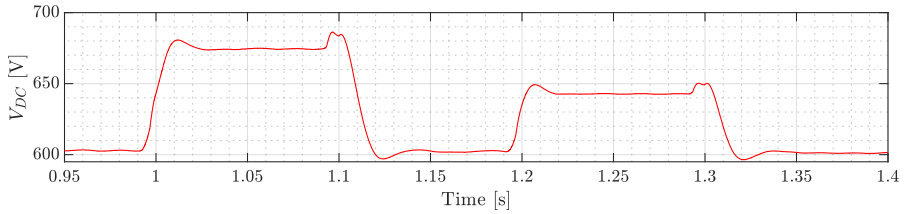
ramp slope. Longer ramps might give enough time to the DC BUS for resetting its value and have variable evaluations more similar to what depicted in Figure 4.9. Focusing on $\delta(t)$ (Figure 4.10c) one could notice that steady-state discrete values are reached without a sudden step as drawn in Figure 4.9c. This delay is due to the transient necessary for going from the highest V_{DC} value on each piece of path to V_{DCM}. However, as emphasized before, V_{DCM} is never reached.

Staircase between $200V$ and $600V$

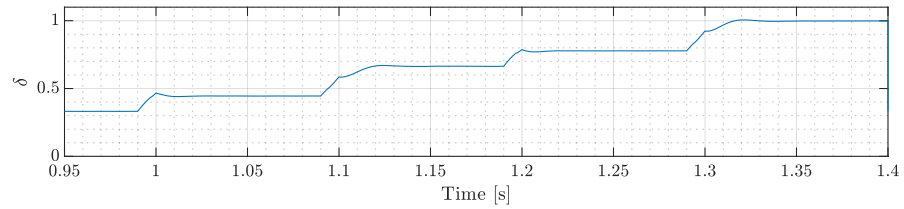
Similarly to what done in Part 4.3.2 the whole span $[200; 600]V$ have been ranged by mean of a voltage staircase with steps height $100V$ every $0.1s$. However, it should be pointed that it has not been used an ideal staircase. Indeed, vertical fronts last $10ms$. Steps too steep might produce powerful overshoots and saturate both V_{DC} and δ. As seen before, the whole simulation takes $1.4s$. If compared with Figure 4.10, multiple differences on the variables behaviours can be spotted in Figure 4.11. Every voltage step introduces positive and negative overshoots. Every overshoot is linked to δ transient with an inversely proportional evolution. Different tuning on IAR controllers might improve the response of the V_{DC} variation.



(a) Output voltage V_o evolution



(b) DC link voltage V_{DC} evolution



(c) Duty cycle δ evolution

Figure 4.11: Voltage steps ripple-free tracking variables evolution

4.4 General Control Strategy Simulations

Most of the assumption done in Chapter 3 have been verified trough out simulations. All the simulation have involved the equivalent IBC and have considered three legs only. All the simulation share the parameters listed in Table 4.6. The solver

Table 4.8: General control strategy simulations parameters

Parameter	Symbol	Value	Unit
Number of legs	N	3	
DC link voltage	V_{DC}	600	V
Switching frequency	f_{sw}	20	kHz
Sampling frequency	f_s	60	kHz
Reactors inductance	L	0.3	mH
Reactors resistance	R	0	Ω
Filter capacitance	C	16	μF
Filter ESR	R	0	Ω
Resistive load	R_l	4	Ω

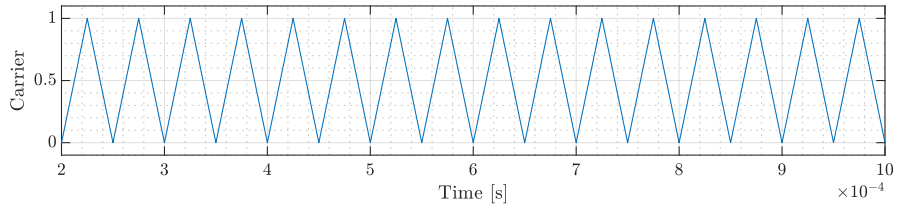
parameters used in the simulations are presented in Table 4.9.

Table 4.9: General control strategy simulations settings

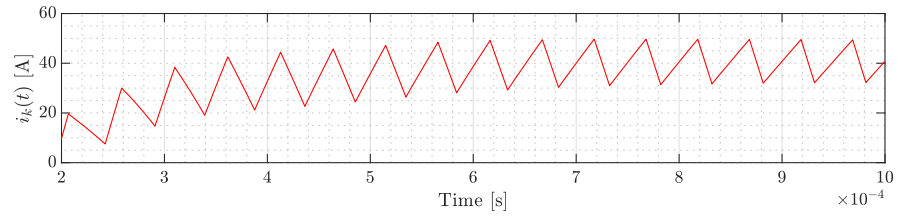
Parameter	Value	Unit
Simulation time	0.1	s
Simulation type	Variable step	
Solver	ode45 Dormand-Prince	

4.4.1 Mean Value Sampling Strategy

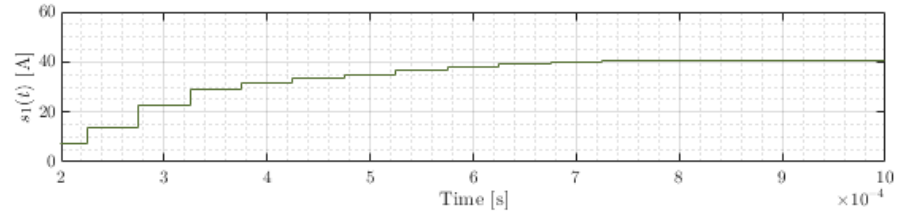
As explained in Section 3.3, carrier have been used for sampling the legs' currents average value without picking up the current ripple and avoiding further computations or filtering.



(a) First leg carrier



(b) First leg current evolution



(c) First leg sampled current evolution

Figure 4.12: Sampling strategy on the first leg

As visible in Figure 4.12, linking the sampling time to the upper peak of the carrier (Figure 4.12a) makes possible sampling the leg's average current $I_k(t)$ without incurring in the ripple visible in Figure 4.12b. Moreover, as shown in Fig 3.22, linking the sampling time to the top peak produces a current sample in the negative slope of the $i_k(t)$ triangular waveform.

Figure 4.13 shows the time evolution of all the legs' currents in the equivalent IBC. As mentioned above, despite the sampling (Table 4.8) occurs with a frequency of $20kHz$, the whole rate of refresh is three-time faster.

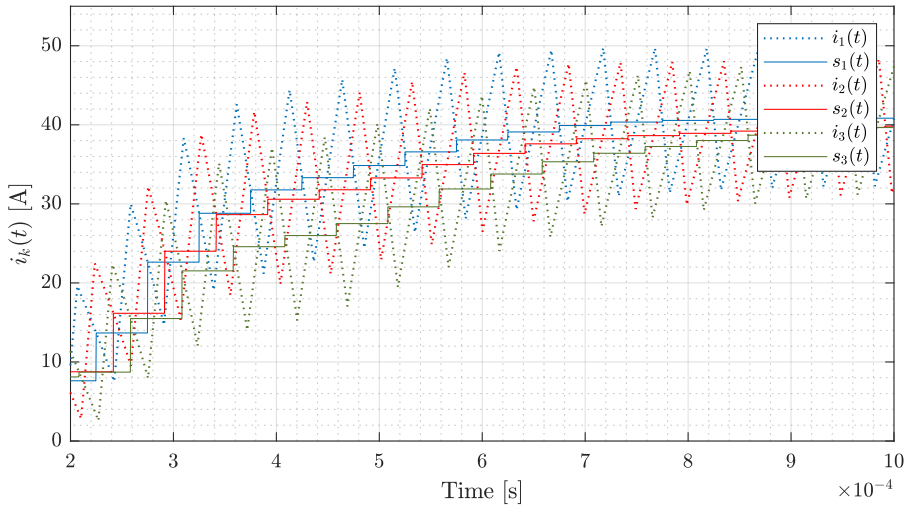


Figure 4.13: Real and sampled equivalent IBC legs' currents evolution in time

4.4.2 Precharge Current Staircase

As shown in Figure 3.11, a current preliminary staircase may be considered. As it can be seen in Figure 4.14 multiple steps of $10A$ have been performed for reaching the final steady-state current value. No oscillating response is noticed.

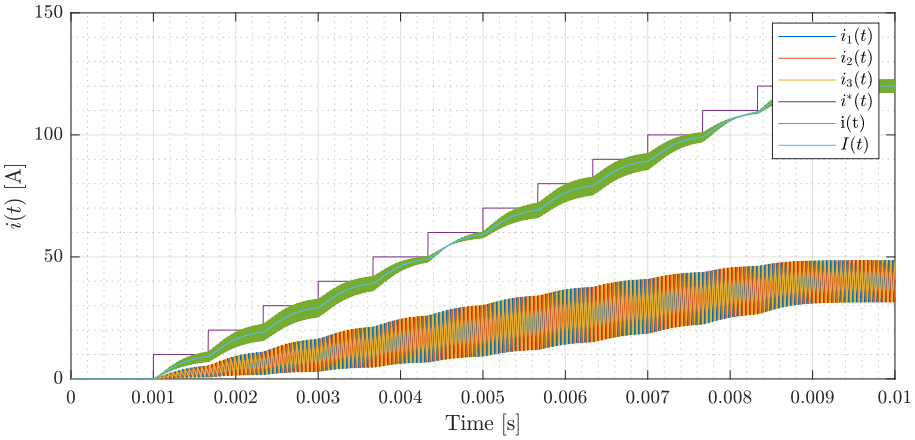


Figure 4.14: Currents evolution on a precharge staircase

4.4.3 Current Rebalancing Network

Current rebalancing network introduced in section 3.2 has been implemented in two forms. The first test has been carried out using the current sequential binding approach. Meanwhile, the second test employees the decoupled approach involving the involutory matrix introduced in (3.87) and (3.88). In both cases, one of the legs has been unbalanced by adding a 1Ω resistor.

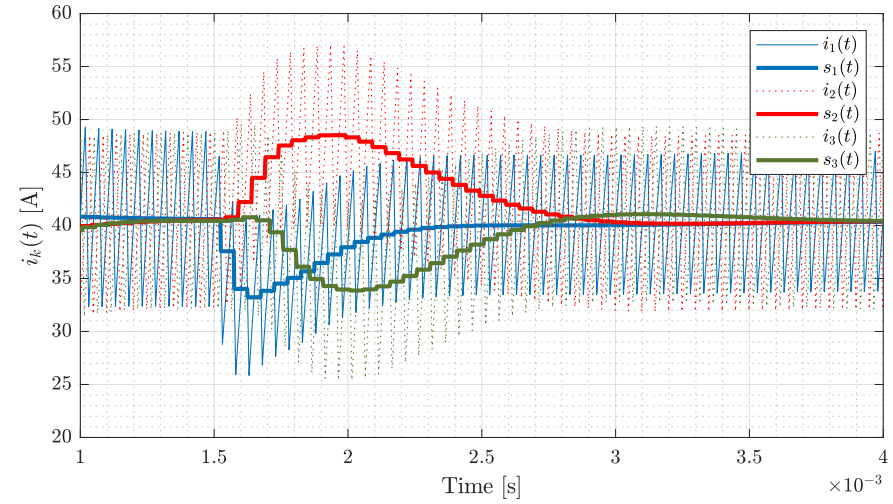
Current Sequential Binding

As visible in Figure 4.15, the unbalance happens at $t = 1.5ms$. The first leg increases its impedence and as a first effect there is a drop in the current $i_1(t)$ (displayed with blue waveforms in Figure 4.15a). As visible in Figure 4.15c, the total current $i(t)$, suddenly drop. After $200\mu s$ a proper rebalancing effect can be seen. Both controllers adjust duty cycles of second and third legs trying to nullify the current error among them. As expected, unbalanced leg increases the duty cycle and it remains constant around a value higher than the one computed before the fault. After different evolutions lasting $1.5ms$, δ_2 and δ_3 stabilize to the working point comouted before the unbalance. It is worth noticing that having defined duty cycles displacements $\Delta\delta$ using two different reference currents (even thought the transfer function has not changed) introduces different rebalancing controllers responses.

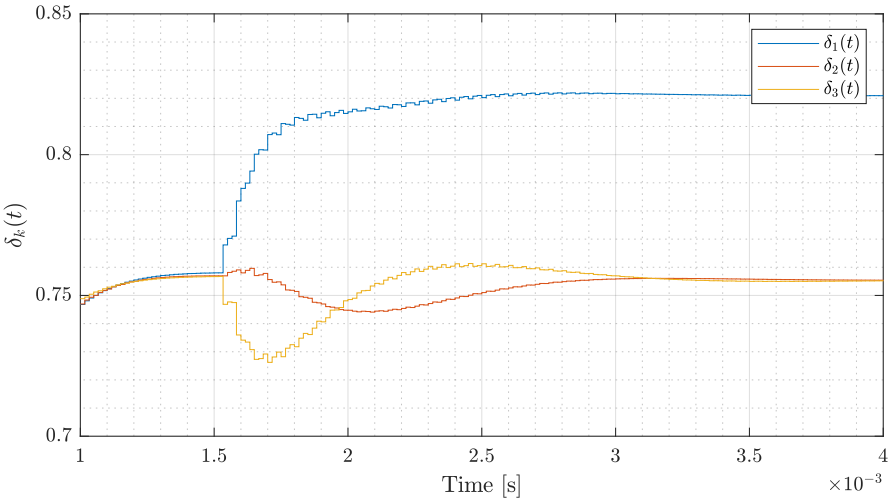
Furthermore, since δ_1 has grown, the ripple in the first leg is not anymore equal as the one of the remaining legs. Having δ_1 moved closer to one of the discrete duty cycle introduced in Chapter 2, maximum ripple $\Delta i_{1M}(t)$ decreased. This ripple displacement produces an irregular ripple profile in $i(t)$ (Figure 4.15c) after the clearance of the unbalance. Current ripple $i_1(t)$ envelope is completely surrounded inside $i_2(t)$ and $i_3(t)$ current envelopes.

Decoupled Approach

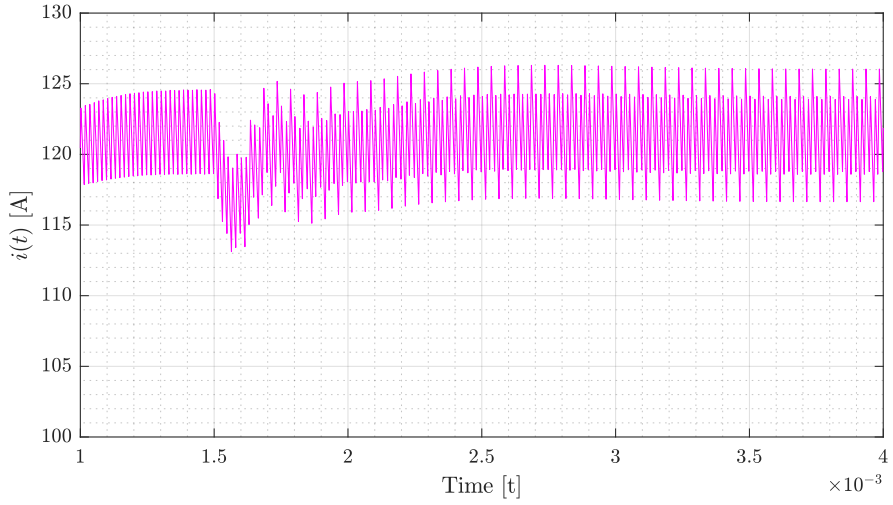
Similarly to the previous case, having increased the impedance on the second leg produces a sudden drop in the current $i_2(t)$ (Figure 4.16c). However, since both duty cycles displacements $\Delta\delta$ have been bounded to the first leg, the answers produced by rebalancing controllers are perfectly matching and are overlapping one another (Figure 4.16a). No relevant differences in the unbalance compensation time have been introduced with this second approach.



(a) Legs' currents $i_k(t)$ evolution

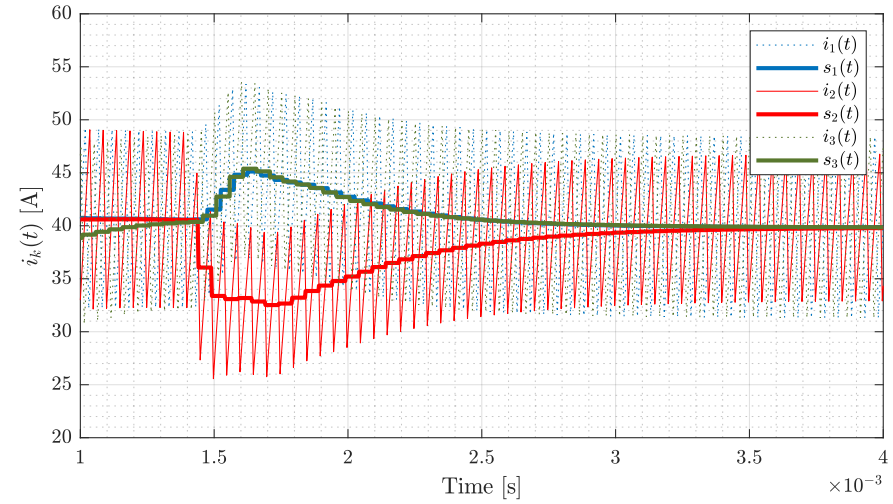


(b) Duty cycles $\delta_k(t)$ recomputation

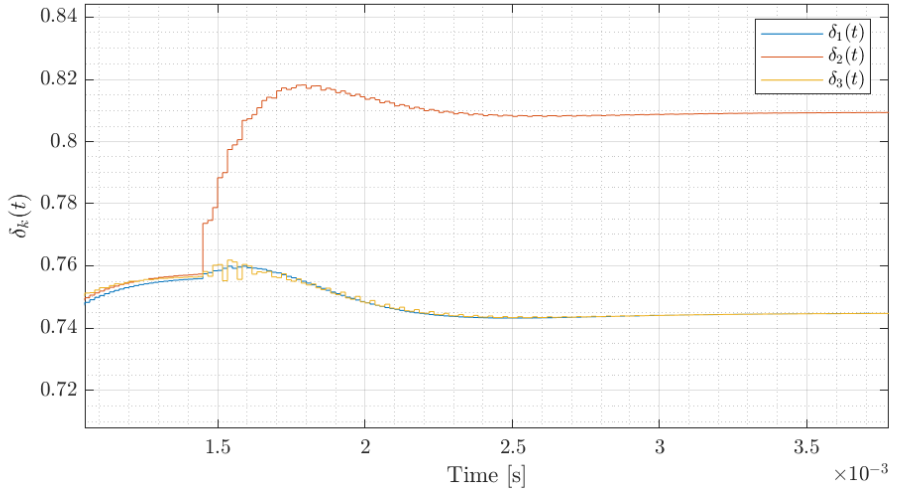


(c) Output current $i(t)$ evolution

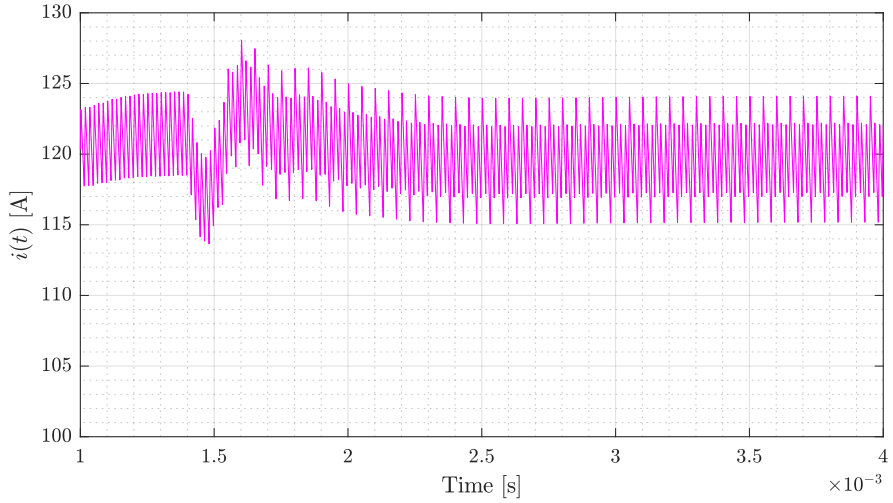
Figure 4.15: Currents rebalancing after employing the current sequential binding approach



(a) Legs' currents $i_k(t)$ evolution



(b) Duty cycles $\delta_k(t)$ recomputation



(c) Output current $i(t)$ evolution

Figure 4.16: Currents rebalancing after employing decoupled binding to first leg approach

4.5 Experimental Measurement

The configuration described in Part 4.2.3 (collected in Table 4.10) have been used for carrying out experimental measurement. The setup has been implemented in the University Laboratory. The instruments used for acquiring the findings shown below are listening in Table 4.11.

Table 4.10: Single module three-phase testing bench parameters

Parameter	Symbol	Value	Unit
Number of legs per side	N	3	
DC link voltage	V_{DC}	90	V
Switching frequency	f_{sw}	20	kHz
Sampling frequency	f_s	60	kHz
A/D resolution	M	12	bit
Reactors inductance	L	1	mH
Reactors resistance	R	900	$m\Omega$
Filter capacitance	C	16	μF
Filter ESR	R_C	900	$m\Omega$
Resistive load	R_l	6	Ω

Table 4.11: Devices employed for the experimental measurements

Device	Model
Oscilloscope	YOKOGAWA DLM2024
Current sensors	LEM LA 55-P
DSP	Texas Instruments TMDXCNCD28377D
Main voltage source	TDK Lambda GEN100-33
IGBT three-phase power module	Mitsubishi PS22A79

4.5.1 Averaged Main Control Step Response

As visible in Figure 4.17, no overshoot and oscillation have been found in the averaged main control step response. The system goes to regime ($i_{out} = 10A$) in about $7ms$. As visible in the zooming (bottom right dashboard in Figure 4.17) the current average value is the same for all the three legs current i_k (pink, yellow and blue waveforms) even thought duty cycles δ are slightly different one another. Finally it is possible notice that voltage V_o (green waveform) reaches $60V$ and no ripple is present because of the filtering branch presence.

Figure 4.17: Averaged main control step response

4.5.2 Capacitor Branch Removal Assumption

As visible in Figure 4.18, output voltage V_o (green waveform) ripple diseappear as soon as the capacitive branch is connected. No effects have been noticed on the legs current. As expected, steady state behaviour is not affected by the filtering branch removal eventhoutght it have been considered in the model.

Figure 4.18: Capacitor branch removal effect on output voltage V_o

4.5.3 Inductance Unbalance Robustness Test

In Figure 4.19, it is possible notice that the inductance variation produces a ripple amplitude variation well visible in the pink waveform envelope change in the top main dashboard. From (1.47) it is possible notice that having increased the inductance caused a ripple reduction. Furthermore, it is possible notice that no variation on the output voltage V_o (green waveform) have been introduced. The output current average value I_{out} remains constant.

Figure 4.19: Unbalanced inductance component effect on leg current ripple

4.5.4 Current Rebalancing in Unbalanced System

As visible in Figure 4.20, currents i_k (pink, green and blue waveforms) are strongly unbalanced. Leg's current represented with the yellow waveform have been completely shut down by opening the leg circuit. However, current rebalancing network (current sequential binding approach), does a proper computation of δ_k values and fully compensates the unbalance. Voltage V_o (green waveform) reaches $60V$ regardless on the unbalance magnitude as done in all the other measurements (Figures 4.17, 3.17 and 4.19). As explained above, current rebalancing network, tries to balance legs' currents. Moreover, having unbalanced the third (last) leg ($N = 3$), it also tends to fully track the total current reference i^*_{out}. This effect it is not always guaranteed and depends on the approach used and on what leg have been disconnected.

Figure 4.20: Current unbalance compensation

Overall, experimental measurements have validated the analytical computations and the simulations outcomes. Multiple assumptions and approaches have been tested and no relevant error have been observed.

Conclusion

Overall it has been possible to propose a converter topology able to take advantage of the designing constraints that the market is expected to demand. The whole topology of the back-to-back converter relies on low cost two-level three-phase power modules. Both converter sides (IAR and IBC) are made out of multiple stacked highly standardized base block. This topology ensures a high resilience to faults and maintenance needs. Moreover, thanks to interleaving topology flexibilities, is possible to ensure a posteriori power expansions following the market trend in different scenarios. Relevant attention must be dedicated to notice that all the power blocks present an inherent capability to carry bidirectional power flows, ensuring grid support in terms of power storage and energy quality services.

For what it concerns the technical improvements introduced, substantial ripple reduction in all the converter's key areas have been achieved. Front end grid current ripple have been strongly reduced thanks to the multiple legs dedicated for each phase. DC link voltage ripple has been reduced, and therefore, capacitors operative life is expected to increase. Noticeable output current ripple reduction has been introduced by adequately taking advantage of the IBC topology and the DC BUS regulation capability of the IAR.

An original methodology denominated ripple-free strategy has been introduced. It has been studied from a generic point of view, emphasizing all the benefits and drawbacks that staking a certain number of legs could introduce. General close form designing formulas have been presented. A nine leg version has been shown as a proposed DC/DC stage. Multiple simulations on most of the assumptions and findings have been carried out. Having minimized the output current ripple promotes a proper battery utilization accordingly to literature recommendations.

A generic control system able to merge together multiple effects has been discussed. An averaged controller able to guarantee CC charging operations has been introduced. Multiple assumptions able to provide outcomes on different precision levels have been deeply displayed. A current rebalancing network able to guarantee identical module utilization has been presented. Multiple approaches are discussed, and some of them have been simulated and experimentally tested. Control signal provided from averaged main controller and current rebalancing network should work in according to the ripple-free strategy and the voltage oriented control able to ensure ripple minimization and power factor optimization respectively.

Thought the work, multiple mathematical and software tools had been used. The system has been characterized and treated using standard and updated methodologies such as Clarke, Park, Laplace, Steinmetz transformations, and state-space representation. Outcomes have been tested employing standard designing software such as MATLAB Simulink and Code Composer Studio for the digital implementation.

Comprehensively multiple main areas of a converter capable of being inserted in

the economic scenario of a green shifting society able to introduce and condensate together technical improvements have been studied. Further study could be done on extending the findings on a model employing a more significant number of legs. Rebalancing control strategy applied on the AC input side might provide relevant outputs. A complete characterization of the rebalance capabilities at any current unbalance for all the possible approaches could provide valid outcomes. Inverse power flow simulation test might improve and introduce new features that have not been studied yet.

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List of Figures

List of Tables

Acronyms

AC Alternating Current. 1, 2, 9, 10, 13, 24, 38, 96

AF Alternative Fueled. 7

AR Active Rectifier. 12, 14, 18–21

BC Buck Converter. 12, 13

BEVs Battery Electric Vehicles. 7, 8, 13, 25

BMS Battery Management System. 10, 62

CAN Controller Area Network. 11

CC Constant Current. 25, 26, 61, 95

CCS Carbon Capture and Storage. 6

CCS Combined Charging System. 9–11

CHAdeMO CHArge de MOve. 10, 11

CNG Compressed Natural Gas. 7

CPWM Centered Pulse Width Modulation. 22

CV Constant Voltage. 25, 26

DC Direct Current. 1, 2, 9, 10, 12–18, 20, 21, 23, 24, 37–43, 45, 48, 52, 83, 95

DSP Digital Signal Processor. 63

EAFO European Alternative Fuels Observatory. 7

EC European Commission. 6

EMF Electromotive Force. 51

EMI Electromagnetic Interference. 14

EPA Environmental Protection Agency. 6

ESR Equivalent Series Resistance. 24, 56

EU European Union. 6

EV Electric Vehicle. 2, 7–12

EVSE Electric Vehicle Supply Equipment. 9–12, 25

FC Flying Capacitor. 12

FCEVs Fuel Cell Electric Vehicles. 7

FCs fast chargers. 9

FPGA Field-Programmable Gate Array. 63, 72

G2V Grid to Vehicle. 1, 2, 38

GB/T Guobiao Standard. 10

GDP Gross Domestic Product. 6

GHGs Greenhouse Gasses. 6–8

I/O Input and Output. 14

IAR Interleaved Active Rectifier. 13, 18, 20, 23, 24, 50, 62, 71, 74, 75, 83, 95

IBC Interleaved Buck Converter. 13, 24, 26, 48, 50–52, 55, 62, 63, 74, 76, 78, 80, 81, 84, 85, 95

ICEVs Internal Combustion Engine Vehicles. 6, 7, 11

ICPWM Interleaved Centered Pulse Width Modulation. 38

IPCC Intergovernmental Panel on Climate Change. 6

ISVPWM Interleaved Space Vector Pulse Width Modulation. 38

LCA Life Cycle Assessment. 8

LDN Level Doubling Network. 12

LPG Liquefied Petroleum Gas. 7

LULUCF Land Use, Land-Use Change, and Forestry. 6

MIMO Multiple Inputs, Multiple Outputs. 71

MISO Multiple Inputs, Single Output. 56

MMC Modular Multi-level Converter. 12

NPC Neutral Point Clamped. 12

O&M Operation and Maintenance. 2, 9

PFC Power Factor Correction. 12

PHEVs Plug-in Hybrid Electric Vehicles. 7

PI Proportional–Integral Controller. 20, 50, 65

PIDF Proportional–Integral–Derivative-Filtering Controller. 62

PLC Power Line Communication. 11

PWM Pulse Width Modulation. 16, 18, 28, 29, 50, 62

RES Renewable Energy Sources. 6, 7

RMS Root Mean Square. 22

S&H sample and hold. 72

SISO Sultiple Inputs, Single Output. 56, 71

SOC State of Charge. 24–26, 51, 52, 61

SOH State of Health. 26, 62

SPWM Sinusoidal Pulse Width Modulation. 22

TCO Total Cost of Ownership. 7

TRL Technology Readiness Level. 7

UN United Nations. 6

UNFCCC United Nations Framework Convention on Climate Change. 6

V2G Vehicle to Grid. 1, 2, 8, 13

V2H Vehicle to Home. 8

V4G Vehicle for Grid. 8

WHO World Health Organization. 6

ZEVs Zero-Emissions Vehicles. 8

Nomenclature

$\approx$	Approximately
$\Delta\delta$	Duty cycle displacement
Δi	Current displacement
Δi_k	Current ripple
Δi_{kM}	Maximum current ripple
ΔV_{DC}	DC link voltage error
ΔZ_k	Impedance displacement
δ	Duty cycle
δ'	Conventional duty cycle
δ_M	Maximum duty cycle
δ_m	Minimum duty cycle
δ_r	Actual duty cycle
$\lfloor x \rfloor$	Floor function
$\in$	Is member of
$\lvert x \rvert$	Absolute value
$\mathcal{L}$	Laplace transform
ω	Angular frequency
$\propto$	Direct proportionality symbol
$\lfloor x \rceil$	Round function
C	DC link capacitance
C_b	Charge capacitance
c_k	Carrier
C_t	Electrochemical processes capacitance
D	Displacement transfer function

e	Error signal
f	Grid frequency
f_s	Sampling frequency
f_{sw}	Switching frequency
f'_{sw}	Equivalent switching frequency
G	Transfer function
G'	Output transfer function
I	Average current
I	IAR input current
i	Total current
i_b	Battery current
i_C	Capacitor current
i_k	Leg current
i_M	Maximum charging current
i_{DC}	IAR output current
i_{IBC}	IBC input current
i_{kp}	Leg current
i_{nor}	Norton equivalent current
i_{out}	Output current
L	Reactors inductance
L'	Equivalent reactors inductance
M	A/D resolution
M	Total number of block
m	Modulating index
m_k	Modulating signal
M_s	Number of block per side
max	Maximum value
N	Number of legs per side
N_b	Number of legs per base block

P	Rated power
p	Subsection index
P_b	Base block rated power
P_C	Capacitor power
P_{IAR}	IAR power
P_{IBC}	IBC power
R	Reactors resistance
r	Ripple ratio
R'	Equivalent reactors resistance
R_C	Capacitor ESR
R_l	Resistive load
R_P	Parallel branch equivalent resistance
R_S	Series equivalent resistance
R_s	Battery series resistance
R_t	Electrochemical processes resistance
R_{dis}	Discharge resistance
S	Pole
S_k	Base block switch
t	Time
t_{on}	Active time
t_{sw}	Switching period
t'_{sw}	Equivalent switching period
u	Internal voltage
V	IAR front end voltage
v	Thévenin equivalent voltage
V_g	Line to line RMS voltage
v_k	Pole voltage
v_L	Inductor voltage
v_s	Switch voltage

v_{ab}	Line to line pole voltage
V_{bat}	Open circuit battery voltage
V_{bat}	Open circuit maximum battery voltage
V_{DCM}	Maximum DC link voltage
V_{DCm}	Minimum DC link voltage
V_{DCr}	Actual DC link voltage
V_{DC}	DC link voltage
V_{eq}	Equivalent IBC voltage
v_{gp}	Grid phase voltage
V_{IBC}	IBC output voltage
v_{kp}	Pole voltage
V_{oM}	Maximum output voltage
V_{om}	Minimum output voltage
V_o	Output voltage
V_{the}	Thévenin equivalent voltage
W_C	Capacitor energy
x^*	Reference value
xC	C-rate
Z	Leg impedance
Z'	Equivalent leg impedance
Z_L	Equivalent leg impedance