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Master Degree Programme in Electrical Energy Engineering

MASTER THESIS

in Power Electronic Circuits M

Development of a Test Bench for Multilevel Cascaded H-Bridge Converter with Self-Balancing Level Doubling Network

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Abstract

This Master degree project was developed during an exchange program, established between the University of Bologna and the Technical University of Munich (TUM). The research activity was conducted at the Institute of Energy Conversion Technology (TUM department) in collobaration with Prof. Dr.-Ing. Hans-Georg Herzog and his research team.

A symmetric 3-Phase Cascaded H-bridge Multilevel Inverter (CHBMLI), that is available in the TUM university laboratory, is reconfigured to operate as proposed using a Level Doubling Network (LDN). The LDN takes the form of a 3-phase half-bridge inverter that shares a common DC bus connected to a floating capacitor. This configuration allows almost to double number of output voltage levels. The LDN concept has inherent self-balancing capability that guarantees to maintain voltage across the LDN capacitor at nearly constant value and without any closed-loop control, while it does not consume or supply any power, apart from losses in the circuit. The proposed topology preserves the merit of CHBMLI modular structure, improving overall inverter's reliability with reduced number of switching devices and required isolated DC sources compare with standard CHBMLI topology. Therefore, it significantly improves power quality, allows to reduce average device switching frequency, while minimizing cost and size of the power filter. Operation of the circuit is extensively verified by simulation in MATLAB/Simulink framework and experiments, performed on a grid-connected 3-phase five level laboratory prototype, specifically built as a part of the current Master Thesis. This work is a first step towards studying the proposed topology. Nevertheless, it provides a baseline for future analyses of the architecture and its possible variations.

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1 Introduction

The primary trends of all power supply market segments are: increased efficiency; reduced environmental impact; higher power density; and cost reduction. To meet these requirements a multidisciplinary research - EEBatt project 'Distributed stationary battery storage systems for the efficient use of renewable energies and support of grid stability' was developed by the TUM's Munich School of Engineering (MSE).

The main goal of the EEBatt project is to investigate, develop and produce a decentralized energy storage device, which ensures that locally generated electrical power can be consumed locally [1].

As a part of EEBatt project, Power Electronics subproject dealt with the development of a power electronic conversion system that would link distributed storage batteries systems to the low voltage distribution grid [1]. A variety of industry-recognized power electronics topologies had been compared and an appropriate Cascaded H-Bridge Multi Level Inverter (CHBMLI) topology was finally selected. Furthermore, numerous configurations from 3-phase three-level (3Ph3L) to 3-phase seventeen-level (3Ph17L) were implemented in hardware to confirm their performance with regard to simulation models. Eventually, the most efficient and reliable test bench was used to develop a converter prototype itself and its control system that was eventually applied for the project stationary battery storage system.

High quality of voltage and current waveforms both at the input and output terminals of a converter is important. The waveforms are affected by the following factors: 1) topology used; 2) application; 3) control algorithm; 4) size of the filter; and 5) the choice of switching frequency. As the switching losses of semiconductor devices, in high-voltage/current applications, make up a major portion of the device losses, therefore usage of high switching frequency is prohibited [2]. Another possible solution is to use

a multilevel inverter topology that delivers waveforms with better harmonic spectrum, while still maintaining reasonable overall reliability and efficiency of power converter.

1.1 Motivation and Aim

The CHB architecture used for the EEBatt project, as it will be discussed later in Chapter 2, is composed of two or more H-Bridge (HB) submodules connected in series, depending on the number of levels implemented. Figure 1.1 shows a test bench for 3Ph17L standard CHB configuration, built for the EEbatt project. It worth nothing to mention that obvious drawbacks of this topology are a large number of isolated DC power supplies and a high component count when the number of voltage level rises.

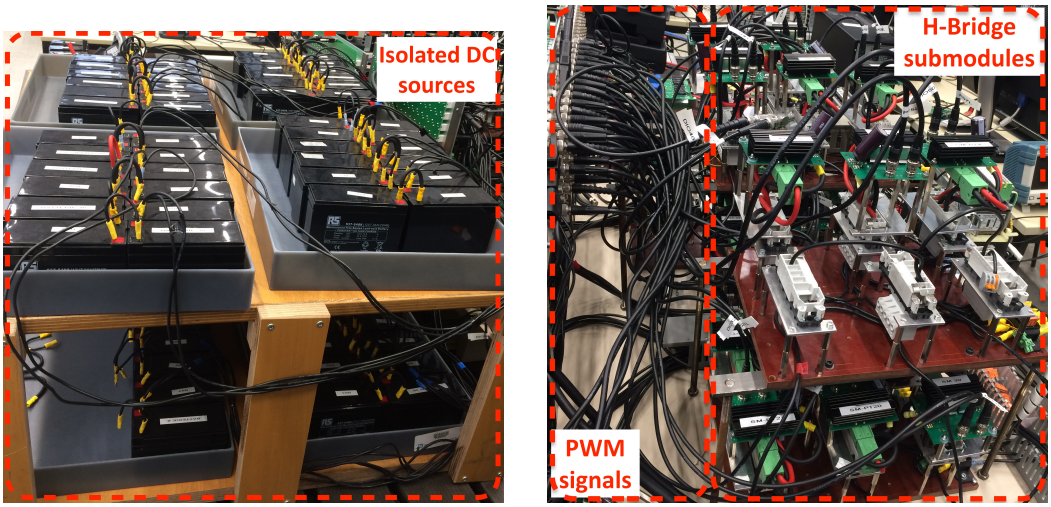


Figure 1.1 – Laboratory test bench of 3-phase seventeen-level CHB multilevel inverter [3]

The primary goal of this thesis is to improve reliability and performance of the test bench by introducing a Level Doubling Network (LDN) into existing CHBMLI circuit. Implementation of the proposed topology and usage of appropriate modulation technique will give an opportunity to reduce average device switching frequency, minimizing commutation losses, to achieve minimum harmonic distortion and eventually cut down total number of component used in the inverter, improving its reliability. The operating principle of the LDN configuration is introduced in [4] and will be extensively examined in the current work with regard to EEbatt project application.

To achieve this aim, the LDN submodule must be implemented in hardware, properly connected and controlled taking into consideration, the existing structure of the laboratory CHB inverter. Another objective is to develop a modulation approach that will allow to generate required gate signals arrangement to control semiconductor devices in both (CHB and LDN) circuits.

1.2 Methodology and Limitations

Since implementation of proposed topology is based on well-known CHBMLI circuit, within this thesis, the incremental model of the project development process, as shown in Figure 1.2, is used.

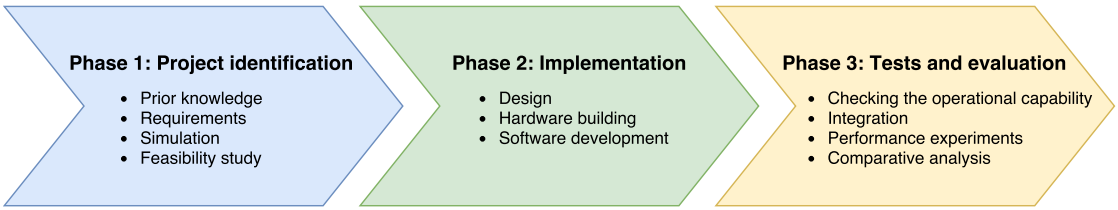


Figure 1.2 – The incremental model of the project development process

The work is divided into three main phases. The first phase is the project definition, which includes: 1) literature overview on already developed techniques that can be used for the current project; 2) determination of requirements and standards that must be fulfilled during the implementation process; 3) calculation of basic parameters and simulation of system model; 4) feasibility study to confirm desired outcome. The second phase is the hardware and software development, where the LDN submodule is designed based on printed circuit board (PCB) architecture, built up and integrated into the existing test bench. The third phase covers performance tests and their evaluation. The first step of this phase is to check operational capability of the LDN submodule separately from the CHBMLI circuit in order to verify the quality of the production. This submodule is then connected with the rest of the CHB inverter, to create the desired topology. Meanwhile, software adaptation in terms of modulation strategy for controlling a new circuit must be done. Further, the operational (performance) study is done to determine if the whole system works as expected, acquiring necessary data for a final evaluation step.

Due to limits of the present work, following restrictions are taken into account:

- Only the 3-phase five-level topology of proposed circuit will be considered.

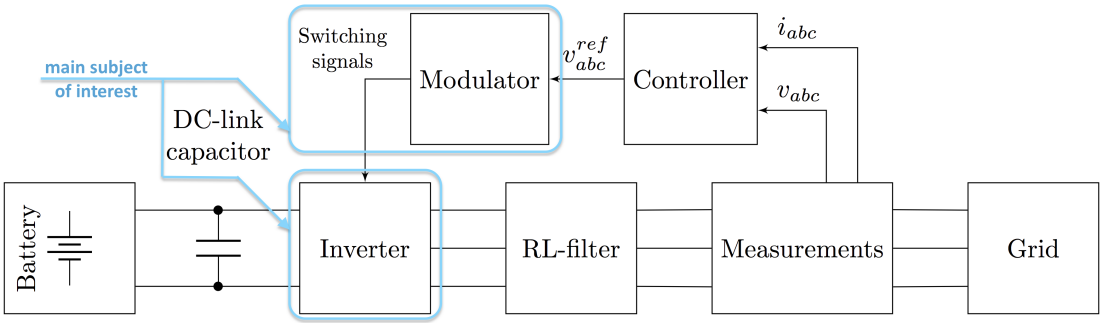


Figure 1.3 – Block-diagram of the developing circuit

- Balanced three phase system. No faults or continuous unsymmetrical modes will be studied.
- Solely Level Shifted pulse-width modulation (PWM) will be examined and implemented. The modulation will be carried out with switching frequency 1 kHz and unity modulation index only.
- Only grid connection application, particularly used in the EEBatt project, as shown in Figure 1.3 will be performed.

Other specific constraints of this work will be presented in the subsequent chapters.

1.3 Overview

A literature review of the existing and most industry recognizable techniques to rise the number of levels will be presented in Section 2.1. The single-phase and three-phase five-level (1Ph5L and 3Ph5L, respectively) version of the proposed HB with LDN topology will be used to report the theoretical notions of the considering configuration in Section 2.2. In Section 2.3 will be given the summary of the most common PWM based modulation techniques for multilevel inverters (MLIs).

To ensure acceptability and reliability of the proposed circuit in the EEBatt application, the 3Ph5L version will be executed and examined. By default, this paper considers just three phase topologies, unless otherwise specified in the text. Required description and specification parameters of the components and the test bench itself will be introduced in Chapter 3.

Subsequently simulation study of 3Ph5L HB inverter with LDN, using MATLAB/Simulink will take place. Obtained simulation results will be introduced in Chapter 4 along with the results gained from the experimental measurements. Further, the comprehensive analysis of the data will be conducted.

In conclusion, the outcomes of the thesis and recommendations for the future developments of the test bench will be presented in Chapter 5.

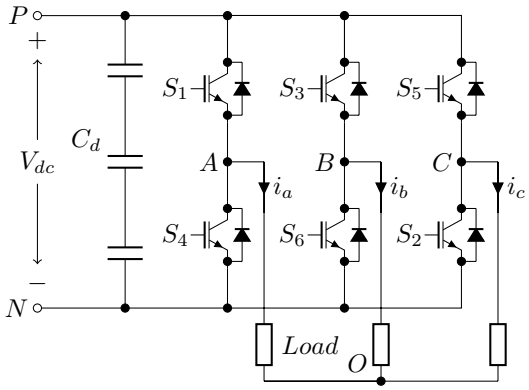
2 Theoretical basis

2.1 Multilevel Inverter Topologies

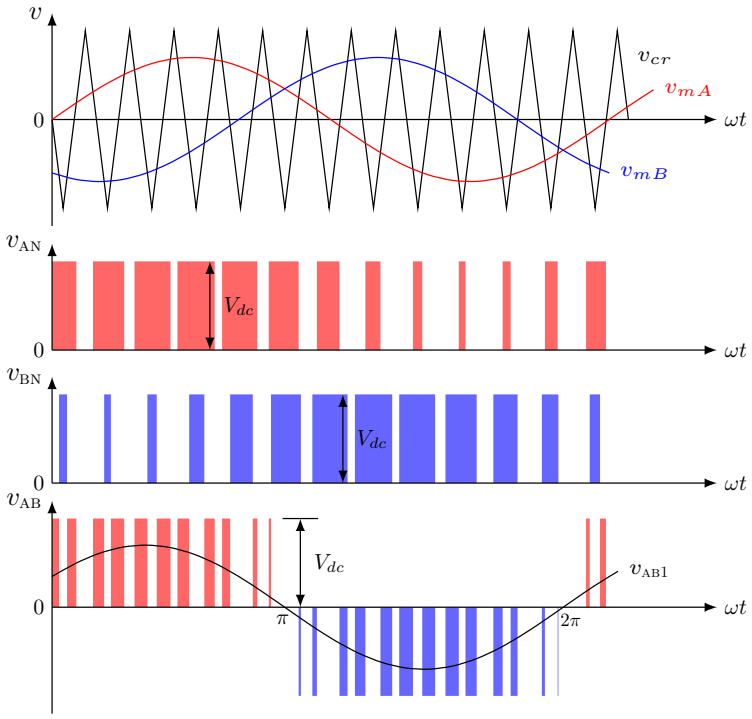
Conventional three phase two-level (2L) inverters, a simplified circuit diagram of that illustrated in Figure 2.1a, are used to generate a three-phase AC voltage with variable magnitude and frequency from a fixed DC voltage. The resultant inverter terminal voltage v_{AN}, which is the voltage at the phase A terminal with respect to the negative DC bus N, is equal to the DC voltage V_{dc}. Generated stepped waveform can be seen in Figure 2.1b. Since the waveform of v_{AN} has only two levels, 0 and V_{dc}, the inverter is known as a 2L inverter.

The inverter line-to-line voltage v_{AB} can be determined by $v_{\mathrm{AB}} = v_{\mathrm{AN}} - v_{\mathrm{BN}}$. The waveform of its fundamental-frequency component v_{AB1} is also given in the Figure 2.1b [5]. A carried-based sinusoidal pulse-width modulation (PWM) scheme is reviewed in Section 2.3.

Despite the fact that traditional two-level inverters, in comparison with multilevel (ML) topologies, are simple (i.e. topology and PWM scheme), relatively cheap and relailable, but on the other hand they have higher voltage stress on switching devices for the same maximum output voltage and generate lower harmonics for the same switching frequency. Therefore it often requires a large-size LC filter installed at its output terminals [5]. Taking that into account, multilevel inverters (MLI) became more and more popular in last decades, due to **the increased power ratings**, **enhanced voltage limit capability of semiconductor devices**, and **reduced electromagnetic interference emission**. The other features also include **better quality of output waveform** and as consequence better power quality, **low switching losses**, **high voltage capability**, **lower** $\frac{dV}{dt}$ **stress**, **reduced requirement of passive filters**, **lower torque ripple in motor application** and **possible fault-tolerant operation** [2, 6, 7]. These properties and the



(a)



(b)

Figure 2.1 – Simplified three-phase two-level inverter (a) and two-level waveform with sinusoidal PWM (b) [5]

advancement in semiconductor technology make multilevel converters (MLCs) attractive for high-power applications. Specifically, these benefits contribute to the feasibility of the MLIs for direct integration of medium or high voltage utility grid averting the need for bulky transformers. This is a crucial advantage since this possibility for direct integration of medium/high voltage utility grid is not suitable for a single power semiconductor switch based two-level inverter [7].

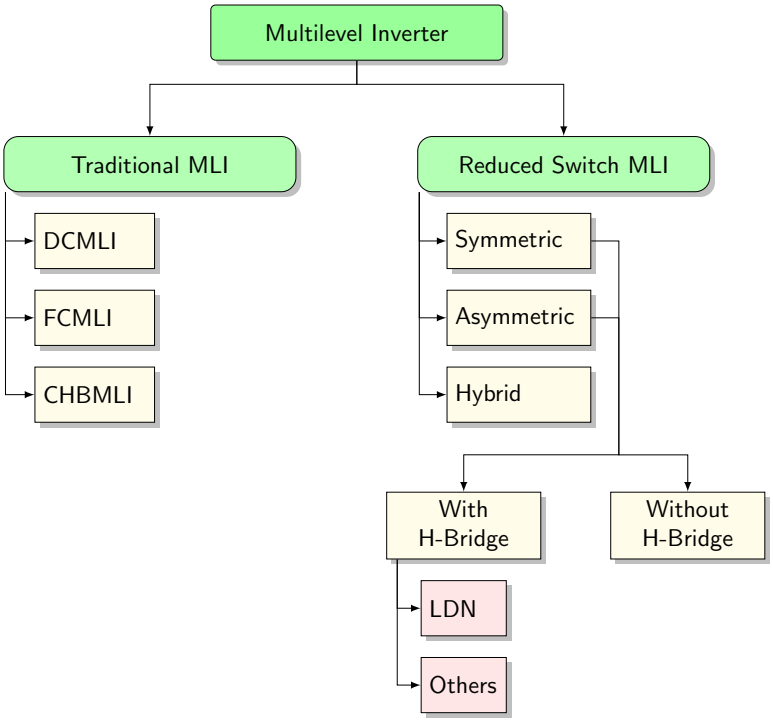


Figure 2.2 – Simplified tree diagram of MLI classification [7]

The ML voltage source inverters (VSIs) have a variety of configurations. The well-known MLI topologies are Diode Clamped MLI (DCMLI), Flying Capacitor MLI (FCMLI) and Cascaded H-bridge MLI (CHBMLI) [7]. This section gives an overview of aforementioned conventional multilevel converters. The operating principle of these converters is discussed, and their performance is analyzed based on their topologies, limitations and control techniques. Special attention in Section 2.2 will be drawn to so called Reduced Switch MLI group and particularly to a CHBMLI with self-balancing Level Doubling Network (LDN), the topic of this Master Thesis. Performance parameters of proposed MLI and their calculation methods are examined with a focus on achieving minimum harmonic distortion and high efficiency in comparison with existing solutions. Figure 2.2 shows the

simplified tree diagram of MLI classification that has been taken as a roadmap of this work.

2.1.1 Diode Clamped Multilevel Inverter

The diode-clamped multilevel inverter employs clamping diodes and cascaded DC capacitors to produce AC voltage waveforms with multiple levels. The concept can be extended to any number of levels by increasing the number of capacitors and diodes. However, due to capacitor voltage balancing issues, the three-level topology, often known as neutral-point clamped (NPC) inverter, has found wide application in high-power medium-voltage drives. The main features of the NPC inverter include **reduced** $\frac{dV}{dt}$ and **total harmonic distortion (THD) in its AC output voltages** in comparison with the two-level inverter discussed earlier, as well as associated, with this topology, control strategies help to **minimize semiconductor losses** [5]. It is also characterized by relatively small DC link capacitors, due to the reason that all of the phases share a common DC bus and thus the capacitance requirements of the converter are minimized, a simple power circuit topology, a low component count, and straightforward protection and modulation schemes [2].

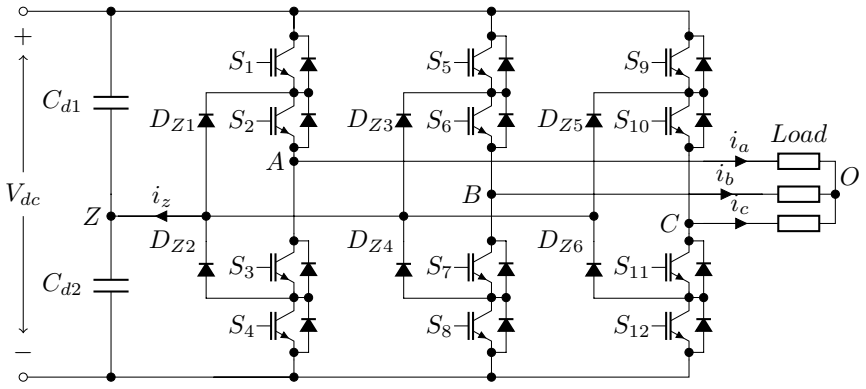


Figure 2.3 – Simplified three-phase three-level NPC inverter [5, 8]

Figure 2.3 illustrates a three phase three-level NPC voltage-source inverter. The circuit model is a bidirectional three-level VSI, with three legs, one per phase, each containing two series-connected high-side switches and two series-connected low-side switches. Often, insulated-gate bipolar transistors (IGBTs) with anti-parallel diodes are used as the switches for an NPC converter, but other two-quadrant switch configurations can also be employed.

On the DC side of the inverter, the DC bus capacitor is split into two series-connected capacitors, with the mid-point connected to each of the three IGBT legs, providing a floating neutral point Z. Clamping diodes D_{z1} and D_{z2} (as an example considering just leg A) are placed between the capacitor mid-point Z and the one-quarter and three-quarter points of each leg. The voltage magnitude across each of the DC capacitors C_{d1} and C_{d2} is normally equal to $\frac{V_{dc}}{2}$ (for higher level topologies the magnitude can be calculated as $\frac{V_{dc}}{(m-1)}$, where m is number of voltage levels), assuming that these capacitors are sufficiently large such that the voltage across each of them is kept constant. The mid-point potential of a capacitive voltage divider in the DC link is used to stabilize the voltage distribution between devices with the help of clamping diodes. The topology adds the zero level to the output voltage waveform and, thus, also serves to reduce its harmonic content. The three-level inverter topology permits operation at double voltage (in comparison with two-level topology), which also doubles the maximum output power [2]. The capacitors can be charged or discharged by neutral current i_z, causing **neutral-point voltage deviation** [5].

Due to the active power consumption and energy exchange between the DC link capacitor and AC source, the unbalancing phenomenon of DC link capacitor voltages will occur [9]. Such unbalance is a common concern for DCMLI topology and some of its variations. Several methods have been proposed to overcome the voltage balancing problem of the floating capacitor with considerable effort, necessitating either some algorithm [9–12] or external voltage balancing network [13]. Occurance of the effect leads to an incorrect modulation of the output voltage and hence, incorrect volt-seconds, which influences the machine currents introducing distortion, increasing THD. This interaction may lead to unstable operation of the drive system. Furthermore, an excessive neutral point potential error imposes higher voltage stress on the semiconductor devices and capacitors [10]. It is also theoretically verified that the conventional PWM algorithm could not be applied to achieve the equalization under all operation condition. The higher the level used in the DCMLI is much more complex the balance operation becomes due to the rapid increase of voltage vectors and three-phase switching states [9, 11].

The output voltage of this topology contains three level such as $\frac{V_{dc}}{2}$, 0 and $-\frac{V_{dc}}{2}$. The operating status of the switches in the NPC inverter can be represented by switching states [P], [O] and [N], respectively. The positive polarity output voltage (switching state [P]) is generated by turning on the upper two switches in leg A and the inverter terminal voltage v_{AZ}, which is the voltage at terminal A with respect to the neutral point Z, is $\frac{V_{dc}}{2}$, while [N] indicates that the lower two switches conduct, leading to $v_{AZ} = -\frac{V_{dc}}{2}$ [5, 7].

When inner switches S_2 and S_3 are turned on (switching state [O]), the inverter output terminal voltage v_{AZ} is connected to the neutral point through one of the clamping diodes, see commutation patterns during a transition from state [O] to [P] in Figure 2.4. Depending on the direction of load current i_a, one of the two clamping diodes is turned on. For instance, a positive load current ($i_a > 0$) forces D_{z1} to turn on, and the terminal A is connected to the neutral point Z through the conduction of D_{z1} and S_2 [5]. Bold green lines indicate the current path in case of a positive load current ($i_a > 0$), while bold blue ones signify negative load current flow ($i_a < 0$). Dashed red IGBTs represent

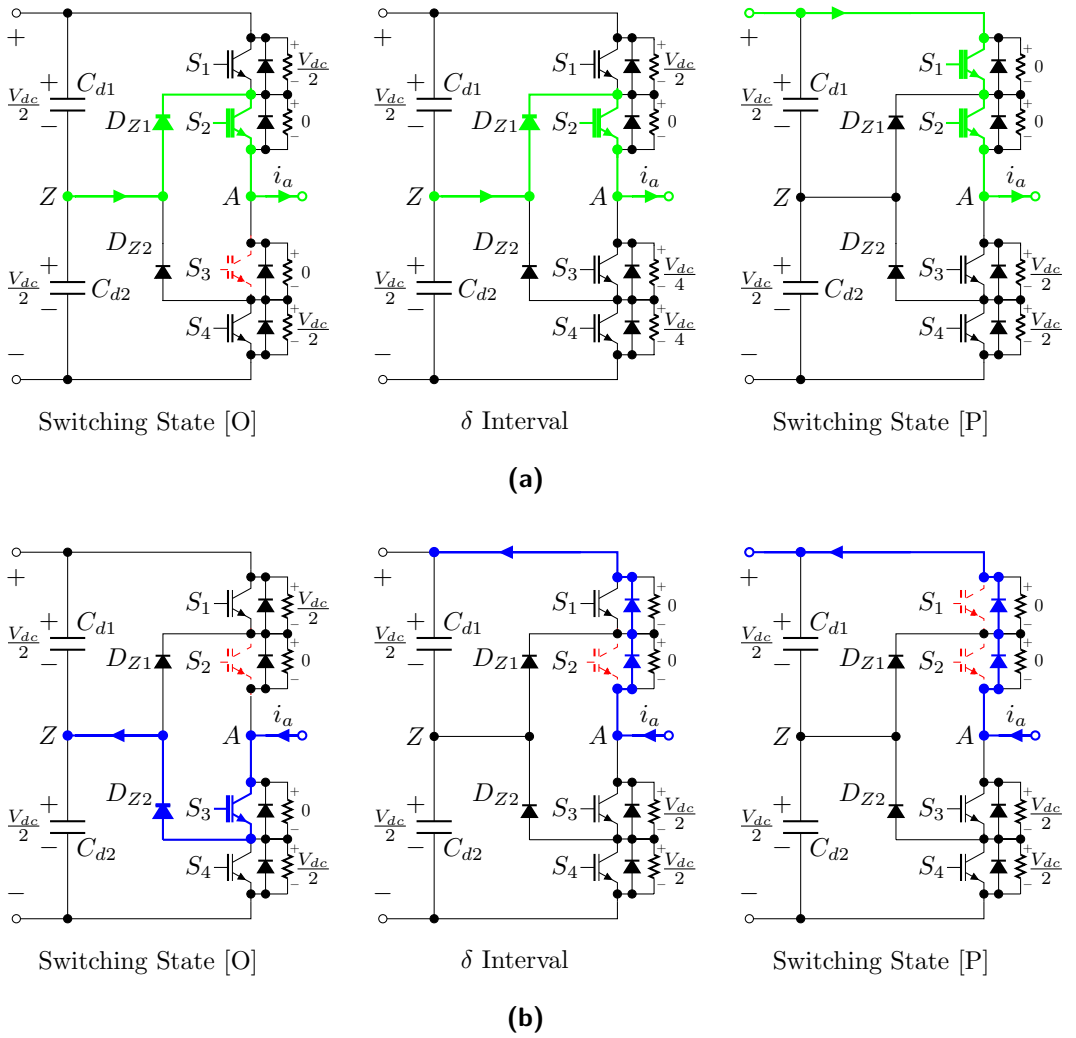


Figure 2.4 – Commutation during a transition from switching state [O] to [P] with $i_a > 0$ (a) and $i_a < 0$ (b) [5]

a turned on switch during a particular state but not involved in conduction path. The resistors that are connected in parallel to active diodes and switches have a purpose to equally share voltage across neighbor semiconductors in a leg.

The switches S_1 and S_3 operate in complementary manner. With one switch on, and the other must be off. Therefore, a blanking time of δ must be introduced in switching pattern to avoid short circuits. Similarly, S_2 and S_4 are a complementary pair as well.

Considering the same voltage across the DC link capacitors, the voltage stress on each of the active switching device is clamped to the voltage of each capacitor by the clamping diodes. Therefore, it can be concluded that **all the switching devices** in the three-level NPC inverter withstand only half of the DC bus voltage during the commutation from switching state [O] to [P], [P] to [O], [N] to [O], or vice versa [5]. The clamping diodes are normally connected in series to share the blocking voltage in real application. Taking into consideration multilevel topologies with m - number of voltage levels, then each active device is only required to block a voltage level of $\frac{V_{dc}}{(m-1)}$, the clamping diodes must have different voltage ratings for reverse voltage blocking. If DCMLI operates under PWM technique, the diode reverse recovery of these clamping diodes becomes the major design challenge in high-voltage and high-power applications [7, 14].

It should be pointed out that the switching between [P] and [N] is strictly prohibited for the following reasons: (a) it involves all four switches in an inverter leg, two being turned on and the other two being commutated off, during which the dynamic voltage on each switch may not be kept same; and (b) the switching loss is doubled [5].

To sum up, the three phase three-level DCMLI inverter offers the following features:

- **It requires only one DC source for generating the required output voltage level**. In addition to that, it demands a relatively small DC link capacitors.
- **No dynamic voltage sharing problem**. Each active device is only required to block a voltage level of $\frac{V_{dc}}{(m-1)}$ during commutation, where m is number of voltage levels [5].
- **The control logic** of three-level and five-level structures **is simple, highly reliable and more effcient** in fundamental switching frequency [2, 7].
- **Low $\frac{dV}{dt}$ and THD of the output voltage**, and consequently, low electromagnetic interference in comparison to the two-level inverter operating at the same voltage rating and device switching frequency [5].

However, the **voltage balancing problem across the DC bus capacitors** and the **usage of higher clamping diodes increases the complexity and largeness of the system**, which are the major drawbacks of DCMLI. The **capacitor balancing is diffcult** when the number of levels exceeds three [7].

References [2, 5, 7–14] cover most of the important modulation, control, and topological aspects.

2.1.2 Flying Capacitor Multilevel Inverter

Active switching devices, diodes, and capacitors, all can be used as a clamping device. However, due to operational principle they have different properties. Diodes have the characteristics of unidirectional conduction, and how it was explained in the previos section, they can be used for unidirectional clamping. An active switche with a parallel diode can provide a bidirectional path by itself, and it can realize main switch and flying-capacitor clamping. Capacitors are electrical energy storage passive components, thus they can participate in voltage synthesizing and sustain the main switch blocking voltage[14]. Basing on this capacitor's property, the flying capacitor multilevel inverter (FCMLI) topology was developed.

The FCMLI structure is similar to the DCMLI structure but the floating capacitors are placed instead of clamping diodes. A FCMLI consists of $(m-1)$ DC link capacitors and $\frac{3}{2}(m-1)(m-2)$ count for m level inverter. Figure 2.5 shows a typical configuration of a three-phase five-level flying-capacitor inverter. This inverter generates phase inverter voltage v_{AN}, which is the voltage at the inverter terminal A with respect to the negative DC bus N with following values (similar for ther other phases): V_{dc}, $\frac{3V_{dc}}{4}$, $\frac{V_{dc}}{2}$, $\frac{V_{dc}}{4}$ and 0.

Due to the topology structure, the FCMLI inverters have some features such as:

- **Modular structure** for the switching devices, including **the absence of clamping diodes**.
- **Output voltage waveforms with reduced** $\frac{dv}{dt}$ (the voltage stress to clamp each device of the circuit given in Figure 2.5 is $\frac{V_{dc}}{4}$) and **THD** [5].
- The **symmetrical swithches loss distribution** and the resulting high first carrier band frequency of the converter voltage make this topology suitable for high speed drives and test benches [2].

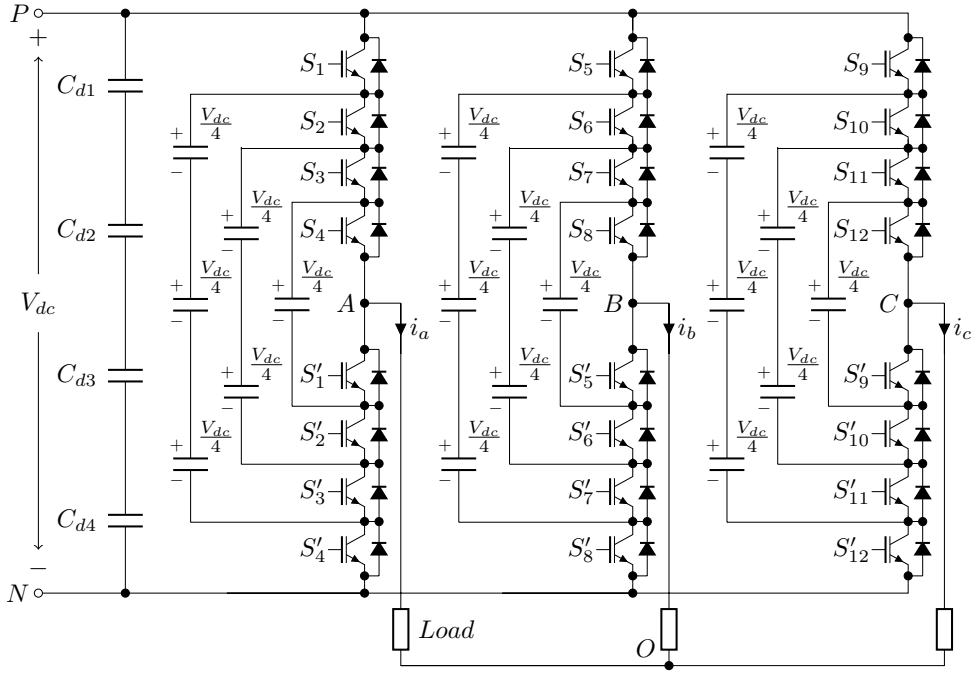


Figure 2.5 – Simplified three-phase five-level flying-capacitor inverter [5]

- **The voltage synthesis** of FCMLI is **more flexible** than a DCMLI. Many studies have shown that except under certain conditions, a simple open-loop control guarantees natural balancing of the flying capacitors [15]. When the number of levels is more than five, the proper redundant state selection gives the ability to regulate the voltage across the flying capacitors, eliminating the problem of voltage balancing [7, 16, 17].

However, for applications with highly inductive load and/or for low switching frequency, the natural balancing property gets very slow. For those cases, a filter circuit of the type tuned at the switching frequency and connected in parallel with the load may be used to achieve the natural balancing [15, 18, 19]. Nevertheless, this extra filter increases cost of the system and introduces extra power losses. Although the dynamics of balancing are improved with the tuned circuit, it may make the response too slow to follow the rapid variations of the input voltage [15, 19].

Other limitations of the topology are:

- Usage of **a large number of DC capacitors with separate pre-charge circuits**, making the system more expensive and difficult to package, especially for topologies with a number of generated voltage levels more than five [5, 7].
- **The switching frequency and switching losses are high** in real power transmission [7].
- **Complex capacitor voltage balancing control**. Even though, as it was mentioned above, under some operational modes it is possible to apply open loop balancing, however voltage imbalance may occur, the output voltage quality degrades and blocking voltages imposed on power devices may increase beyond the rated values. Thus, to insure the safe operation of power devices under all operational conditions, it is necessary to take into account the capacitor voltage balancing when designing the control schemes for the FCMLI [2, 5, 7].

The detailed analysis of the advantages and drawbacks for FCMLI is given in the following sources [2, 5, 7, 15, 18, 19].

2.1.3 Cascaded H-bridge Multilevel Inverter

A Cascaded H-bridge Multilevel Inverter (CHBMLI) differs in several ways from DCMLI and FCMLI in how to achieve the multilevel voltage waveform. This section gives a brief overview on two arrangements of the CHB inverter: symmetrical and asymmetrical.

Symmetrical arrangement

The general case of a symmetrical three-phase multilevel CHB inverter is shown in Figure 2.6. As it can be seen, the converter is built up out of n series connected H-bridge cells for one phase leg. Each H-Bridge consists of 4 active switches (IGBT and MOSFET are generally used, depending on an application), one isolated DC source of equal voltage among all the supplies and a DC link capacitor. The bus link capacitor is used in DC to AC inverters to decouple the effects of the inductance from the DC voltage source to the power bridge. This capacitor provides a low impedance path for the ripple currents that are a result of the output inductance of the load, the bus voltage and the swithcing frequency of the inverter. The bus link capacitor also plays a role in reducing the leakage inductance of the inverter power bridge [20].

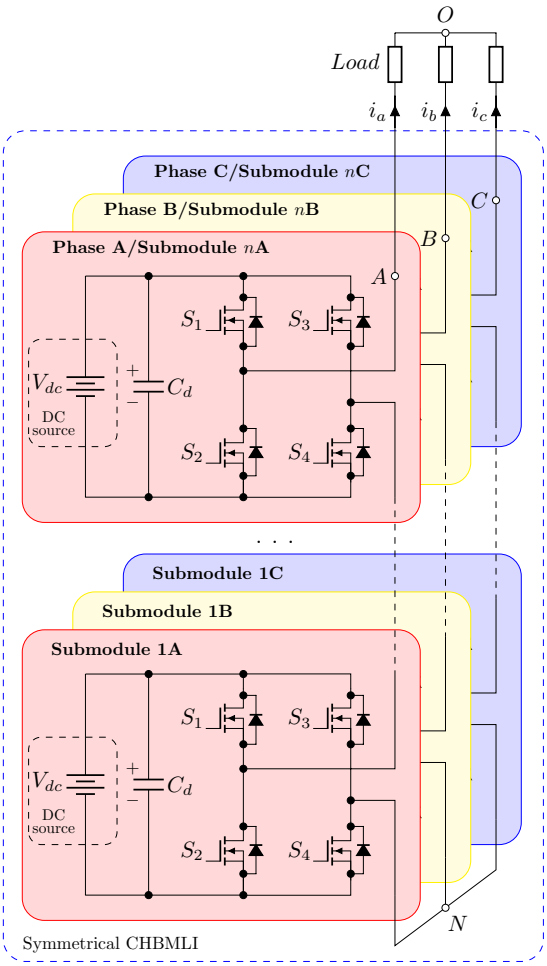


Figure 2.6 – Simplified three-phase CHBMLI with equal DC voltage

The CHBMLI can produce a phase voltage with $m = 2n+1$ voltage levels. When switches S_1 and S_4 of one submodule conduct, the output voltage of the H-bridge cell is V_{dc}. Depending on a required voltage level, the inverter phase voltage V_{AN}, which is the voltage at the inverter terminal A with respect to the inverter neutral N, can be obtained by similar conduction of other cells, resulting in the maximum achievable level nV_{dc} for positive half-cycle or less value by bypassing some of the cells through S_1 and S_3 (or S_2 and S_4) commutation. To gain $V_{\text{AN}} = 0$ all the DC sources in phase A should be bypassed. Similarly, with S_2 and S_3 in each cell of phase A switched on, $V_{\text{AN}} = -nV_{dc}$. Due to modular structure of CHBMLI, some voltage levels can be obtained by sets of different (redundant) switching states. It provides a **great flexibility for switching pattern design**, especially for Space Vector Modulation (SVM) schemes [7]. It is also

worth noting that the inverter phase voltage V_{AN} may not necessarily equal the load phase voltage V_{AO}, which is the voltage at node A with respect to the load neutral O [5].

The main features of the topology are:

- **Reduced requirements to the switch power rating**. Since, the CHBMLI is composed of a multiple units of single-phase H-bridge power cells, the voltage that switches must withstand is determined by a DC voltage source of that cell. Consequently the swithes are less affected by dynamic and static power losses.
- **Lower THD and improved power quality**. CHBMLI reproduce sinusoidal waveforms better than conventional full-bridge inverters with less filter efforts, the THD being a function of the number of discrete voltage levels exploited to synthesize the output waveform [21].
- This topology has **flexible structure** and it is easily extended to any number of levels.
- The modular structure of CHB inverters is naturally **well-suited for distributed power conversion**, because each cell can be powered by photovoltaic and fuel cells.
- CHBMLI topology requires **less number of components**, comparing to DCMLI and FCMLI because it does not have clamping diodes and clamping capacitors. In addition to that, it is free from voltage balancing problem typical for DCMLI and FCMLI.
- **CHB inverters are able to operate under faulty conditions** because of their modular structure. By bypassing the faulty cell and replacing it with a backup H-Bridge cell, the inverter's interruption is prevented in the event of diverse faults [22].

Despite of the aforementioned advantages, the drawbacks of CHB inverters are:

- **A large number of required isolated power supplier**. Regardless of the fact, that the cells can be supplied by phase-shifted transformers in order to provide high power quality at the utility side, however, this kind of solution increases the cost and complexity of the converter.
- **Unequal power distribution among power cells when Level-Shifted modulation is used**. This is particularly harmful for DC batteries, due to unequal discharging between batteries connected to HB submodules that generate lower and higher voltage levels. Consequently, the life-span of those batteries significantly differs.

Asymmetrical arrangement

The CHBMLI allows the utilization of DC sources with different voltage magnitude and generates higher number of output voltage level with the same number of H-bridge power cells. This allows more voltage steps in the inverter output voltage waveform for a given number of power cells [5].

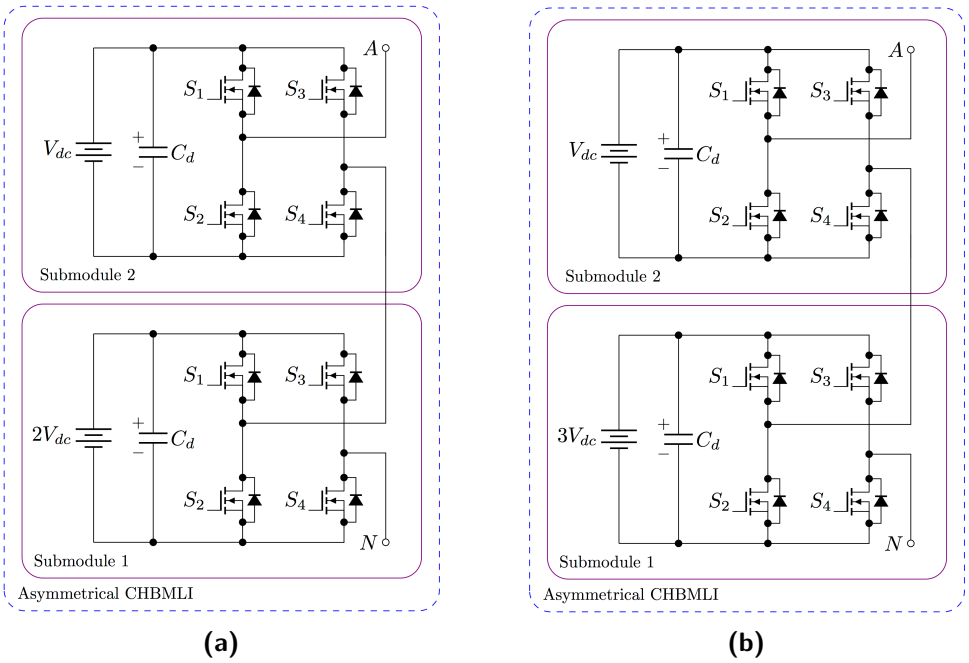


Figure 2.7 – Per phase diagram of CHBMLIs with unequal DC voltage. (a) Two-cell seven-level topology. (b) Two-cell nine-level topology [5]

Figure 2.7 shows two inverter topologies, where the DC voltages for the H-bridge cells are not equal. By different combination of additive and subtractive switching states between adjacent DC sources for producing the desired output voltage level at certain instants of time, the two-cell seven-level inverter leg is able to produce the following voltage levels: $3V_{dc}$, $2V_{dc}$, V_{dc}, 0, $-V_{dc}$, $-2V_{dc}$, and $-3V_{dc}$. Similarly, the two-cell nine-level inverter leg, obtained by series connection of two H-bridge power submodules with DC sources of V_{dc} and $3V_{dc}$ voltages, respectively, can generate levels: $\pm 4V_{dc}$, $\pm 3V_{dc}$, $\pm 2V_{dc}$, $\pm V_{dc}$ and 0.

Additional merits of the asymmertric CHB topology are:

- **Different ratio of DC sources can be applied** for generating the different output voltage levels.

- This topology allows **to switch the higher power cells at fundamental frequency**, reducing the switching losses of the converter and thus improving efficiency [23].

However, the merits of the modular structure in asymmetrical configuration are essentially lost since power is not evenly distributed among the converter cells, **eliminating the input current low-order harmonics cancelation effect** of the multipulse rectifier system of the traditional CHB [23]. In addition, **switching pattern** design becomes much more **difficult** due to the reduction in redundant switching states [5]. Moreover, unequal power sharing does not allow the bridges to be easily replaced (as the high side and low side bridges most likely to be made by different power devices), as well as it requires different thermal designs for each power cell [4, 23]. Therefore, this inverter topology is not very attractive for medium-voltage (MV) drives and many other applications.

2.2 Level Doubling Network

2.2.1 Single- and Three-Phase Topologies and Operating Principle

Although there are numerous advantages of the existing MLIs topologies, however, creating new topologies, modulation strategies and control schemes is still quite popular area of research. That fact that traditional MLIs require for more component count to extend the number of levels and as a consequence increased requirements of driver circuits, heat dissipation and protection circuits to such devices, forces to seek for alternative solutions. In order to overcome aforementioned problems, a reduced component count topologies are introduced. Generally, design of a new topology follows three categories such as structural modification, placement of asymmetric DC source instead of symmetric ones and combination of structure modification with the placement of asymmetric DC source [7]. This section explains the principle of the Level Doubling Network in operation with CHBMLI, as one of the example of Reduced Switch MLI topologies. Furthermore, here will be discussed so called inherent self-balancing capability of the proposed configuration and an approach for sizing of the LDN capacitor will be described.

The general single-phase version of the discussed topology is shown in Figure 2.8. The topology is constructed by adding to a conventional CHB topology an extra half-bridge, which is connected to a capacitor that maintains a half of the HB cell's voltage by a

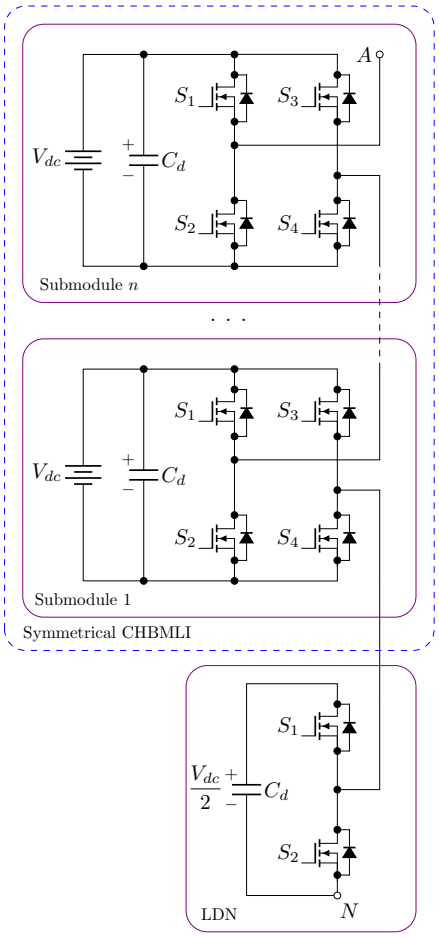


Figure 2.8 – Simplified single-phase circuit diagram of the proposed topology [4]

self-balancing mechanism [4]. It also should be noted that the concept of LDN is valid for any MLI topology reported in literature so far [24] and for their variations [25–27].

Considering just symmetrical CHBMLI circuit depicted in Figure 2.8 and assuming that there are n number of H-bridge submodules (each with a DC bus voltage V_{dc}), then the MLI circuit can generate $2n + 1$ of inverter line-to-neutral voltage without the LDN ($-nV_{dc}$ to nV_{dc} in steps of V_{dc}). By adding to the aforementioned circuit the half-bridge with a pre-charged capacitor of voltage $\frac{V_{dc}}{2}$ (naturally it is not necessary, due to self-balancing mechanism that will be explained later), the new circuit will generate additional n levels in the positive half cycle with inverter output voltages: $\frac{V_{dc}}{2}$, $\frac{3V_{dc}}{2}$, $\frac{5V_{dc}}{2}$,..., $\frac{(2n-1)V_{dc}}{2}$. Similar situation will be observed in the negative half cycle with additional n levels of inverter output voltages: $\frac{-V_{dc}}{2}$, $\frac{-3V_{dc}}{2}$, $\frac{-5V_{dc}}{2}$,..., $\frac{-(2n-1)V_{dc}}{2}$. However, since the additional

levels are created by a positively charged capacitor with regard to neutral point N, in the negative half cycle these extra levels are obtained by algebraically summing the half-bridge voltage $\frac{V_{dc}}{2}$ with generated by the symmetrical CHBMLI circuit voltages: $-V_{dc}$, $-2V_{dc}$,...,$-nV_{dc}$, respectively. It is also important to note that, for n number of voltage cells (H-bridge submodules), the half-wave symmetry restricts maximum number inverter terminal voltage levels in both positive and negative sides to be $4n+1$. Thus, the $\frac{(2n+1)V_{dc}}{2}$ level that is built by connecting all available DC sources in series with LDN capacitor cannot be used. Finally, at the end of one complete cycle, the DC bus voltage

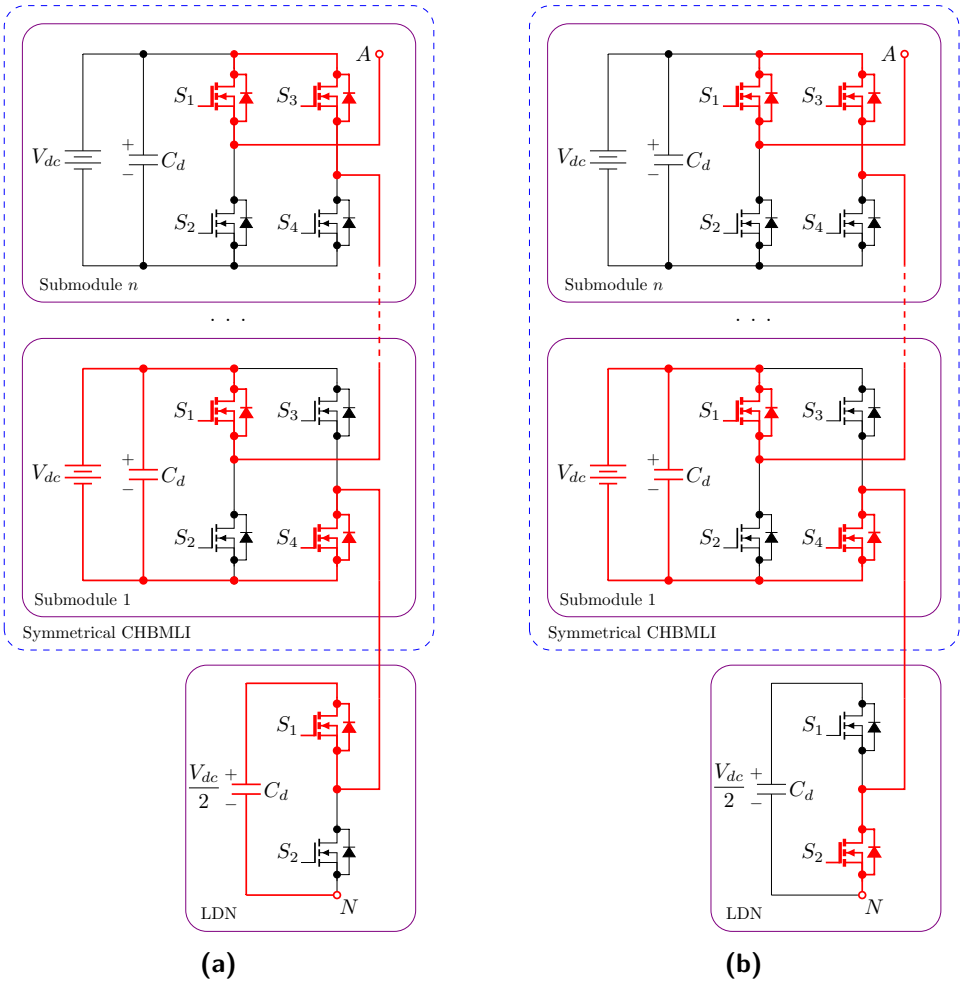


Figure 2.9 – Operating modes of the proposed inverter topology along with LDN for generating positive voltage levels. (a) Positive odd voltage level generated by adding the LDN voltage. (b) Positive even voltage level generated by bypassing the LDN [4]

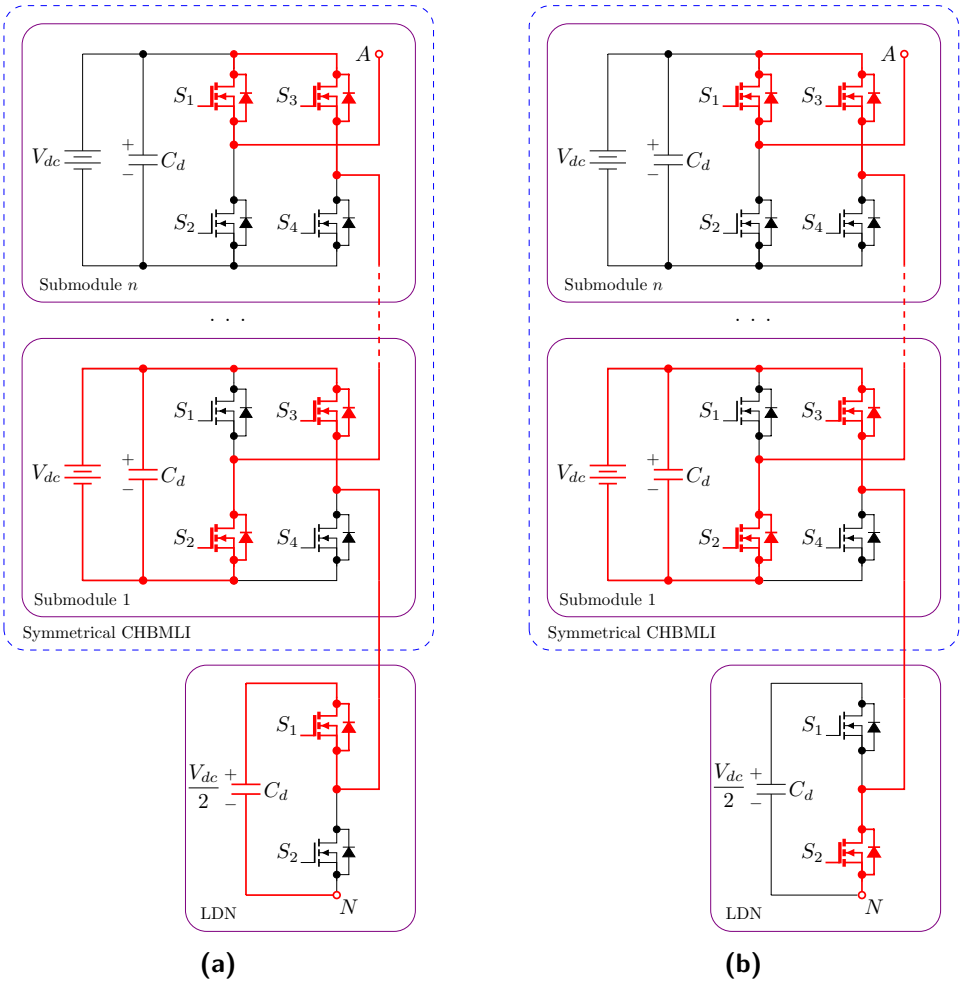


Figure 2.10 – Operating modes of the proposed inverter topology along with LDN for generating negative voltage levels. (a) Negative odd voltage level generated by algebraically adding the positive LDN voltage to negative voltage with respect to inverter neutral point. (b) Negative even voltage level generated by bypassing the LDN [4]

of the LDN module will ideally remain unchanged. This will be valid for any power factor [4].

The described single-phase inverter (similarly, each phase of its three-phase version) may operate in one of the four different modes illustrated in Figures 2.9 and 2.10. When the inverter produces an even voltage level with either positive or negative polarity, the LDN capacitor will be bypassed, as shown in Figures 2.9b and 2.10b. When an odd voltage level is generated, LDN will always be in the circuit, as depicted in Figures 2.9a and 2.10a.

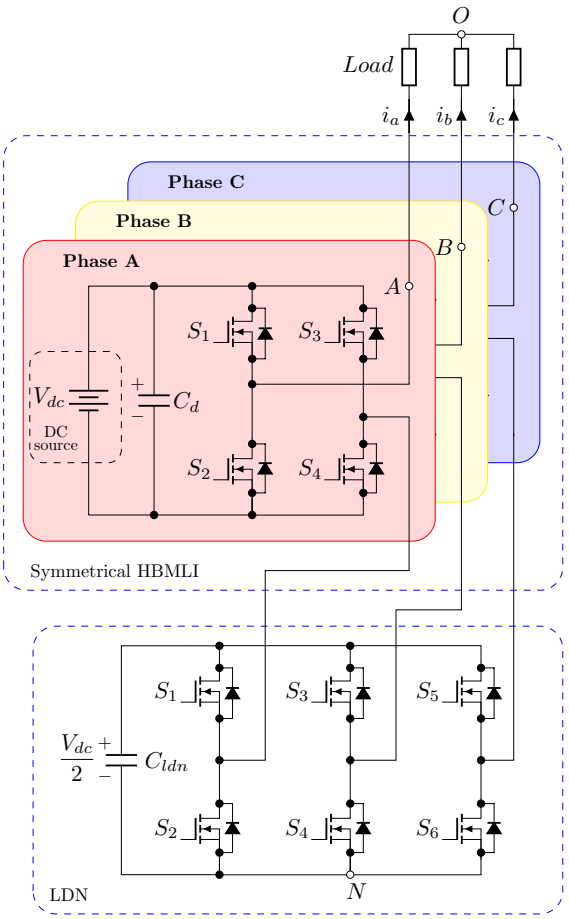


Figure 2.11 – Circuit diagram of the 3-phase five-level HB with LDN MLI[4]

To build a three-phase system as shown in Figure 2.11, three half-bridges (one half-bridge per phase) in parallel are required. Thus, effectively, all three half-bridges share a common DC bus. For a multiphase system, these LDNs of all phases also may be connected to a common DC bus, reducing the DC bus current ripple (with corresponding reduction of LDN capacitance, see Subsection 2.2.4). A switching table per one phase (see Table 2.1) is formed for a circuit configuration represented in Figure 2.11 [4]. Two aspects of the switching operation should be mentioned. Firstly, the 0 and $\frac{V_{dc}}{2}$ levels can be obtained by two combinations of HB module switching states. For instance, to attain the 0 level either S_2, S_4 must be on and S_1, S_3 are off, or similarly S_1, S_3 are on and S_2, S_4 are off. Therefore, these redundant switching states can be utilized to minimize the switching losses of the inverter. Secondly, as it was stated earlier, due to symmetry constraints, the

Table 2.1 – Switching table for one phase of 3-phase five level HB with LDN

Volt. level	Submodule 1A				LDN leg A	
	S_1	S_2	S_3	S_4	S_1	S_2
V_{dc}	1[1]	0	0	1	0	1
$\frac{V_{dc}}{2}$	0	1	0	1	1	0
0	0	1	0	1	0	1
$-\frac{V_{dc}}{2}$	0	1	1	0	1	0
$-V_{dc}$	0	1	1	0	0	1

last possible positive level in the discussed topology ($\frac{3V_{dc}}{2}$) cannot be used, however it is still possible to achieve that.

$$\begin{cases} V_{\mathrm{AB}} = V_{\mathrm{AN}} - V_{\mathrm{BN}} \\ V_{\mathrm{BC}} = V_{\mathrm{BN}} - V_{\mathrm{CN}} \\ V_{\mathrm{CA}} = V_{\mathrm{CN}} - V_{\mathrm{AN}} \end{cases} \tag{2.1}$$

$$\begin{cases} V_{\mathrm{AO}} = \dfrac{V_{\mathrm{AB}} - V_{\mathrm{CA}}}{3} \\ V_{\mathrm{BO}} = \dfrac{V_{\mathrm{BC}} - V_{\mathrm{AB}}}{3} \\ V_{\mathrm{CO}} = \dfrac{V_{\mathrm{CA}} - V_{\mathrm{BC}}}{3} \end{cases} \tag{2.2}$$

The **five-voltage levels** outlined in Table 2.1 are the levels of inverter phase terminal voltage (V_{AN}, V_{BN}, V_{CN}) for the given in Figure 2.11 topology, which are the voltages at terminals A, B and C with respect to the inverter neutral point N, respectively. To obtain line-to-line voltages (V_{AB}, V_{BC}, V_{CA}), set of Equation 2.1 can be used, resulting in a total of **nine-voltage levels**. Furthermore, the output load phase voltages, which are the voltages at terminals A, B and C with respect to the load neutral point O may be determined by a set of Equation 2.2. The calculation will give **seventeen-voltage levels**.

Table 2.2 – Number of voltage levels for three-phase CHBMLI with LDN

V_{AN}, V_{BN}, V_{CN}	V_{AB}, V_{BC}, V_{CA}	V_{AO}, V_{BO}, V_{CO}
$4n+1$	$8n+1$	$16n+1$
m	$2m-1$	$4m-3$

[1]Switching state '0' stands for 'off' and '1' for 'on'.

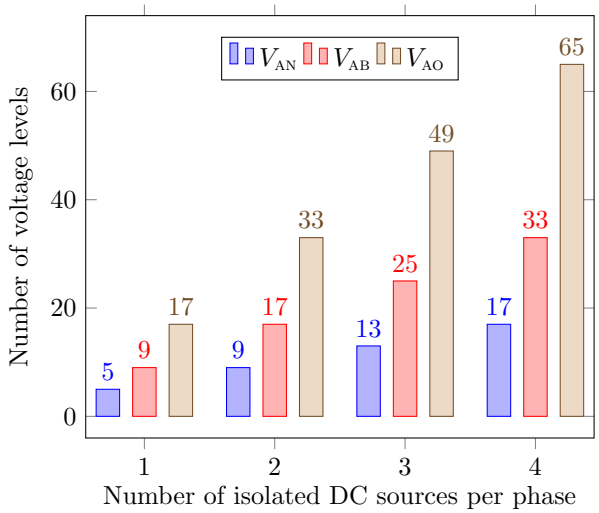


Figure 2.12 – Number of voltage levels vs number of isolated DC sources per phase for three-phase CHBMLI with LDN

In general, for proposed topology, if n is a number of H-bridges with isolated DC sources and m is a number of inverter phase terminal voltage levels, then the available number of voltage levels for each of aforenamed categories can be computed by formulas represented in Table 2.2. Figure 2.12 shows calculated numbers of voltage levels for some variations of 3-phase CHBMLI with LDN.

2.2.2 Energy Balance

In proposed topology, the DC bus of the LDN module does not consume or supply any power. If this delivers a given amount of power in the first half cycle, it will absorb the same amount of power in the next half cycle [4].

Bearing in mind the three-phase topology shown in Figure 2.11 and assuming that the inverter is driving a load with a power factor of $cos\phi$, the aforementioned statement can be proved with some basic assumptions:

- The output voltage and current waveforms have half-wave symmetry.
- A load with back EMF has half-wave symmetry in the back EMF.

There will be $2n$[1] discrete intervals per half cycle when the LDN will apply a positive voltage at its terminal. Note that the LDN will always apply a positive voltage with respect to inverter neutral point N when it will be required to generate an odd voltage level. For the rest intervals, its terminal voltage will be zero [4]. Figure 2.13 represents voltage and current waveforms in a general case of the inverter operation.

The energy delivered/absorbed by the LDN at any i^{th} interval is

$$W_i = VI_m \int_{\theta_{2i-1}\pm\phi}^{\theta_{2i}\pm\phi} sin\theta d\theta \tag{2.3}$$

where I_m is the peak magnitude of the sinusoidal load current; ϕ is the phase difference between the load current and the reference voltage; V is the DC bus voltage.

The energy delivered or absorbed by this network will depend on the sign of the integration [4]. Thus, the total energy delivered in the first half cycle (W_{1st}) and second half cycle (W_{2nd}), respectively, are

$$W_{1st} = VI_m \sum_{i=1}^{2n} \int_{\theta_{2i-1}\pm\phi}^{\theta_{2i}\pm\phi} sin\theta d\theta \tag{2.4}$$

$$W_{2nd} = VI_m \sum_{i=2n+1}^{4n} \int_{\theta_{2i-1}\pm\phi}^{\theta_{2i}\pm\phi} sin\theta d\theta \tag{2.5}$$

Equation 2.5 can be modified to

$$W_{2nd} = VI_m \sum_{i=1}^{2n} \int_{\theta_{4n+2i-1}\pm\phi}^{\theta_{4n+2i}\pm\phi} sin\theta d\theta \tag{2.6}$$

Due to half-wave symmetry of reference voltage signal and consequently output inverter terminal voltage (see Figure 2.13), it may be found that

$$\theta_{4n+1} = \pi + \theta_1, ..., \theta_{8n} = \pi + \theta_{4n} \tag{2.7}$$

[1] n is a number of H-bridges with isolated DC sources.

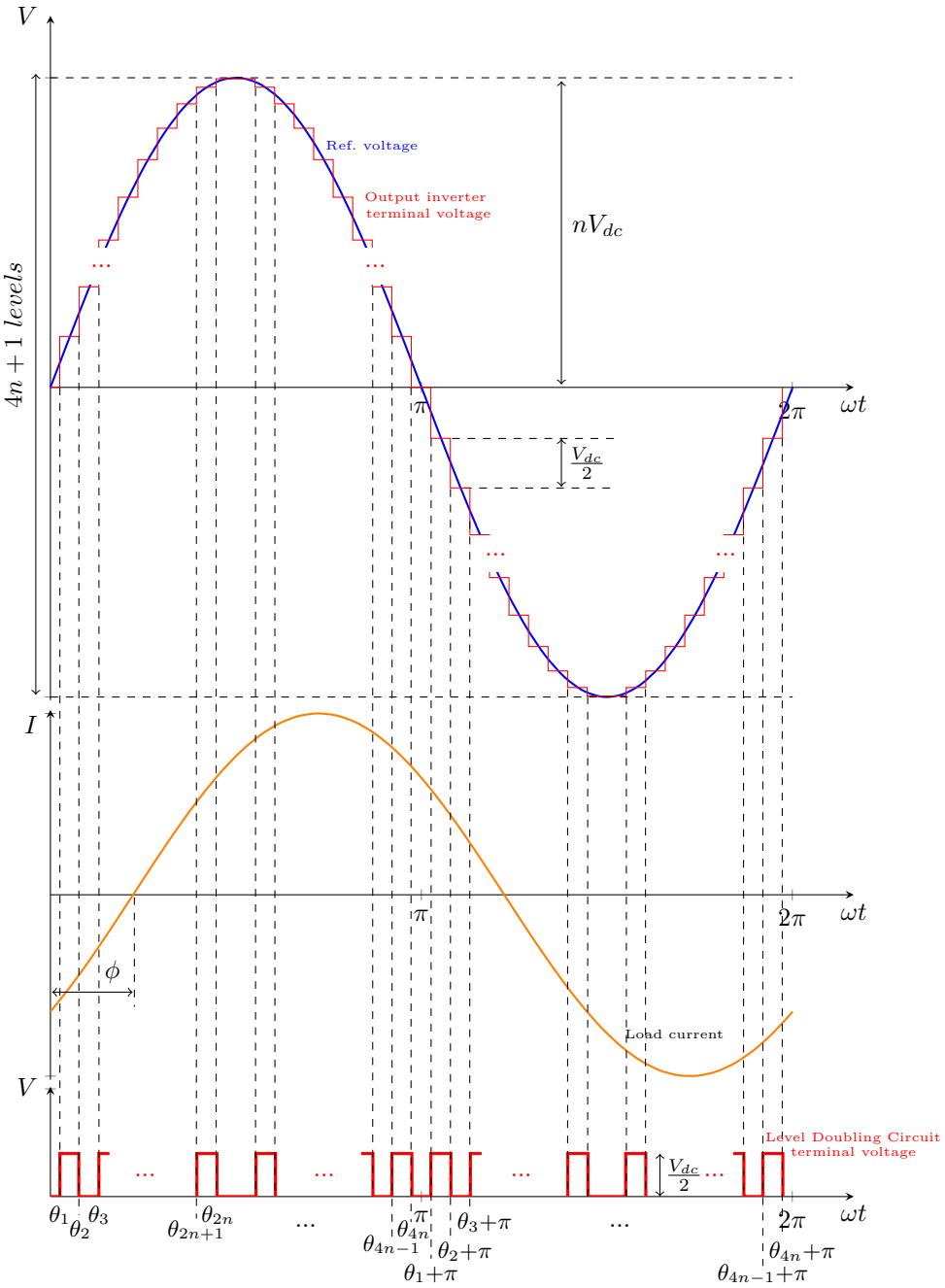


Figure 2.13 – Determining waveform for the LDN [4]

Following this logic, the right-hand-side integrals of 2.6 may be rewritten as

$$\int_{\theta_{4n+2i-1}\pm\phi}^{\theta_{4n+2i}\pm\phi} sin\theta d\theta = \int_{\theta_{\pi+2i-1}\pm\phi}^{\theta_{\pi+2i}\pm\phi} sin\theta d\theta \tag{2.8}$$

Taking into account 2.4, 2.6 and 2.8, finally can be obtained:

$$W_{1st} = -W_{2nd} \tag{2.9}$$

The LDN capacitor absorbs/releases certain amount of energy from/to a circuit in a first half cycle, while it releases/absorbs the same amount of energy to/from the circuit, in the next half cycle [4].

2.2.3 Self-Balancing Capability under Transients and Disturbances

A capacitor in the LDN module is floating. After initial start-up transient conditions and when a steady-state condition is reached, the LDN capacitor only has to supply a small amount of charge to the circuit on each switching cycle. Nevertheless, when any of upper switches in LDN network is turned on/off (since lower ones operate in a complimentary manner), current flowing through the capacitor causes charging and discharging, thus, the capacitor voltage fluctuation occurs. The amount of charge transferred depends upon the load current and the switching frequency. Moreover, during the normal operation some short- and long-term disturbances may occur for a number of reasons. Hence, depending on the application and operational condition there might be high or relatively low voltage deviations from the desired DC bus voltage.

To deal with the obvious capacitor voltage fluctuation, this section presents the self-balancing capability of the LDN capacitor without any closed-loop control [4]. The assumptions for this explanation as they were mentioned in previous section, are:

- Here only single phase configuration is considered.
- The output voltage and current waveforms have half-wave symmetry.
- There is a negligible DC component in the output current waveform under steady state.
- A load with back EMF has half-wave symmetry in the back EMF.

Assuming that the value of desired voltage V_{ldn} that should be maintained at LDN's DC bus is unknown. Also, taking into consideration the case when the proposed single-phase inverter, illustrated in Figure 2.8, feeds a load with complex impedance Z and back EMF E. Therefore, at any n^{th} level of output inverter terminal voltage with LDN in operation it is possible to determine the expression of the net charge delivered/absorbed

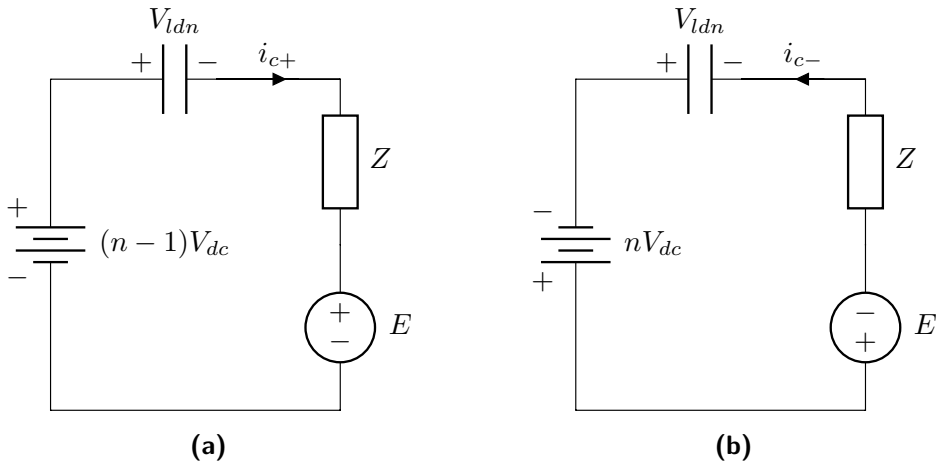


Figure 2.14 – Generalized equivalent circuits of the inverter at any n^{th} level with LDN. (a) Positive half-cycle. (b) Negative half-cycle [4]

by the LDN capacitor in the given interval. Considering, for simplicity, time interval between θ_{2n-1} and θ_{2n} as well as its equivalent in negative half-cycle of output inverter terminal voltage, depicted in Figure 2.13, the following generalized equivalent circuits of the inverter at the positive and negative half-cycles can be obtained, shown in Figures 2.14a and 2.14b, correspondingly.

The net charge delivered/absorbed by the LDN capacitor in the two intervals is [4]:

$$Q = \left[\frac{(n-1)V_{dc} + V_{ldn} \pm E}{Z} + \frac{-nV_{dc} + V_{ldn} \mp E}{Z}\right] T = \left[\frac{(2V_{ldn} - V_{dc})}{Z}\right] T \qquad (2.10)$$

By analyzing Equation 2.10 it can be noticed that if $2V_{ldn} > V_{dc}$, then the capacitor discharges and by doing so, will reduce voltage at its terminals. In case $2V_{ldn} < V_{dc}$, this capacitor gets charges from the circuit, rising its terminal voltage. Therefore, in steady-state, when $Q = 0$ in 2.10, the capacitor terminal voltage will be $V_{ldn} = \frac{V_{dc}}{2}$ that is desired LDN's DC bus voltage and will be reached without any DC bus voltage balancing techniques or an additional closed-loop control [4].

It worthes to mention that in three-phase symmetrical and balanced system without neutral wire, where, by definition, DC components and any harmonics multiple of 3 of the current fundamental cannot circulate (otherwise this system is not symmetrical and balanced), the so called self-balancing mechanism can be explained by the presence of low order even harmonics (2nd, 4th) in both output line-to-neutral voltage and current,

resulting in the interation of corresponding harmonics in current and voltage across the LDN capacitor (V_{ldn}). As a consequence of this interaction the average power is generated. This portion of average power responsible for charging/discharging the LDN capacitor, maintaing voltage across this capacitor around $V_{dc}/2$.

2.2.4 Capacitor Sizing

The electrical performance requirements of LDN's printed circuit board (PCB) and the entire inverter play a big part in determining the amount of capacitance required. Moreover, the size of a capacitor for the LDN circuit is strongly application dependent [4]. The load transient amplitude, voltage deviation requirements, loop stability considerations and capacitor impedance each affects capacitor selection. Other important issues to consider are minimizing PCB area and capacitor cost.

This subsection presents a comprehensive analysis of the DC bus capacitor current in 3-phase CHBMLI with LDN, which provides the basis for the LDN's capacitor sizing. Due to the limitation of this work, the theoretical value of the capacitor for LDN network was calculated just for the five- and nine-level of aforementioned topology. The inverter is assumed to supply a sinusoidal current waveform with magnitude of 25A. The calculation parameters are given in Table 2.3.

The following factors should be taking into consideration for LDN's capacitor selection:

1. The value of output current passing through the capacitor. Since the current comprises several harmonics located at different frequencies, it is necessary to determine the RMS values of all the capacitor current harmonics [8]. The higher the magnitude of the currents, the higher is the LDN capacitor requirements [4].

2. The capacitor current ripples strongly depend on power factor. Therefore, theoretically required capacitance will be calculated for various power angles in order to determine maximum required value.

3. The modulation technique influences on a selection of the capacitor. This calculation will be performed for a case of Level-Shifted PWM with various amplitude modulation indices.

4. The switching frequency another factor that determine the magnitude of the ripple voltage.

5. When the number of phases increases, connecting them to the common LDN DC bus, it dramatically decreases requirements for a LDN capacitor.

Table 2.3 – Capacitor sizing calculation parameters

Calculation parameters	Value	
	Five-level MLI	Nine-level MLI
Number of H-bridges per phase, n	1	2
Inverter structure	Symmetric	
Number of phases at output	3	
Reference signal frequency, f (Hz)	50	
Switching frequency, f_s (kHz)	1	
DC bus voltage of H-bridges, V_{dc} (V)	52.26	
Affordable DC bus voltage oscillation, ΔV (%)	10	
Magnitude of phase current, I_m (A)	25	
Minimum value of LDN capacitance, C_d (mF)	16.8	18.7

The Level Doubling concept works similarly with or without third harmonic injection in phase voltage or its equivalent the Min-Max technique [4]. However, due to limitation of the work and the fact that third harmonic injection reduces the capacitor requirements of LDN [4], further will be considered just a case of standard PWM technique without third harmonic injection. Nevertheless, a MATLAB code for numerical sizing of LDN capacitor given in Appendix A allows to calculate required capacitance with use of THIPWM strategy and its equivalent the Min-Max technique for different multilevel arrangements.

The phase currents of the inverter are given as:

$$\begin{cases} I_{\mathrm{A}}(t) = I_m sin(\omega t) \\ I_{\mathrm{B}}(t) = I_m sin(\omega t - 2\pi/3) \\ I_{\mathrm{C}}(t) = I_m sin(\omega t + 2\pi/3) \end{cases} \tag{2.11}$$

where I_m is the current waveform magnitude, ω is the frequency of the current waveform. Therefore, the currents through the LDN DC bus are [4]:

$$\begin{cases} I^{\mathrm{A}}_{\mathrm{LDN}}(t) = I_{\mathrm{A}}(t) f^{\mathrm{A}}_{\mathrm{LDN}}(t) \\ I^{\mathrm{B}}_{\mathrm{LDN}}(t) = I_{\mathrm{B}}(t) f^{\mathrm{B}}_{\mathrm{LDN}}(t) \\ I^{\mathrm{C}}_{\mathrm{LDN}}(t) = I_{\mathrm{C}}(t) f^{\mathrm{C}}_{\mathrm{LDN}}(t) \end{cases} \tag{2.12}$$

where $f^{\mathrm{A}}_{\mathrm{LDN}}(t)$ is the switching function for phase A (similar for phases B and C). This function is determined by switching pattern of corresponding LDN's leg and varies depending on chosen modulation technique and a number of inverter terminal voltage levels. Formulation of the function in case of Level-Shifted PWM modulation is given in Appendix A.

Due to the fact that in the considered topology, (see Figure 2.11) LDNs' leg are sharing a common DC bus, the current through the capacitor can be calculated as [4]:

$$I_{\mathrm{LDN}} = I^{\mathrm{A}}_{\mathrm{LDN}} + I^{\mathrm{B}}_{\mathrm{LDN}} + I^{\mathrm{C}}_{\mathrm{LDN}} \tag{2.13}$$

This current across the LDN has highly nonlinear behavior due to numerous commutation of the switches in the corresponding leg. However, by sharing a common DC bus, three phase current's waveformes, overlapping each other, construct final waveform of the current [4].

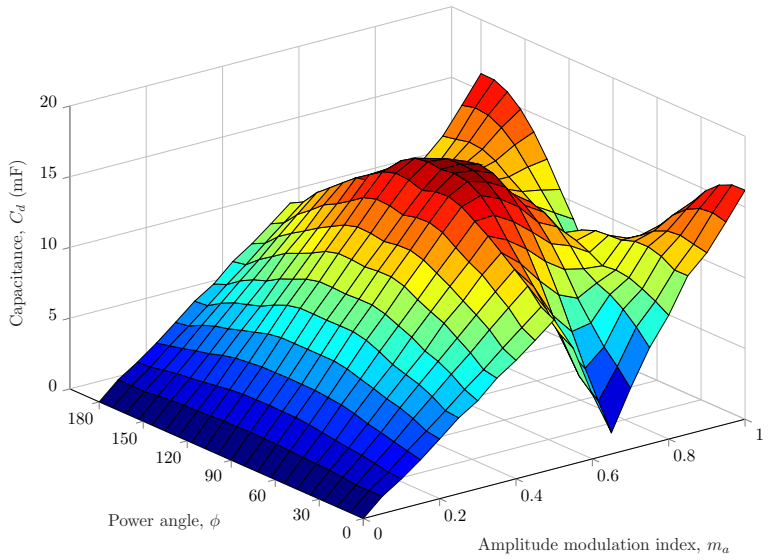
The required capacitance is determined by the affordable amplitude of the DC bus voltage oscillations (ΔV), which also depends on the capacitor current harmonic content. Assuming that, in the worst case, all these harmonics (or equivalently all peaks of voltage harmonics) are in phase, the minimum required capacitance is given by [8]:

$$C_d^{min} = \frac{1}{\Delta V} \sum_h \frac{I_h}{2\pi f_h} \tag{2.14}$$

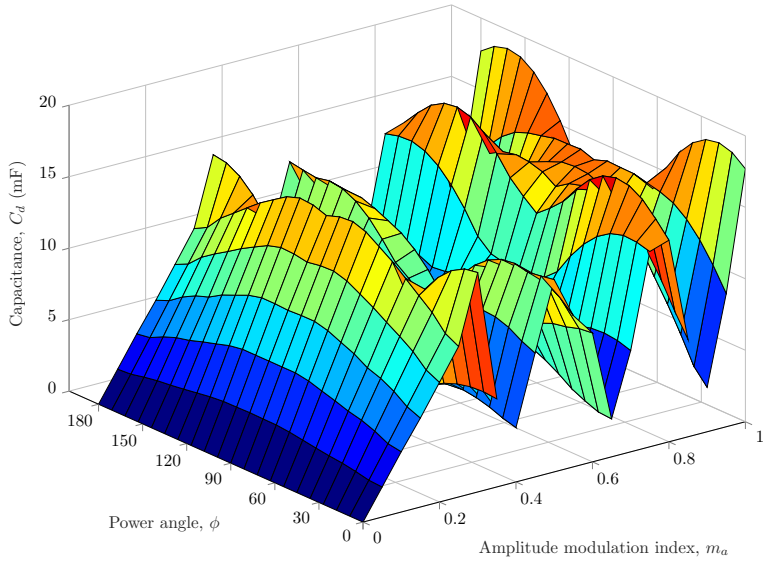
where I_h is the amplitude of current harmonic and f_h its frequency. The sum term in Equation 2.14 corresponds to peak-to-peak net charge produced by the current harmonics.

The required minimum value of LDN capacitance for considered topology, to keep DC bus voltage ripple across LDN in affordable 10% range, can be found from plots represented in Figure 2.15 for corresponding number of voltage levels.

It can be noticed from these plots that the required value of LDN capacitance to a certain extent may vary between different number of inverter terminal voltage levels and moreover, it has a slightly increasing behavior when number of the levels rises. However,



(a)



(b)

Figure 2.15 – Requirements for LDN capacitance as a function of modulation index and power angle. (a) Five-level MLI. (b) Nine-level MLI

for a given value of output current magnitude, it stays around a certain value. It is also clear from the graphs that the ripple currents are higher for both topologies at similar power factor (ϕ approaches to 90°). Nevertheless, their maximum values correspond to different modulation indices due to distinct number of inverter terminal voltage levels.

As it will be shown later, the higher value of the LDN capacitor increases the start-up transient but makes the system less sensitive to load disturbances [4].

One more aspect should be disscussed in this subsection, that one of the primary objective in selecting LDN capacitors is to reduce the ripple voltage amplitude seen at the input of the module. This reduces the RMS ripple current to a level which can be handled by bulk capacitors (normally used electrolytic capacitors). The biggest design limitation for electrolytic capacitors in inverter applications is the amount of ripple current that the electrolytic capacitor can sustain. This limits the design criteria of the designer to figuring out how many individual capacitors are required for a given design rather than the total amount of capacitance that is required [20]. To share the higher amount of ripple current the big LDN capacitance can be commonly achieved through the parallel connection of smaller capacitors.

Ceramic capacitors placed right at the input of the LDN module (in this case between higher and lower switches) reduce ripple voltage amplitude. Only ceramics have the extremely low ESR that is needed to reduce this ripple voltage amplitude. These capacitors must be placed close to the module input pins to be effective [28]. This requirement will be executed later during the PCB design and soldering stages.

2.3 Modulation Strategy

Multilevel converters are mainly controlled with carrier based sinusoidal PWM extended to multiple carrier arrangements of two types: Phase Shifted (PSPWM) and Level Shifted (LSPWM), which includes Phase Disposition (PD-PWM), Phase Opposition Disposition (POD-PWM)and Alternative Phase Opposition Disposition (APOD-PWM) [29]. Other modulation techniques are also applicable (e.g. Space Vector Modulation (SVM)).

Phase Shifted PWM

Phase Shifted PWM is mainly designed for multicell topologies. A multilevel inverter with m voltage levels requires $(m-1)$ triangular carriers. All the triangular carriers have the same frequency and peak-to-peak amplitude, but there is a phase shift between any two adjacent carrier waves, given by [5]

$$\phi_{cr} = \frac{360^\circ}{(m-1)} \tag{2.15}$$

Due to the proper phase shift, all the power cells operate under the same switching conditions and therefore present an even power distribution. This aspect is very important, when cascaded topologies of inverter with isolated sources are used. However, since the carrier signals are not synchronised, the output line-to-line and load voltages have some additional $\frac{dV}{dt}$. This leads to a higher voltage distortion [29]. Reference [5] covers most of the important aspects of this kind of modulation technique.

Level Shifted PWM

Similar to Phase Shifted technique, the Level Shifted multicarrier modulation scheme requires $(m-1)$ triangular carriers, all having the same frequency and amplitude. The triangular carriers are vertically shifted such that the bands they occupy are contiguous [5]. Figure 2.16 shows Level Shifted Pulse-Width Modulation (LSPWM) for five-level inverters. Each carrier is associated to a specific voltage level. When the reference is over one carrier, the corresponding level is generated. Therefore, when LSPWM is used with cascaded H-bridge inverters, the cells will be used only when the corresponding level is reached, producing a uneven power distribution and switching conditions between the cells. This will avoid the current harmonic cancellation at the input, and increase the input current distortion. These harmonics can be important due to the amount of power involved in high power applications, making it more difficult to meet standards [29].

Nevertheless, due to limitation of the current work and the fact that, for the time being, Level Shifted modulation is applied on a test bench of the EEBatt project, therefore, further only Level Shifted modulation will be discussed. However, it is possible to realize other modulation techniques for topologies with LDN [4, 30].

As illustrated in Figure 2.11, the proposed topology consists of standard HB submodules and LDN circuit. To control switches in HB cells, the typical schema of LSPWM should be used. However, to control switches in the LDN module, a special modification must be done.

The modulation method is based on the comparison of a reference signal with the level shifted carriers, segment by segment, generating corresponding level. The modulation principle will be explained for the topology shown in Figure 2.11. Applying a sine reference signal and PD-PWM carriers depicted in Figure 2.16a, it can be easily shown that to follow required switching pattern, summarized in 2.1, the uppermost V_{cr2+} and innermost

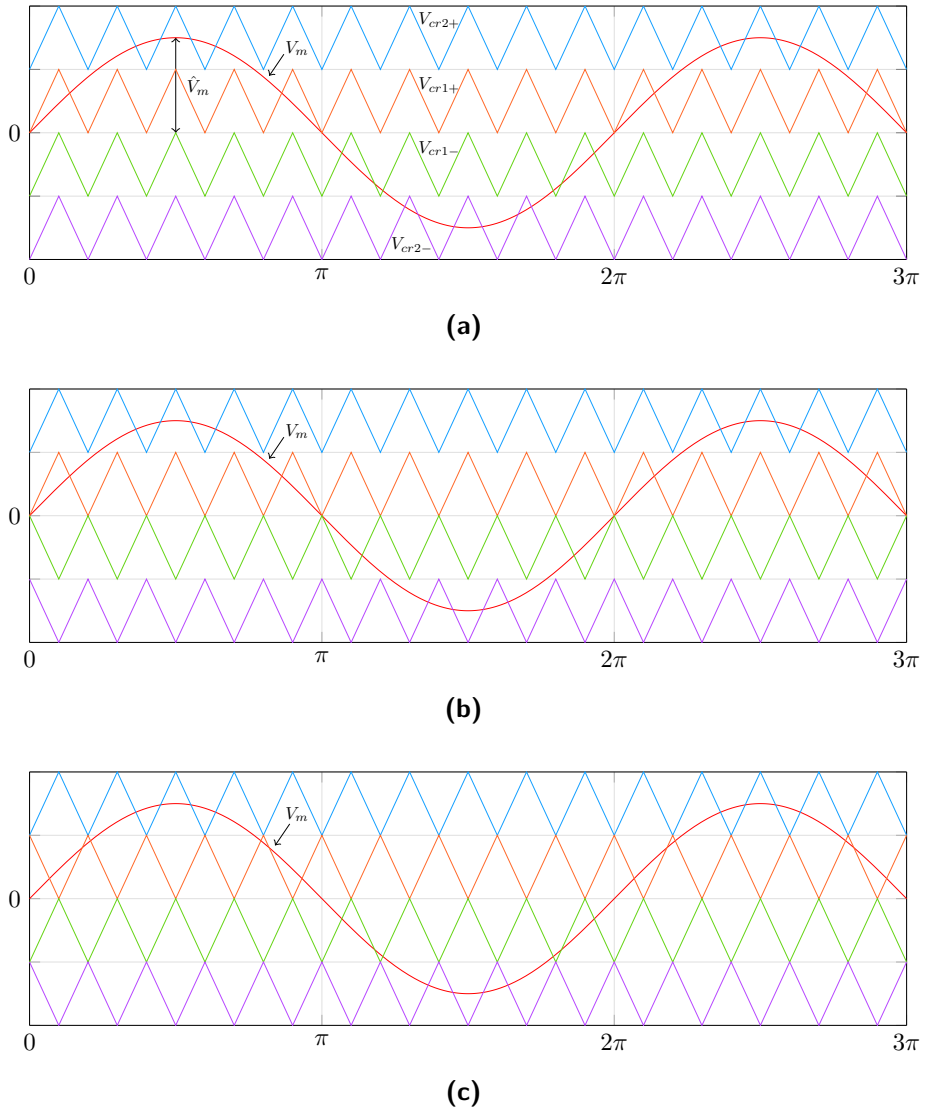


Figure 2.16 – Level Shifted multicarrier modulation for five-level inverters. (a) Phase Disposition (PD-PWM). (b) Phase Opposition Disposition (POD-PWM). (c) Alternative Phase Opposition Disposition (APOD-PWM) [5]

V_{cr1-} carriers are used to generate gatings for switches S_1 and S_4 in HB power cells. The inner switches S_2 and S_3 operate complementarily with S_1 and S_4.

While, to obtain switching sequence of the gate pulses for upper switch S_1 in the LDN module, the sine modulating signal shall be compared with each triangular carrier. For instance, when the instant value of the reference signal is in a range between 0 and 0.5 of its amplitude, and it is less the corresponding value of innermost V_{cr1+} carrier

in the level, than the gate signal to turn on the switch S_1 in the LDN module shall be generated. However, in the range between 0.5 and 1.0 the same comparison must result in the switching state 'off'.

Equation 2.16 represents a mathematical model to compute gate signals for S_1 switch in the LDN module.

$$V_{gt} = (V_m > 0.5) \cdot u_1 + (0 < V_m < 0.5) \cdot u_2 + (-0.5 < V_m < 0) \cdot u_3 + (V_m < -0.5) \cdot u_4$$

$$\begin{aligned} u_1 &= \begin{cases} 1, & \text{if } V_m < V_{cr2+} \\ 0, & \text{otherwise} \end{cases} \qquad u_2 = \begin{cases} 1, & \text{if } V_m > V_{cr1+} \\ 0, & \text{otherwise} \end{cases} \\ u_3 &= \begin{cases} 1, & \text{if } V_m < V_{cr1-} \\ 0, & \text{otherwise} \end{cases} \qquad u_4 = \begin{cases} 1, & \text{if } V_m > V_{cr2-} \\ 0, & \text{otherwise} \end{cases} \end{aligned} \tag{2.16}$$

where '1' is logical true and '0' is false, V_m - reference signal (in p.u.), V_{cr} - level shifted triangular carriers in accordance to Figure 2.16a.

How it can be seen from equation above, this method naturally has one huge drawback, growing complexity of modulation when the number of levels is rasing. With new additional levels to this model, comparison between reference signal and newer carriers shall be added.

2.4 Control Technique

Up to now the basic operational principle and modulation technique were considered for a general case of power inverter application, unless otherwise additionally stated. However, to start discussing control part of the inverter, the particular application should be specified. The current work has been aimed to develop a new topology for a grid-connected inverter as a part of EEbatt project [1]. Figure 1.3 demonstrates a basic block-schema of the proposed circuit. Therefore, from now on, the system will be examined.

A number of Bachelor and Master theses, as well as a variety of research papers were dedicated to a control problem of the system. Most of theoretical aspects, simulations and results of practical experiments for considered so far control techniques can be found in [3, 31]. In this work just Vector Current Control technique will be discussed. The block-diagram of Vector Current Control is shown in Figure 2.17. Inputs to a regulator are

three-phase currents and values of two measured line-to-line voltages from the grid side. Phase voltages are real-time calculated from line-to-line values. After the transformation of actual three phase currents I_{abc} into dq-frame, giving I_{dq}^{act}, these current components are subtracted from their desired reference values I_{dq}^{ref}. Then, the error signal $e = I_{abc}^{ref} - I_{abc}^{act}$ is controlled by PI controller resulting in the reference voltage used for generation of PWM signals. By varying values of d-component I_d and component along q-axis I_q, the control of active power P and reactive power Q can be provided, respectively [21]. Theoretical description of vector representation in stationary $(\alpha - \beta)$ and rotating $(d - q)$ reference frames can be found in [32].

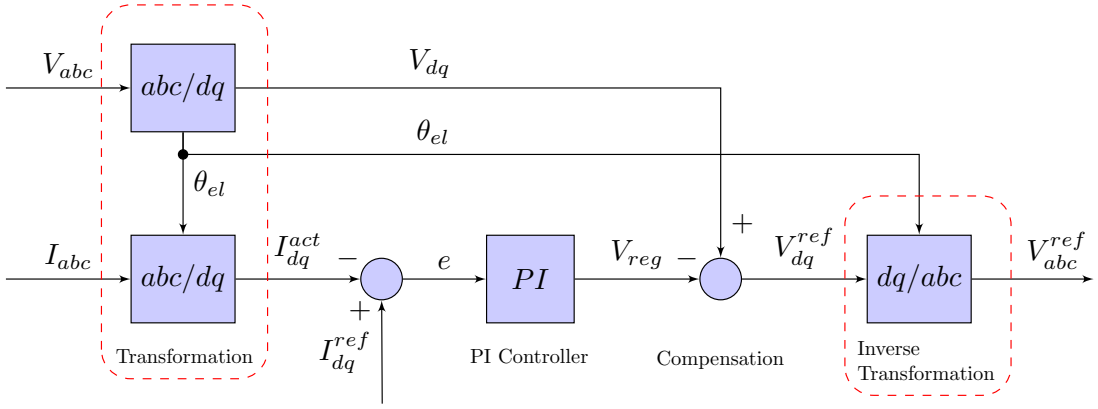


Figure 2.17 – Block-diagram of Vector Current Control technique

As it was shown in Subsection 2.2.3, the LDN circuit does not require any close-loop control. Therefore, by adding a LDN module to the already existing test bench, it will not modify the existing control schema.

2.5 Requirement of Components for MLI Topologies

As it was shown in previous subsections, 'traditional' MLI topologies (DCMLI, FCMLI and CHBMLI) have numerous applications in industry, due to their performance and other beneficial characteristics. However, another quite important characteristic of power electronics, their component requirements, must be considered here. Table 2.4 shows a demand of the main elements of the compared MLIs per phase. It also should be stated that due to the features of considered MLI with LDN only voltage levels m = 5,9,13... can be compared.

Table 2.4 – Requirement of main components for the 3-phase MLI topologies

Components/MLI type	Diode Clamped	Flying Capacitor	Cascaded H-bridge	CHB with LDN[1]
Isolated DC source	1	1	$\frac{3}{2}(m-1)$	$\frac{3}{4}(m-1)$
DC-bus caps	$m-1$	$m-1$	–	1
Active switches	$6(m-1)$	$6(m-1)$	$6(m-1)$	$3(m+1)$
Clamping diodes[2]	$3(m-1)(m-2)$	–	–	–
Clamping caps	–	$\frac{3}{2}(m-1)(m-2)$	–	–
Total	$m(3m-2)$	$\frac{1}{2}(3m+5)-3$	$\frac{15}{2}(m-1)$	$\frac{1}{4}(15m+13)$

Figure 2.18 illustrates total values of components are needed for compared topologies with respect to different number of voltage levels. It can be easily noticed that amount of power electronic elements rise rapidly in case of DCMLI and FCMLI. While, in case of

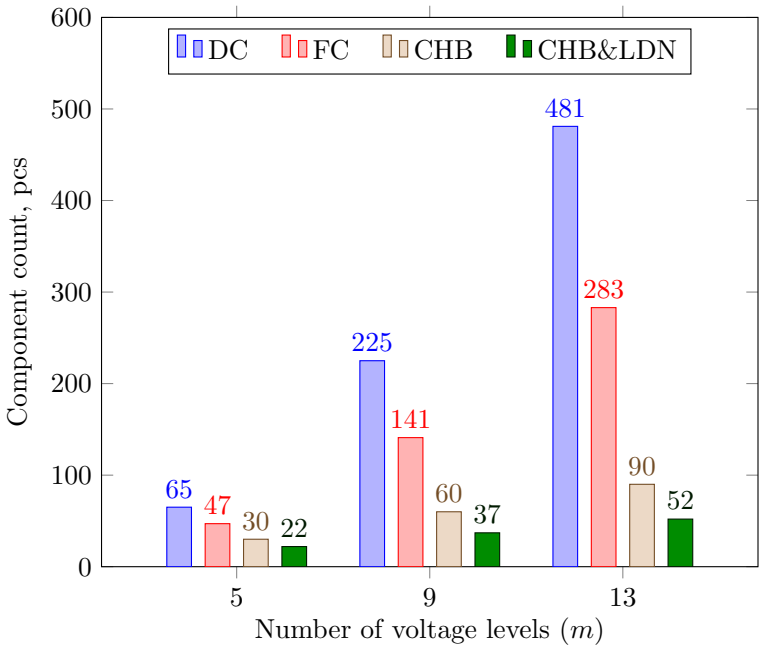


Figure 2.18 – Number of main components for the 3-phase MLI topologies

[1] With m = 5,9,13...
[2] All diodes and active switches have the same voltage rating.

CHBMLI that grow is not so dramatic. However, the difference becomes considerable in comparison with proposed CHBMLI with LDN. For instance, for a MLI that generates 13 voltage levels, component requirements almost twice less for the LDN topology in comparison with 'traditional' CHBMLI.

It will be shown later in Section 4.3 that component count plays a significant role in reliability of a power electronic device.

3 Test Bench for 3-Phase Five-Level HB Multilevel Inverter with LDN

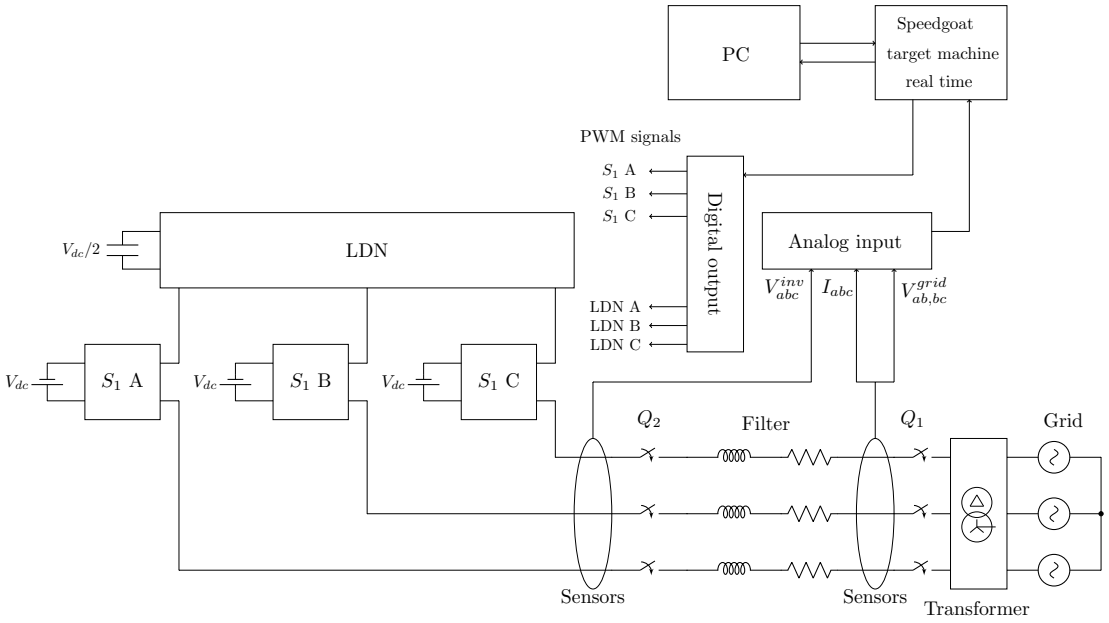


Figure 3.1 – Block-diagram of the test bench

Figure 3.1 shows the block diagram of a grid-tie system, which includes batteries, 3-phase five-level HB inverter with LDN, a series RL-filter (an inductor with internal resistance), voltage and current sensing tools, a microcontroller that combines functions of controller and modulator, and finally grid, which connected through a transformer to adjust grid voltage, minimize short-circuit power, creating 'weak grid'. This transformer has a delta-wye winding connection. It employs a delta-connected winding on its primary and a wye/star connected winding on its secondary. A neutral point O provided on wye output (inverter) side. There are basically tree operational modes of this system that will be considered through the work:'zero current' mode that corresponds to synchronization of

two systems 'grid-inverter/batteries' with no current flowing between them, 'discharging' or 'grid-feeding' mode, where current flows from the inverter side, discharging batteries and 'charging' or 'battery-feeding' mode, where current flows from grid feeding batteries. More details about considering cases and reference sign convention will be given in Chapter 4. In the current work, just a three-level HB inverter connected with LDN submodule, generating overall up to five voltage levels, will be tested.

This section will give the basic information about the components of the test bench, including the set up parameters required for a simulation model, as well as for real experiments. The full datasheet information can be found on manufacturer websites.

3.1 Supply Battery

Each HB submodule is connected to its individual series connected package of lead-acid batteries (overall 4 batteries in the package). The battery specification is given in Table 3.1.

Table 3.1 – Parameters of the Lead-acid battery

Parameter	Value	Unit
Battery type	RS*pro* 537-5488	
Voltage per unit	12	V
Capacity	7.0[1]	Ah
Internal resistance	23	mΩ
Maximum charging current limit	2.1	A
State of charge	100[2]	%

By using a rated voltage per battery, given in Table 3.1 it is possible to determine overall nominal voltage of the package, resulting in 48 V. With given nominal voltage and the State of charge (SoC) value 100%, the fully charged voltage across the battery package is found to be 52.26 V. Therefore, this value of the battery voltage will be taken into the simulation model and calculation of the required capacitance. Also using this value all subsequent plots will be normalized with it.

[1] At 20hr rate to 1.80V per cell and 25°C
[2] At 25°C

3.2 H-bridge Submodule

The simple H-bridge cell consists of two legs with two switching devices in each leg. In Figure 3.2, an HB PCB is depicted.

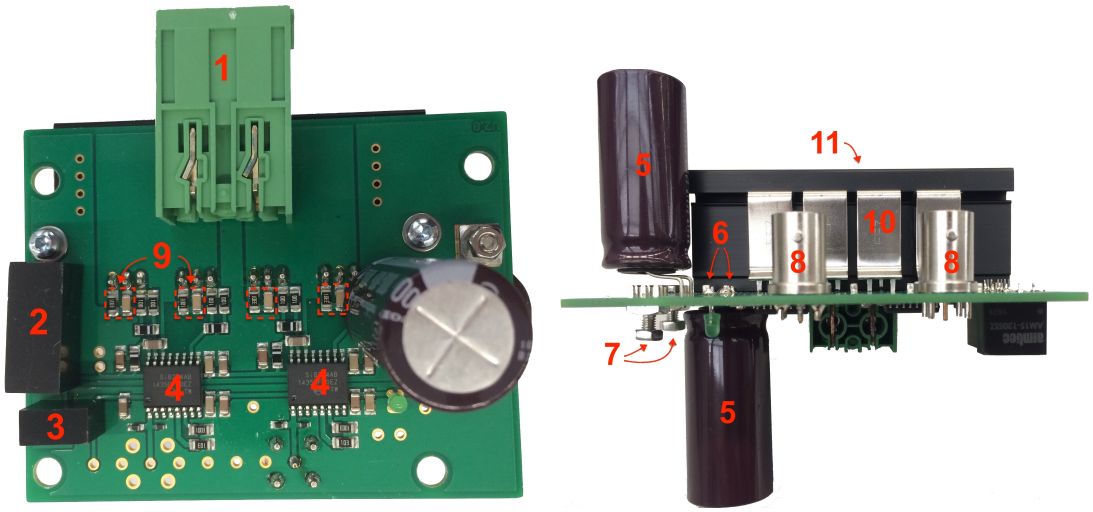


Figure 3.2 – HB printed circuit board overview

The components of the PCB are summarised in Table 3.2.

Positions 2 and 3 indicate isolated DC/DC converters with output voltage 12 V and 5 V, respectively. These converters are particularly used for isolating and converting DC power rails. The galvanic isolation allows those devices to be configured to provide an isolated negative rail in systems where only positive rails exist.

The SI8234AB is a high-side/low-side isolated driver (position 4), which combines two independent, isolated drivers into a single package. All drivers operate with a supply voltage of 12 V. The main purpose of the gate drives in this circuit is to transform an analog signal coming from modulation schema into a gate signal suitable to lead the MOSFETs.

The IPI023NE7N3 G is an isolated N-channel power MOSFET. These switches operate with drain-source voltage up to 75 V and feature simultaneously the lowest ON-state resistances.

Table 3.2 – Components of PCB for an HB submodule

#	Component	Type	Specification
1	AC output terminals	-	-
2	Isolated single output DC/DC converter	TMR 6-4812WI (Traco Power)	Input: 18-75 VDC, Output: 12 VDC, 500 mA
3	Isolated single output DC/DC converter	AM1S-1205SZ (Aimtec)	Input: 10.8-13.2 VDC, Output: 5 VDC, 200 mA
4	Isolated high-side/low-side gate driver	SI8234AB-D-IS (Silicon Lab)	peak current 4.0A
5	Electrolytic capacitor	UVY2A102M (Nichicon)	1000 μF ±20%, 100 V
6	Ceramic capacitor	C5750X7S2A106M230KB (TDK)	10 μF ±10%, 100 V, 1206
7	DC input terminals	-	48 VDC
8	PWM input terminals	-	-
9	RC snubbers	CRG1206F3K3 (TE Connectivity) CC1206KRX7R0BB472 (Yageo)	3.3 kΩ, ±1% 0.25 W, 1206 4.7 nF ±10%, 100 V, 1206
10	MOSFET	IPI023NE7N3 G (Infineon)	n-channel, 120 A, 75 V, 2.3 mΩ
11	Heat sink	KUEHKOERPER (Fischer Elektronik)	3.5 K/W

3.3 LDN Submodule

The LDN submodule takes form of a half-bridge inverter, the DC terminals of which connected to a capacitor (or series connected capacitors). Figure 3.3 demonstrates a PCB of LDN submodule.

Table 3.3 – Components of PCB for a LDN submodule

#	Component	Type	Specification
5	Electrolytic capacitor	WCAP-ATUL (Wurth Elektronik)	820 μF ±20%, 100 V
12	DC input terminals	-	18-75 VDC
13	DC output terminals	-	12 VDC
14	DC output terminals	-	5 VDC

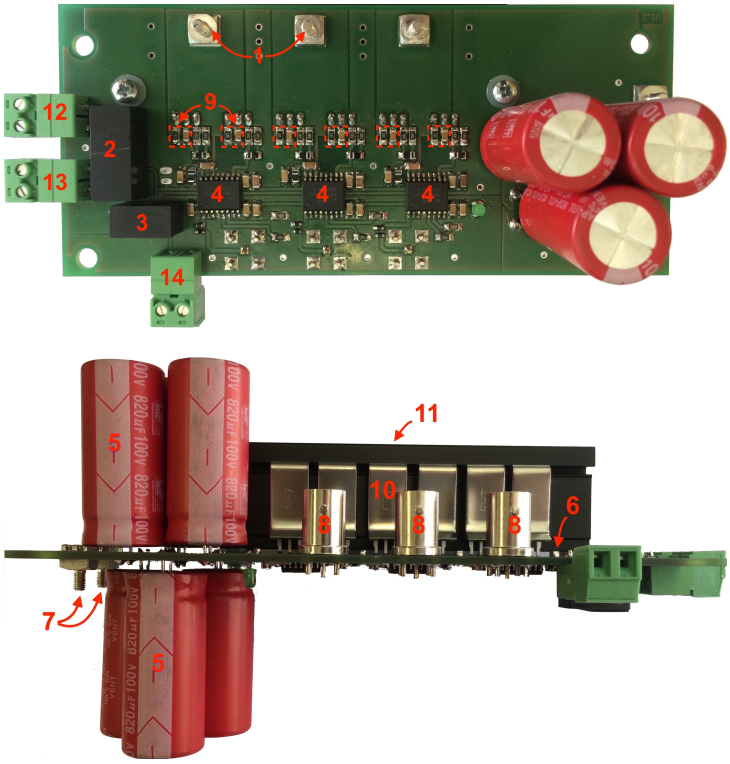


Figure 3.3 – LDN printed circuit board overview

It can be easily distinguished that the LDN submodule consists of the same power electronic components that are used in HB submodule described in previous subsection. That is another benefit of proposed topology. Moreover, taking into consideration the fact that voltage stress on the main components as twice less as in HB submodule, then all these components can be selected with reduced electrical characteristics.

Most of the components of the LDN submodule are also summarised in Table 3.2. Rest of them that are not mentioned or have to be changed are given in Table 3.3.

The LDN submodule was designed and manufactured in the framework of the present work. The schematics and layout for it can be found in Appendix B.

3.4 Output Filter

To cancel out high-frequency harmonics caused by pulsewidth modulation, a three-phase RL-filter (where R is internal resistance of an inductor) is used. A grid-connected inverter

has different harmonic spectra on the converter side of the passive filter, possible resonance conditions (due to the interaction of the filter with the system impedance), or variation of the harmonic emission with the operating point of the power converter. Therefore, parameters of a passive filter must be selected very carefully. The design procedure was described in [33]. Currently, the filter, used in the test bench, operates with parameters summarized in Table 3.4.

Table 3.4 – Parameters of the filter

Parameter	Value	Unit
Filter type	RNDr 30 (Michael Riedel Transformatorenbau GmbH)	
Rated voltage	3x400 (AC)	V
Rated current	30.0	A
Operating frequency	50/60	Hz
Internal resistance	3x37.3 ±10%	mΩ
Inductance	4	mH

3.5 Grid Transformer

Essentially, that is the main task of the transformer in this circuit, converting low voltage and high current from the primary side to the high voltage and low current on the secondary side and vice versa. The windings notation was selected based on a load sign convention, where 'inverter/battaries' structure considers as a consumer. Also, the transformer with its operation principle provides galvanic isolation between grid and the test bench.

The transformer has a delta-wye winding connection. It employs a delta-connected winding on its primary and a wye/star connected winding on its secondary. A neutral point O provided on wye output (inverter) side. The transformer parameters are given in Table 3.5.

Table 3.5 – Parameters of the transformer

Parameter	Value	Unit
Transformer type	DRV 66 178	
Rated power	47.8	kVA
Operating frequency	50	Hz
Primary winding		
Connection	delta (Δ)	
Rated voltage	231	V
Operating current range	$0 \div 119.5$	A
Secondary winding		
Connection	wye (Y)	
Rated voltage	400	V
Operating current range	$0 \div 69$	A

3.6 Voltage and Current Transducers

To control the inverter for desired operation, voltage and current values required to be sensed for processing by the digital controller.

Table 3.6 – Parameters of the voltage transducer [34]

Parameter	Value	Unit
Transducer type	LV 25-600	
Primary nominal rms voltage	600	V
Primary voltage, measuring range	$0 \ldots \pm 900$	V
Primary nominal rms current	10	mA
Secondary nominal rms current	25	mA
Conversion ratio	600 V : 25 mA	
Overall accuracy $T_a = 25°C$	± 0.8	%
Linearity error	< 0.2	%

The design of the test bench implements sensing scheme based on voltage transducer LV 25-600 and magneto-resistive current sensor demoboard CMK3000 with PCB-mountable

CMS current sensors that has a typical bandwidth of 2 MHz. The voltage sensor is able to measure DC, AC and pulsed voltage with galvanic separation between the primary and secondary circuits. The main parameters of the voltage transducer are specified in Table 3.6.

The CMS3000 current sensor is designed for highly dynamic electronic measurement of DC, AC, pulsed and mixed currents with integrated galvanic isolation. The Magneto-Resistive technology enables an excellent dynamic response without the hysteresis that is present in iron core based designs. The principal parameters of the current sensor are given in Table 3.7.

Table 3.7 – Parameters of the current sensor [35]

Parameter	Value	Unit
Sensor type	CMS3050ABA	
Primary nominal *rms* current	50	A
Primary current, measuring range	0 ± 200	A
System *rms* voltage	300	V
Frequency bandwidth (-3 dB)	2	MHz
Overall accuracy $T_a = 25°C$	± 0.8	%
Linearity error	± 0.15	%

Table 3.8 – Parameters of the oscilloscopes [36]

Parameter	Value		Unit
Oscilloscope type	TPS2014B	TPS2024B	-
Bandwidth	100	200	MHz
Isolated Channels	4		-
Sample rate	1	2	GS/s
Record length	2500		points
Probes	TPP0101 100 MHz, 10X	TPP0201 200 MHz, 10X	-
Current probe/BNC	C35 (Chauvin-Arnoux) 10-100-1000A/V 1200 A, 100 kHz AC/DC		

All measured data acquired by digital oscilloscopes Tektronix, basic information of which summarazed in Table 3.8. Unintentionally grounding a circuit under test is a common cause of poor measurement results and circuit damage. Connecting two or more grounded

probes can cause ground loops, and if the current is high enough can result in ruined components and equipment. Most importantly, taking floating measurements without the proper instruments and probes can pose a safety hazard. Input connector shells of used oscilloscopes are isolated from each other and from earth ground, allowing to take measurements safely.

Other specific parameters can be found in corresponding datasheets on websites of the manufacturers.

3.7 Real-Time Target Machine

The Real-time target machine RTTM is expressly designed for Simulink Real-Time for a seamless workflow [37] and represents the interface between the hardware and software parts of the test bench. With Simulink Real-Time it is possible to extend a Simulink simulation model with driver blocks, automatically generate real-time applications, define instrumentation, and perform interactive or automated runs on a RTTM equipped with a real-time kernel, multicore central processing unit (CPU), input/output (I/O) and protocol interfaces, and field programmable gate arrays (FPGAs)[38]. Thus, this configuration allows to collect information from the grid through the analog input IO106-64/32-MDR and to send corresponding PWM signals to each submodule in the inverter through the digital output block IO316-100k as shown in Figure 3.1.

Moreover, a RTTM has scope functions that allow real-time monitoring of the system:

- **Target scope** that visualize real-time behavior of the system variables and measured signals at an external screen.
- **File scope** that collects data during the real-time runs with high sampling frequency in a file and allow later processing of the information.

It is also important to underline that the ground terminal of RTTM is connected to the ground of the measurement system [33].

4 Results and Comparison

The performance of 3Ph5L HB inverter with LDN is evaluated by simulating the corresponding circuit in MATLAB/Simulink. The output voltage and current waveforms together with their THDs (TDDs) are analyzed in detail. Moreover, performance of the LDN submodule itself is investigated. Table 4.1 shows main parameters used for simulation.

The simulation results are verified by operating a prototype of symmetric 3Ph5L HB inverter with LDN. The major parameters of the hardware setup are also taken from Table 4.1.

Later, behavior of 3Ph5L CHBMLI is examined to check an operational equivalence between aforementioned topologies.

For a lower modulation index, the inverter output voltage will have a lower number of levels. Fundamental switching frequency with a lower number of levels will result in higher TDD of the current output [4]. However, due to limitation of current work along with hardware constrains, solely Level Shifted PWM modulation will be examined and implemented. This modulation will be carried out with switching frequency at 1 kHz and unity modulation index only. Nevertheless, this fact helps verify operational behavior of proposed topology at relatively low switching frequency.

From now on it will be assumed that the system 'grid-inverter/battery' operates, based on the load sign convention. In other words, 'inverter/battery' side considers to be a consumer, while 'grid' is a supplier.

To validate the concept, there are three operating modes must be studied:

- **'Zero current'** mode. It corresponds to grid connected inverter with no current circulating between two systems. The d component of the controlled current in per unit system is kept to be zero ($I_d = 0$).

Table 4.1 – Simulation and hardware setup details

Parameters	Value
Grid Parameters	
Line-to-neutral voltage ('charging' mode), V_{rms} (V)	40(65)
Frequency, f (Hz)	50
Power angle, ϕ (deg)	0
3-phase short-circuit level at base voltage, S_{sc} (MVA)	1
Reactance to Resistance ratio, X/R	2.0
Filter Parameters	
Resistance, R_f (mΩ)	3 x 37.3
Inductance, L_f (mH)	4
Inverter Parameters	
Number of H-bridges per phase, n	1
Number of phases at output	3
Switching frequency, f_s (kHz)	1
H-bridge DC bus capacitance, C_{hb} (mF)	2.1
LDN capacitance, C_d (mF)	16.56
Battery Parameters	
Fully charged DC voltage, V_{dc} (V)	52.26
Effective current, I_{eff} (A)	9.9

- **'Discharging'** mode. This mode represents the case when batteries supply power grid with rated current. The d component of the controlled current in per unit system is -1 ($I_d = -1$).

- **'Charging'** mode. This mode is equivalent to the case when the power grid charges batteries with rated current. The d component of the controlled current in per unit system is 1 ($I_d = 1$).

Due to distinct performance of inverter, there are two different cases can be considered: neutral points of grid and inverter sides are connected to each other, forming 'one neutral point'; 'floating neutral point' - neutral points of grid and inverter sides are disconnected

from one another. A floating 3-phase wye-connected grid means the phase leg models are no longer independent because line-to-neutral voltage from grid side now depends on the switched voltages of the three phase legs (see detailed explanation in Subsection 2.2.1). Thus, because of an obvious advantage to gain more voltage levels and as a consequence lower voltage and current THDs (TDDs), further only 'floating neutral point' case will be investigated.

4.1 3-Phase Five-Level HB Inverter with LDN

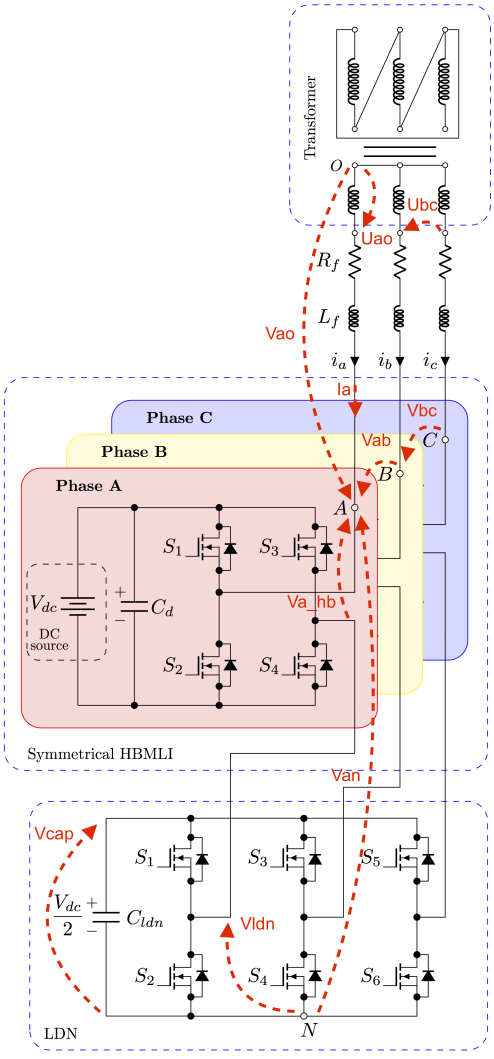


Figure 4.1 – Circuit diagram of the 3-phase five-level HB inverter with LDN

A symmetric CHBMLI test bench, that is available in the university laboratory, is reconfigured to operate as proposed inverter. Figure 4.1 shows a circuit diagram of the 3-phase five-level HB inverter with LDN that has been tested. To have better understanding what voltages and currents will be discussed in subsequent subsections, there are also illustrated measured quantities.

'Zero current' mode

As it is stated in Table 4.1, all measurements, except 'charging' mode, are taken with RMS value of grid voltage equals to 40 V. This value is the reference voltage for the vector control used in the inverter and it is not enough to form desired nine levels of line-to-line voltage. To obtain all nine levels, the V_{rms} should be set to 60 V. The corresponding voltage waveform is shown in Figure 4.1. As it can be noticed, the waveforms are obtained from experiment very good correlate with ones gained from the simulation.

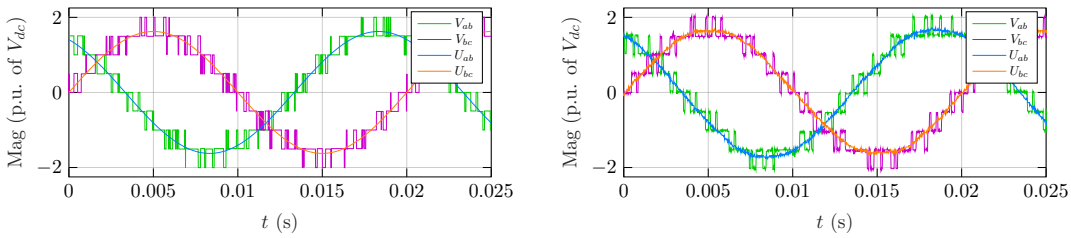


Figure 4.2 – Normalized line-to-line voltages from grid side (U_{ab}, U_{bc}) and inverter side (V_{ab}, V_{bc}), V_{rms} =60 V: (a) Simulation (b) Experiment

Further, unless otherwise specified, the RMS value of grid voltage that equals to 40 V, will be considered only. The corresponding waveforms are captured in Figure C.1. The THD analysis is given in Figure C.2. There, seven levels at line-to-line voltage can be observed in both, simulation and experiment. A comparison between waveforms shows quite reasonable matching. The fundamental component in simulation/experiment has magnitude 59.17/59.40 V. Since there is no standards regulating line-to-line harmonic content, later only waveform equivalence will be checked.

In Figure 4.3 normalized voltages and current, obtained from simulation and measured during the experiment condition, are depicted. As it can be seen, the results are also in agreement between each other. The inverter phase voltage has exactly five levels, as it was

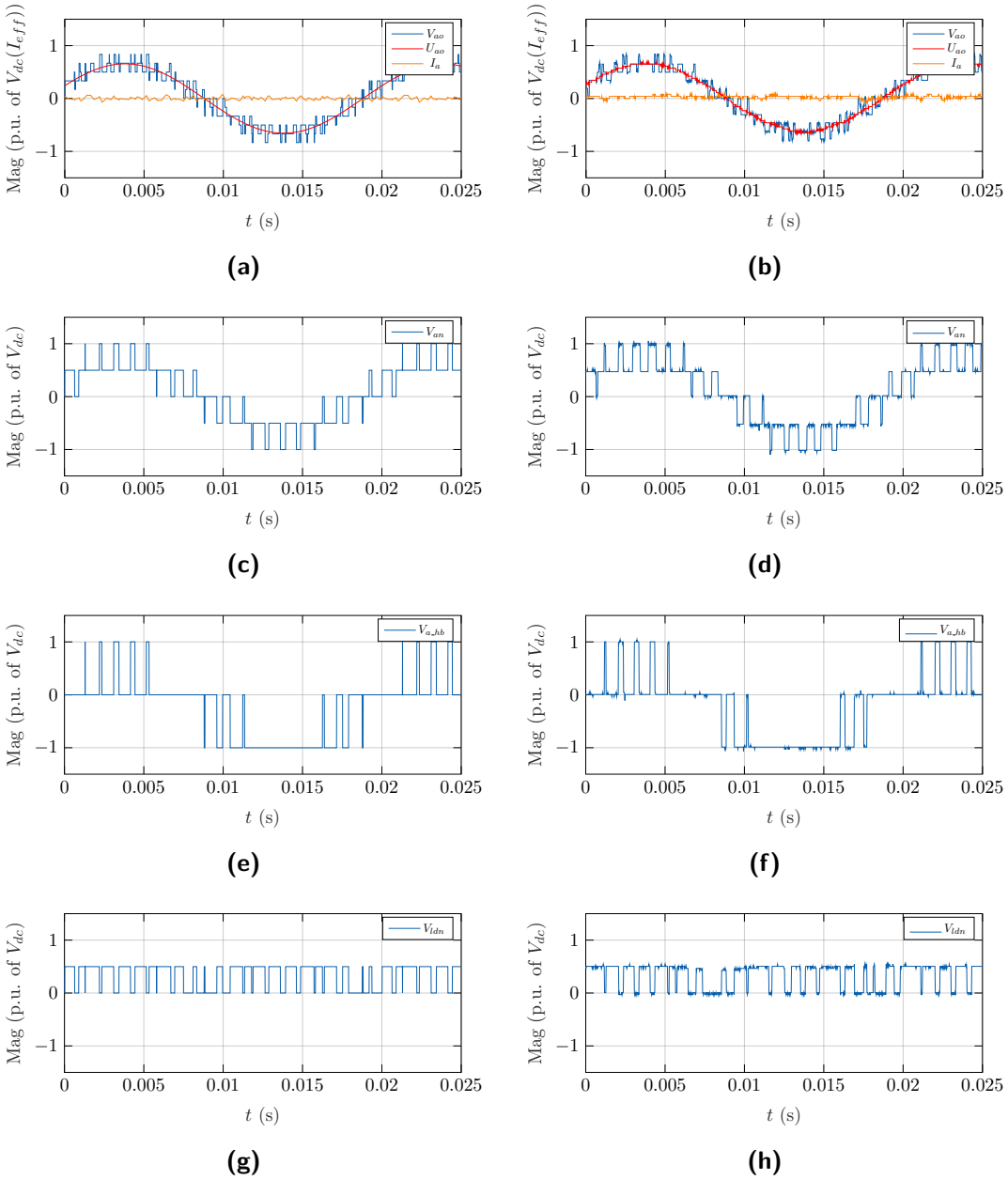


Figure 4.3 – Normalized grid line-to-neutral voltage (U_{ao}), inverter line-to-neutral voltage (V_{ao}) and current (I_a): (a) Simulation (b) Experiment. Normalized inverter phase voltage (V_{an}) (c) Simulation (d) Experiment. Normalized voltage across the HB, phase A (V_{a_hb}) (e) Simulation (f) Experiment. Normalized voltage across the LDN, phase A (V_{a_ldn}) (g) Simulation (h) Experiment

predicted in theory. It also interesting to see the formation of those levels from voltage across the HB (V_{a_hb}) and voltage across the LDN (V_{a_ldn}) for phase A. Operation of HB and LDN submodules in the inverter complies with expected behavior. Therefore, an inverter line-to-neutral voltage (V_{ao}) is accurately tracking the reference - a grid line-to-neutral voltage (U_{ao}). The THD comparison is given in Figure 4.4. It can be seen that magnitudes of the fundamental component lies pretty close, therefore the harmonic contents can be compared. Overall, the harmonic spectrum from both simulation and experiment looks pretty much similar. There are small difference between voltage THD, due to uncertainties of real application (true values of resistance, inductance, capacitance), conducted measurements (accuracy errors, ambient temperature, EMI, etc.). Nevertheless, those values are quite close to each other.

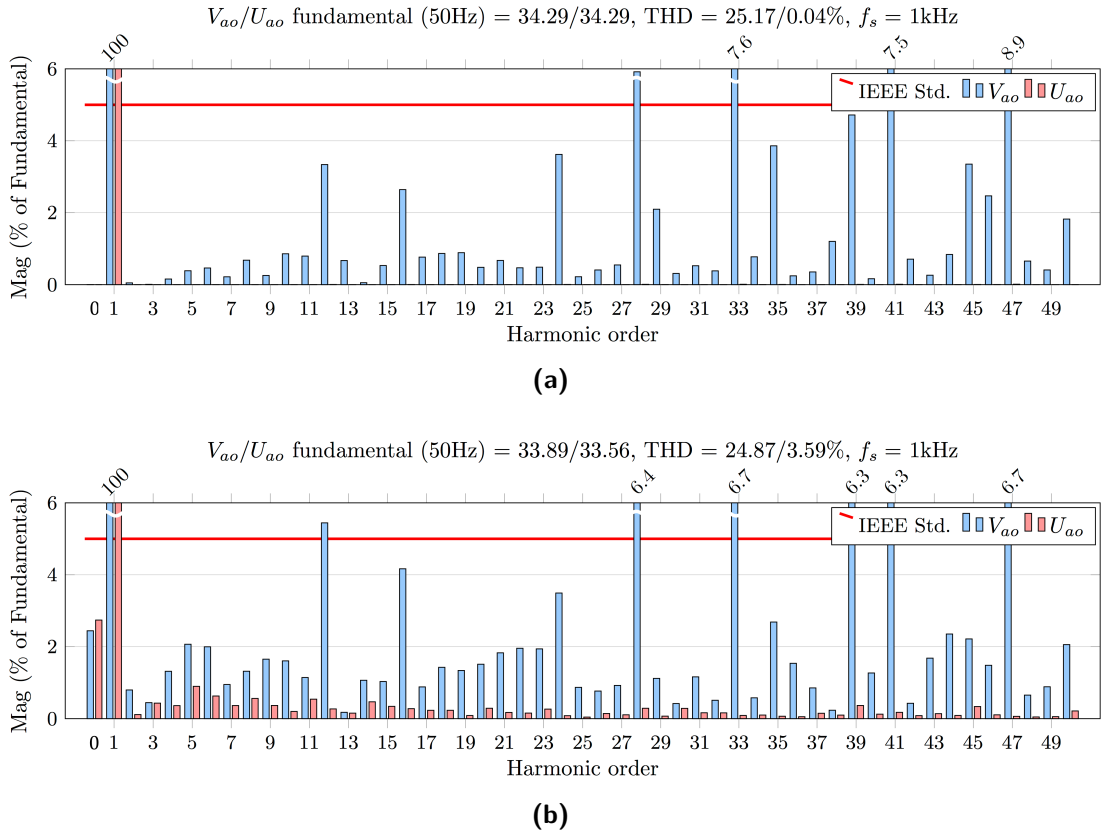
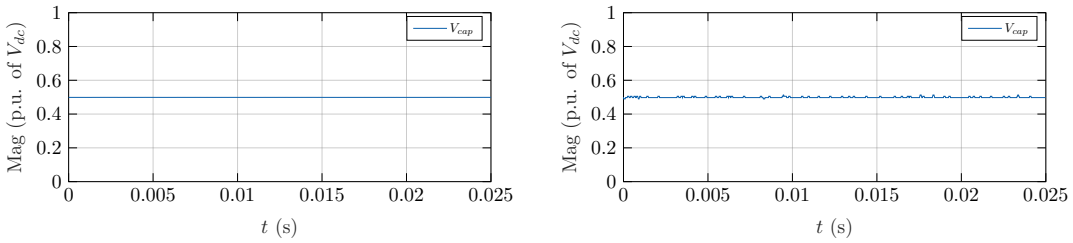


Figure 4.4 – Harmonic content of line-to-neutral voltages from grid side (U_{ao}) and inverter side (V_{ao}): (a) Simulation (b) Experiment

Another aspect to mention, that according to IEEE Standard 519-2014 such a topology cannot be directly connected to the grid, due to high harmonic distortion (THD must be



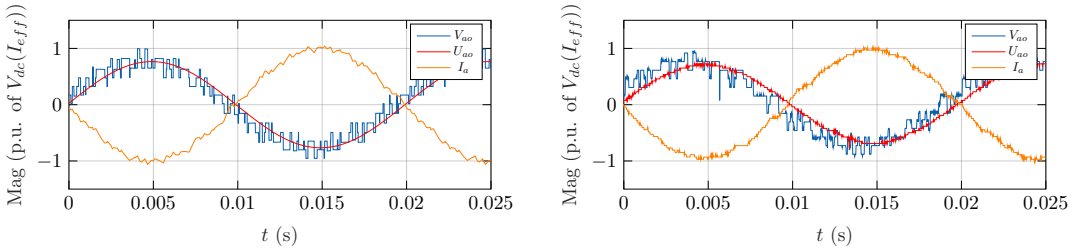
(a) **(b)**

Figure 4.5 – Normalized voltage across the LDN capacitor (V_{cap}): (a) Simulation (b) Experiment

$< 8.0\%$, individual harmonics - $< 5.0\%$ (highlighted by a red line on each voltage plot)) of line-to-neutral voltage at a point of common coupling (PCC). However, applying a first order filter with nominal parameters, given in Table 4.1, will greatly improve harmonic content and allow to meet the standard.

Figure 4.5 demonstrates measurements of voltage across the LDN capacitor (V_{cap}). As it can be seen from simulation and verified from test ideally the voltage must remain constant around 0.5 p.u. (26.13 V). However, because of distinct voltage at batteries terminals and values of their SoC, small fluctuation is possible. Nonetheless, owing to self-balancing capability of the LDN capacitor voltage across it stays in the range 0.482-0.513 p.u. ($-3.6 \div 2.6\%$), which is less than affordable 10% deviation.

'Discharging' mode



(a) **(b)**

Figure 4.6 – Normalized grid line-to-neutral voltage (U_{ao}), inverter line-to-neutral voltage (V_{ao}) and current (I_a): (a) Simulation (b) Experiment

'Discharging' mode is characterized by power flow from batteries to the grid. Due to another limitation point of the present work, the unity power factor was considered

only. Therefore, phase shift between line-to-neutral voltage and current in corresponding phase must be 180 deg. Figure 4.6 confirms this expectation. The simulation results also in acceptable extent correlate with those obtained from test, despite greater phase shift between grid line-to-neutral (U_{ao}) and inverter line-to-neutral(V_{ao}) voltages, in experiment, and needed to keep required power flow between two systems. The current waveform has nearly sinusoidal shape.

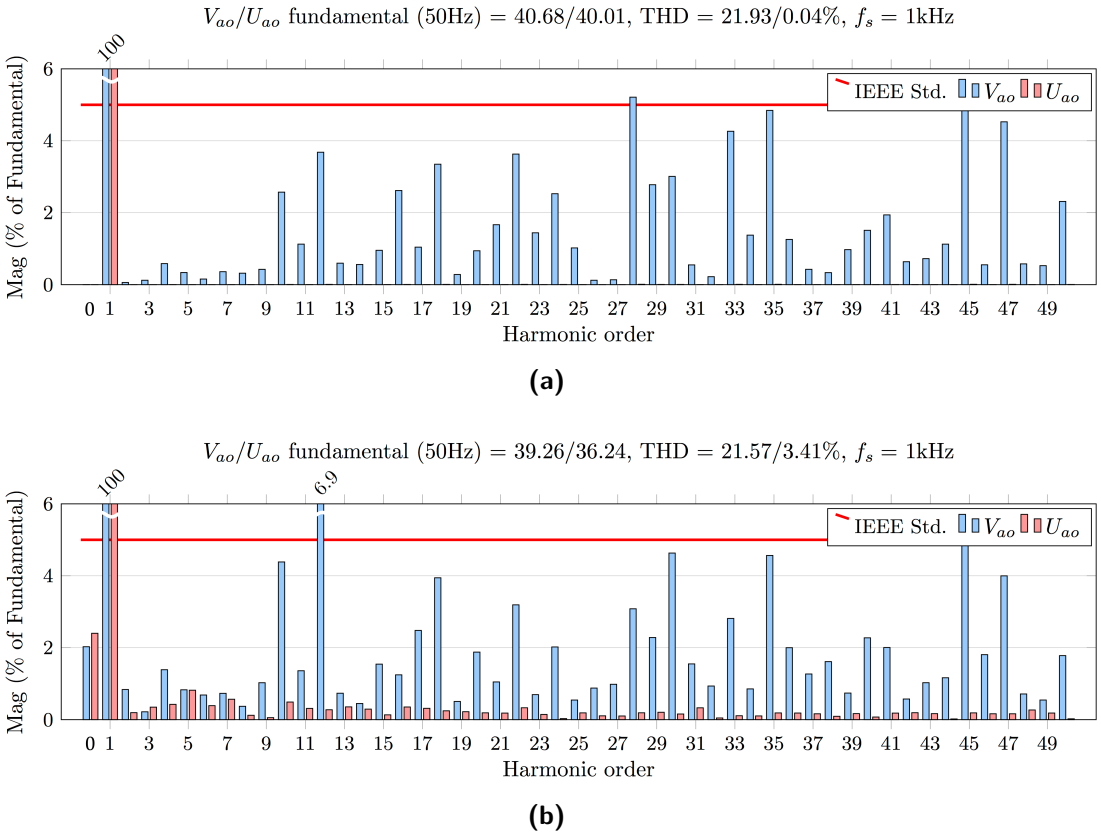
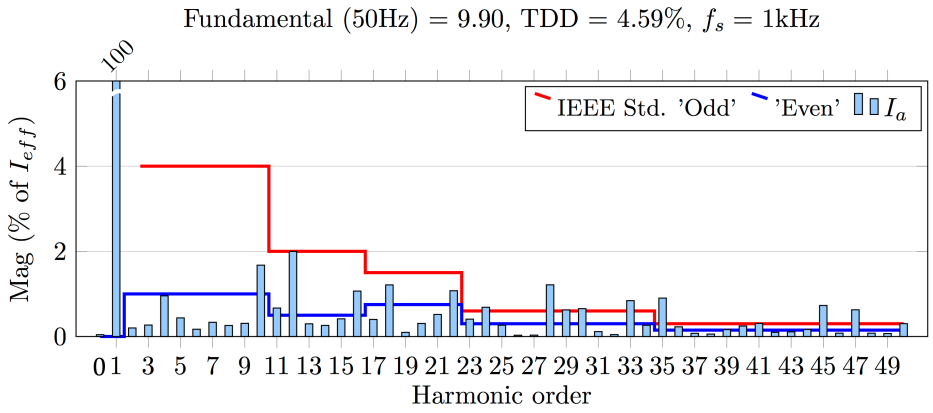


Figure 4.7 – Harmonic content of line-to-neutral voltages from grid side (U_{ao}) and inverter side (V_{ao}): (a) Simulation (b) Experiment

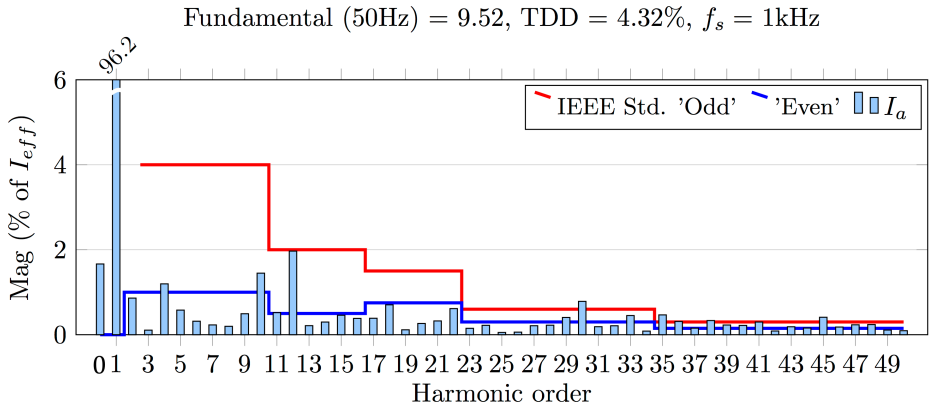
The harmonic contents of inverter line-to-neutral voltages from simulation and experiment reasonably correspond one another.

Line-to-line voltage waveforms for considering mode are illustrated in Figure C.3. The THD analysis is given in Figure C.4.

The harmonic contents of current in phase A (I_a) from simulation and experiment have good matching between each other, apart from relatively high DC component in

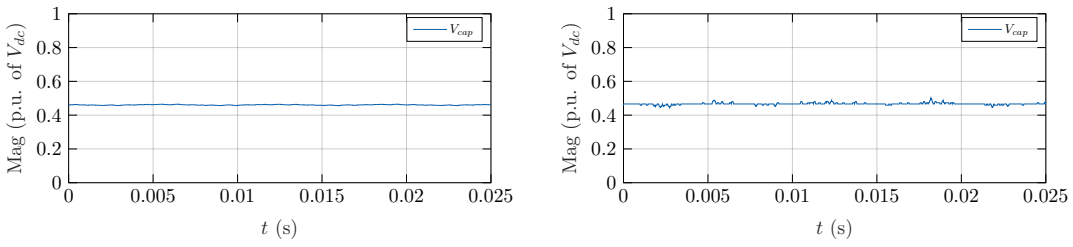


(a)



(b)

Figure 4.8 – Harmonic content of current in phase A (I_a): (a) Simulation (b) Experiment



(a) **(b)**

Figure 4.9 – Normalized voltage across the LDN capacitor (V_{cap}): (a) Simulation (b) Experiment

experiment results, see Figure 4.8. Serious thoughts must be given the issue to eliminate this DC offset, due to the fact that in IEEE STD 519-2014 standard it is strictly prohibited. As a result of high impedance of the transformer in the test bench, individual harmonic distortion in the IEEE standard will be considered for I_{SC}/I_L ratio less than 20. The corresponding harmonic limits are depicted in the current plots by red (odd harmonics) and blue (even harmonics) step-like lines. The value of I_{eff} given in Table 4.1 has been chosen as a maximum demand load current. As it can bee seen from Figure 4.8 total demand distortion (TDD) of current in phase A is less than specified in the standard limit of 5.0%, however due to presence of DC component and high values of individual harmonics of even order (e.g. 4th, 10th, 12th, 30th ...) this current does not meet the IEEE STD 519-2014 standard.

The acquired data of voltage across the LDN capacitor (V_{cap}) is shown in Figure 4.9. This voltage swing within the range 0.445-0.502 p.u. ($-11 \div 0.4\%$), which is a bit greater than affordable 10% deviation. However, due to the reason that V_{cap} normalized with constant value of fully charged batteries, but operation of 'discharging' mode will bring value of battery's terminal voltage down, as a consequence voltage across the LDN capacitor will find a new steady state condition.

'Charging' mode

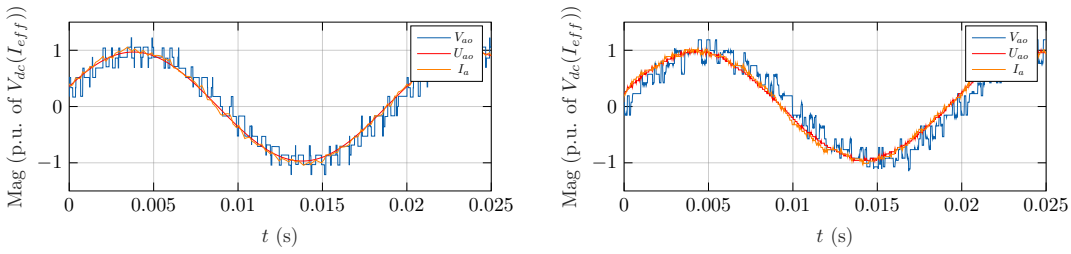
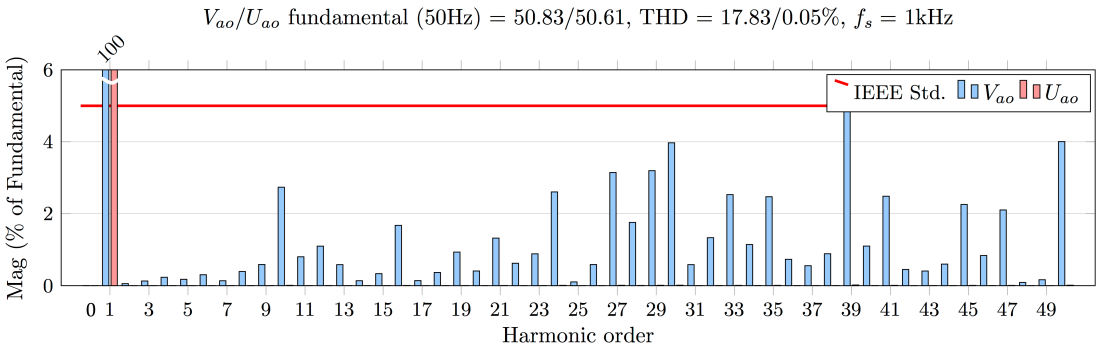


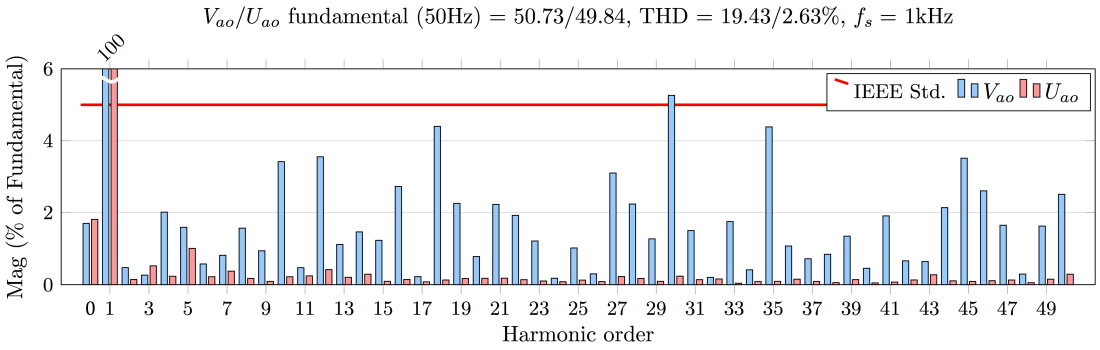
Figure 4.10 – Normalized grid line-to-neutral voltage (U_{ao}), inverter line-to-neutral voltage (V_{ao}) and current (I_a), V_{rms} =65 V: (a) Simulation (b) Experiment

'Charging' mode indicates that power flows from the grid to batteries. As it was mentioned earlier, here just unity power factor is considered. Thus, phase shift between line-to-neutral voltage and current in corresponding phase must be 0 deg. With relatively good inverter line-to-neutral voltage waveform and V_{rms} =40 V it was possible to charge the batteries only with $I_d = 0.2$. However, in order to implement required experiment ($I_d = 1$), V_{rms}

was set up at value 65 V. Figure 4.10 shows the aforementioned voltage and current waveforms. The simulation results match up with those obtained from test, despite greater phase shift between grid line-to-neutral (U_{ao}) and inverter line-to-neutral(V_{ao}) voltages, in experiment, which was also the case in 'discharging' mode.



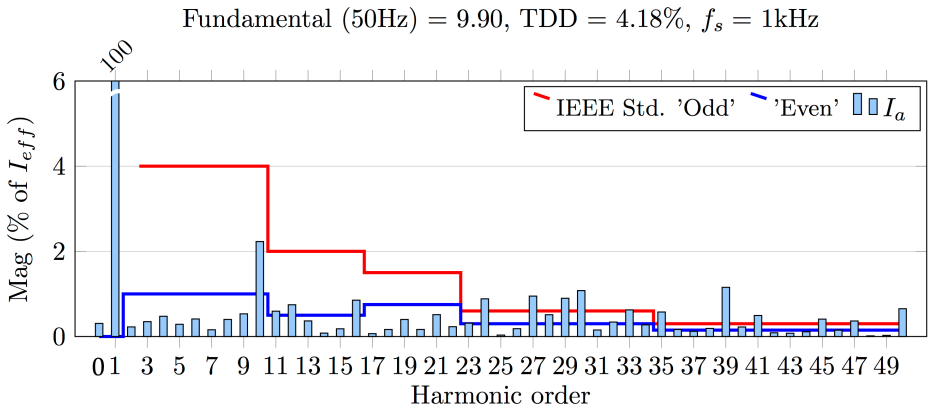
(a)



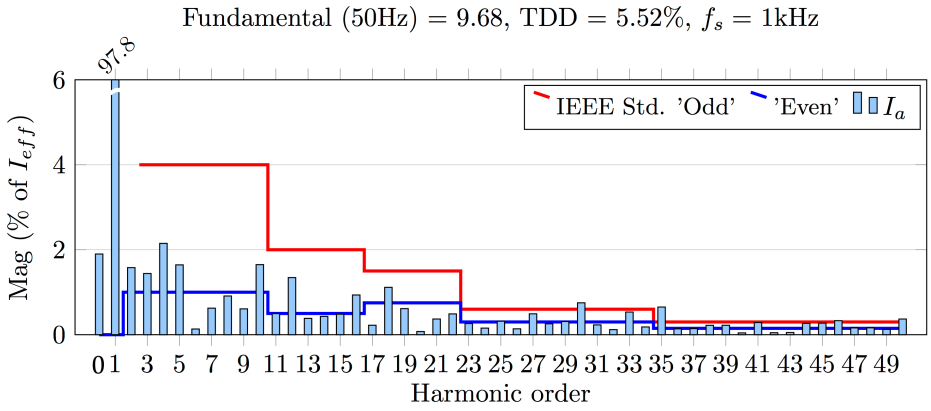
(b)

Figure 4.11 – Harmonic content of line-to-neutral voltages from grid side (U_{ao}) and inverter side (V_{ao}), V_{rms} =65 V: (a) Simulation (b) Experiment

It is visible from Figure 4.11 that inverter line-to-neutral voltage is more distorted, in comparison to the simulation, mostly due to high values of even harmonics (4th, 8th, 12th, 16th, 18th, 30th, etc.) and some odd ones (5th, 35th, etc.), ending up with THD equal to 19.43%. As a result, increasing half-wave asymmetry of the voltage waveform (see Figure 4.11b) can be observed. Owing to unity power factor, the same harmonic content is present in the current of corresponding phase (see Figure 4.12b). Again great attention must be paid to elimination of a DC component in the current, as well as even harmonics. As a consequence of these issues, inverter line-to-neutral voltage and current at PCC does not meet the requirements of IEEE Standard 519-2014.

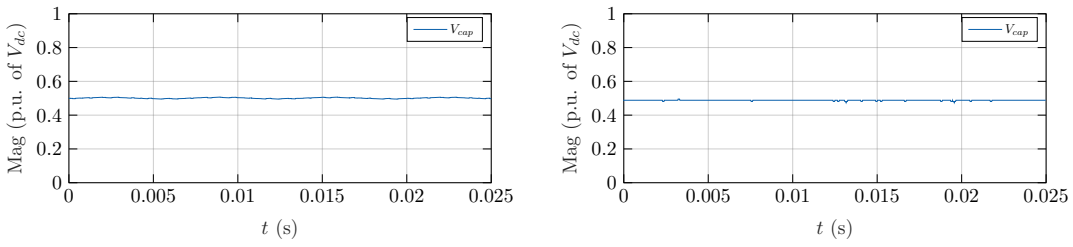


(a)



(b)

Figure 4.12 – Harmonic content of current in phase A (I_a): (a) Simulation (b) Experiment



(a) **(b)**

Figure 4.13 – Normalized voltage across the LDN capacitor (V_{cap}): (a) Simulation (b) Experiment

Voltage across the LDN capacitor remains stable in both simulation and experiment (see Figure 4.13). This voltage oscillate within the range 0.474-0.495 p.u. ($-5.2 \div -1\%$), which lies in affordable 10% deviation range.

4.2 3-Phase Five-Level Inverter with Two Cascaded HB Cells

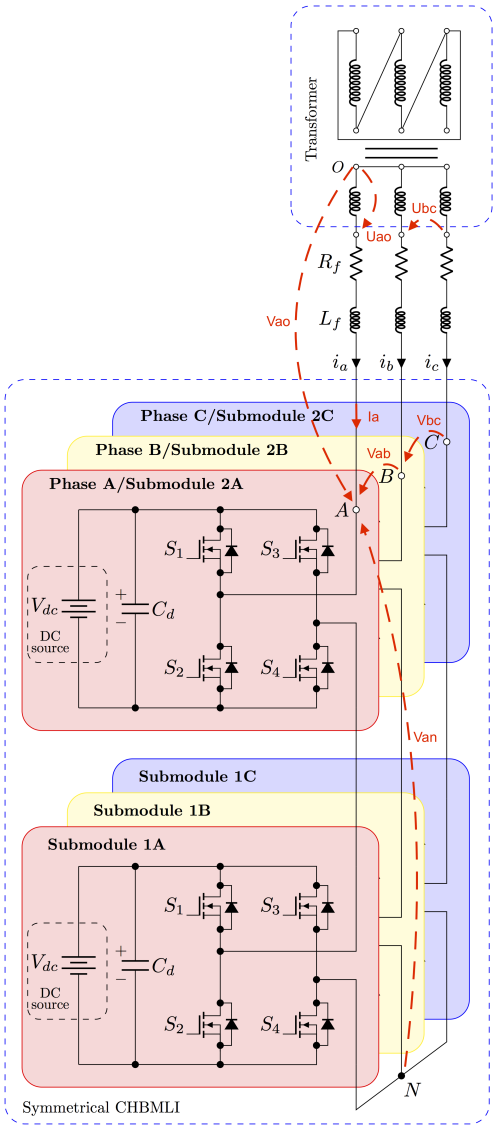


Figure 4.14 – Circuit diagram of the 3-phase five-level CHB inverter

Figure 4.14 shows a circuit diagram of the standard 3-phase five-level CHB inverter. Again, all measured quantities depicted in this figure. Due to some limitations in the tested hardware, the same measurements as in case of previously discussed topology, were performed with V_{rms} =80 V. Here, all the voltage plots will be normalized with $2V_{dc}$. Although, in this occasion the obtained results cannot be fully compared with those that are gained from tests of 3Ph5L HB inverter with LDN, however it is still possible to evaluate overall performance of these two inverters.

'Zero current' mode

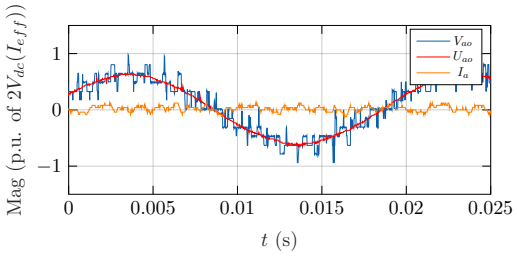


Figure 4.15 – Normalized grid line-to-neutral voltage (U_{ao}), inverter line-to-neutral voltage (V_{ao}) and current (I_a), 'zero current' mode ($I_d = 0$)

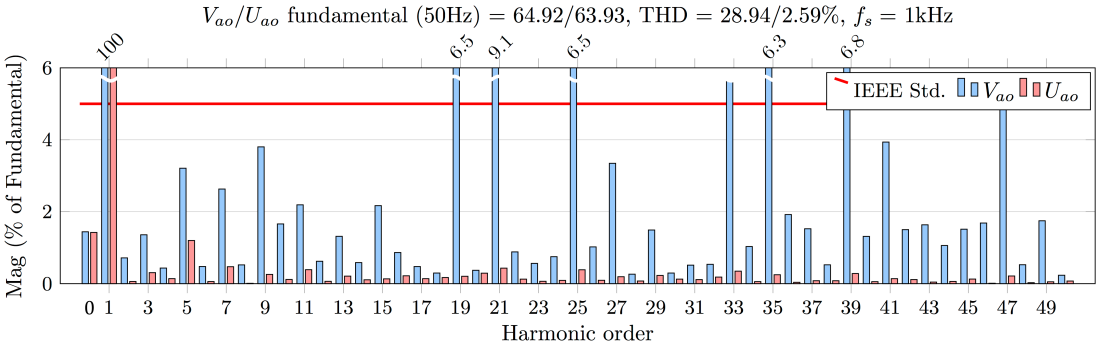


Figure 4.16 – Harmonic content of line-to-neutral voltages from grid side (U_{ao}) and inverter side (V_{ao}), 'zero current' mode ($I_d = 0$)

The shape of inverter line-to-neutral voltage (V_{ao}), depicted in Figure 4.15, is not so different from corresponding one, illustrated in Figure 4.3b. However, if harmonic contents are be also taken into account (see Figures 4.16 and 4.4b, respectively) then it is possible to notice that even harmonics in the CHB inverter have very low magnitude, while in the case of proposed topology, those harmonics make up a considerable contribution in

the overall voltages' THD and as a result in current's TDD. On the other hand, odd harmonics up to 33th have low impact on THD in case of the inverter with LDN. The relatively big LDN capacitor draws discharging/charging current when the instantaneous input voltage is lower/higher than the DC voltage across the LDN capacitor. The pulsed current drawn by this capacitor is rich in harmonics because it is discontinuous (see Subsections 2.2.3 and 2.2.4).

Line-to-line voltage waveform for considering mode is illustrated in Figure C.7. The THD analysis is given in Figure C.8.

'Discharging' mode

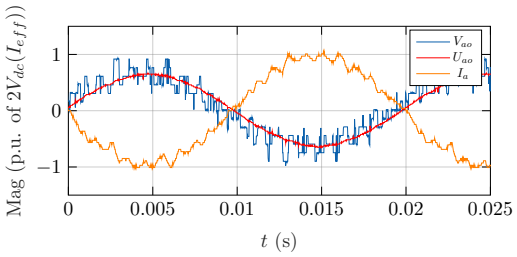


Figure 4.17 – Normalized grid line-to-neutral voltage (U_{ao}), inverter line-to-neutral voltage (V_{ao}) and current (I_a), 'discharging' mode ($I_d = -1$)

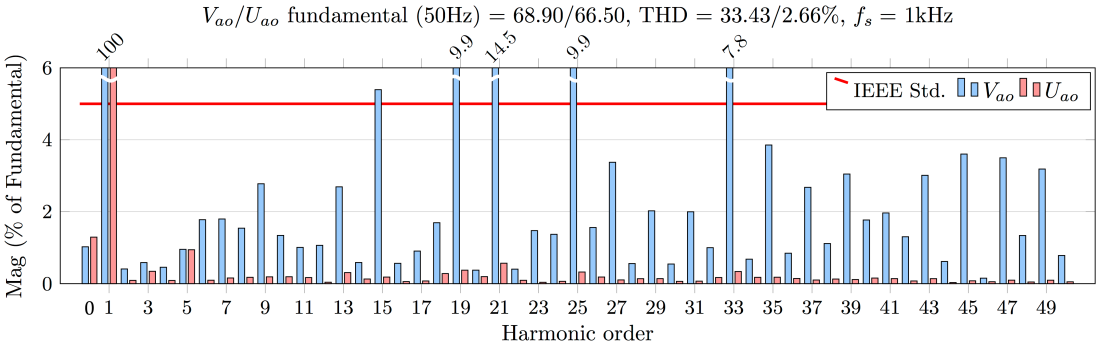


Figure 4.18 – Harmonic content of line-to-neutral voltages from grid side (U_{ao}) and inverter side (V_{ao}), 'discharging' mode ($I_d = -1$)

The same analysis of line-to-neutral voltage, described for 'zero current' mode, can also be applied in this case. More attention here must be given to discharging current. The current waveform, depicted in Figure 4.17, follows a sinusoidal shape, however due to

presence of odd harmonics (15th, 19th, 21st, 25th, 27th, 33th, 35th, etc.) with relatively high magnitude (see Figure 4.19), the waveform is way far from an ideal sine wave.

Line-to-line voltage waveform for 'discharging' mode is shown in Figure C.9. The THD analysis is given in Figure C.10.

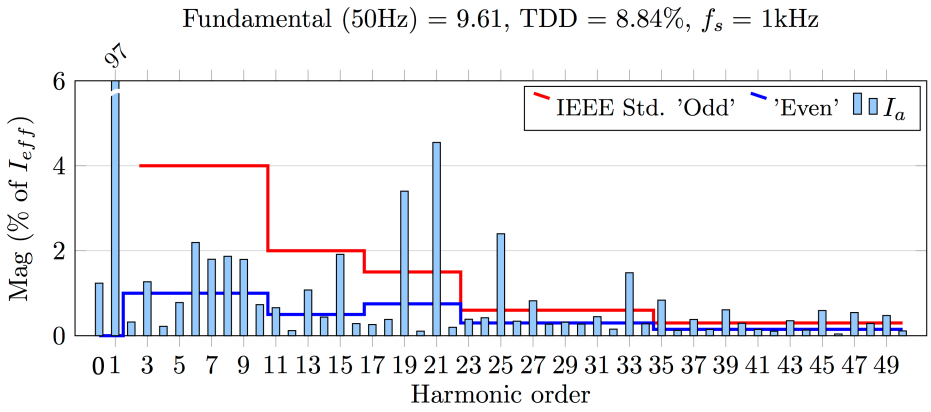


Figure 4.19 – Harmonic content of current in phase A (I_a), 'discharging' mode ($I_d = -1$)

'Charging' mode

'Charging' mode for 3Ph5L CHB inverter with hardware setup mentioned above characterized by highly distorted voltages and currents. This can be easily recognized from Figure 4.20 and corresponding harmonic analyses, depicted in Figures 4.21 and 4.22. This is because of conditionally low grid voltage, which does not correspond required power to be delivered to the batteries. However, taking into account that this topology is not a topic of present work, there is no need to present results, obtained for higher value of V_{rms}.

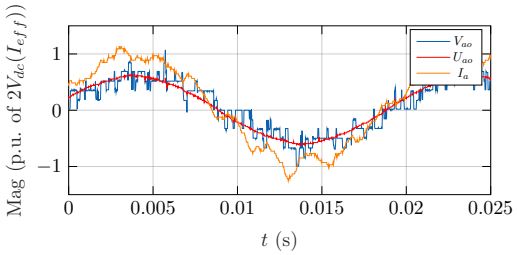


Figure 4.20 – Normalized grid line-to-neutral voltage (U_{ao}), inverter line-to-neutral voltage (V_{ao}) and current (I_a), 'charging' mode ($I_d = 1$)

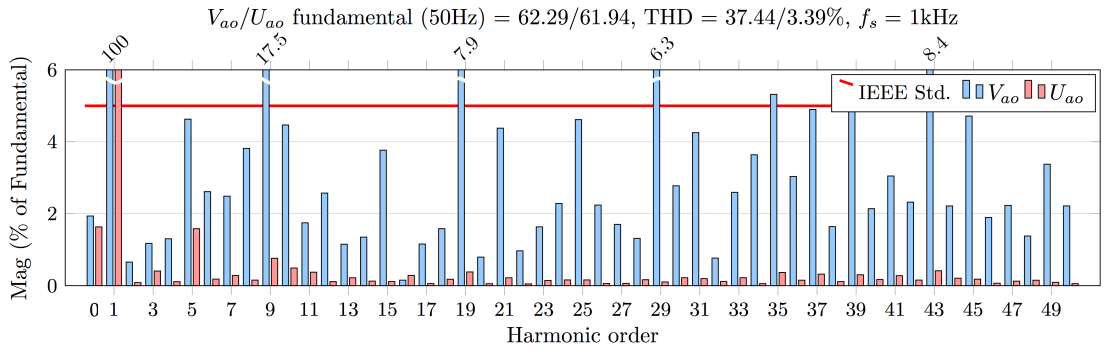


Figure 4.21 – Harmonic content of line-to-neutral voltages from grid side (U_{ao}) and inverter side (V_{ao}), 'charging' mode ($I_d = 1$)

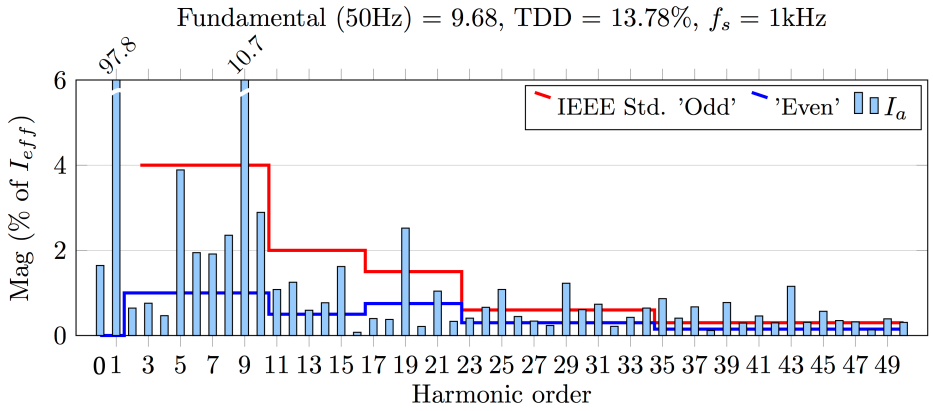


Figure 4.22 – Harmonic content of current in phase A (I_a), 'charging' mode ($I_d = 1$)

Overall, inverter line-to-neutral voltages and current at PCC of the system does not meet the requirements of IEEE Standard 519-2014, due to high harmonic distortion.

4.3 Comparative Reliability Analysis

One of the important characteristics of power electronic devices and their components is reliability. Development of existing technologies and new applications have restricted design and manufacturing in terms of space reduction, weight containment, operating temperatures, increasing voltages and currents, and system integration [39]. Recently reliability assessments of power electronic devices have been conducted by numerous of researchers [40–43]. Many widely used circuits have been investigated, however, numerous

of them still have to be studied. A comparative reliability analysis of three main circuit topologies (DCMLI, FCMLI and CHBMLI), which are commonly used in industry, is given in [40]. This section introduces a comparative reliability evaluation of well known 3-phase five-level (3Ph5L) CHB inverter and the 3Ph5L HB with LDN topology, presented in [4].

Table 4.2 – Comparison of component requirements

Component	3Ph5L CHB		3Ph5L HB with LDN	
	Quantity, pcs	Failure rate λ, Failures/10^6 hours	Quantity, pcs	Failure rate λ, Failures/10^6 hours
Active switch (MOSFET)	24	0.7927	18	1.2304
Electrolytic capacitor (V_{dc})	12	0.3055	6	0.3055
Electrolytic capacitor ($V_{dc}/2$)	-	-	6	0.1630
Ceramic capacitor (V_{dc})	162	0.0570	81	0.0570
Ceramic capacitor ($V_{dc}/2$)	-	-	35	0.0151
Resistor	96	1.717e-06	72	4.23e-06
Diode (V_{dc})	60	0.0053	30	0.0108
Diode ($V_{dc}/2$)	-	-	15	0.0031
LED	6	0.0016	4	0.0031
Power connector	24	0.0012	17	0.0022
Control connector	24	0.0119	16	0.0188
Soldered connections	1032	0.0520	757	0.0520
Gate drives	12	0.0660	9	0.0660
DC/DC voltage converters	12	0.0173	8	0.0173
PCB plate	6	6.256e-04	4	0.0011

These two inverters are able to generate the same number of voltage levels, whereas using different amount of components. The reliability of both multilevel inverters is examined at system level based on prediction of the failure probability and simulation results of certain faulty regimes. The reliability prediction is a bottom-to-top procedure, which involves calculation of the mean time to failure for every single component. The reliability

indices of the whole inverter have been estimated based on parts stress method used in MIL-HDBK-217F reliability standard, since this standard contains the information about the base failure rate of the components used in compared inverters.

The simplified circuit diagrams of two compared topologies are illustrated in Figures 4.1 and 4.14. The starting point for investigating these multilevel inverters, in accordance with MIL-HDBK-217F standard, is to calculate the number of components for both compared devices and to define the failure rates for each component used.

Table 4.2 summarizes types and quantities of elements from which those submodules were built up, along with their calculated failure rates, taking into account proper stress factors. Stress factors, by which failure rates under reference conditions can be converted to values applying for operating conditions (actual junction temperature and actual electrical stress on the components), were defined based on measures, taken during previous experiments. Summing all failure rates to assess reliability of an inverter as whole, means, that a failure in any element of the system causes total system failure. In this calculation it is assumed that all the components are non-repairable and in case failure must be replaced by a new one. It should be noted that in inverters with three phases, when a component failure occurs, reconfiguration of the structure or varying the expected voltage levels of the phase voltages should be similar in phase legs. Otherwise, the output voltage of the inverter will not be desirable.

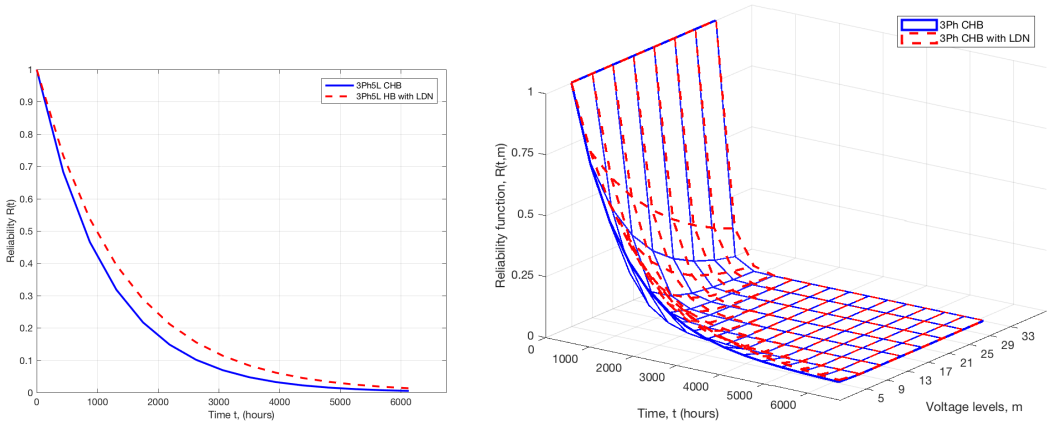


Figure 4.23 – Reliability function for compared MLI topologies: (a) for 3Ph5L (b) for different number of voltage levels m

The assessment is based on the built prototypes available in the laboratory. For both of inverters were used identical parts. However, due to distinct number of components used

and reduced voltage stress on the main circuit elements of LDN submodule, the reliability function has shape illustrated in Figure 4.23. Here the case of the continuous system operation was considered. Results are obtained by the aforementioned method show that 3Ph5L HB with LDN inverter has better performance in terms of reliability, whereas converting the same power unit. An increase in the voltage levels, leading to the rise of the components number, causes system reliability to reduce significantly. Nevertheless, the inverter with LDN still has better reliability potential compare to conventional CHBMLI.

Failure of power converters can be a result of many reasons, such as break down of components, poor design or assembling, environmental hazard, accidents during the operation. The main failure causes are illustrated in Figure 4.24.

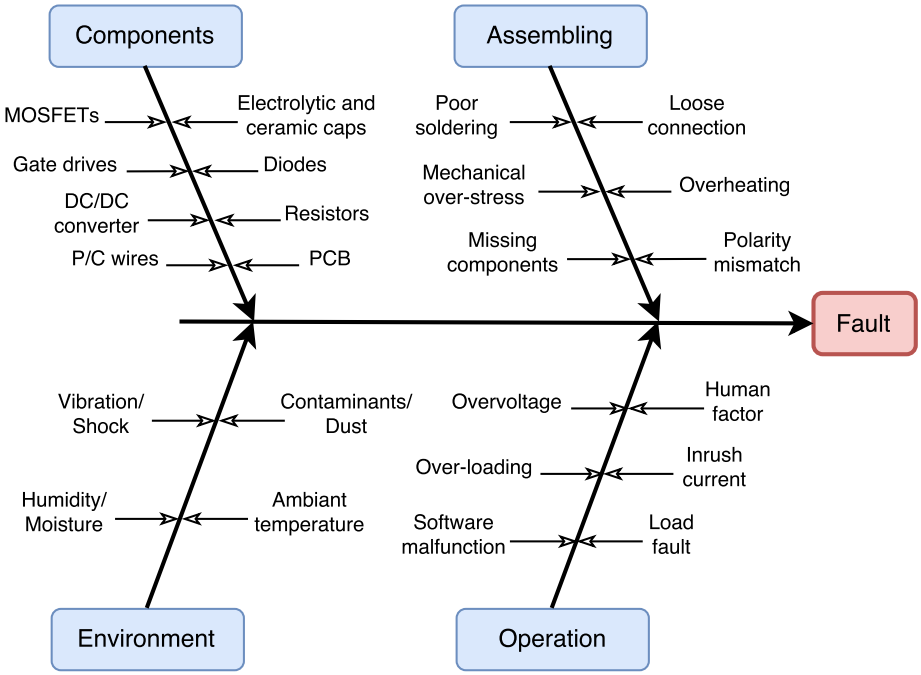


Figure 4.24 – Fishbone (Ishikawa) diagram of the failure causes

To find the weaknesses of the proposed inverter design, before design is realized, the Design Failure Modes and Effect Analysis (DFMEA) has been applied. The DFMEA is a bottom-up approach that examines the effects of single point failures on overall system performance [39]. In the following analysis it will be assumed failure only one of the mentioned components. Thus, multiple breakdowns are not considered. Moreover, the effect of malfunctions due to failures of hardware/software used for modulation and control, insufficiency of preventive maintenance, and operation outside of safe operating

area is not considered. A commonly used DFMEA ranking chart is given in [39] (Table 15.2).

Owing to modular structure of the compared topologies, the impact of failure can be considered independently for the composite submodules. Matlab/Simulink software has been used to simulate potential effects of component's failure.

A risk priority number (RPN), formulated by Equation 4.1, provides a relative measure of the importance of each effect [39].

$$RPN = Severity \times Occurance \times Detection \tag{4.1}$$

The higher the RPN, the higher the priority of its associated failure mode that must be taken into consideration during design and running time. The design failure modes and effect analyses for an LDN and an HB submodules of the proposed inverter are summarized in Tables D.1 and D.2, respectively. The corresponding schematics of the LDN submodule are given in Appendix B.

Bearing in mind 3Ph5L HB inverter with LDN, DFMEA shows that in LDN submodule the most frequent effect of a component failure is asymmetric regime, which normally lead to an increase of voltage across the LDN capacitor and thus to its subsequent greater voltage stress. Commonly electrolytic capacitors are employed as an LDN cap, due to the need of high capacitance. If voltage stress is high enough to break down the dielectric strength of the electrolytic capacitor, it will lead to catastrophic consequences such as a fire or an explosion. Because of this fact, the severity of those modes may be considered at maximum hazard level. Special attention must be paid to a proper selection of the LDN capacitor. On the other hand, simulation of the proposed inverter circuit with shorted pins of the LDN capacitor demonstrates that this problem may not result in dangerous situation (the magnitude of discharging current decays very quickly, in the range of few miliseconds), but instead will provide an opportunity for continuous operation with reduced performance, depending on the requirements given by a specific application. This simulation results must be verified by corresponding experiments in the future works.

Any failure occurred in HB submodule, which does not lead to short circuiting of DC (battery pins) or output AC terminals, will not cause hazardous effect to the HB module, but conversely if this type of failure happens in the proposed inverter, it will lead to aforementioned problem with the LDN capacitor.

Giving consideration to 3Ph5L CHB topology, DFMEA demonstrates that even though this inverter is devoid of the issue with overvoltage of an electrolytic capacitor, nevertheless one of the most vulnerable spots of compared inverters, namely short circuiting of DC buses, here plays a significant part. Keeping in mind, that failure of many HB submodule items (DC-link caps, smoothing ceramic caps, etc.) connected to these DC buses may lead to aforenamed dangerous effect, as well as the higher number of HB submodules in the examined inverter structure, thus the potential risk of this event is much greater, in comparison to 3Ph5L HB inverter with LDN.

Here, it can be concluded that, firstly, depending on the particular application, design of the presented inverter must find preventive solutions for studied failures. Secondly, in terms of fault-tolerance characteristics, the three-phase HB topology with LDN has potential advantage over 'classical' CHBMLI inverter, protecting the system from significant loss or unexpected interruptions and improves availability.

There is no doubt that other factors such as cost and performance should also be considered for the selection of an inverter. However, using accurate reliability model on selection stage either to compare different inverter topologies (or design solutions) or to confirm that the final product matches the reliability requirements is a crucial aspect of power electronics application.

5 Conclusions and Future Work

5.1 Conclusions

This work has presented a 3-phase five-level HB inverter with LDN and an implementation of Level Shifted PWM technique for that topology with an emphasis on grid-connected, low switching frequency applications. The proposed concept can be applied to all form of existing MLIs to almost double the number of levels. However, operating with a symmetric CHBMLI topology, this has not only increased the amount of voltage levels but also maintained uniform power loading of the individual HB cells.

A symmetric 3-phase CHBMLI, that is available in the university laboratory and initially built as a test bench for the EEbatt project, was reconfigured to operate as proposed inverter. The LDN submodule is designed based on PCB architecture, built up, checked for operational capabilities and integrated into the existing circuit. Meanwhile, the software adaptation in terms of modulation strategy for a new circuit was fulfilled. However, due to the fact that the LDN circuit employs inherent self-balancing mechanism, while it does not consume or supply any power, there is no need in modification of existing and/or implementing an additional closed-loop control. Further, the operational (performance) studies were performed to determine if the whole system works as expected, acquiring necessary data for a final evaluation step.

The simulation results that have been a priori acquired, match well with the corresponding experimental counterpart, confirming the effectiveness of the proposed topology. This fact justifies the sufficiency of simulation model has been used. The size of the LDN capacitor, calculated by a technique that was developed in this work, confirms its acceptable value in both simulation and experiment.

The testing results were examined in terms of meeting the requirements of IEEE STD 519-2014 standard. According to this standard, the implemented 3Ph5L HB inverter

with LDN cannot be directly connected to the grid, due to relatively high THD of a line-to-neutral voltage and TDD of a phase current at a PCC. However, applying a first order filter with fairly low nominal parameters, has greatly improved harmonic content and allowed to meet the standard restrictions.

To confirm that voltage and current waveforms have equivalent shape as they have in the case of 3-phase five-level CHB inverter, the corresponding measurements were performed. Due to some limitations in the tested hardware, the RMS value of grid voltage was set up as 80V. Although, in this occasion the obtained results cannot be fully compared with those from tests of 3Ph5L HB inverter with LDN, however, it is still possible to verify the overall performance of these to inverters. This verification shows reasonable matching of experimentally gained waveforms. Nonetheless, additional experiments with the identical setup parameters must be done in future works.

5.2 Future Work

The presented configuration of a power inverter is expected to be very useful in medium-voltage applications. However, the LDN concept is relatively new approach of power electronic converter design that will find its own niche. Nevertheless, the implemented topology and its possible variations need more research efforts, especially in the field of very low switching frequency applications with acceptable THD(TDD). Future research should be focused on examining the following aspects:

- A search of an optimal switching frequency for PWM modulation.
- Implementation of different modulation strategies and their performance comparison.
- Inverter's performance evaluation under variation of modulating index and power factor.
- Thermal stability study with special attention to reliability evaluation for different thermal cycling with its experimental verification.
- Other possible configurations, including 3-phase CHB topologies with LDN, that are able generate greater number of output voltage levels (9, 13, 17...).
- Comparative analysis of power losses among different topologies.

All these studies may lead to minimizing both on-state and dynamic power losses, enhancing the overall efficiency and reliability of the power converter. This is an important trend for future research and for industrial applications.

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List of Abbreviations

Symbols (glossaries) | **A** | **C** | **D** | **E** | **F** | **H** | **I** | **L** | **M** | **N** | **P** | **R** | **S** | **T** | **V**

Symbols (glossaries)

1Ph5L Single-phase-five-level

2L Two-level

3Ph17L Three-phase-seventeen-level

3Ph3L Three-phase-three-level

3Ph5L Three-phase-five-level

A

AC Alternating current

APOD-PWM Alternative phase opposition disposition pulse-width modulation

C

CHB Cascaded H-bridge

CHBMLI Cascaded H-bridge multilevel inverter

CPU Central processing unit

D

DC Direct current

DCMLI Diode clamped multilevel inverter

DFMEA Design failure modes and effect analysis

E

EMF Electromotive force

EMI Electromagnetic interference

ESR Equivalent series resistance

F

FCMLI Flying capacitor multilevel inverter

FIT Failures in time

FPGA Field programmable gate array

H

HB H-bridge

HV High-voltage

I

I/O Input/output

IGBT Insulated-gate bipolar transistor

L

LDN Level doubling network

LED Light-emitting diode

LSPWM Level shifted pulse-width modulation

M

ML Multilevel

MLC Multilevel converter

MLI Multilevel inverter

MOSFET Metal-oxide-semiconductor field-effect transistor

MSE Munich School of Engineering

MTTF Mean time to failure

MV Medium-voltage

N

NPC Neutral-point clamped inverter

P

PCB Printed circuit board

PCC Point of common coupling

PD-PWM Phase disposition pulse-width modulation

POD-PWM Phase opposition disposition pulse-width modulation

PSPWM Phase shifted pulse-width modulation

PWM Pulse-width modulation

R

RMS Root-mean-square

RPN Risk priority number

RTTM Real-time target machine

S

SoC State of charge

SVM Space vector modulation

T

TDD Total demand distortion

THD Total harmonic distortion

THIPWM Third harmonic injection pulse-width modulation

TUM Technical University of Munich

V

VSI Voltage source inverter

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Appendix A. Numerical Calculation of LDN Capacitor

```
% MATLAB code for numerical calculation of the LDN capacitor,
% rms current and peak-peak voltage ripple for MLI CHB with LDN inverters.
% In the calculation the level-shift modulation is used.

% Adopted from Power Electronic Converters for Microgrids, First Edition.
% Suleiman M. Sharkh, Mohammad A. Abusara, Georgios I. Orfanoudakis and
% Babar Hussain. 2014 John Wiley & Sons, Ltd.

clear all;
clc;

%--------------------------------
%INPUTS
%--------------------------------
n = 1; % Number of H-bridges per phase
strategy = 1; % 1:SPWM, 2:SPWM+1/6 3rd harm. 3:Min/Max injection
f = 50; % Reference signal frequency in Hz
fs = 1000; % Switching frequency in Hz
dts = 5e-6; % Sampling time in seconds

%--------------------------------
%NORMALISATION
%--------------------------------
Vdc_bus = 52.26/2; % DC bus voltage across LDN in V
Δ_V = 10; % Affordable DC bus voltage oscillation in %
Io_mag = 25; % Magnitude of phase current in A

%--------------------------------
%CALCULATION
%--------------------------------
```

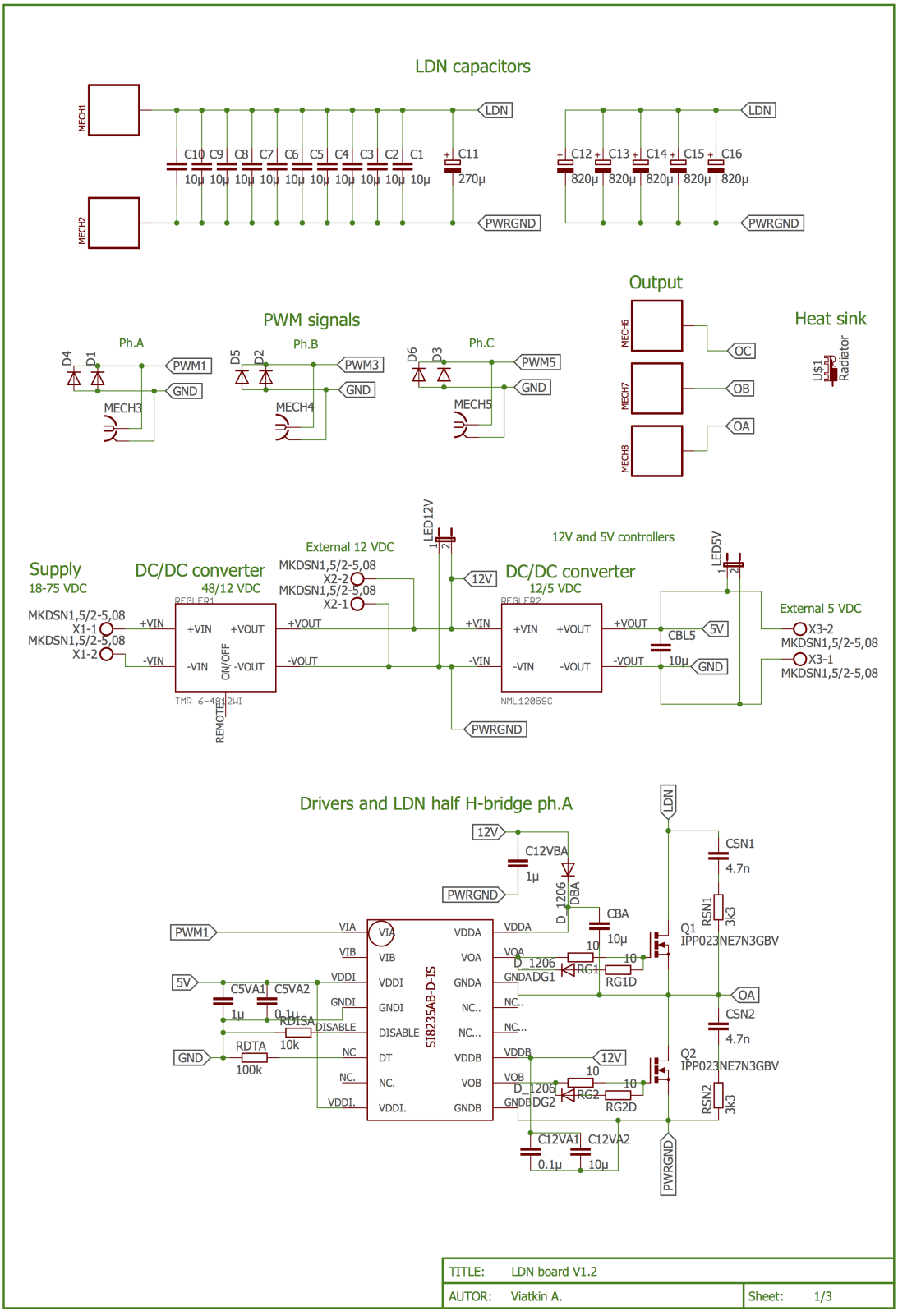
```
m = 4*n+1; % Number of inverter terminal voltage levels
if strategy == 1
    ma_max = 1; % Maximum amplitude modulation index
end
if strategy == 2 || strategy == 3
    ma_max = 1.15; % Maximum amplitude modulation index
end

count = 0;
pw_ang = zeros(1);
for phi = 0:9/180*pi:pi
    count = count + 1;
    pw_ang(count) = phi;

    count1 = 0;
    mod_ind = zeros(1);

for ma = 0:0.05:ma_max
    count1 = count1 + 1;
    mod_ind(count1) = ma;

    count2 = 0;
    I_C_ldn_rmssq = 0; % i.e. i_ldn_rms square
    I_C_ldn = zeros(1);
    time = zeros(1);
    dutyA = zeros(1);
    dutyB = zeros(1);
    dutyC = zeros(1);

for t = 0:dts:1/f-dts
    count2 = count2 + 1;
    time(count2) = t;

    %Reference calculation
    RefA = ma*sin(2*pi*f*t);
    RefB = ma*sin(2*pi*f*t - 2*pi/3);
    RefC = ma*sin(2*pi*f*t + 2*pi/3);
    cmSignal = 0; % Common-mode voltage reference signal
    if strategy == 2
        cmSignal = -1/6*ma*sin(3*2*pi*f*t);
    end
    if strategy == 3
        cmSignal = - 1/2*(max([RefA RefB RefC]) + min([RefA RefB RefC]));
    end
```

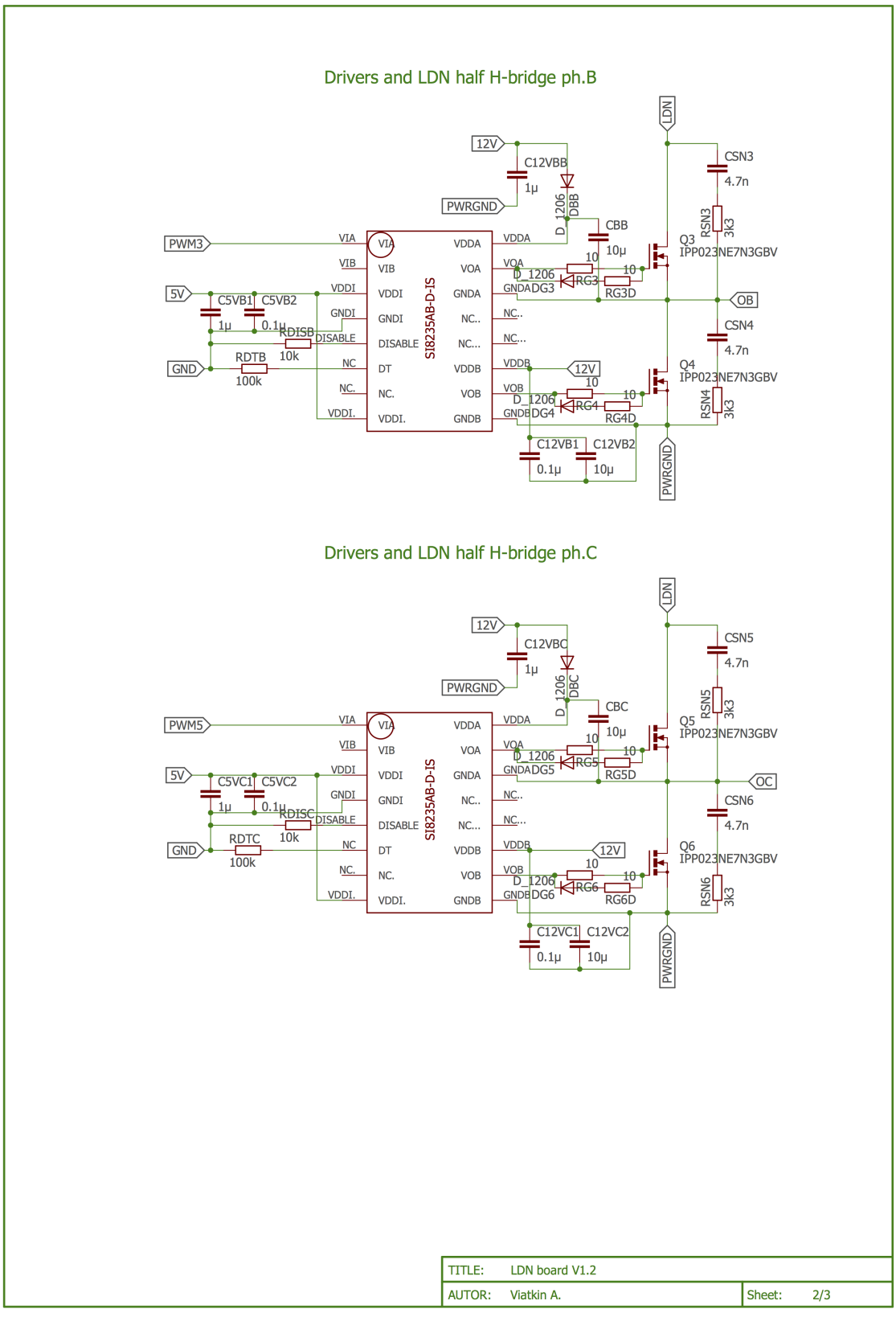
```
75      RefA = RefA + cmSignal;
76      RefB = RefB + cmSignal;
77      RefC = RefC + cmSignal;
78
79      %Reference modification for level-shift modulation
80      RefAm = 1 - abs(RefA);
81      RefBm = 1 - abs(RefB);
82      RefCm = 1 - abs(RefC);
83
84      sumA = zeros(1);
85      sumB = zeros(1);
86      sumC = zeros(1);
87
88  for k=1:1:(m-1)/2-1
89      sumA = sumA + ((2*k/(m-1) < RefAm)&(RefAm < ...
            2*(k+1)/(m-1))).*(2*(k+1)/(m-1) - RefAm);
90      sumB = sumB + ((2*k/(m-1) < RefBm)&(RefBm < ...
            2*(k+1)/(m-1))).*(2*(k+1)/(m-1) - RefBm);
91      sumC = sumC + ((2*k/(m-1) < RefCm)&(RefCm < ...
            2*(k+1)/(m-1))).*(2*(k+1)/(m-1) - RefCm);
92  end
93
94      RefA = (RefAm < 2/(m-1)).*RefAm + sumA;
95      RefB = (RefBm < 2/(m-1)).*RefBm + sumB;
96      RefC = (RefCm < 2/(m-1)).*RefCm + sumC;
97
98      %Carrier generation / Symmetrical triangular carrier
99      CR = ((-1)*sawtooth(2*pi*fs*t, 0.5) + 1)*(1/(m-1));
100
101     %Duty cycle calculation for phase A
102     dutyA(count2) = (RefA ≥ CR)*1;
103
104     %Duty cycle calculation for phase B
105     dutyB(count2) = (RefB ≥ CR)*1;
106
107     %Duty cycle calculation for phase C
108     dutyC(count2) = (RefC ≥ CR)*1;
109
110     %Three-phase load currents
111     iA = Io_mag*sin(2*pi*f*t-phi);
112     iB = Io_mag*sin(2*pi*f*t-phi-2*pi/3);
113     iC = Io_mag*sin(2*pi*f*t-phi+2*pi/3);
114
115     %Current through the LDN capacitor
```

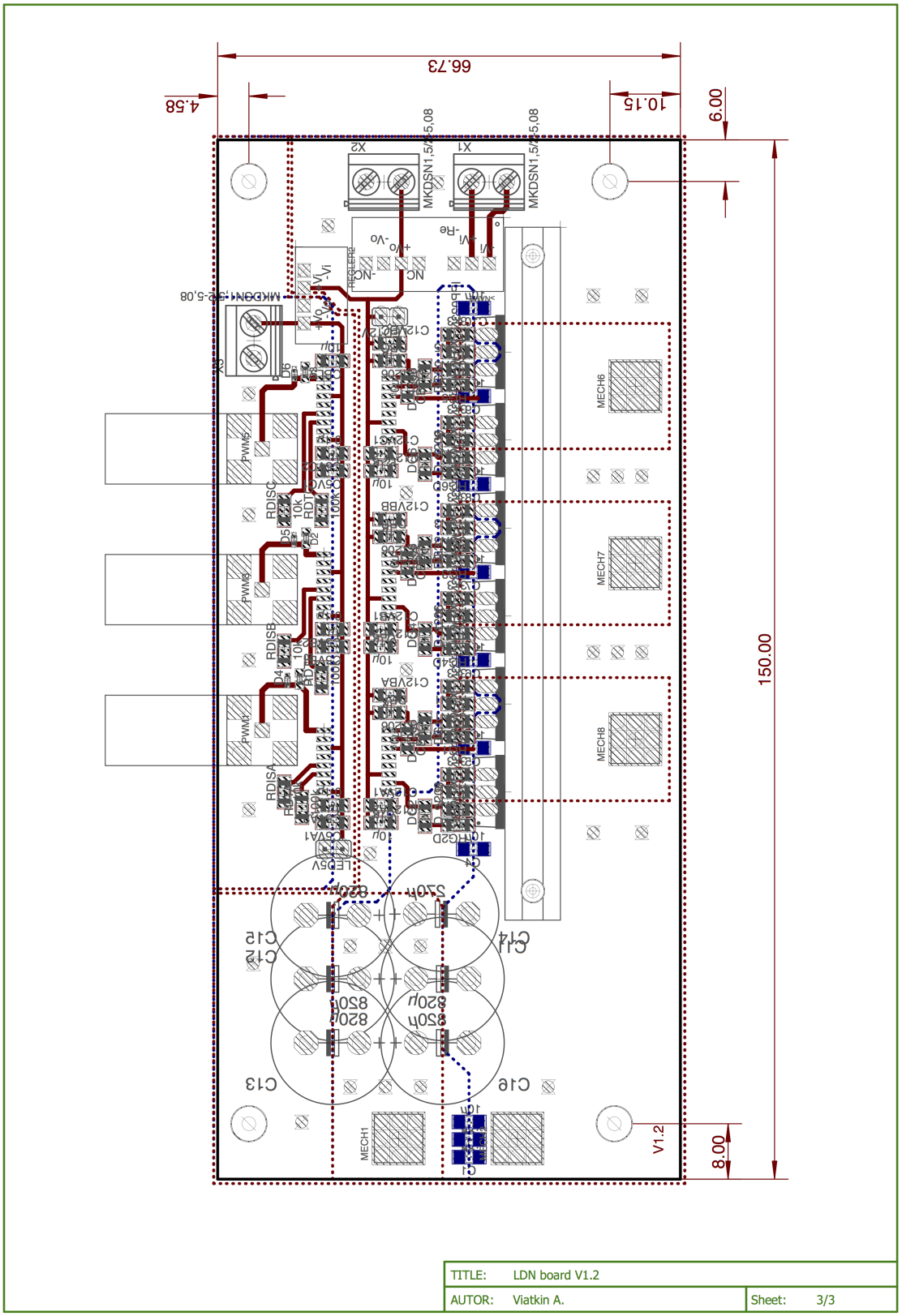
```
116     I_C_ldn_rmssq = I_C_ldn_rmssq + (iA*dutyA(count2))^2 + ...
            (iB*dutyB(count2))^2 + (iC*dutyC(count2))^2;
117     I_C_ldn(count2) = iA*dutyA(count2) + iB*dutyB(count2) + ...
            iC*dutyC(count2);
118 end
119
120 dQ_C_ldn = I_C_ldn.*dts;
121 Q_C_lnd = cumsum(dQ_C_ldn);
122 Q_C_ldn_pp = max(Q_C_lnd) - min(Q_C_lnd);
123
124 %Capacitance for LDN network with allowed 10% DC bus voltage ripples
125 Cap_m(count1) = Q_C_ldn_pp/(Vdc_bus*Δ_V/100);
126 end
127 Cap_phi(count, :) = Cap_m;
128 end
129
130 %--------------------------------
131 %PLOTS
132 %--------------------------------
133 figure
134 ax1 = subplot(2,1,1);
135 plot (ax1, time, I_C_ldn/Io_mag)
136 grid on
137 title('Time-domain representation of Icap(t)')
138 xlabel('t (s)')
139 ylabel('Icap(t)/Imag')
140
141 fftLength = length(I_C_ldn);
142 xdft = fft(I_C_ldn,fftLength);
143 Icaph = abs(xdft/fftLength);
144 plot_fft = Icaph(1:fftLength/2+1);
145 plot_fft(2:end-1) = 2*plot_fft(2:end-1);
146 freq = 1/dts*(0:(fftLength/2))/fftLength;
147 axis(ax1,[0 inf -1.2 1.2])
148
149 ax2 = subplot(2,1,2);
150 plot(ax2, freq,plot_fft/Io_mag)
151 grid on
152 title('Single-Sided Amplitude Spectrum of Icap(t)')
153 xlabel('f (Hz)')
154 ylabel('|Icap(f)|/Imag')
155
156 figure
157 surf(mod_ind, pw_ang/pi*180, Cap_phi*1000)
```

```
158 colormap jet
159 set(gca, 'XTick',0:0.2:1)
160 set(gca, 'YTick',0:30:180)
161 set(gca, 'ZTick',0:5:18)
162 title('Requirements for LDN capacitance as a function of modulation ...
        index and power angle')
163 xlabel('Amplitude modulation index, ma')
164 ylabel('Power angle, phi')
165 zlabel('Capacitance, Cd (mF)')
166
167 %------------------------------
168 %RESULTS
169 %------------------------------
170 %Capacitor rms current for LDN network
171 I_C_ldn_rmssq = I_C_ldn_rmssq/count2;
172 I_C_ldn_rms = sqrt(I_C_ldn_rmssq); %A
173
174 %Minimum capacitance for LDN network with allowed 10% DC bus voltage ...
        ripples
175 Cap_min = max(max(Cap_phi)); %F
```

Appendix B. Schematics and Layout for LDN submodule

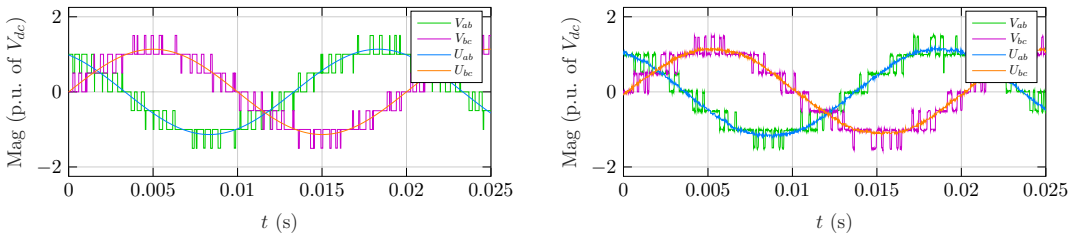



Drivers and LDN half H-bridge ph.B
LDN
12V
C12VBB
1µ
PWRGND
D_1206
DBB
CBB
10µ
CSN3
4.7n
RSN3
3K3
Q3
IPP023NE7N3GBV
PWM3
VIA
VIB
5V
VDDI
GND
GNDI
C5VB1
C5VB2
1µ
0.1µ
RDISB
DISABLE
10k
RDTB
100k
NC
NC.
VDDI.
SI8235AB-D-IS
VDDA
VOA
GNDA
NC..
NC...
VDDB
VOB
GNDB
10
D_1206
DG3
RG3
RG3D
OB
CSN4
4.7n
Q4
IPP023NE7N3GBV
RSN4
3K3
12V
DG4
RG4
RG4D
C12VB1
C12VB2
0.1µ
10µ
Drivers and LDN half H-bridge ph.C
LDN
12V
C12VBC
1µ
PWRGND
D_1206
DBC
CBC
10µ
CSN5
4.7n
RSN5
3K3
Q5
IPP023NE7N3GBV
PWM5
VIA
VIB
5V
VDDI
GND
GNDI
C5VC1
C5VC2
1µ
0.1µ
RDISC
DISABLE
10k
RDTC
100k
NC
NC.
VDDI.
SI8235AB-D-IS
VDDA
VOA
GNDA
NC..
NC...
VDDB
VOB
GNDB
10
D_1206
DG5
RG5
RG5D
OC
CSN6
4.7n
Q6
IPP023NE7N3GBV
RSN6
3K3
12V
DG6
RG6
RG6D
C12VC1
C12VC2
0.1µ
10µ
TITLE: LDN board V1.2
AUTOR: Viatkin A.
Sheet: 2/3


66.73
4.58
10.15
6.00
150.00
8.00
MKDSN1,5/2-5,08
X1
X2
MECH1
MECH6
MECH7
MECH8
PWM6
PWM7
PWM8
RDISA
RDISB
RDISC
C12VBA
C12VBB
C12VBC
C5VA1
LED5V
C13
C14
C15
C16
V1.2
TITLE: LDN board V1.2
AUTOR: Viatkin A.
Sheet: 3/3

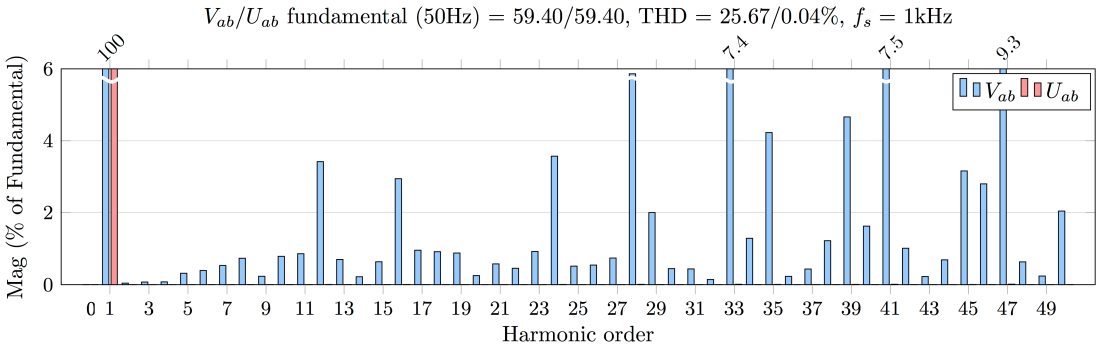
Appendix C. Simulation and Experiment Results

3-phase five-level HB inverter with LDN

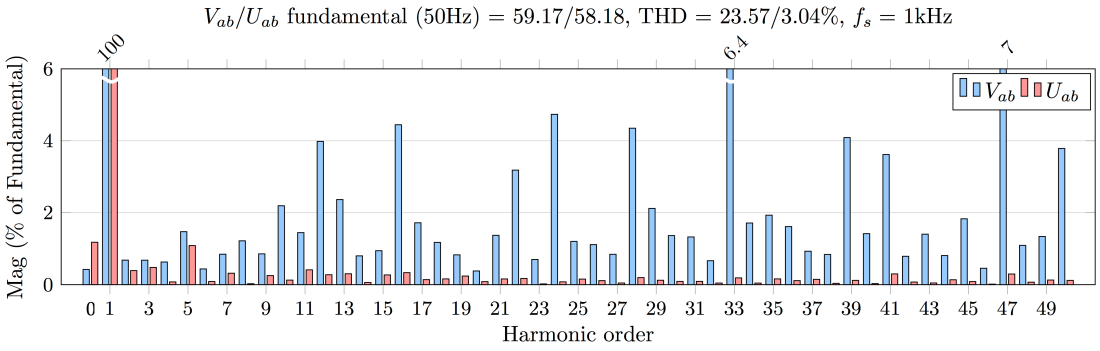


(a) **(b)**

Figure C.1 – Normalized line-to-line voltages from grid side (U_{ab}, U_{bc}) and inverter side (V_{ab}, V_{bc}), 'zero current' mode ($I_d = 0$), $V_{rms} = 40V$: (a) Simulation (b) Experiment

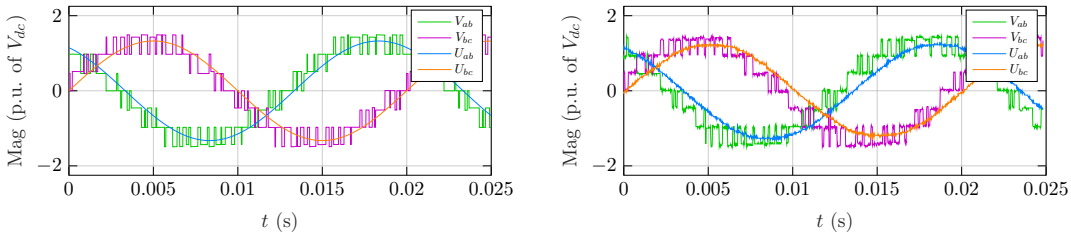


(a)



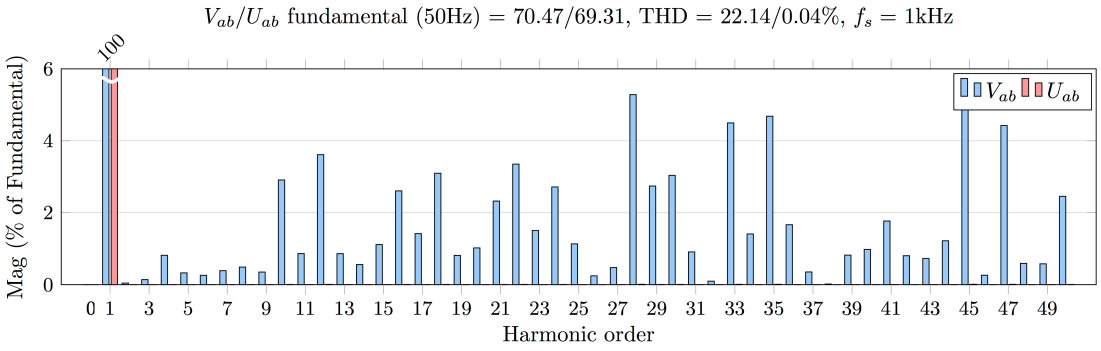
(b)

Figure C.2 – Harmonic content of line-to-line voltages from grid side (U_{ab}) and inverter side (V_{ab}), 'zero current' mode ($I_d = 0$), $V_{rms} = 40V$: (a) Simulation (b) Experiment

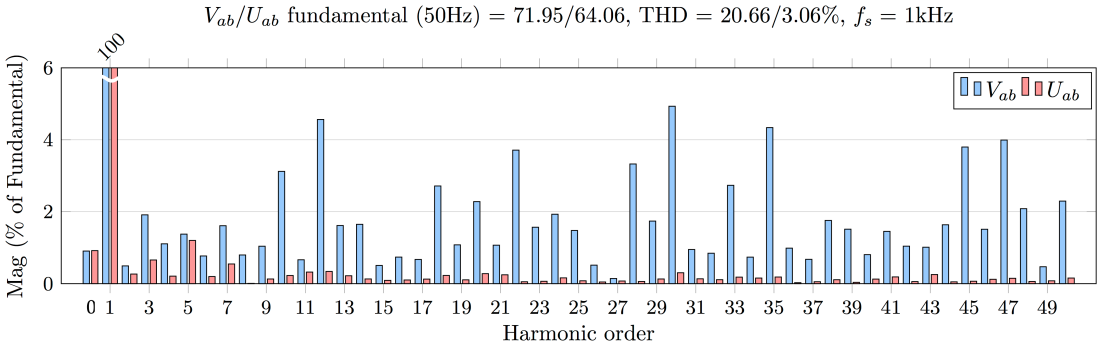


(a) **(b)**

Figure C.3 – Normalized line-to-line voltages from grid side (U_{ab}, U_{bc}) and inverter side (V_{ab}, V_{bc}), 'discharging' mode ($I_d = -1$): (a) Simulation (b) Experiment

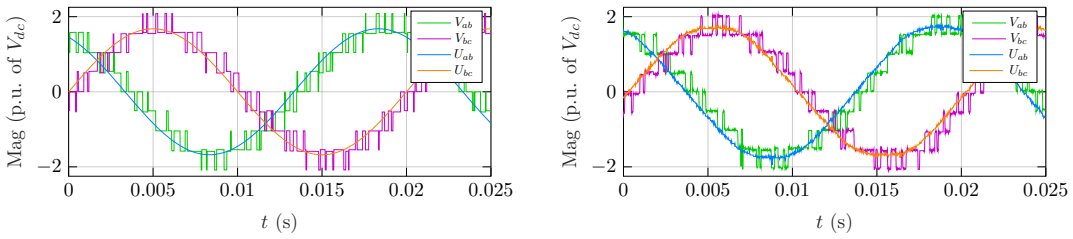


(a)



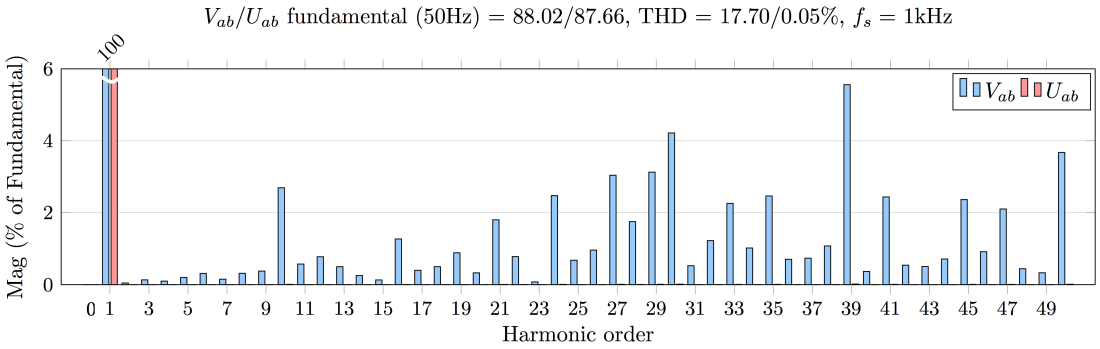
(b)

Figure C.4 – Harmonic content of line-to-line voltages from grid side (U_{ab}) and inverter side (V_{ab}), 'discharging' mode ($I_d = -1$): (a) Simulation (b) Experiment

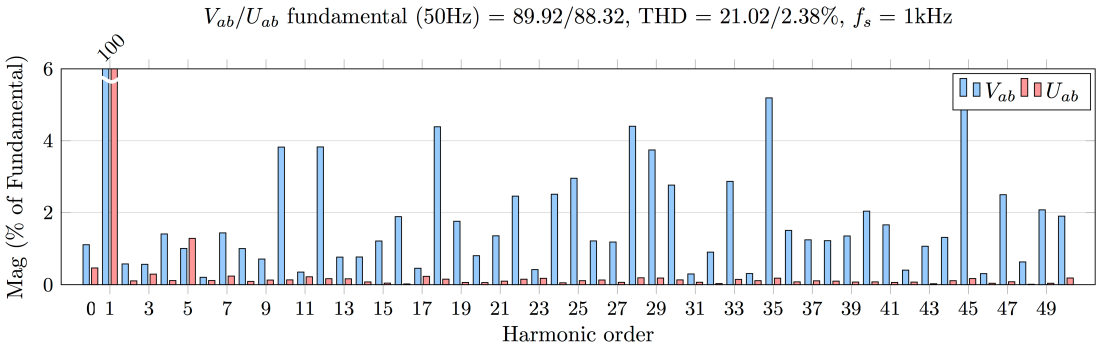


(a) **(b)**

Figure C.5 – Normalized line-to-line voltages from grid side (U_{ab}, U_{bc}) and inverter side (V_{ab}, V_{bc}), 'charging' mode ($I_d = 1$), $V_{rms} = 65V$: (a) Simulation (b) Experiment



(a)



(b)

Figure C.6 – Harmonic content of line-to-line voltages from grid side (U_{ab}) and inverter side (V_{ab}), 'charging' mode ($I_d = 1$), $V_{rms} = 65V$: (a) Simulation (b) Experiment

3-phase five-level CHB inverter (experiment results)

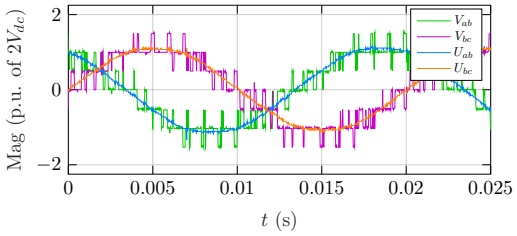


Figure C.7 – Normalized line-to-line voltages from grid side (U_{ab}, U_{bc}) and inverter side (V_{ab}, V_{bc}), 'zero current' mode ($I_d = 0$), $V_{rms} = 80V$

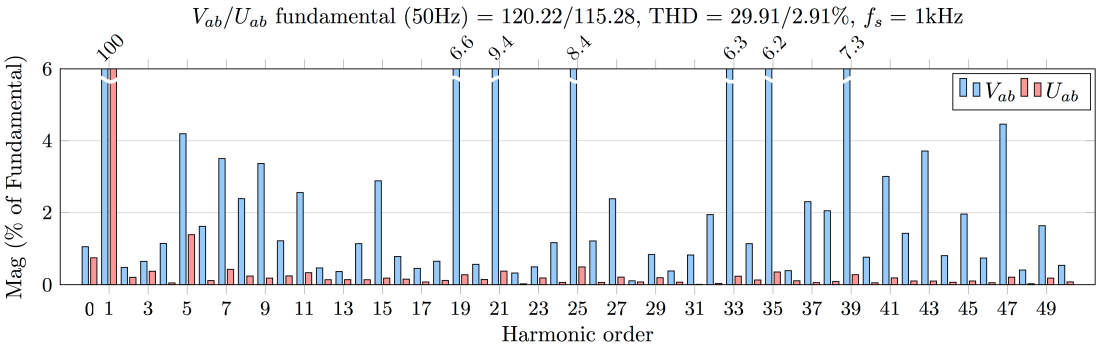


Figure C.8 – Harmonic content of line-to-line voltages from grid side (U_{ab}) and inverter side (V_{ab}), 'zero current' mode ($I_d = 0$), $V_{rms} = 80V$

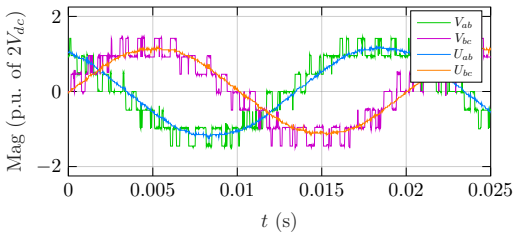


Figure C.9 – Normalized line-to-line voltages from grid side (U_{ab}, U_{bc}) and inverter side (V_{ab}, V_{bc}), 'discharging' mode ($I_d = -1$), $V_{rms} = 80V$

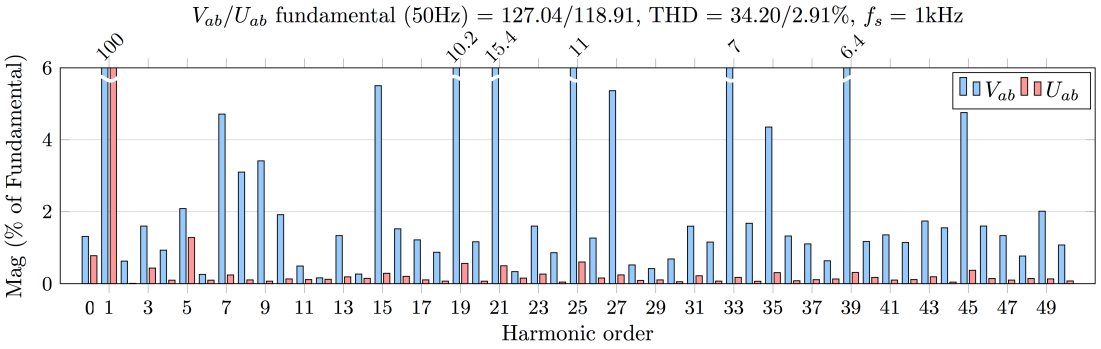


Figure C.10 – Harmonic content of line-to-line voltages from grid side (U_{ab}) and inverter side (V_{ab}), 'discharging' mode ($I_d = -1$), $V_{rms} = 80V$

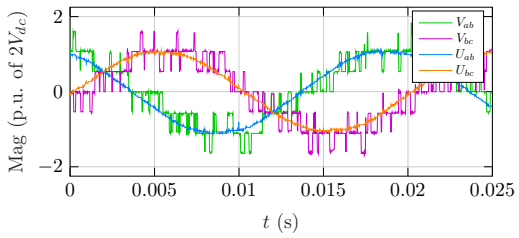


Figure C.11 – Normalized line-to-line voltages from grid side (U_{ab}, U_{bc}) and inverter side (V_{ab}, V_{bc}), 'charging' mode ($I_d = 1$), $V_{rms} = 80V$

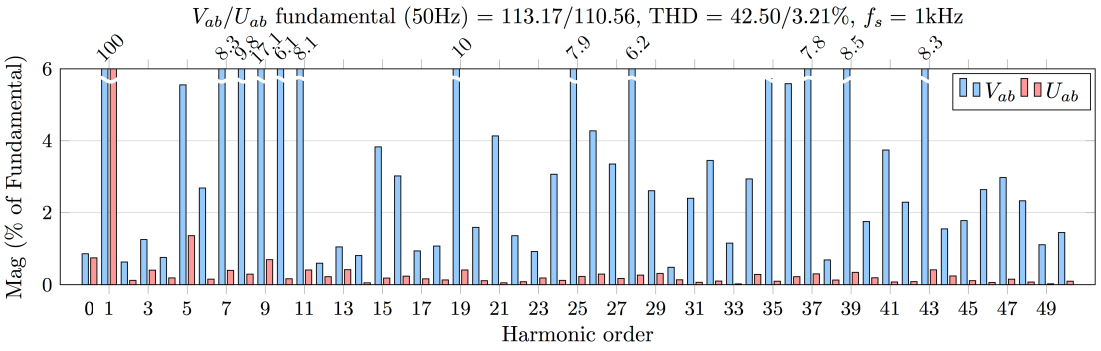


Figure C.12 – Harmonic content of line-to-line voltages from grid side (U_{ab}) and inverter side (V_{ab}), 'charging' mode ($I_d = 1$), $V_{rms} = 80V$

Appendix D. Design failure modes and effect analysis

Table D.1 – Design failure modes and effects analysis for LDN submodule

Item	Function description	Potential failure mode	Potential effect(s) of failure	Severity (S)	Potential cause(s)/ mechanism of failure	Occurrence (O)	Current design controls detection	Detection (D)	**RPN**
Electrolytic caps (C11-C16)	LDN caps	OPEN	Slight increase in V_{cap} fluctuation leading into small asymmetry of generated voltage levels	2	Over-stress of component, heat, component break	1	Turn on test	2	**4**
		SHORT	The power circuit is still able to operate with reduction in performance. Reduction in voltage levels, current close to sinewave in all operating modes	3	Solder bridge	1	Visual inspection, Turn on test	2	**6**
Ceramic caps (C1-C10)	LDN caps	OPEN	No effect	1	Over-stress of component, heat, component break	1	Turn on test	2	**2**
		SHORT	The power circuit is still able to operate with reduction in performance. Reduction in voltage levels, current close to sinewave in all operating modes	3	Solder bridge	1	Visual inspection, Turn on test	2	**6**
Terminals MECH1, MECH2; Power LDN, PWRGND rails	Power circuit	OPEN	Overvoltage between the power terminals, damage LDN caps and other components	5	Poor soldering, loose connection, over-heating	1	Visual inspection Turn on test	3	**15**

		SHORT	The power circuit is still able to operate with reduction in performance. Reduction in voltage levels, current close to sinewave in all operating modes	3	Solder bridge	1	Visual inspection Turn on test	2	**6**
Diodes (D1-D6)	PWM circuit	OPEN	No effect	1	Poor soldering, missing component, over-heating	1	Visual inspection Turn on test	2	**2**
		SHORT	Due to asymmetric operation (PWM pin of one phase is grounded), V_{cap} rapidly increases, damaging LDN caps	5	Overvoltage, solder bridge	1	Turn on test	3	**15**
Terminals MECH3-MECH5; Control PWM, GND rails	PWM circuit	OPEN	Due to asymmetric operation (PWM pin of one phase is grounded), V_{cap} rapidly increases, damaging LDN caps	5	Poor soldering, loose connection	1	Visual inspection Turn on test	2	**10**
		SHORT		5	Solder bridge	1		2	**10**
Terminals MECH6-MECH8; Power OA,OB, OC rails	Power circuit	OPEN	Due to asymmetric operation (one phase is open), current through LDN caps increases, output voltages are asymmetrical	4	Poor soldering, loose connection	1	Visual inspection, Turn on test	2	**8**
		SHORT OA to OB, OB to OC, OC to OA	Due to rapid LDN caps discharge huge current will go through circuit, damaging the LDN caps and other components	5	Solder bridge	1	Turn on test	2	**10**

DC/DC converter 48/12V	Control circuit power supply	OPEN	Control circuit and gate drives are disabled. V_{cap} rapidly increases, damaging LDN caps	5	Poor soldering, loose connection	1	Visual inspection Turn on test	2	**10**
		SHORT (input pins); Polarity mismatch	Cause the permanent damage of the DC/DC converter. Control circuit and gate drives are disabled. V_{cap} rapidly increases, damaging LDN caps	5	Solder bridge, polarity mismatch	1	Visual inspection Turn on test	2	**10**
		SHORT (output pins)	Control circuit and gate drives are disabled. V_{cap} rapidly increases, damaging LDN caps	5	Solder bridge	1	Visual inspection Turn on test	2	**10**
DC/DC converter 12/5V	Control circuit power supply	OPEN	Control circuit and gate drives are disabled. V_{cap} rapidly increases, damaging LDN caps	5	Poor soldering, loose connection	1	Visual inspection Turn on test	2	**10**
		SHORT (input, output pins); Polarity mismatch	Cause the permanent damage of the DC/DC converter. Control circuit and gate drives are disabled. V_{cap} rapidly increases, damaging LDN caps	5	Solder bridge, polarity mismatch	1	Visual inspection Turn on test	2	**10**
Gate drives	Control circuit	OPEN (enabled pins)	Due to asymmetric operation (the gate drive is disabled), V_{cap} rapidly increases, damaging LDN caps	5	Poor soldering	1	Visual inspection Turn on test	2	**10**
		SHORT		5	Solder bridge	1		2	**10**

MOSFETs (d-s)	Power circuit	OPEN	Due to asymmetric operation (one MOSFET is open), V_{cap} rapidly increases, damaging LDN caps	5	Poor soldering, over-heating, component break	1	Visual inspection, Turn on test	3	**15**
		SHORT	Due to rapid LDN caps discharge huge current will go through circuit, damaging the LDN caps and other components	5	Solder bridge	1	Turn on test	2	**10**
Caps CBL5, C5VA1, C5VA2, C12VBA, CBA, C12VA1, C12VA2	Control circuit voltage stabilization	OPEN	No effect	1	Poor soldering, missing component	1	Visual inspection Turn on test	2	**2**
		SHORT	Control circuit and gate drives are disabled. V_{cap} rapidly increases, damaging LDN caps	5	Solder bridge	1	Visual inspection Turn on test	2	**10**
Caps CSN1, CSN2	Power circuit (snubbers)	OPEN	Increased voltage ripples, possible overvoltage	2	Poor soldering, missing component	1	Visual inspection Turn on test	2	**4**
		SHORT	Asymmetrical operation, due to current flow between d-s pins. This current is small, owing to high resistance in the circuit, however may lead d-s short circuit	4	Solder bridge	1	Visual inspection Turn on test	2	**8**
Resistors RSN1, RSN2	Power circuit (snubbers)	OPEN	Increased voltage ripples, possible overvoltage	2	Poor soldering, missing component	1	Visual inspection Turn on test	2	**4**
		SHORT	No effect	1	Solder bridge	1	Visual inspection Turn on test	2	**2**

Table D.2 – Design failure modes and effects analysis for HB submodule

Item	Function description	Potential failure mode	Potential effect(s) of failure	Severity (S)	Potential cause(s)/ mechanism of failure	Occurrence (O)	Current design controls detection	Detection (D)	**RPN**
Electrolytic caps (C11,C12)	DC-link caps	OPEN	Almost no effect due to the batteries are fully charged, if it is not the case, than slight asymmetry can be observed	2	Over-stress of component, heat, component break	1	Turn on test	2	**4**
		SHORT	Due to short circuit between battery's terminals, destroys the module, may also destroy the battery and lead to fire. Asymmetric operation leads to an increase of V_{cap} of LDN caps	5	Solder bridge	1	Visual inspection, Turn on test	3	**15**
Ceramic caps (C1-C10)	DC-link caps	OPEN	No effect	1	Over-stress of component, heat, component break	1	Turn on test	2	**2**
		SHORT	Due to short circuit between battery's terminals, destroys the module, may also destroy the battery and lead to fire. Asymmetric operation leads to an increase of V_{cap} of LDN caps	5	Solder bridge	1	Visual inspection, Turn on test	3	**15**

Terminals MECH1, MECH2; Power I+, PWRGND rails	Power circuit	OPEN	Highly asymmetric regime, leading to an increase of V_{cap} of LDN caps	4	Poor soldering, loose connection, over-heating	1	Visual inspection Turn on test	3	**12**
		SHORT	Due to short circuit between battery's terminals, destroys the module, may also destroy the battery and lead to fire. Asymmetric operation leads to an increase of V_{cap} of LDN caps	5	Solder bridge	1	Visual inspection Turn on test	3	**15**
Diodes (D1-D4)	PWM circuit	OPEN	No effect	1	Poor soldering missing component over-heating	1	Visual inspection Turn on test	2	**2**
		SHORT	Highly asymmetric regime, leading to a slight increase of V_{cap} of LDN caps	4	Overvoltage, solder bridge	1	Turn on test	3	**12**
Terminals MECH3, MECH4; Control PWM, GND rails	PWM circuit	OPEN	Highly asymmetric regime, leading to a slight increase of V_{cap} of LDN caps	4	Poor soldering, loose connection	1	Visual inspection Turn on test	2	**8**
		SHORT		4	Solder bridge	1		2	**8**
Output terminals; Power O+,O- rails	Power circuit	OPEN	Highly asymmetric operation (one phase is open), current through LDN caps increases, output voltages are asymmetrical	4	Poor soldering, loose connection	1	Visual inspection, Turn on test	2	**8**

		SHORT O+A to O+B, O+B to O+C, O+C to O+A	Due to short circuit between output terminals huge current will go through circuit, damaging the module and other components	5	Solder bridge	1	Turn on test	3	**15**
DC/DC converter 48/12V	Control circuit power supply	OPEN	Control circuit and gate drives are disabled. Highly asymmetric regime, leading to a slight increase of V_{cap} of LDN caps	4	Poor soldering, loose connection	1	Visual inspection Turn on test	2	**8**
		SHORT (input pins); Polarity mismatch	Cause the permanent damage of the DC/DC converter. Control circuit and gate drives are disabled. Highly asymmetric regime, leading to a slight increase of V_{cap} of LDN caps	4	Solder bridge, polarity mismatch	1	Visual inspection Turn on test	2	**8**
		SHORT (output pins)	Control circuit and gate drives are disabled. Highly asymmetric regime, leading to a slight increase of V_{cap} of LDN caps	4	Solder bridge	1	Visual inspection Turn on test	2	**8**
DC/DC converter 12/5V	Control circuit power supply	OPEN	Control circuit and gate drives are disabled. Highly asymmetric regime, leading to a slight increase of V_{cap} of LDN caps	4	Poor soldering, loose connection	1	Visual inspection Turn on test	2	**8**

		SHORT (input, output pins); Polarity mismatch	Cause the permanent damage of the DC/DC converter. Control circuit and gate drives are disabled. Highly asymmetric regime, leading to a slight increase of V_{cap} of LDN caps	4	Solder bridge, polarity mismatch	1	Visual inspection Turn on test	2	**8**
Gate drives	Control circuit	OPEN (enabled pins)	Due to asymmetric operation (the gate drive is disabled), leading to a slight increase of V_{cap} of LDN caps	4	Poor soldering	1	Visual inspection Turn on test	2	**8**
		SHORT		4	Solder bridge	1		2	**8**
MOSFETs (d-s)	Power circuit	OPEN	Due to asymmetric operation (one MOSFET is open), there is a slight increase of V_{cap} of LDN caps	4	Poor soldering, over-heating, component break	1	Visual inspection, Turn on test	3	**12**
		SHORT	Huge current will go through circuit, damaging the module and other components	5	Solder bridge	1	Turn on test	2	**10**
Caps C5VL1, C5VL2, C12VBL, CBL, C12VL1, C12VL2	Control circuit voltage stabilization	OPEN	No effect	1	Poor soldering, missing component	1	Visual inspection Turn on test	2	**2**
		SHORT	Control circuit and gate drives are disabled. Highly asymmetric regime, leading to a slight increase of V_{cap} of LDN caps	4	Solder bridge	1	Visual inspection Turn on test	2	**8**

Caps CSN1, CSN2	Power circuit (snubbers)	OPEN	Increased voltage ripples, possible overvoltage	2	Poor soldering, missing component	1	Visual inspection Turn on test	2	**4**
		SHORT	Asymmetrical operation, due to current flow between d-s pins. This current is small, owing to high resistance in the circuit, however may lead d-s short circuit	4	Solder bridge	1	Visual inspection Turn on test	2	**8**
Resistors RSN1, RSN2	Power circuit (snubbers)	OPEN	Increased voltage ripples, possible overvoltage	2	Poor soldering, missing component	1	Visual inspection Turn on test	2	**4**
		SHORT	No effect	1	Solder bridge	1	Visual inspection Turn on test	2	**2**