Alma Mater Studiorum - Università di Bologna
Campus di Cesena

Dipartimento di
Ingegneria dell'Energia Elettrica e dell'Informazione
"Guglielmo Marconi"

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AN EIS-BASED LOW-POWER SOLUTION FOR ONLINE AND IN-SITU LITHIUM-ION BATTERY MONITORING IN AUTONOMOUS DRONES

Elaborato in
Misure Elettroniche

Relatore:
Prof. MARCO CRESCENTINI

Presentata da:
MORENA FABOZZI

Correlatore:
Dott.ssa ROBERTA RAMILLI

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Sesssione I

Abstract

In recent years, the electrification process has revolutionized various applications across mobility sectors, leading to the development of numerous battery-powered systems and devices. These high-energy applications, such as electric vehicles and drones, require batteries that ensure optimal performance, long-term reliability, and safety to guarantee widespread adoption. Therefore, it is essential to develop robust battery monitoring systems.

This thesis presents a compact and low-power system for online monitoring of lithium-ion batteries based on electrochemical impedance spectroscopy. The project focuses on designing a hardware solution using low-cost off-the-shelf components to facilitate integration into real-world battery management systems, e.g., for mounting in commercial drones. The proposed architecture employs a two-voltage measurement procedure that acquires the battery voltage response to a multisine excitation within the 1-1000 Hz frequency range while indirectly assessing current through a reference resistor. This approach significantly reduces measurement time, making the system suitable for monitoring batteries during regular operation.

To validate system performance, a comprehensive CAD-based analysis was conducted using *TINA-TI* software. Simulations focused on overall system behavior, thermal noise contribution from components, and power consumption. The results demonstrated negligible power consumption compared to the application's power budget, as well as high resolution since the system has the capability to detect impedance variations down to 1 mΩ.

In conclusion, this project contributes to the development of more efficient strategies for battery management and maintenance, offering potential benefits in terms of battery performance, longevity, and reliability.

Contents

List of Acronyms

Introduction

In recent years, the world has experienced a remarkable process of electrification across various sectors, driven by research and development of smart, connected, and sustainable urban solutions [1]. The convergence of the energy and mobility sectors has become increasingly visible in a variety of battery-powered applications and industries, encompassing a wide range of vehicles, transportation modes [2, 3], and other use cases [4]. Autonomous drones - or unmanned aerial vehicles (UAVs) - are examples of this convergence. Due to their inherent versatility and adaptable designs for specific purposes, UAVs have become essential tools for accomplishing a wide variety of tasks swiftly and efficiently. Among other applications, UAVs are increasingly being integrated into the logistics market [5], for inspection services [6], surveillance [7, 8], and environmental monitoring [9].

Given the rapid expansion of UAVs and the strong push for electrification of the mobility sector as a whole, optimizing battery performance has become a critical research topic [10, 11]. In this regard, lithium-ion batteries (LIBs) stand out among other commercial rechargeable battery technologies, as they provide well-suited features for e-mobility applications [12]. Despite being the most effective rechargeable energy storage systems currently available, a deeper assessment of their characteristics and aging mechanisms is essential in order to address lifetime, safety, and performance requirements. Consequently, LIB packs are equipped with a battery management system (BMS) that continuously evaluates battery state parameters, such as State of Charge (SOC) and State of Health (SOH), through online monitoring [13]. This approach ensures reliable, safe, and cost-effective service while minimizing downtime and maintaining optimal battery operation and health. At the same time, such monitoring is leading to the development of machine-learning-driven charging

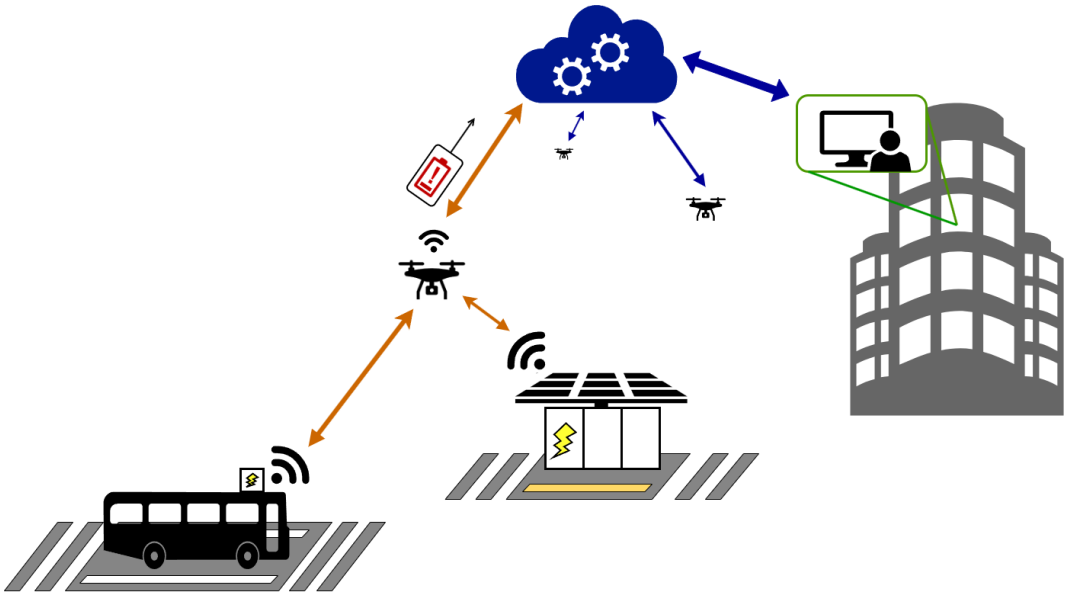


Figure 1: LIB-powered UAV ecosystem integrated into transportation services, showcasing wireless communication, cloud services, and online battery monitoring capabilities.

strategies, which aim to ultimately extend battery life and reduce the need for frequent battery replacements [14]. Figure 1 illustrates a typical real-world use case where drones are interconnected through wireless communication and cloud services. UAVs may communicate their status, such as battery discharge levels, to dynamically modify their flight mission and utilize wireless charging stations or e-bus rooftops as needed.

The SOC is an indicator of the remaining energy capacity in a battery at a given moment. The traditional methods of SOC estimation include Coulomb counting and voltage-based approaches [15]. However, these methods require initial SOC knowledge and periodic calibration, in addition to suffering from uncertainties in modeling, timing drifting errors, and often requiring battery rest periods to reduce these effects [16]. The SOH metric evaluates the aging level of batteries, providing valuable information for predicting when battery replacement is necessary. Nonetheless, direct SOH measurement is unfeasible, resulting in a challenging estimation task [17]. Although these conventional methods have been extensively researched, they suffer from intrinsic problems that make them unsuitable for online monitoring applications [18].

Other methods of determining battery state parameters are based on the estimation of the LIB impedance since it provides valuable insights into the LIB electrochemical state, which is intrinsically affected by several factors, such as remaining capacity, aging, and temperature [19]. Electrochemical impedance spectroscopy (EIS) is a widely employed non-invasive technique for the characterization of LIB cells in the laboratory [20]. EIS has been extensively used in numerous studies to assess battery performance under various operational conditions, including SOC [21] and SOH estimation [22], temperature monitoring [23], and analysis of electrochemical aging processes [24]. Unfortunately, these applications require specialized bench-top equipment, which makes EIS primarily limited to offline ex-situ laboratory measurements. Driven by the capabilities of EIS to accurately evaluate LIB impedance - as it can potentially overcome current and voltage method limitation - research efforts are focused on designing low-cost and portable EIS systems that enable impedance estimation while the measurement system operates [25, 26]. The work cited in Ref. [25] presents an embedded EIS measurement system optimized for laboratory measurements, which require significant reductions to enable deployment in real-world applications. Furthermore, in Ref. [26] a cost-effective and compact EIS system is presented, based on a commercially available integrated circuit that provides high-precision impedance measurement. This approach exhibits limitations in UAV applications which require less power-consuming conditioning circuitry. Therefore, there are still unresolved challenges in the development of an online EIS measurement system that is directly connected to a LIB within a battery-powered device operating in its actual-world setting [13].

EIS techniques rely on measuring the battery response to a designed excitation signal, which is typically evaluated over a frequency range of 1 to 1000 Hz [20]. Traditional EIS employs a single-frequency excitation signal, where the excitation consists of a single sinusoidal component whose frequency is varied across the desired range; battery response measurement and the corresponding impedance evaluation are taken at each frequency point. On the contrary, broadband techniques employs excitation signals composed of multiple frequency components, enabling measurements at multiple frequencies concurrently [27]. Compared to conventional narrowband excitation methods,

broadband excitation signals - especially those employing multisine excitation signals - offer advantages in terms of measurement speed, making them well-suited for online applications [28].

An online EIS monitoring system integrated directly into battery-powered devices is a promising research topic, which presents the discussed challenges of reducing measurement time, minimizing system size and power consumption. This thesis proposes a compact and low-power system for online monitoring, designed to facilitate integration into LIB-powered devices and provide real-time operation during battery usage. The sensing approach is based on multisine EIS, to make a rapid and accurate low impedance estimation (few mΩ) within the $1 - 1000$ Hz frequency range. An architecture implementing the EIS technique is proposed, which includes off-the-shelf components carefully selected to address our objectives. The prototype also includes an *Arduino Nano IOT* board, which is used for system management, especially providing communication between board components and with the external environment. The proposed system is analyzed using CAD tools to evaluate system-level signal behavior and noise performance, as well as to assess the impedance of the LIB cell and validate the analysis. While the *Arduino* board simplifies prototyping, a dedicated multi-protocol microcontroller with integrated wireless capabilities could potentially replace it to further reduce system size and provide a purpose-built solution. Future work could also explore loop-powered solutions, wherein the monitored battery serves as the power source for the monitoring system itself.

This thesis is structured as follows. Chapter I presents a theoretical background to battery characterization, describing battery state parameters, estimation methodologies described in literature focusing on the specific technique selected for this application. Chapter II delineates the proposed measurement system, outlining the requirements imposed by our specific use case; while Chapter III illustrates the implementation of the proposed system architecture, detailing the selection of components and layout strategies employed for the printed circuit board (PCB) design. Chapter IV shows the preliminary performance assessment results, which include system-level, noise, and power consumption analyses. Finally, Chapter V draws the conclusions and identifies potential enhancements for future versions.

This thesis project has resulted in a publication presented at the *IEEE MetroAutomotive 2024* conference [29].

Chapter 1

Battery State Estimation

Given the complex nonlinear nature of batteries and their numerous state variables, an accurate methodology is required to ensure optimal battery state estimation for BMS. This chapter describes various theoretical approaches developed to address the battery state estimation requirements. Particular attention is given to techniques tailored for online monitoring, thereby facilitating the regular operation of the battery under test in UAV applications.

1.1 State Parameters

BMSs require a precise knowledge of key battery state parameters, such as SOC and SOH, to be able to characterize critical aspects of battery performance, including remaining capacity and expected lifespan [15]. Nonetheless, their estimation poses significant challenges given the complex electrochemical processes within batteries and their sensitivity to operating conditions.

State of Charge

The SOC represents the energy currently stored in a battery, typically expressed as a percentage relative to the battery full capacity. Accurate estimation of SOC is essential for determining the maximum power capabilities of a battery, especially in mobility applications where the system requires comprehensive knowledge of the available power to make appropriate operational decisions.

SOC is defined as the ratio of the currently available amount of charge Q_{av} to the maximum available amount of charge when the battery is fully charged

Q_{full} [30]:

$$SOC = \frac{Q_{av}}{Q_{full}} \times 100\% \tag{1.1}$$

The available charge amount is related to the available capacity, which refers to the energy a given battery could supply in a specific application under actual conditions. Indeed, this parameter may differ from battery nominal capacity since the battery state can be influenced by various factors, such as age, external and environmental conditions.

The available capacity is usually measured through a procedure that involves the full charge of the battery followed by a discharge until it reaches a predefined voltage level, all while maintaining constant measurement conditions, such as discharge nominal current and temperature. Due to the inherent nature of this approach, it is solely accessible in offline measurements. Other methodologies should be employed for online measurements, as described in the subsequent sections.

State of Health

The SOH represents the actual capacity of the battery, expressed as a percentage relative to its nominal value. It reflects battery current life condition and is essential for assessing battery lifespan, making health prognoses and monitoring battery performance degradation over time.

Specifically, the battery capacity decreases and its resistance increases over the lifetime of a battery. Hence, SOH can be characterized through two different expressions relying on capacity or resistance variations as follows [17]:

$$SOH = \frac{C_{actual}}{C_{nominal}} \times 100 \tag{1.2}$$

$$SOH = \frac{R_{EOL} - R_{actual}}{R_{EOL} - R_{new}} \times 100 \tag{1.3}$$

In eq. (1.2), C_{actual} represents the battery current maximum capacity after a discharge cycle, and $C_{nominal}$ represents the nominal capacity of a new battery. In eq. (1.3), the battery internal resistance when new, in the current state, and at the end of life (i.e., when its internal resistance becomes two times the initial value) are represented by R_{new}, R_{actual}, and R_{EOL}, respectively.

Directly obtaining SOH in online monitoring could be challenging, especially when employing approaches based on eq. (1.2) which require a battery

discharge. Methodologies based on impedance estimation might be more suitable for SOH evaluation, leveraging the relationship between impedance spectrum and battery cell aging.

1.2 Estimation Methodologies

This section briefly presents the principal methodologies outlined in the literature for monitoring battery state parameters, focusing on their strengths and weaknesses compared to the selected EIS technique.

1.2.1 Coulomb Counting

The Coulomb counting technique is a widely employed method for SOC estimation in LIBs. This approach relies on the integration of the current flowing in and out of the battery over time [16].

Despite its simple structure and implementation, which make it a solid basis for simple systems, the accuracy of the Coulomb counting technique depends on the availability of the battery initial SOC and nominal capacity for SOH estimation. These values may not always be accessible, especially in real-world applications where discharge conditions may change and different batteries may be used. For instance, factors such as battery aging and temperature variations may affect the nominal capacity, potentially leading to SOH estimation errors. Moreover, the method tends to accumulate errors over extended monitoring times, which could potentially lead to a drift in the estimation. It becomes necessary to do frequent system calibration to prevent accumulated errors and determine the correct values. This requirement is a significant drawback for online monitoring since recalibration may not always be as feasible as it is in laboratory testing.

To mitigate these limitations, Coulomb counting is often combined with other methods, such as model-based methods or voltage-based ones, in order to enhance its robustness and accuracy [31].

1.2.2 OCV-Based Estimation

The open-circuit voltage (OCV) method is a simple technique used for battery state parameter estimation. The OCV is defined as the voltage between the two terminals of the battery when no current is flowing.

For SOC estimation, the method requires a prior construction of an OCV-SOC look-up table based on the relationship between these two metrics. This look-up table is created by measuring the OCV at various SOC levels under specific operating conditions. During the monitoring phase, the SOC is then determined by measuring the battery OCV and checking the corresponding SOC value in the look-up table [32]. Furthermore, for the SOH estimation, the method requires precise battery models that characterize battery aging processes. The model responses could be combined with the charging curve to predict battery SOH [33].

In contrast to the Coulomb counting technique, the OCV-SOC relationship exhibits slight changes over the battery lifespan, making it a good option for combining to provide a more robust and accurate SOC estimation system [34]

Nevertheless, this approach has several limitations in real-world applications, especially related to the OCV measurement. The battery requires an extended rest period to achieve the equilibrium condition and guarantee an accurate OCV measurement. This requirement makes the method unsuitable for online monitoring when the battery needs to operate in normal conditions.

1.2.3 Impedance-Based Estimation

Impedance-based methods have gained popularity for battery state parameter estimation, especially for SOC and SOH estimations of various battery types, including LIBs. These methods exploit the information regarding battery behavior acquired from the observation of battery impedance variations at selected frequencies.

Electrochemical impedance spectroscopy is a well-established technique in this category [20]. It requires an electrochemical model that describes the battery internal processes and states. An equivalent circuit model (ECM) could be employed in many applications to characterize the battery impedance [15] as it is a simplified representation of the complex electrochemical processes occurring within the battery. This model could include simple electrical components such as internal ohmic resistance, polarization resistance and capacitance, inductance, constant phase and Warburg elements. This characterization facilitates the creation of look-up tables that relate these parameters to the battery SOC and SOH.

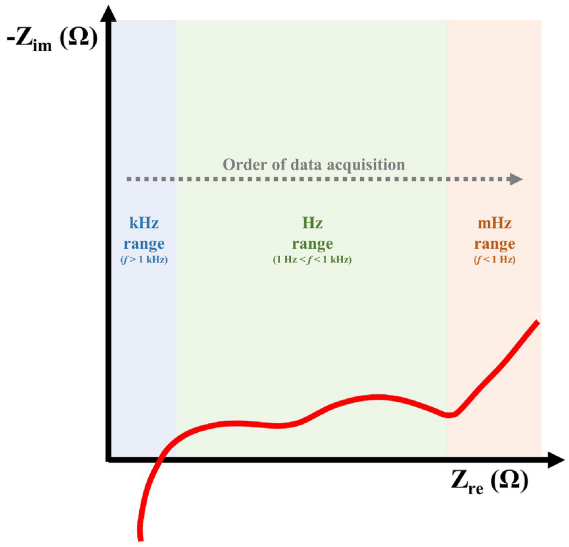


Figure 1.1: Graphical representation of a typical LIB EIS measurement presented in a complex impedance plot [20].

The main challenge of these methods involves measuring very low impedance magnitudes, typically in the order of a few mΩ for LIBs [35]. Researchers are focusing on overcoming these challenges since the technique offers non-invasive monitoring and valuable insights into battery behavior. Moreover, it could potentially be performed online without the need for calibration or rest periods, which the previously discussed methods require.

Its implementation in online and *in-situ* battery monitoring systems could be complex, given the actual requirement for specialized equipment to perform accurate impedance measurements [36]. However, impedance-based methods employed in online applications are still an active area of research due to their potential to provide detailed information about battery states [21, 22, 24].

Interpretation of Battery Impedance Spectrum: Cole-Cole Plot

The Cole-Cole plot is widely used for representing battery impedance. In this graph, x-axis shows the real part of the impedance and y-axis shows the negative imaginary part. Figure 1.1 depicts a typical impedance spectrum of a battery cell, illustrating various behavior at different frequencies.

The impedance spectrum is divided into three different regions that correspond to specific electrochemical processes and frequency ranges:

- High-frequency range (kHz): This region is characterized by a small inductive tail located in the fourth quadrant of the Cole-Cole plot. This behavior is influenced primarily by inductive parasitic effects associated with the connection between the battery cell and the measurement system. These effects include the response of connecting wires and of electrical metallic contacts.

- Middle-Frequency Range (Hz): This region is composed of one or more semicircular arcs that reflect the electrochemical processes occurring at the interfaces within the battery cell, especially between the electrodes and the electrolyte. This behavior is characterized by a combination of resistive and capacitive effects, often modeled in ECM using parallel resistor-capacitor (RC) circuits or constant phase element (CPE).

- Low-Frequency Range (mHz): The low-frequency tail represents the diffusion of solid-state lithium-ion within the active material of the cell electrodes. This phenomenon, modeled using the Warburg impedance, is significant for understanding the battery's long-term behavior and capacity, making this region crucial for accurate estimation of the battery state parameters.

In order to guarantee accurate monitoring of the battery state parameters, measurements should focus on the middle-frequency and low-frequency range. Indeed, fig. 1.2 shows how the impedance spectrum varies under different conditions, including SOC (fig. 1.2a), number of charging-discharging cycles (fig. 1.2b), and temperature (fig. 1.2c). These variations are more evident in the transition region between the last arc in the middle-frequency range and the beginning of the tail in the low-frequency range, making this frequency band particularly interesting for battery monitoring. For instance, as illustrated in fig. 1.2, an increase in the width of the middle-frequency arc may be associated with a lower SOC level, decreased operating temperature, or battery aging.

By carefully analyzing these spectral features and employing specific algorithms, it becomes possible to isolate and attribute impedance variations to specific effects.

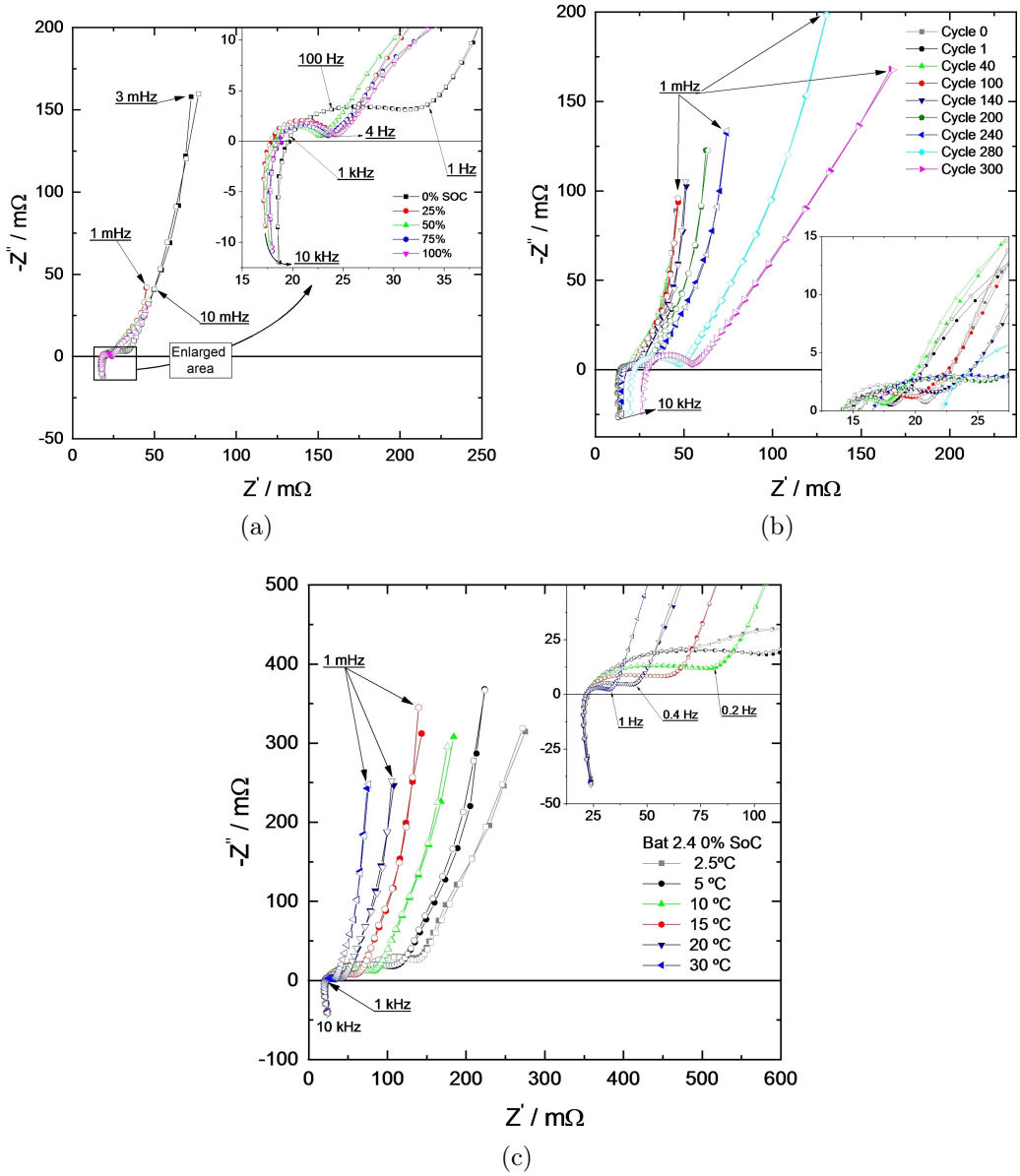


Figure 1.2: Impedance spectra for varying (a) SOC, (b) cycle count, and (c) temperature [37].

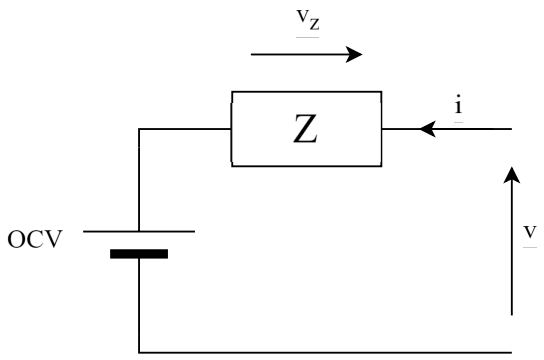


Figure 1.3: Simplified ECM of a battery under linear time-invariant (LTI) conditions [38].

1.3 Electrochemical Impedance Spectroscopy

Electrochemical impedance spectroscopy is a well-established technique employed in battery monitoring.

In EIS, a battery is perturbated by a small-amplitude AC excitation signal, and the corresponding response is measured. Typically, a sinusoidal voltage or current is employed in order to evaluate the battery impedance using Ohm's law across a range of frequencies. In galvanostatic experiments, the current is the input signal and the voltage is the measured output; while in potentiostatic experiments, the voltage is the input signal and the current is the measured output.

Galvanostatic approach is the most commonly employed method for EIS on batteries due to their low impedance. The generic model of the measurement system, as depicted in fig. 1.3, can be represented in the following simplified form [38]:

$$v(t) = OCV + v_z(t) = OCV + Z * i(t) \tag{1.4}$$

where $v(t)$ is the voltage measured across the battery, OCV is the open-circuit voltage (assumed constant), Z is the battery impedance, $i(t)$ is the excitation current signal, and $v_z(t)$ is the battery voltage response to the perturbation.

This model assumes a LTI system, which must guarantee both linearity and time-invariance requirements [35]. However, batteries have a nonlinear behavior due to diffusion and charge transfer effects with regular amplitude perturbations. Therefore, in order to preserve the linearity criteria, a small-

amplitude AC excitation signal is required, typically in the range of few mA. This signal should also be large enough to produce a measurable response, defining an important trade-off in the project of the measurement system.

Similarly, time-invariance requires no variations in battery state during the measurement time. This steady-state approximation is challenging to achieve due to various factors that influence impedance, such as temperature, SOC, and aging effects. In order to guarantee a stationary system, fast measurement may help to minimize the impact of these time-dependent variations on the impedance measurements.

1.3.1 Excitation Signal

Single-Sine Excitation

Classical EIS employs a single-tone excitation signal, typically a sinusoidal current signal with a small amplitude I_k at a selected angular frequency ω_k expressed as

$$i(t) = I_k cos(\omega_k t) \tag{1.5}$$

The voltage response is also a sinusoidal signal at the same frequency, with different amplitude and phase, as determined by the battery impedance value. In this approach, selected angular frequencies $\omega_k = 1, 2, ..., N$ are applied sequentially in order to evaluate the impedance at each frequency.

Despite its simplicity and straightforward implementation, this methodology presents significant limitations for online monitoring applications. Indeed, for a desired wide-frequency band or very low-frequency monitoring, the measurement time becomes excessively long. Moreover, additional time is required between subsequent experiments in order to wait for transients to fade out at each frequency. This longer measurement time contradicts the time-invariance assumption, especially in dynamic real-world applications where batteries are used during measurement and are characterized by continuous state changes.

These limitations make the classical single-tone approach unsuitable for online monitoring.

Multisine Excitation

Broadband excitation may be employed to overcome the limitations of single-tone excitation [39].

An example is the multi-sine excitation composed of various frequency components simultaneously applied to the battery. The excitation signal is represented by the sum of sinusoidal signals at different frequencies :

$$i(t) = \sum_{k=1}^{N} I_k cos(\omega_k t + \phi_k) \tag{1.6}$$

where each sinusoidal component has an amplitude I_k, an angular frequency ω_k, and a phase ϕ_k. Since all of the above variables can be individually set for each component, it is possible to select a subset of frequency components to investigate a specific portion of the impedance spectrum, guaranteeing much flexibility. Typically, the implementation of the excitation signal is characterized by constant amplitude across components and random phases to minimize the overall crest factor [40].

Compared to single-sine experiments, multi-sine guarantees a shorter measurement time since all frequencies of interest are excited simultaneously [41, 42]. This feature is crucial to address the time-invariance approximation. However, it also presents challenges that involve linearity criteria. The superposition of multiple frequency components may result in an overall current excitation signal exceeding the desired few mA amplitude. A trade-off is essential in order to choose an optimal number of frequency components and corresponding amplitudes, which will allow for fast measurements and good signal-to-noise ratio (SNR) while keeping the overall amplitude within acceptable limits. This strategy involves the reduction of the individual component amplitudes, potentially compromising the SNR for each frequency and corrupting important information.

Therefore, this project focuses on the design of a high-precision, low-noise system capable of accurately measuring very small voltage responses.

Chapter 2

Measurement System Design

The ability to precisely monitor and analyze the electrochemical behavior of LIB is crucial for ensuring their safe and efficient operation in various domains, including UAV applications. Among the different methods used for battery monitoring, the EIS technique has shown to be an efficient diagnostic tool for BMS, providing information about electrochemical processes used to assess battery SOC and SOH. While several studies have shown that EIS is widely applicable in laboratory contexts, there are significant challenges when implementing it for real-time cell-level monitoring of rechargeable LIBs. These challenges include power consumption constraints, high-resolution sensing, temperature stability, reliability over time, and integration into real-world applications.

A system architecture is proposed to address these challenges for online EIS monitoring at the cell level. The proposed EIS measurement system is based on a galvanostatic approach, where the current signal applied to the battery under test causes a voltage response. This system measures the voltage and current signal simultaneously through two different channels, where a reference resistor is used to indirectly assess the current signal. The overall system architecture for the proposed battery impedance analyzer is depicted in fig. 2.1.

2.1 System Architecture

The impedance measurement module is the core of the system. It includes a high-resolution digital-to-analog converter (DAC) for generating the current

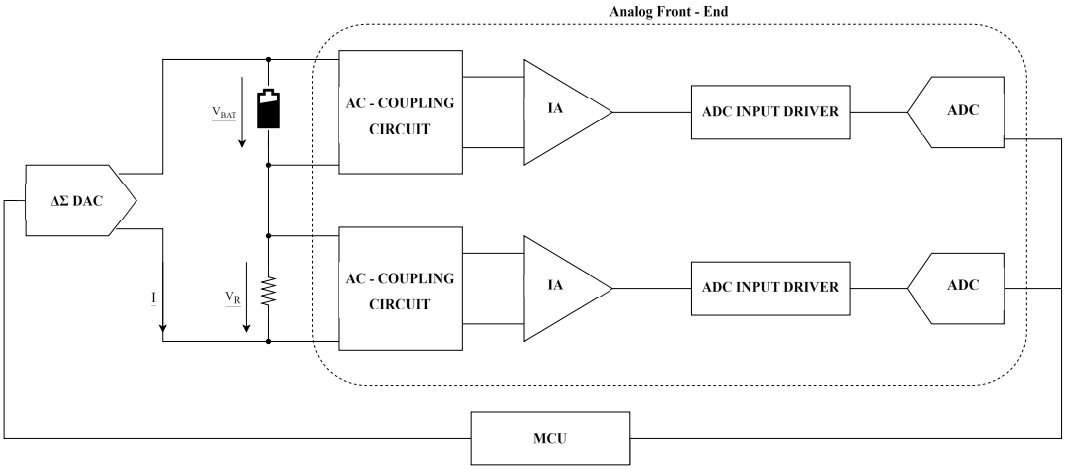


Figure 2.1: Block diagram representation of the proposed impedance analyzer for online EIS monitoring of battery cells.

excitation signal, a high-accuracy reference resistor for current measurement, and a dual-channel analog front-end (AFE) for voltage signal acquisition and conditioning. The AFE is composed of a low-noise instrumentation amplifier (IA) for amplifying the small amplitude of voltage responses and a high-resolution analog-to-digital converter (ADC) for sampling and digitizing the signals for subsequent signal processing. The selection of these components is essential to ensure accurate and reliable impedance measurements.

The DAC is crucial in generating the multisine excitation signal and minimizing quantization noise. The $\Delta\Sigma$ DACs, with their inherent oversampling and noise-shaping techniques, are preferred due to the restrictions on the excitation signal amplitude described in section 1.3 on page 14 and the low impedance characteristics of the battery under test. This preference allows for enhanced performance regarding signal-to-quantization noise ratio (SQNR) and effective number of bits (ENOB). Additionally, current-output DACs offer straightforward hardware configuration, eliminating the need for additional external components to convert the voltage signal into current. This configuration facilitates efficient current injection with minimal added noise, rendering it well-suited for this application. The output current range is required to provide mA amplitudes to satisfy the linearity constraints of EIS, as discussed in section 1.3 on page 14.

For the best current sensing results, it is recommended that a reference re-

sistor with a resistance value of the same order of magnitude as the battery DC resistance is chosen. As discussed in section 2.2, the synchronous transduction technique is essential to ensure an accurate current measurement.

The AFE is of utmost importance for conditioning and measuring voltage responses, especially considering the small amplitude of the signal under test. The AFE comprises two measurement paths simultaneously measuring the battery voltage response and the voltage drop across the reference resistor. This simultaneous acquisition approach ensures better synchronization between the two channels, which is crucial for accurate impedance measurements to reduce phase error due to misaligned measurements, as described in details in section 4.3.1. The following description refers solely to a single path, as they are complementary for the previously mentioned reason.

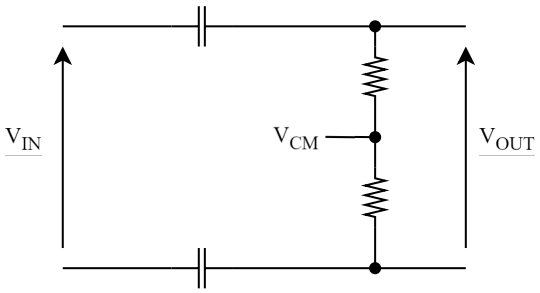


Figure 2.2: AC-coupling circuit schematic with two capacitors and two resistors.

The AC-coupling circuit, consisting of two capacitors and two resistors, as shown in fig. 2.2, is employed to block the battery OCV and other spurious DC components. This circuit facilitates a more precise detection of the differential voltage across the components, which contains relevant information. The resistor's role is to set the input common-mode voltage of the following amplification stage to a suitable value within the amplifier input voltage range, using the reference voltage V_{CM}. It is essential to carefully select the high-pass filter cut-off frequency to avoid attenuating the excitation signal frequency components within the frequency range of interest.

Given the low amplitude of the current excitation, designed to be in the order of few mA, and the low impedance values, typically in the range of tens of mΩ, the resulting differential voltage response across the components is expected to be relatively small, approximately in the range of hundreds of µV.

In order to ensure an appropriate SNR for accurate impedance measurements, a low-noise IA with an externally configurable and very high gain is used. This stage is essential for amplifying the low-voltage signals to levels suitable for the subsequent processing.

Following the IA stage, an ADC is employed for digitizing the amplified signal. The successive approximation register (SAR) ADCs offer a simple and efficient solution that aligns with the application, where the frequency range of interest is limited to a few kHz and power efficiency is crucial. Given these requirements, components that provide higher sampling frequency, such as flash or pipeline ADCs, are not necessary. Moreover, SAR ADCs offer an optimal trade-off between resolution and power consumption, especially when compared to $\Delta\Sigma$ ADCs at lower frequencies.

An ADC driver circuit is required to optimize the SAR ADC performance. The driver circuit, illustrated in fig. 2.3, is composed of three key components: a low-pass filter, an operational amplifier, and an anti-aliasing filter. The low-pass filter removes noise contributions introduced by the IA and provides coupling with the subsequent operational amplifier stage. It is designed to ensure that the relevant frequency components of the signal are not attenuated or distorted. The operational amplifier is configured as a unity-gain buffer, followed by an RC filter. This configuration provides proper driving and filtering capabilities, ensuring the ADC receives a clean and well-conditioned signal, while also isolating the signal source from the switched-capacitor input stage, which may potentially introduce sampling charge injection noise. Furthermore, it allows the driver circuit to address the bandwidth requirements of the ADC, which the IA cannot meet due to the high gain needed for amplifying the low-voltage signals.

The selection of dual-channel components for the IA and ADC facilitates a more compact system realization - as they are integrated on the same chip - and minimizes channel-to-channel dispersion, ensuring consistent performance across channels. Indeed, using single-channel components may lead to variations in individual channel characteristics, such as gain, offset, and response to external parameters. In our specific application, this different behavior between measurement paths could introduce additional sources of errors, presenting further challenges for system calibration and potentially compromising

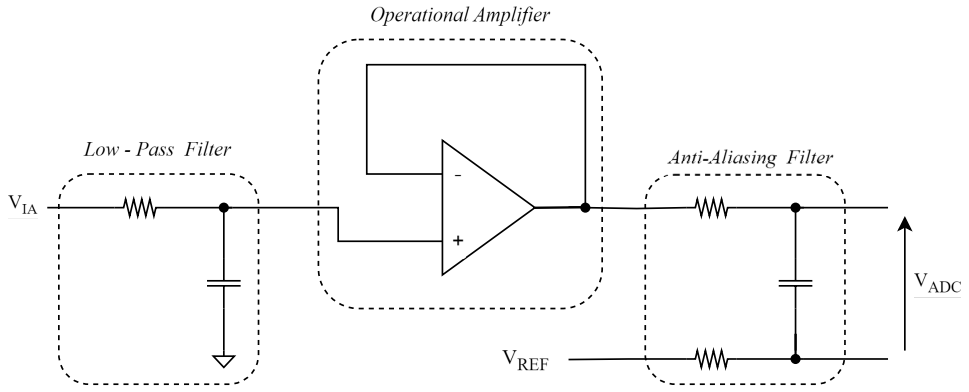


Figure 2.3: ADC input driver circuit schematic designed to condition the signal for accurate analog-to-digital conversion.

the accuracy of the entire system.

The digitized voltage signals obtained from the ADC are processed by a microcontroller unit (MCU), which is responsible for generating the excitation signal sequences, receiving the sampled voltage response sequences, and performing the necessary digital signal processing operations. The estimation of impedance is accomplished through frequency-domain techniques, such as the discrete Fourier transform (DFT), which separates the frequency components and calculates the impedance values based on the voltage and current measurements, as outlined in section 2.2. Moreover, the implementation of wireless communication interfaces facilitates remote monitoring and data transmission. This feature, crucial for UAV applications, allows for real-time transmission of impedance monitoring data upon the availability of a communication hot-spot, thereby enabling the integration of the system with cloud-based platforms. Consequently, centralized data analysis, remote diagnostics, and predictive maintenance strategies can be achieved, ensuring optimal battery performance and timely intervention for UAV operations.

2.2 Impedance Estimation: Two-Voltage Measurements

The impedance estimation procedure employs a two-voltage measurement technique, as illustrated by the simplified circuit example in fig. 2.4 on the next page. This method involves concurrently measuring two voltages across diffe-

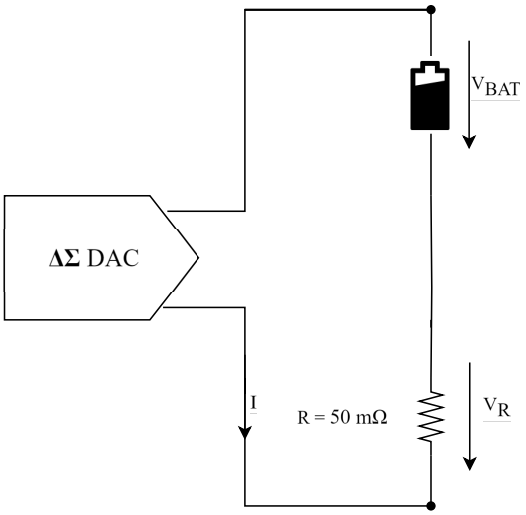


Figure 2.4: Simplified circuit diagram for impedance estimation of a battery cell using a reference resistor to ensure accurate current measurement.

rent points in the circuit: the first voltage V_{BAT} is measured across the battery under test, and the second voltage is measured directly across the reference resistor R connected in series with the battery. These measurements, combined with the known value of the reference resistor, allow for indirect evaluation of the current I flowing through the battery. In this application, the excitation current is a multisine signal designed to stimulate specific frequencies f_i, at known amplitudes as per eq. (1.6) on page 16. After the measurements, the system also provides an impedance estimation based on respective DFTs of the voltage responses, enabling the evaluation of the desired battery state parameters.

A high-accuracy reference resistor is carefully selected to match the order of magnitude of the battery DC resistance, typically a few mΩ, as well as to consider factors including tolerance, temperature coefficient, and power rating to provide an accurate assessment of the actual excitation signal applied to the battery. The battery complex impedance is defined in the frequency domain as the following

$$Z_{BAT}(f) = \frac{V_{BAT}(f)}{I(f)} \tag{2.1}$$

where $V_{BAT}(f)$ is the battery voltage response, and $I(f)$ is the current excitation evaluated from the voltage drop across the reference resistor R. With

reference to the Ohm's law, the evaluation of the battery complex impedance may be shown solely based on the obtained voltage measurements as:

$$Z_{BAT}(f) = \frac{V_{BAT}(f)}{V_R(f)} R \tag{2.2}$$

The voltage time-signals $v_{BAT}(t)$ and $v_R(t)$ are acquired and then digitized using an ADC within a measurement time of approximately 1 s, resulting in output digital sequences $V_{BAT}[k]$ and $V_R[k]$, respectively. The fast Fourier transform (FFT) technique is then used to analyze the digital streams and evaluate the corresponding DFT. A peak search technique is used to improve the numerical resolution and find the peaks corresponding to the excitation frequencies f_i. The $V_R[k]$ stream is the preferred input for the peak search algorithm because its waveform exhibits lower noise in comparison to $V_{BAT}[k]$, thereby enabling more precise identification of the frequency bins associated with the excitation frequencies f_i. Subsequently, the algorithm employs the previously selected frequency bin locations to extract the peak values of the battery voltage sequence at those specific frequency components. In addition, a rectangular window and a zero-padding factor of 7 (padding the signal length by $2^7 = 128$) are employed to minimize spectral leakage and improve the numerical resolution of the DFT by better overcoming the intrinsic low SNR of the obtained voltage signals. After the detection of the amplitude and phase values of the complex coefficients of the DFT sequences at the excitation frequencies f_i, the system can determine the impedance $\hat{Z}_{BAT}(f_i)$ using the preceding equation as

$$\hat{Z}_{BAT}(f_i) = \frac{\hat{V}_{BAT}(f_i)}{\hat{V}_R(f_i)} R \tag{2.3}$$

where $\hat{V}_{BAT}(f_i)$ and $\hat{V}_R(f_i)$ are the respective FFT coefficients of the battery voltage response and the reference resistor voltage response at the frequency f_i.

This frequency-domain analysis characterizes battery impedance over the desired frequency range, providing a spectrum that could be used in BMS to monitor battery state effectively.

Chapter 3

Implementation with Off-the-Shelf Components

This chapter presents an innovative system implementation composed of high-resolution commercial off-the-shelf components and optimized hardware configurations. The choice of off-the-shelf components offers several advantages, such as cost-effectiveness, proven reliability, widespread availability, and ease of integration, still ensuring a custom-design solution.

The proposed system aims to provide reliable impedance estimation through accurate current and voltage measurements for battery state estimation and diagnostic purposes, by carefully selecting components that satisfy the requirements and incorporating robust signal processing techniques. Moreover, the system's compact design and low power consumption make it suitable for portable, space-constrained, and battery-powered applications. The system implementation of the battery impedance analyzer is shown in fig. 3.1.

3.1 Selection of Key Components

3.1.1 Digital-to-Analog Converter

The *Texas Instruments* 16-bit $\Delta\Sigma$ *DAC161S997* digital-to-analog converter was selected to generate the analog excitation current signal due to its high resolution, low-noise performance, low-power consumption, and capability to meet the desired amplitude requirements [43]. Typical applications includes 2-wire and 4-wire transmitters operating with a $4 - 20$ mA current-loop, as

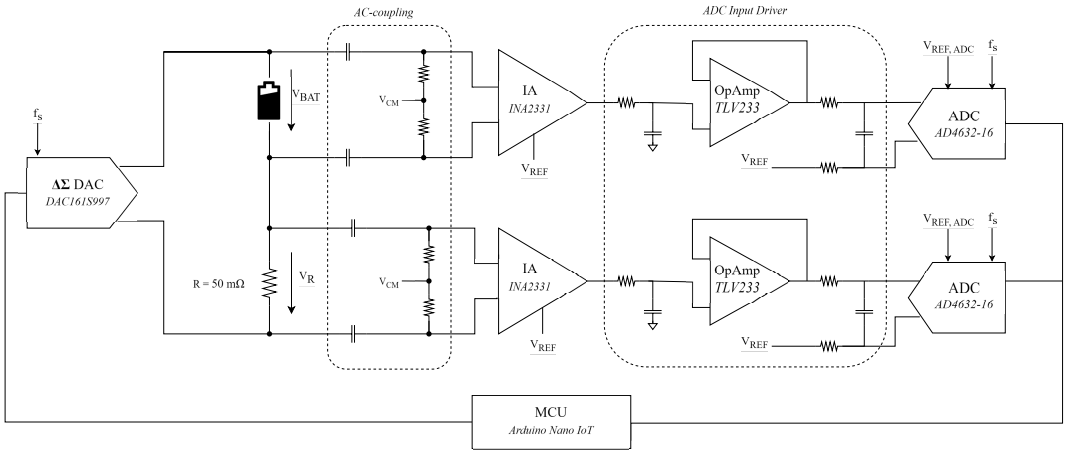


Figure 3.1: Block diagram highlighting the selected off-the-shelf component of the proposed impedance analyzer for online EIS monitoring of battery cells.

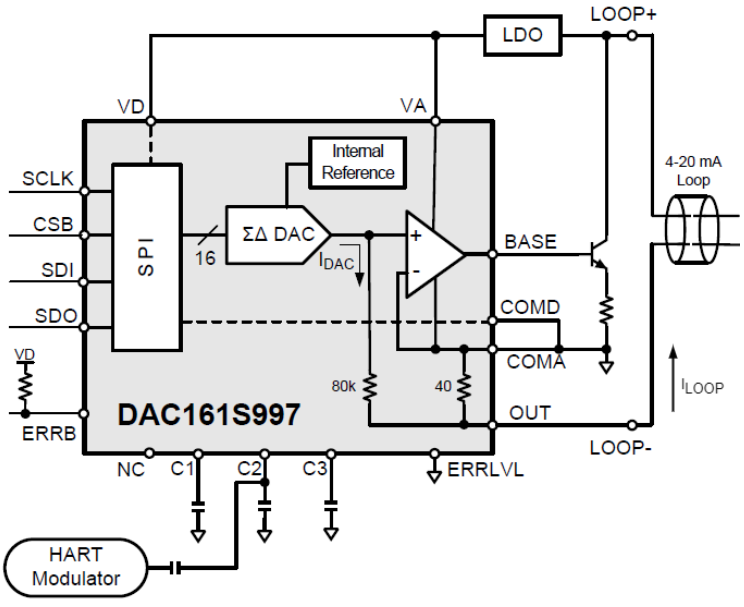


Figure 3.2: Block diagram representation of the digital-to-analog converter *DAC161S997* [43]

well as the regulation of process variables for industrial system control and actuator management.

The DAC incorporates a $\Delta\Sigma$ modulator, which produces an output current signal I_{DAC} as a pulse train. This pulse train is filtered using a third-order RC filter with external capacitors to ensure accurate filtering and to maintain stability margins. Initially, a standard capacitor value of 2.2 nF is chosen, subject to potential changes during testing.

The output current I_{LOOP}, shown in fig. 3.2 (i.e., the current that flows through the battery), is a function of the binary sequences received from the MCU by the DAC. Specifically, the 16-bit sequence *DACCODE* generates an output current according to the equation

$$I_{LOOP} = 24\,\text{mA}\frac{DACCODE}{2^{16}} \tag{3.1}$$

with values ranging from 0.19 to 23.95 mA and full accuracy guaranteed in the $4 - 20$ mA range, as shown in fig. 3.3.

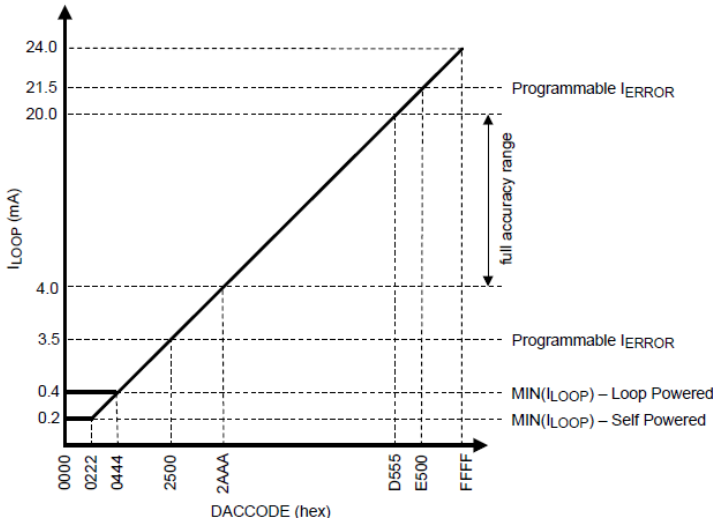


Figure 3.3: DC Transfer function of the digital-to-analog converter *DAC161S997* [43]

The corresponding current loop consists of the battery under test, considered as the local source of the loop, and the reference resistor R. For this prototype version, a self-powered transmitter configuration was adopted. In this configuration, the local supply powers only the loop and does not power

the DAC, which is supplied externally. In a future version, a loop-powered transmitter configuration, where the DAC is powered by the loop local supply (i.e., the battery under test), could potentially be implemented to reduce power consumption and component count.

Considering the expected measurement time t_{MEAS} of approximately 1 s and the DC amplitude of the excitation current signal I_{MEAN} of 12 mA, it's important to note that the battery discharge expected from a single measurement, denoted as ΔSOC, could be evaluated using eq. (1.1) on page 8:

$$\Delta SOC[\text{ppm}] = \frac{\Delta Q_{dis}}{Q_{full}} \times 10^6 = \frac{I_{MEAN} \cdot t_{MEAS}}{Q_{full}} \times 10^6 = 1.15\text{ppm} \tag{3.2}$$

Here, the full charge capacity of the battery Q_{full} is determined by the electrical characteristics of the selected battery employed for analysis in chapter 4.

The obtained value could be considered negligible in comparison to the conventional supply requirements of UAV operations, highlighting the efficiency of our design.

3.1.2 Instrumentation Amplifier

Since the voltage response produced by the excitation signal has a very small amplitude, an amplification stage is necessary for accurate measurement. An instrumentation amplifier is the best option since it integrates the passive components and amplifier stage into a single chip, making it highly suitable for precise and reliable measurements. Moreover, the dual-channel configuration facilitates the reduction of misalignment between the two measurement chains. The identification of the best option focused on the following key requirements [44]:

- Minimizing noise contribution, especially flicker noise rather than broadband noise, as it is more challenging to filter out in subsequent stages. A maximum flicker noise value of 50 nV/Hz at 1 kHz was considered.

- High input impedance reduces the input bias current, representing the current flowing through the amplifier input terminals. A lower input bias current is preferred since it generates an input voltage offset that could be difficult to calibrate with signal processing techniques since the current injection differs for the two input terminals. A physical resistor

with a significantly different resistance value compared to the amplifier input impedance could be connected to the inputs in order to reduce the voltage offset, as discussed in the section 3.2.1 on page 32.

- Ensuring a sufficient and high bandwidth is essential to guarantee the desired gain factor without filtering out the excitation signal frequency components.

- Optimizing the power consumption to achieve a trade-off between a high gain factor and low power dissipation is the last critical parameter for amplifier selection, in order to ensure the portability requirements for battery-powered applications. The quiescent current was used as a comparison variable to avoid considering different power supply requirements.

In order to address the outlined requirements, three options were considered, as described in table 3.1, based on their respective data-sheets [45, 46, 47].

Component	Voltage Noise $f = 1\,\text{kHz}$	Input Impedance and Input Bias Current [typ.]	Cut-Off Frequency with Gain of 1000	Max Gain	Quiescent Current (per channel) [typ.]
Texas Instruments INA2331	46 µV	10^4 GΩ, 0.5 pA	36 kHz	1000	415 µV
Texas Instruments INA2126	35 nV	1 GΩ, 10 nA	1 kHz	10 000	175 µV
Analog Devices AD8224	14 nV	10^4 GΩ, 25 pA	14 kHz	1000	750 µV

Table 3.1: Comparison of instrumentation amplifier options for EIS monitoring of battery cells.

Given that the ADC and the IA are expected to make the primary contributions to power consumption in the system, the third option, *AD8224*, was initially discarded due to its higher power consumption in comparison to the other alternatives. For the other two options, simulations using SPICE-based analog electronic circuit simulator software were conducted to evaluate the best trade-off. The first option, *INA2331*, exhibits a higher gain-bandwidth product and input impedance, while the *INA2126* exhibits better flicker noise performance and a considerably lower power consumption. Additionally, the second option offers the possibility of achieving higher gain values, which might be verified to produce a feasible cut-off frequency for our application, considering the desired excitation signal frequency range of $1 - 1000$ Hz. Given the cut-off frequencies with the same gain factor of 1000, the *INA2126* cut-off frequency is too close to the desired frequency range, and the simulation shows a 20% attenuation in the 1 kHz frequency component. It is essential to preserve the signal within our range in order to avoid losing information that cannot be recovered after signal processing. For this reason, the *Texas Instruments* dual-channel *INA2331* instrumentation amplifier was selected despite its higher power consumption to amplify the voltage responses from the battery cell and the reference resistor. Simulations and noise analysis are presented in the following chapter to verify that the corresponding noise contribution is lower than the desired minimum detectable signal.

3.1.3 Analog-to-Digital Converter

The choice of an external ADC is driven by the requirement for higher resolution, considering that integrated ADCs in MCUs typically have a maximum resolution of 12 bits, that is not sufficient to ensure accurate measurements where small voltage responses are sampled. Moreover, the ADC is one of the components with higher power consumption. For this reason, the search focused on selecting a component that features low-power operation. Since the excitation signal frequency range of $1 - 1000$ Hz does not require a high sampling rate, a SAR architecture could be selected as the chosen sampling rate is not high enough to significantly increase the chip power dissipation.

The *Analog Devices* dual-channel 16-bit *AD4632-16* SAR analog-to-digital converter was selected for digitizing the amplified voltage signals. Its 16-bit

resolution, with a nominal ENOB of 15.8 bits from the data-sheet specifications [48], provides the required precision to accurately sample the voltage waveform. Despite the employed sampling rate would not be excessively high, it is important to note that even small delays may significantly impact the DFT results, as the phase variations of the battery under test are typically less than one degree. Therefore, a dual-channel simultaneous sampling architecture should facilitate synchronization and minimizing potential timing errors.

The *Texas Instrument ADS8353* analog-to-digital converter was also considered for its dual-channel simultaneous sampling and 16-bit resolution. However, according to the power consumption evaluation in section 4.5 on page 51, its higher supply current of 10 mA, rather than 500 µA of the selected ADC, makes it too power hungry for the application requirements.

3.1.4 Microcontroller Unit

The *Arduino Nano IoT* with Bluetooth Low Energy (BLE) support was selected as the system processing unit. The combination of prototyping capabilities and compact size allows for straightforward implementation. It is employed to handle the storage and generation of the excitation signal, the acquisition of sampled voltage responses, signal processing and wireless communication tasks. In fact, the integrated BLE capability facilitates remote monitoring and configuration of the EIS monitoring system in real-world scenarios.

A reliable communication between the *Arduino* and the external components is essential for effective management and control of the overall measurement system. The selected DAC and ADC present serial peripheral interfaces (SPIs) for communication with *Arduino*, which has only one SPI port, making the programming more challenging. Therefore, a multi-slave SPI protocol has to be implemented, which allows the *Arduino* to manage data transfer between multiple devices simultaneously. When implementing the multi-slave SPI configuration, it is crucial to carefully select the SPI clock frequency based on the maximum operating frequencies of the connected devices and the measurement timing constraints. The selection has to ensure that an entire cycle of measurement is completed within the desired sampling period, i.e., the SPI packet is communicated to the DAC with the excitation signal information,

the analog signal flows through the analog devices, and the two SPI packets (one for each sampling channel) are communicated from the ADC. This process guarantees smoother measurement, avoiding any loss of information and ensuring reliable data transfer.

3.2 Auxiliary Circuits Design

This section focuses on the design of auxiliary circuits that complement the main system and enable its proper functioning.

3.2.1 AC-Coupling Circuit

The function of the AC-coupling circuit is to isolate the DC component of the voltage signals, including the battery OCV and any potential DC component generated by the DC level of the excitation signal, which is within the range of $4 - 20$ mA.

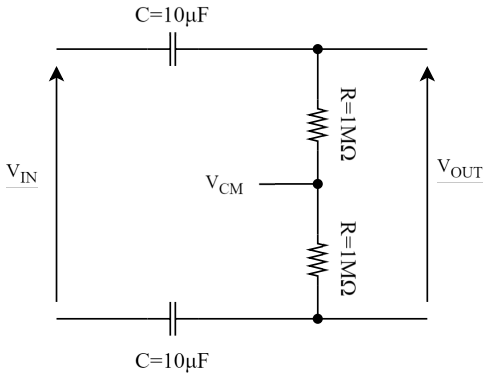


Figure 3.4: AC-coupling circuit schematic with selected component values according to our application.

As shown in fig. 3.4, the AC-coupling circuit is composed of two 10-µF capacitors and two 1-MΩ resistors, resulting in a high-pass filter with a cut-off frequency of 16 mHz. The capacitors are strategically used to block the DC signal and allow only the AC signal to pass through, in order to avoid affecting the operating point of the subsequent amplification stage. The resistors are chosen to ensure proper conditioning of the IA stage, thereby facilitating the selection of an appropriate input common-mode voltage [44]. According to the choice of the IA, characterized by a high input impedance value of 10^4 GΩ, the

resistance value is significantly lower than that to prevent an excessively high input voltage offset [49]. The capacitance value is carefully selected according to the cut-off frequency in eq. (3.3) in order to ensure the minimal attenuation of the lowest frequency component of the excitation signal used for EIS measurements.

$$f = \frac{1}{2\pi RC} \tag{3.3}$$

Consequently, the cut-off frequency is configured to be approximately 100 times smaller than 1 Hz, i.e., around $f = 10mHz$.

This approach ensures preserving the information contained in the differential voltage responses, enabling more accurate impedance estimation without the need for calibration.

3.2.2 Input Driver for Analog-to-Digital Converter

The input driver circuit for a high-precision ADC mainly consists of three parts: a low-pass RC filter, *Texas Instruments TLV2333* operational amplifiers [50], and an additional anti-aliasing filter, as described in section 2.1. Key parameters for the circuit design are the desired frequency range of interest of $1 - 1000$ Hz and the specifications of the selected ADC, i.e., resolution, sampling and hold capacitance of the input stage, the full-scale range of signal values that the ADC can handle, and the acquisition time. The data was obtained from the ADC data-sheet [48] and used in the *Texas Instruments* software tool *Analog Engineer's Calculator* in order to design the input driver correctly [51], as illustrated in fig. 3.5. The formula employed to evaluate the acquisition time is

$$t_{ACQ} = t_{CYC} - t_{CONV} = \frac{1}{f_s} - t_{CONV} \tag{3.4}$$

where t_{ACQ} is the acquisition time, t_{CYC} is the time period between subsequent conversions, t_{CONV} is the conversion time, and f_s is the sampling frequency. Considering the employed sampling frequency of 10 kHz and the conversion time given from the ADC data-sheet, it results

$$t_{ACQ} = \frac{1}{10\text{kHz}} - 300\text{ns} = 99.7\mu\text{s} \tag{3.5}$$

The first filter is used to reduce the broadband noise introduced by the IA at high frequencies. The resulting cut-off frequency of 10.6 kHz is one order of

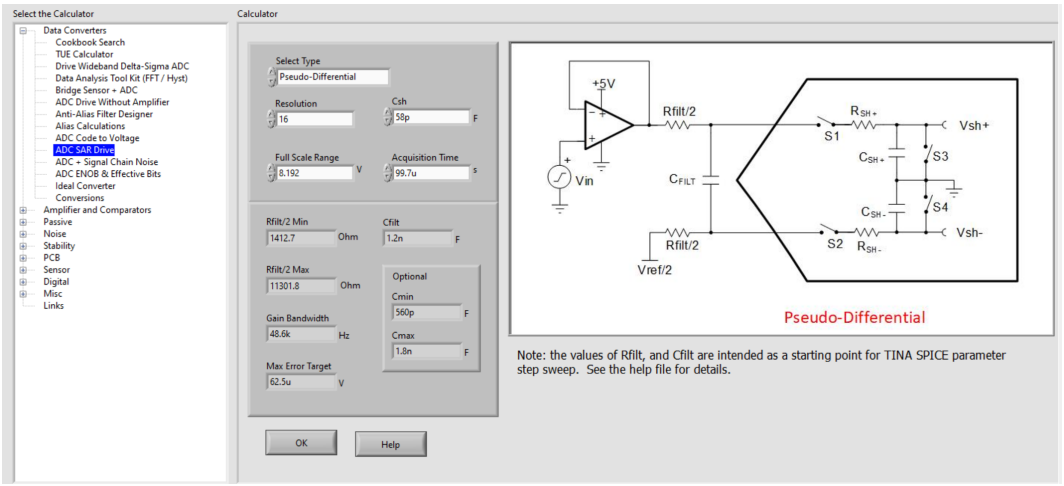


Figure 3.5: Analog Engineer's Calculator for ADC SAR driver according to our application.

magnitude higher than the excitation signal maximum frequency component of 1 kHz.

The operational amplifier has a unity gain configuration to allow proper signal conditioning of the input voltage. The component selection relied on considerations of the output impedance - a low value provides a buffer between the amplified signal and the switched capacitor input of the ADC - and the gain-bandwidth requirements depicted in fig. 3.5 that cannot be addressed by the IA, as the maximum gain of 1000 results in a bandwidth of 36 kHz. Subsequently, the option with lower power consumption and cost was selected.

The anti-aliasing filter consists of two 10-kΩ resistors and a 1.2-nF capacitor, which are used to adapt the signal to the pseudo-differential input of the ADC. The values are selected considering the range of resistance and capacitance the software tool gives. A parametric simulation was conducted in *LTSpice* utilizing the SPICE model of the selected components to identify the optimal resistance value within the permitted range that yields the minimal error at the end of the acquisition cycle, with a maximum requirement shown in fig. 3.5. This filter reduces out-of-band noise, as well as further assists in reducing sampling charge injection noise from the ADC input stage, which might significantly reduce the SNR.

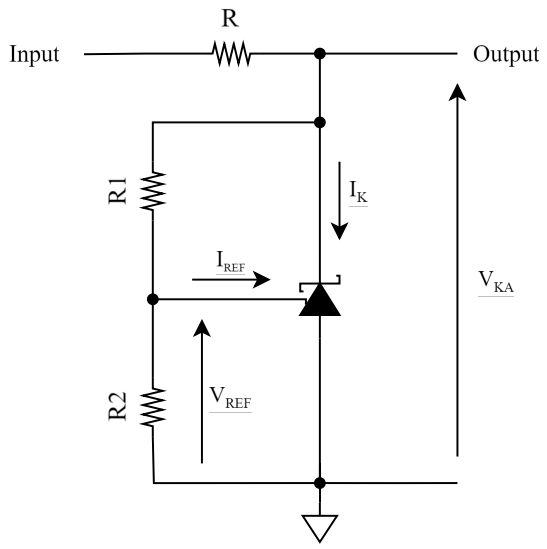


Figure 3.6: Reference voltage schematic

3.2.3 Reference Voltage

The system requires the presence of specific voltage reference to work properly, namely V_{REF}, V_{CM}, and $V_{REF,ADC}$, as depicted in fig. 3.1 on page 26. The IA output signal's reference voltage, or V_{REF}, ensures IA works within the allowed output range. It is further utilized for the pseudo-differential ADC input as the second input in the anti-aliasing filter in order to reduce potential common-mode errors in the voltage generation. The IA's input common-mode voltage, or V_{CM}, is set to address the signal constraints at the IA input. The ADC's reference voltage, or $V_{REF,ADC}$, is designed to exhibit higher stability to enable precise sampling and quantization.

In order to reduce the number of components on the overall board, the *Texas Instruments TLV431* was selected to set both V_{REF} and V_{CM} to half of the supply voltage range of IA. While the input common-mode range is not a significant constraint - since the differential input voltage should be within a few hundred of µV around zero - a reference voltage approximately equal to half of the supply voltage may be more suitable for this requirement to utilize the entire output range. The *TLV431* shunt regulator was selected for its feature to generate an adjustable voltage reference using two external resistors, thereby allowing for board redesign of the resistance values during the prototyping phase, if required. The design procedure for the evaluation

of the resistance values is detailed in eq. (3.6) according to the data-sheet specifications [52]:

$$V_{REF} = V_{NOM} + (I_K - I_{NOM}) \cdot |Z_{KA}| + (V_{KA} - V_{NOM}) \cdot (-2mV/V)$$

$$\begin{aligned} R_1 &= (V_{KA} - V_{REF})/I_{R1} \\ R_2 &= V_{REF}/(I_{R1} - I_{REF}) \end{aligned} \tag{3.6}$$

where V_{NOM} is the nominal reference voltage, I_K is the cathode current for regulation, I_{NOM} is the nominal cathode current, Z_{KA} is the impedance of the circuit, and V_{KA} is the desired reference voltage. The circuit is designed to obtain a reference voltage of 1.65 V:

$$V_{REF} = 1.24\,\mathrm{V} + (100\,\mu\mathrm{A} - 10\,\mathrm{mA}) \cdot 0.25\,\Omega + (1.65\,\mathrm{V} - 1.24\,\mathrm{V}) \cdot (-2\,\frac{\mathrm{mV}}{\mathrm{V}}) = 417.5\,\mathrm{mV}$$

$$R_1 = (1.65\,\mathrm{V} - 417.5\,\mathrm{mV})/50\,\mu\mathrm{A} = 24.65\,\mathrm{k}\Omega \tag{3.7}$$

$$R_2 = 417.5\,\mathrm{mV}/(50\,\mu\mathrm{A} - 1.5\,\mu\mathrm{A}) = 8.6\,\mathrm{k}\Omega$$

The ADC requires a specific and highly stable voltage reference to achieve accurate digitization. Therefore, the *Texas Instruments REF35* high-precision series reference device was selected [53]. It is characterized by a low temperature coefficient of 12 ppm/°C, which can help improve system stability and reliability. This characteristic allows the system to have a voltage variation of only 1.2 mV in the temperature range of $0 - 100$ °C, a value that is negligible compared to the selected voltage reference of 4.096 V, being less than 0.3% of the total.

Highly stable voltage references are essential, as any deviations in the voltage signal can severely impact the accuracy of the analog-to-digital conversion process, potentially compromising the integrity of the digital streams and the overall EIS measurements.

3.3 Printed Circuit Board Implementation

Bringing together the previously discussed components and design considerations, the system is physically implemented through a 4-layer PCB. The board is specifically designed to monitor a cylindrical LIB with a DC resistance value in the order of tens of mΩ. To ensure accurate current measurement, a 50-mΩ

high-precision resistor with 0.5% tolerance is employed as the reference resistor R. The schematic and layout files of the designed board are reported in the appendix.

The board, which is powered by external batteries, comprises additional components for effective design implementation, power management, and signal conditioning, thereby guaranteeing accurate signal measurement. These devices include level shifters, which ensure compatibility between different digital levels in the system; voltage regulators, which maintain stable voltage supplies; decoupling capacitors, which filter out high-frequency noise from voltage supply and reference pins; and circuits to facilitate testing and validation, which are crucial for evaluating the board functionality and performance.

The PCB layout is designed to minimize signal interference and parasitic effects, as well as to ensure optimal power distribution. These factors are essential in achieving high-precision system, considering the various power supplies included (1.8 V, 3.3 V, and 5 V). The internal layers are used for power supply planes, the top layer for component placement, and the bottom layer for signal routing. On the top layer, the analog and digital components are strategically placed in separate sections, with the mixed-signal components (DAC, ADC, and *Arduino*) residing over both sections, with plane separation running under them. This design separates the analog current return path from the digital one, reducing the risk of digital noise coupling into the sensitive analog signals. Given the inherently low SNR of the analog signals, this approach prevents signal degradation and measurement inaccuracies. Moreover, the careful routing of crucial traces such as voltage references, the strategic positioning of decoupling capacitors in close proximity to the device power pins, and the utilization of Arduino's 3.3 V and 5 V pins for supply further contribute to reducing power supply noise and ripple, result in clean, well-regulated, and well-distributed power signals.

The PCB board has the dimensions of 71 mm x 74 mm, including external supply batteries and *Arduino* board. This compact and space-efficient solution allows the placement in portable systems, guaranteeing the deployment in space-constrained applications, such as UAVs.

Chapter 4

Simulation and Performance Analysis

This chapter presents a comprehensive analysis of the proposed system performance for online and *in-situ* EIS monitoring of battery cells, based on simulations conducted using the SPICE-based analog circuit simulator *TINA-TI*. The simulation approach comprises three phases: a system-level simulation, a noise analysis, and a power consumption assessment.

The system-level simulation is designed to assess the signal behavior and integrity within the system under normal working conditions to verify the system proper functioning. The noise analysis examines the system capability to detect minimal variations in the battery impedance, taking into account the noise contributions introduced by the selected components. The power consumption assessment confirms the negligible power impact of the proposed system on the UAV power budget, thereby enabling extended flight times.

4.1 *TINA-TI*

TINA-TI is a SPICE-based analog simulation software developed by *Texas Instruments* that provides standard DC, transient, and frequency domain analyses to simulate electronic circuits and systems using SPICE models.

This software was selected for the project due to its compatibility with the majority of the components used in the system design manufactured by *Texas Instruments*. However, it's important to note that the ADC model could not

be incorporated because it was developed by another manufacturer and could not be transferred to the TINA-TI environment.

The basic and free version employed allows for comprehensive system simulation, including transient and noise analyses. There are some limitations to consider:

- Lack of advanced analyses: The simulator does not provide sophisticated tools such as noise transient analysis, which would have been optimal for a more detailed evaluation of components noise contributions;
- Simulation speed: The complex DAC model significantly slows down the entire simulation process, leading to longer computation times;
- Limited DAC model information: There is a lack of detailed information about the DAC model, which has led to some challenges in simulating the circuit.

A specific issue was related to the simulation of the DAC's third-order RC filter following the $\Delta\Sigma$ modulator. When using standard external capacitors connected to the pins as specified in the typical application section of the data-sheet, the simulation did not yield the expected results. Indeed, the DAC model appears to exhibit the correct output current signal behavior, as per specifications, only when the capacitors are absent. This behavior is unexpected, as the filter - which includes the external capacitors - is necessary for the current pulse train from the modulator output to produce the correct final output current waveform based on the input bit sequence. To verify the actual behavior of the DAC with capacitors, laboratory tests will be conducted on the physical board.

These limitations emphasize the importance of validating simulation results through practical experimentation to resolve the observed issues.

4.2 Battery Model

The initial step involves selecting an appropriate ECM to represent the LIB's electrical behavior during simulation. ECMs are commonly used to simulate the linear dynamic characteristics of batteries, represented by a circuit including voltage sources, resistors, capacitors, and other passive elements. The

employed ECM, shown in fig. 4.1, is an integer-order model. The parameters were determined through experimental EIS measurements made with the *Hioki IM3590* Chemical Impedance Analyzer on a fully-charged LIB at 25 °C. The selected battery is a *Sony Murata US18650VTC6* cylindrical LIB cell with a nominal capacity of 3120 mA h and a nominal voltage of 3.6 V.

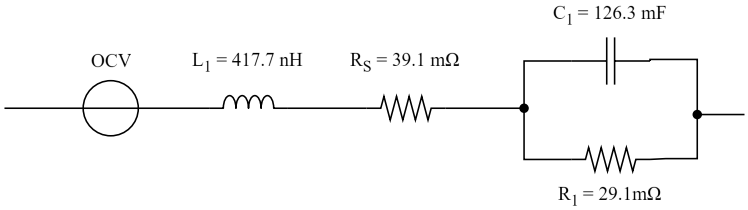


Figure 4.1: Equivalent circuit model of the fully-charged battery cell *Sony Murata US18650VTC6*.

The selected first-order ECM includes an ideal voltage source - which represents the OCV - in series with the internal resistance R_s, the inductance L_1, and a parallel combination of the resistance R_1 and capacitor C_1. The RC network has been incorporated to characterize the transient response during charge-discharge cycles, which the simple series model did not consider.

However, this model exhibits potential inaccuracies in representing the battery impedance shown in fig. 4.2:

- Absence of CPEs: The parallel RC creates a perfect semicircle in the middle-frequency range of the Cole-Cole plot. However, the actual battery response produces a depressed arc, that can be more accurately modeled using CPEs instead of capacitors;
- Absence of Warburg impedance: The Warburg impedance in series models the low-frequency tail with a 45° slope that represents charge diffusion, not included in the selected ECM.

Despite these limitations, this ECM was selected due to its straightforward implementation using solely ideal passive components, thereby simplifying the simulation process. The project aims to test and validate the overall system behavior according to the intended applications rather than precisely characterize the battery in the simulation, so these additional elements in the ECM are not necessary at this stage.

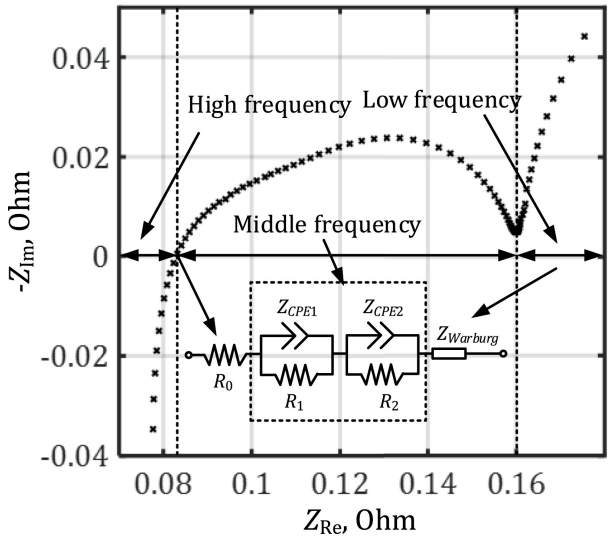


Figure 4.2: Cole-Cole plot of an ECM including CPEs and Warburg impedance [15].

4.3 System-Level Simulation

The system-level analysis aims to assess the overall functionality of the proposed monitoring system. The simulation schematic is composed of the key component SPICE models and auxiliary circuits described in chapter 3 on page 25, with some exceptions. Since this is an analog circuit simulation, the MCU cannot be directly included. The DAC model does not feature SPI ports, but it has 16 digital parallel inputs instead, that are controlled by a multi-bit sequence modeled as piecewise linear functions. Furthermore, the ADC is simulated using an equivalent circuit that models its sample-and-hold input stage, as depicted in fig. 4.3. This model represents a generic terminal (negative or positive) of any channel, according to the ADC specifications [48]. It allows for the simulation of non-idealities in the sampling process, such as settling errors, but does not account for quantization, that will be studied separately in section 4.4 on page 49 using the ENOB and SNR values presented in the data-sheet.

The designed input excitation current at the DAC output is composed of 20 frequency components in the set [1.2, 3.7, 4.9, 6.1, 8.6, 11.0, 14.7, 18.4, 33.1, 49.1, 73.6, 99.4, 132.5, 165.7, 198.8, 231.9, 298.2, 429.5, 528.9, 627.1] Hz. The *MAT-*

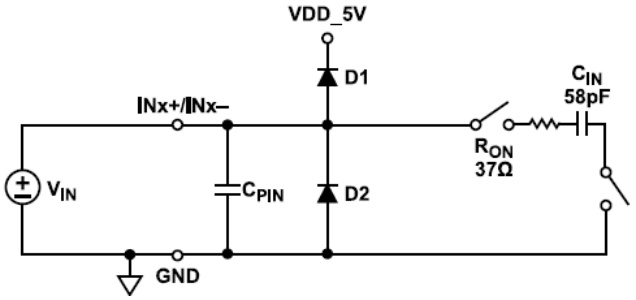


Figure 4.3: Equivalent Circuit for the *AD4632-16* Differential Analog Input [48] for each terminal (negative or positive) of each channel (1 or 2).

LAB function `idinput` was used to generate a set of frequency components according to the desired data rate of 10 kSpS and frequency range of $1 - 1000$ Hz to investigate the middle-frequency region of the Cole-Cole plot. From the generated set, components are chosen to focus on the low-frequency end of the range, which are relevant to the impedance estimation, as described in chapter 1 on page 7. Each component is characterized by random phase and constant amplitude. According to specifications [43], the DAC is designed to induce in the battery an approximate 8-mA total current amplitude with a 12-mA DC offset to cover the entire full accuracy output current range of $4 - 20$ mA. The frequency spectrum of the current excitation signal is reported in fig. 4.4.

The observed output voltage responses at the end of the measurement chain represent the voltage sampled on the ADC switching capacitors, which must be transformed into the frequency domain through DFT via software on *MATLAB*. A coherent sampling approach is employed to avoid introducing additional non-linearities in the DFT process and to ensure that the peaks generated by the frequency components align precisely with the bins of the DFT. This approach uses the same clock signal at 10 kHz for generating the data rate of the multi-bit sequence given as input to the DAC and the sampling frequency used by the ADC.

The simulation analysis the entire system over a complete measurement time of 819 ms. It provides the voltage responses of the battery and the reference resistor at critical stages of the system. These stages include the outputs of the AC-coupling circuits - which show the differential voltage across the

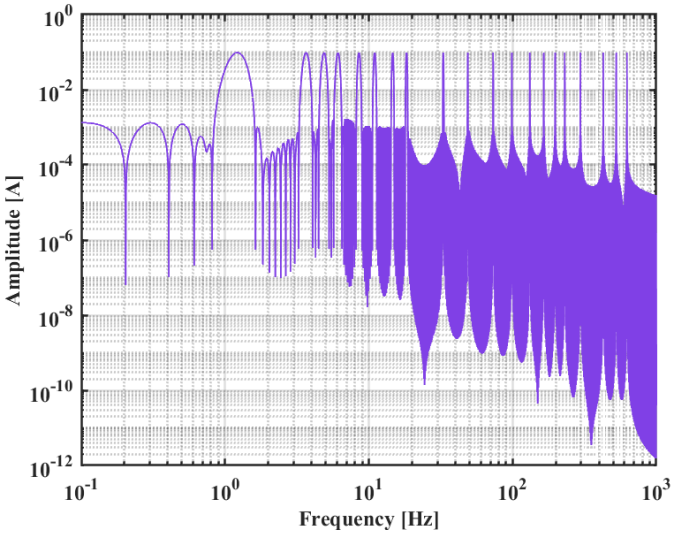
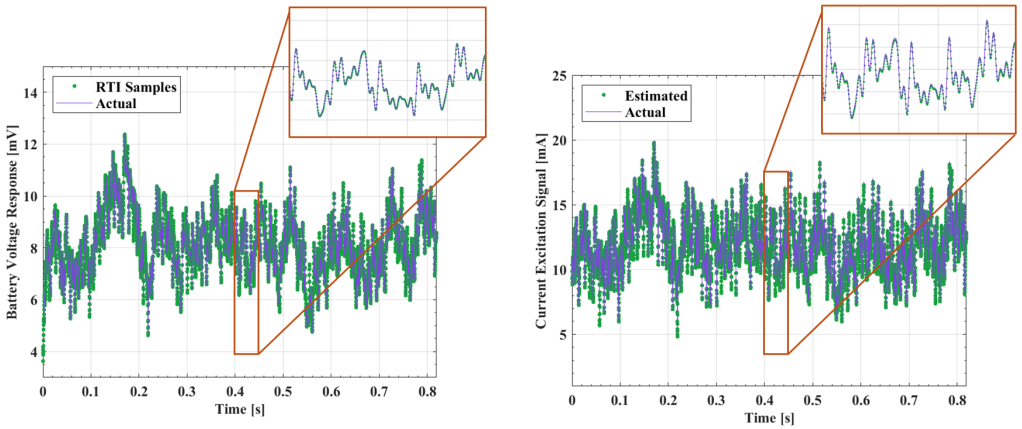


Figure 4.4: Amplitude spectrum of the designed multisine current excitation signal.

components; the output of the instrumentation amplifier - which shows the amplified waveform with a gain factor of 1000; and the output of the ADC input model. The results are firstly presented in the time domain, including the measurement of the battery voltage response (excluding the open-circuit voltage) and the assessment of the current excitation signal, as shown in fig. 4.5. The current signal is evaluated from the reference resistor voltage samples and the selected reference resistor.

Specifically, the results compare the referred-to-input (RTI) battery voltage response sampled at the end of the measurement system and the voltage drop across the battery measured at the output of the AC-coupling circuit. Furthermore, the RTI current estimation is compared with the actual current flowing through the battery under examination captured by the simulation. The comparison shows good agreement, validating the performance of the impedance analyzer. It is important to note that this simulation considers solely possible functional errors and non-linearities, modelled in the SPICE model, such as gain or offset errors. It does not include noise sources, which are considered separately later.

Furthermore, a comparison in the frequency domain is presented using Cole-Cole plot, which illustrates the battery impedance estimation, the ECM



(a) (b)

Figure 4.5: Comparison of the battery voltage response and excitation current. (a) Predicted battery voltage response (excluding OCV) versus voltage samples back-referred to the battery cell level. (b) Estimated current excitation signal flowing into the battery cell versus observed current signal at the battery cell level.

impedance, and the reference impedance measured with the *Hioki IM3590* Chemical Impedance Analyzer, as shown in fig. 4.6. Deviations of the impedance estimation points from expected results may arise due to non-ideal characteristics exhibited by the simulated component models, such as the IA and operational amplifier, as well as errors introduced by the DFT analysis. However, the figure shows good agreement between the simulation points and the ECM, with a deviation of around $2.2\,\mathrm{m}\Omega_{\mathrm{RMS}}$. The estimated samples are also compared with reference impedance measurements performed on the real battery. Deviations in this case may mainly be due to the non-ideal and simplified battery model employed in the simulation.

4.3.1 Quantifying the Impact of Sampling Delay

In fig. 4.7, the battery impedance magnitude and phase are shown. As expected, a very small phase can be observed. To numerically demonstrate the necessity of simultaneous sampling, it is necessary to evaluate the maximum allowable sampling delay to obtain a certain minimum detectable phase. Specifically, the target is taken as the minimum phase variation between two

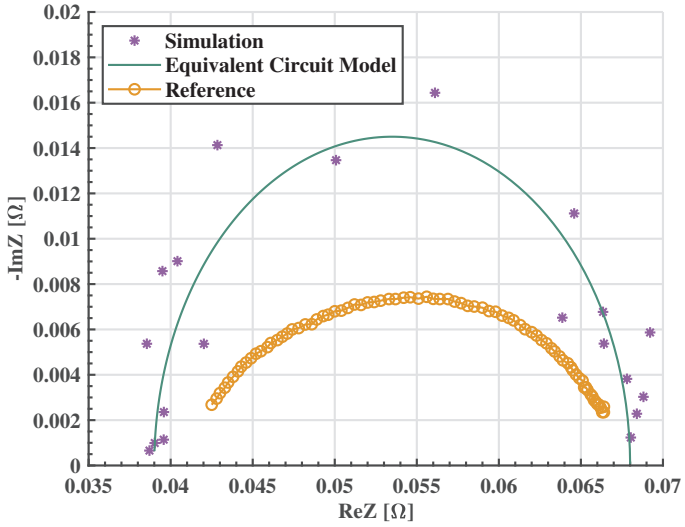
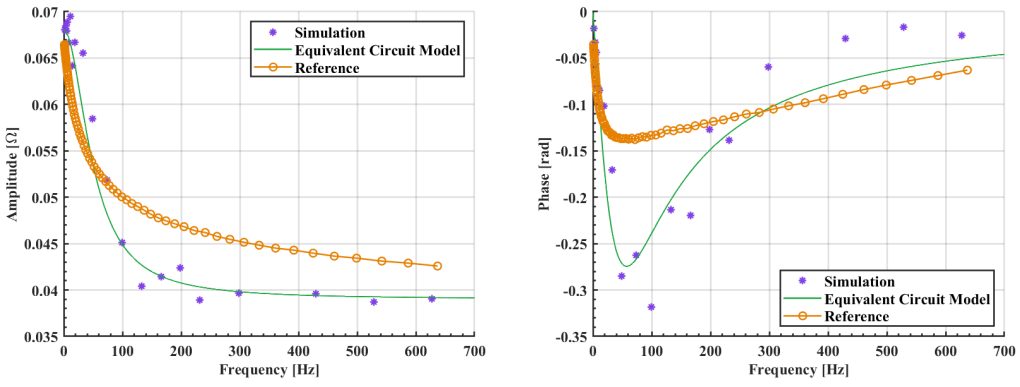


Figure 4.6: Cole-Cole plot comparison between proposed system simulation, ECM response, and the reference measurement.



(a) (b)

Figure 4.7: Amplitude (a) and phase (b) of the battery impedance evaluated from the simulation, ECM, and reference measurement.

points from the reference phase measurement done with *Hioki IM3590*, which is 2.1×10^{-5} rad.

According to the impedance estimation process described in eq. (2.2) on page 23, the impedance takes the following form:

$$Z_{BAT}(f) = \frac{V_{BAT}(f)}{V_R(f)} R \tag{4.1}$$

where $V_R(f)$ and $V_{BAT}(f)$ are the DFT of the reference resistor and battery voltages, respectively. The demonstration starts with specific hypotheses for simplicity:

- The reference resistor R is constant with frequency.
- The two signals are equal, as $v_{BAT}(t) = v_R(t) = x(t)$, and consequently they should have the same DFT.
- An ideal DFT is assumed, such that:

  $$DFT[x_k] = F_s[x_k] = X_s(f)$$

  where $X_s(f)$ is the discrete-time Fourier transform (DTFT) of the signal and x_k is the sequence obtained from sampling the signal $x(t)$, defined as $x_k = x(kT_s)$, with T_s representing the sampling period and k being the sequence coefficient.

Considering a non-simultaneous sampling at the instant kT_s, the battery voltage response will be sampled at the time kT_s, and the reference resistor response will be sampled at the time $kT_s + \Delta t$, where Δt is the delay between the sampling instances. The sampling process is illustrated for clarity in fig. 4.8. As per DTFT properties, the time variations could be represented in the frequency domain as

$$F_s[x(kT_s + \Delta t)] = X_s(f) \exp^{-j2\pi f \Delta t} \tag{4.2}$$

The additional term, introduced by the delay, is a crucial factor in battery impedance measurement. While it does not impact the magnitude estimation, it significantly affects the phase, leading to a phase delay of $-2\pi f \Delta t$ which depends on the frequency.

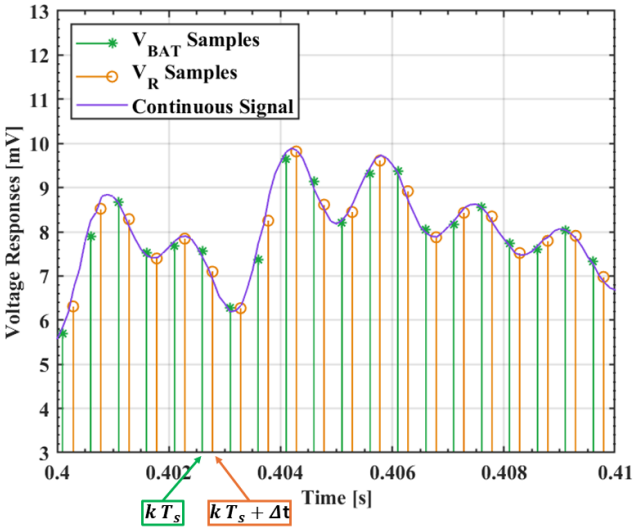


Figure 4.8: Example of a non-simultaneous sampling for battery and reference resistor voltage responses.

According to the obtained phase delay, the desired objective, and considering a margin of one order of magnitude, the formula used to evaluate the minimum allowed sampling delay time is as follows:

$$2\pi f \Delta t < \frac{1}{10} \Delta\phi^{max} \tag{4.3}$$

where $\Delta\phi^{max}$ is the target and the selection of the frequency f may involve the worst-case scenario as the maximum frequency in the desired application band, i.e., 1 kHz. The result is 334 ps. The allowed delay is very short, considering that ADCs not supporting simultaneous sampling use a multiplexer for the channel selection. The acquisition time requirements – i.e., the time required to guarantee proper settling of the analog input voltage – must be ensured for a correct conversion. With research on dual-channel models of multiplexed ADCs, acquisition times are typically in the order of hundreds of ns, higher than the requirements. This result underscores the importance of a simultaneous sampling ADC in our use case.

4.4 Noise Analysis

The noise analysis aims to assess the overall noise contribution introduced by the analog portion of the system, specifically within the frequency range of $1 - 1000$ Hz. Dedicated noise models are employed for amplifiers and resistors in order to consider thermal, shot, and flicker noise for the characterization, with primary focus directed towards the critical thermal noise contribution of the amplification stage. Furthermore, in order to account for the noise contribution from the ADC and DAC, the specifications provided in the data-sheets are utilized, as the components cannot be included in the simulation schematic.

The analysis examines whether the system can detect variations in battery impedance ΔZ_{BAT} as small as $1\,\mathrm{m\Omega}$, which is crucial for accurate impedance monitoring. The battery voltage variation $\Delta V_{BAT,RMS}$ corresponding to the single-tone excitation signal is evaluated based on the excitation current amplitude $I_{0,RMS}$ and the desired minimum detachable impedance, as

$$\Delta V_{BAT,RMS} = I_{0,RMS} \cdot \Delta Z_{BAT} \tag{4.4}$$

The excitation signal has 20 frequency components and a total amplitude of $8\,\mathrm{mA}$ uniformly distributed along the components, which results in a single-tone amplitude of $0.283\,\mathrm{mA_{RMS}}$. Consequently, the battery voltage variations results

$$\Delta V_{BAT}^{RMS} = 0.283\,\mathrm{mA_{RMS}} \cdot 1\,\mathrm{mA} = 0.283\,\mathrm{\mu A_{RMS}} \tag{4.5}$$

After establishing the target, the focus shifts to assessing the noise power contribution of the selected components, starting with the noise analysis in *TINA-TI* at the output of the operational amplifier (which would be the input of the ADC). The simulation provides the total RMS noise plot shown in fig. 4.9, representing the integrated output noise spectral density in the selected band, which is $2.84\,\mathrm{mV_{RMS}}$. The total RMS noise contribution of the ADC is $47.7\,\mathrm{\mu V_{RMS}}$ according to data-sheet, although its operating conditions differ from ours. However, the higher sampling frequency of $500\,\mathrm{kHz}$ used in the data-sheet should lead to higher noise contribution. Hence, this value can be considered for the analysis as it represents a worse-case scenario in comparison to what is expected. This value is negligible compared to the total noise of

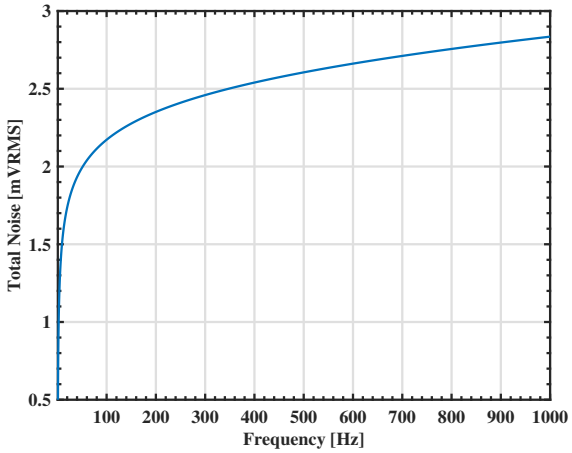


Figure 4.9: Total RMS noise of the analog subsection of the proposed system within the desired $1 - 1000$ Hz frequency band.

the analog acquisition chain, as it is two orders of magnitude smaller. For the DAC, the data-sheet provides an integrated output noise of $300\,\mathrm{nA_{RMS}}$ in the same band considered in the project. This value is also negligible in comparison to the value used in eq. (4.5), as it represents a reduction of three orders of magnitude from the considered single-tone amplitude. Hence, to evaluate noise contribution, solely the total noise of the analog acquisition chain, namely $2.84\,\mathrm{mV_{RMS}}$ or $2.84\,\mu\mathrm{V_{RMS}}$ RTI, is considered.

The simulation result exceeds the required target value in eq. (4.5). However, the DFT ensures a more precise comparison, thereby considering the noise contribution within the single frequency bin used by the FFT techniques rather than the entire band. Given the measurement time of 819 ms, which is the total duration of the excitation signal based on the number of data and the selected data rate, a frequency bin of 1.22 Hz is considered.

The following steps involve the evaluation of the noise power in the selected frequency band, i.e., $8.07\,\mathrm{pV^2_{RMS}}$, and then the determination of the contribution in the single the frequency bin, considering an uniform distribution, as

$$\frac{8.07\,\mathrm{pV^2_{RMS}}}{1000\,\mathrm{Hz}} \cdot 1.22\,\mathrm{Hz} = 9.84\,\mathrm{fV^2_{RMS}} \tag{4.6}$$

The resulting noise amplitude is $99.1\,\mathrm{nV_{RMS}}$. This value satisfies the minimum detectable signal requirements, guaranteeing the detection of a battery impedance as small as $1\,\mathrm{m\Omega}$.

4.5 Power Consumption Evaluation

The power consumption of the system is discussed in the UAV application, where the objective is to achieve a power consumption of the overall measurement system 1000 times lower than the typical application demand. Assuming that an 8-LIB pack supplies the drone, each with a 3 Ah capacity (assuming they are connected in parallel to add their capacities), and that the minimum operational time of the drones might be around 8 hours, the objective is :

$$I_{MAX} = 0.001 \cdot \frac{C_{TOT}}{t_{op}} = 0.001 \cdot \frac{8 \cdot 3Ah}{8h} = 3mA \tag{4.7}$$

where I_{MAX} is the maximum current allowed for the measurement system to consume, C_{TOT} is the total capacity of the 8-LIB pack, and t_{op} is the desired operating time. This requirement represents a worst-case scenario, considering the measurement system operating continuously during the 8-hour drone operation. Normally, measurements may be taken at regular intervals and potentially more frequently when the battery is almost discharged or under a specific SOC level. Therefore, the actual power consumption of the measurement system will be lower in real-world application.

For the evaluation of the power consumption of the board, all components incorporated in the board are considered, with the exception of the *Arduino*. The *Arduino* is excluded due to the prototyping nature of this first version of the board. In future versions, the aim is to substitute the *Arduino* with a low-power MCU with only the required features for the system. According to datasheets, the system's total current consumption is 2.47 mA (maximum value) and 1.95 mA (typical value). It is evident that the consumption addresses the target, satisfying the requirements for a low-power solution. The analysis shows that the IA and ADC are the primary sources of power dissipation. The reduction of the power consumption of the IA required a trade-off between noise and power specifications, as discussed in section 3.1.2 on page 28. Obtaining accurate impedance measurements is the primary objective in this project, considering the minimal amplitude of the voltage responses. Consequently, the selected IA has higher power supply specifications, although not excessively so, to prioritize minimization of the noise power contribution. The ADC power consumption may be reduced by employing a lower sampling rate, e.g., around

10 kHz, as in the simulation, since the power consumption of SAR architectures are influenced by the sampling frequency.

The battery discharge caused by the current excitation and its DC level of 12 mA should also be taken into account. According to eq. (3.2) on page 28, the expected battery discharge over the entire 8-hour measurement period is approximately 3 %.

In conclusion, the power consumption analysis demonstrates the suitability of the proposed EIS measurement system for low-power applications.

Conclusions

This thesis presented the implementation of a low-power, low-noise, and portable system for online and *in-situ* EIS monitoring of LIB cells, composed of off-the-shelf components.

The system employs a multisine excitation signal, which allows for simultaneous excitation of multiple frequencies in order to significantly reduce measurement time compared to traditional single-tone sweeps. This factor is crucial for online monitoring as it ensures the stability of the battery responses, which can be considered steady, avoiding dependence on external conditions during individual measurements. The careful design of the excitation signal is essential for the acquisition of impedance spectrum information to guarantee system linearity and time-invariance assumptions.

To demonstrate the applicability of the multisine excitation approach to online and *in-situ* EIS monitoring, an impedance analyzer architecture using commercially available components was proposed. The system employs a high-precision reference resistor for accurately estimating the battery impedance through simultaneous measurement of both the actual current excitation and the battery voltage response. This design choice enhances system accuracy, leading to improved measurement considering the low-value impedance in this type of application.

The system was validated through comprehensive CAD-based performance analysis in order to investigate power consumption, resolution, and general behavior. The results show good agreement with the behavior of the selected ECM, guaranteeing a minimum detectable impedance variation as small as $1\,\mathrm{m\Omega}$. The selection of a simultaneous sampling dual-channel ADC is based on the requirement for a minimum detectable phase variation of $2.1 \times 10^{-5}\,\mathrm{rad}$. This high accuracy is crucial for the detection of slight variations in battery

impedance related to changes in battery conditions. Furthermore, the system demonstrated significantly low power consumption, which adds only a negligible amount to the overall power budget of our battery-powered application.

The ability to perform fast and accurate EIS measurements in online and *in-situ* applications lead to significant advantages for battery management strategies. This capability facilitates more precise estimation of critical parameters such as SOC and SOH, leading to the development of machine learning-driven algorithms for adaptive charging and maintenance strategies.

Despite the promising results, several areas require further investigation considering the prototype nature of this first version. This work will be followed by a testing phase in real-world conditions to confirm simulation results and validate system performance, especially layout strategies employed to minimize interference from digital signals to sensitive analog signals.

Subsequent versions should focus on replacing the Arduino board with a specific-purpose, low-power MCU to reduce system size and enable integration into existing BMSs. Moreover, different choices of IA could be explored to improve the SNR, either through components with higher gain factors or lower noise contributions. This approach may be suitable for investigating the low-frequency region of impedance spectrum, considering the potential reduction of the allowable bandwidth from the current 1 kHz to a few hundred Hz.

Additionally, future studies should investigate the implementation of loop-powered solution where the battery under test also supply the monitoring system. This approach would remove the need for external power supply and lead to further integration in real-world application. This implementation should focus on reducing power consumption of the monitoring system to have a minimal impact on the application power budget, ensuring robustness and extended operating time.

In conclusion, this project provides a newer low-power solution for online EIS measurements to the field of battery monitoring. The proposed system capability to provide accurate impedance data opens new possibilities for advanced online monitoring strategies, considering that EIS technique is currently well-established primarily in laboratory application due to the requirement of specialized equipment.

Appendices

Schematics

This section presents circuit schematics, which are divided into multiple parts to enhance readability.

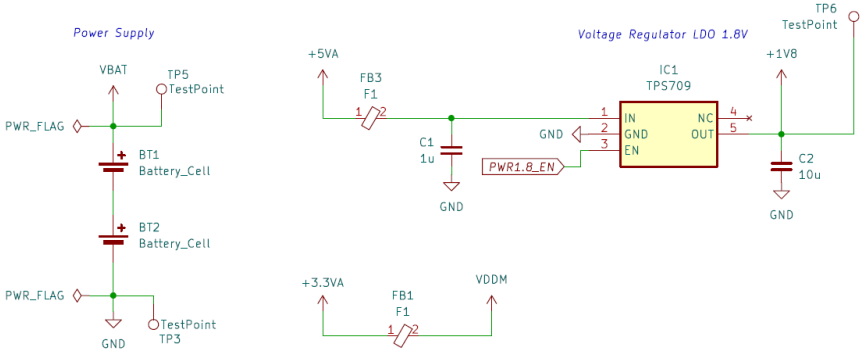


Figure 10: Power management unit: batteries, LDO, and ferrite isolator for analog/digital paths.

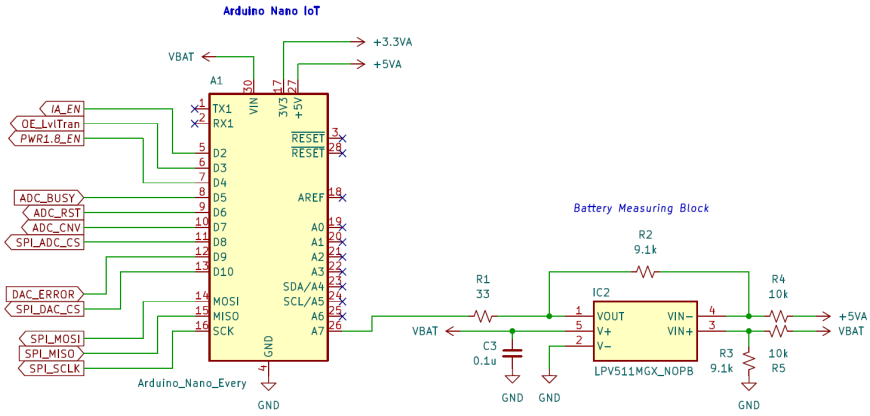


Figure 11: Arduino board and power supply measurement system.

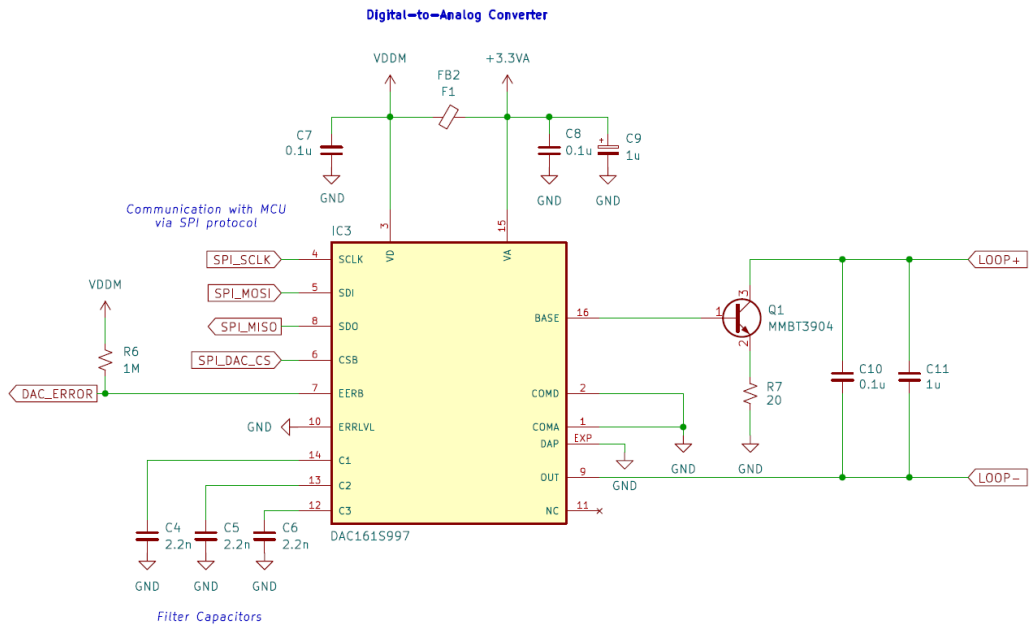


Figure 12: Digital-to-analog converter.

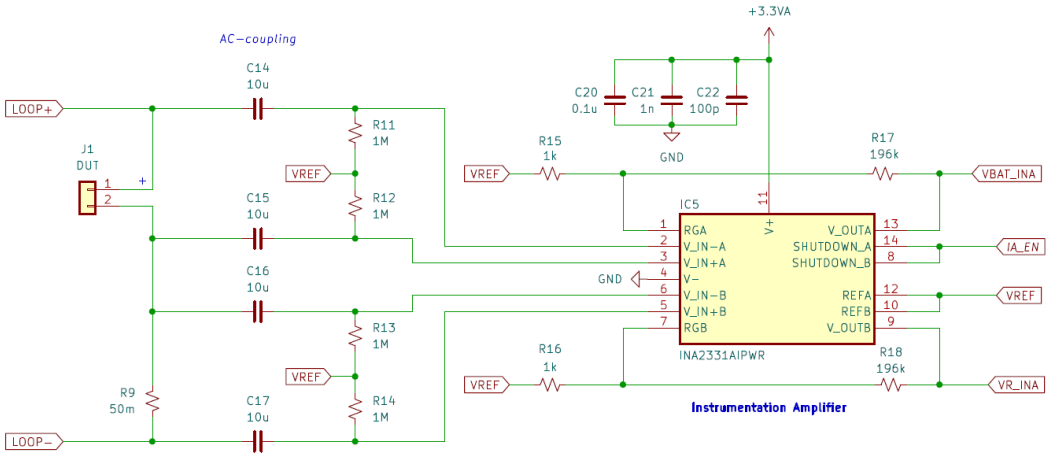


Figure 13: Device under test (DUT), AC-coupling circuits, and instrumentation amplifier (gain: 1000).

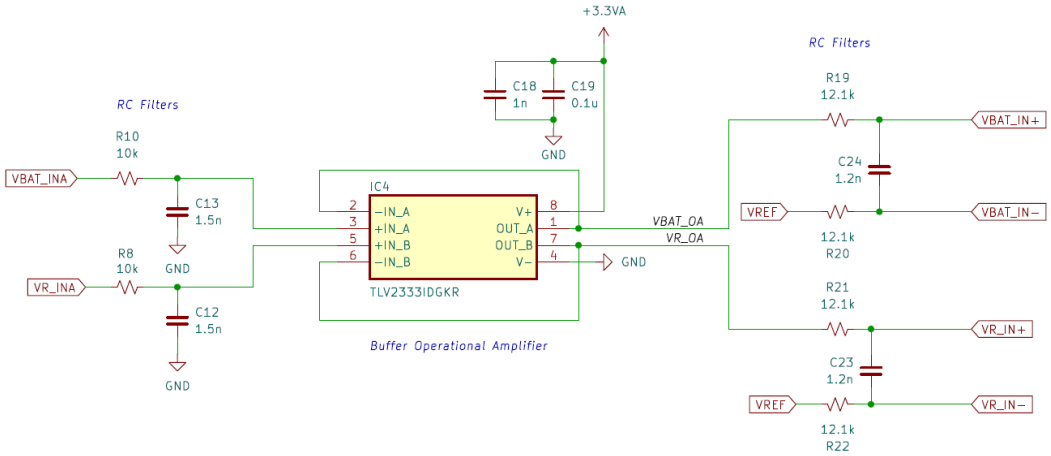


Figure 14: ADC input driver: LPFs, buffer op-amp, and anti-aliasing filters.

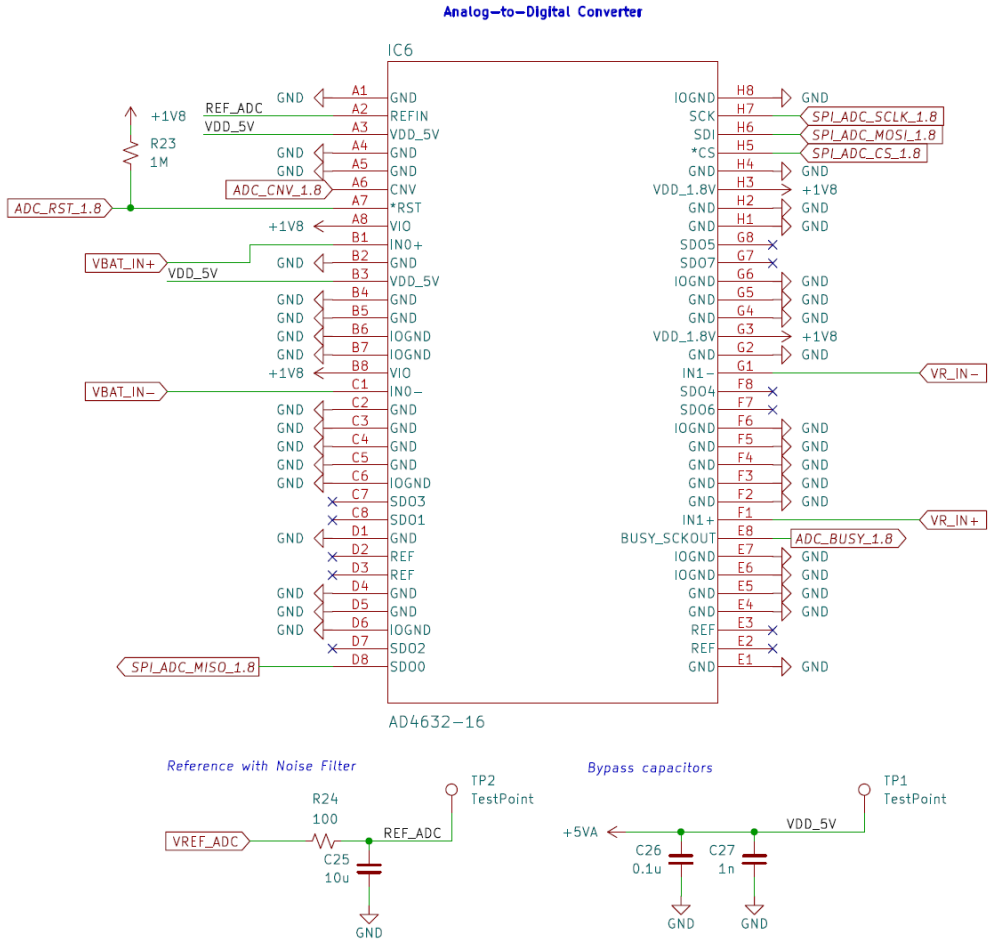


Figure 15: Analog-to-digital converter with reference voltage noise filter and power supply bypass capacitors.

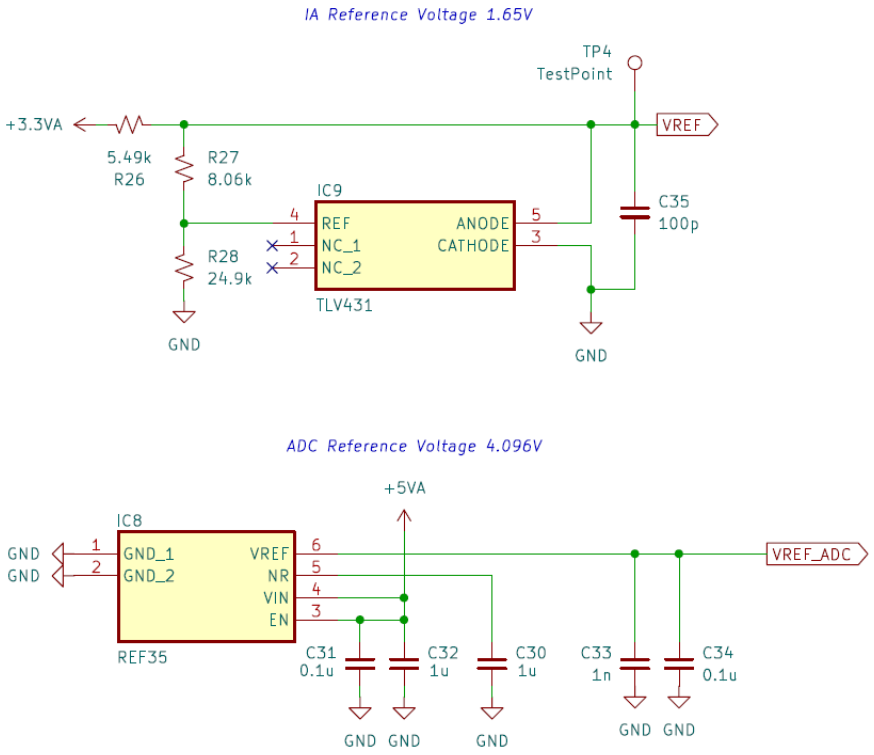


Figure 16: Voltage reference for IA and ADC.

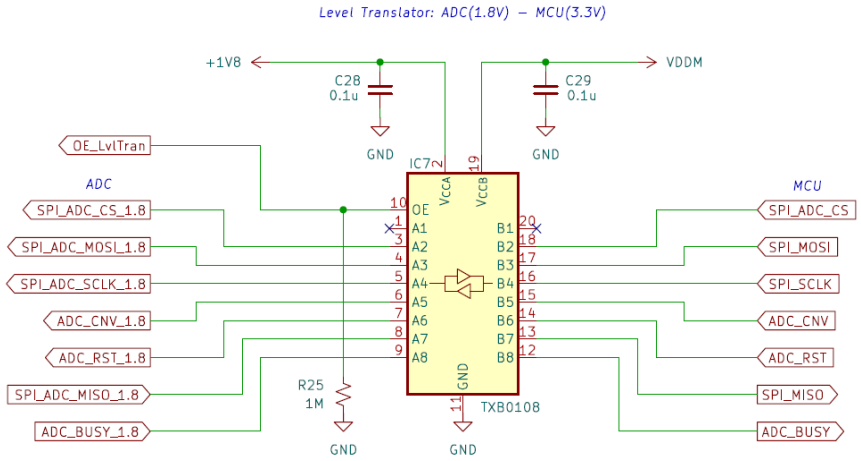


Figure 17: Level translator for 1.8 V ADC and 3.3 V MCU power supplies.

PCB Layout

This section presents the layout of the PCB designed for the system. The following figures illustrate each layer of the 4-layer PCB, highlighting key component blocks.

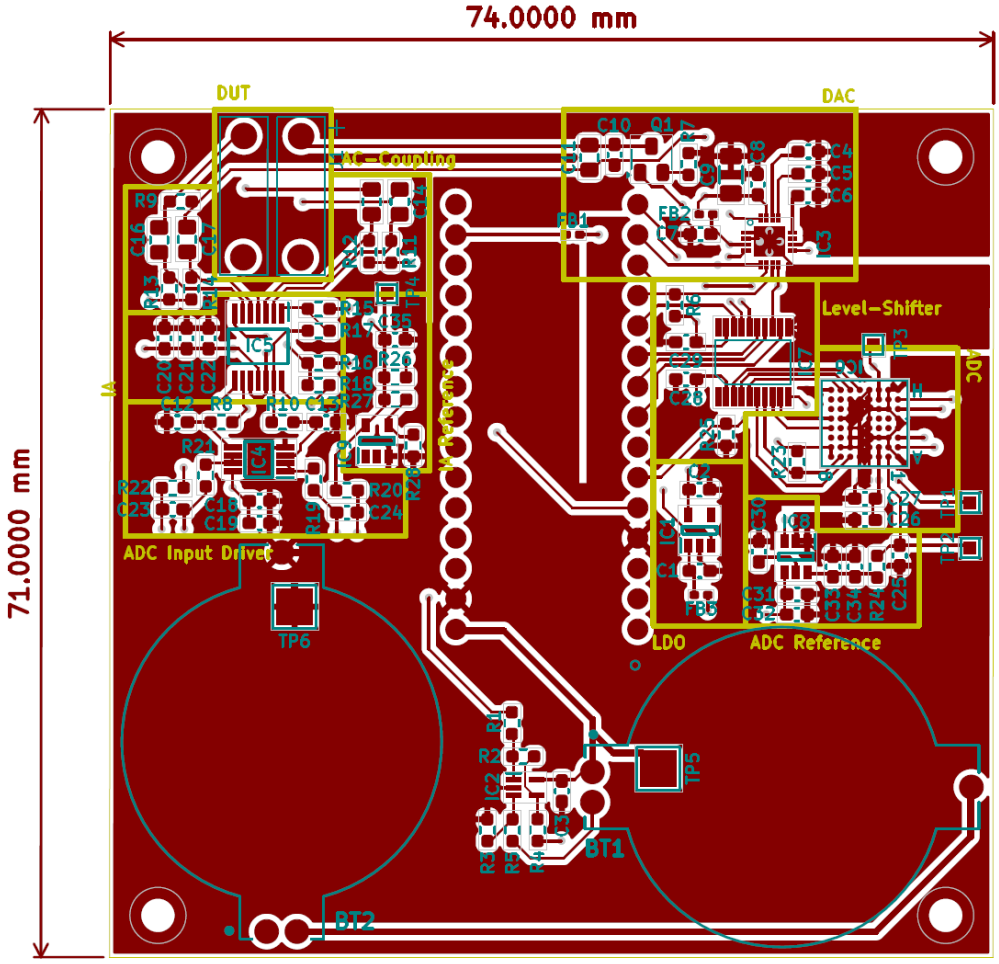


Figure 18: Overview highlighting individual system blocks.

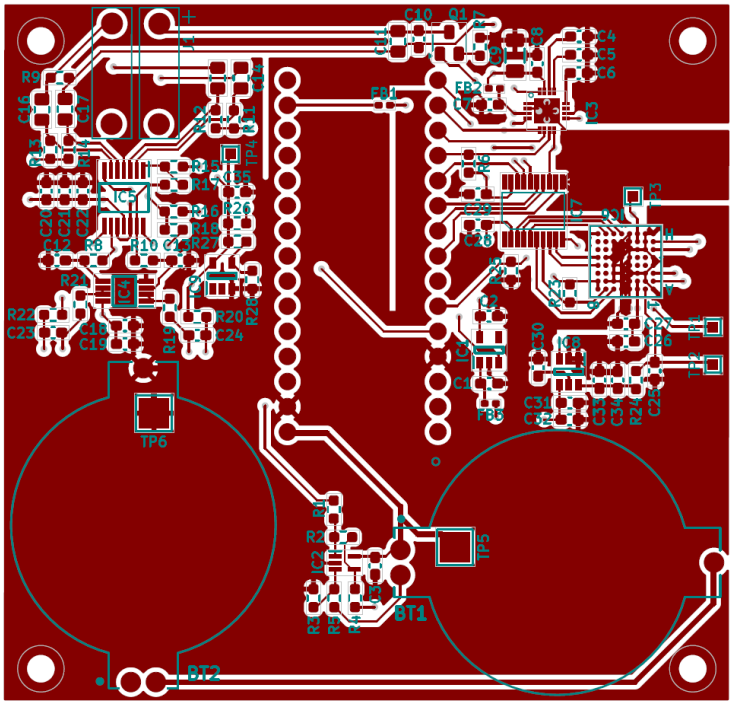


Figure 19: Top layer.

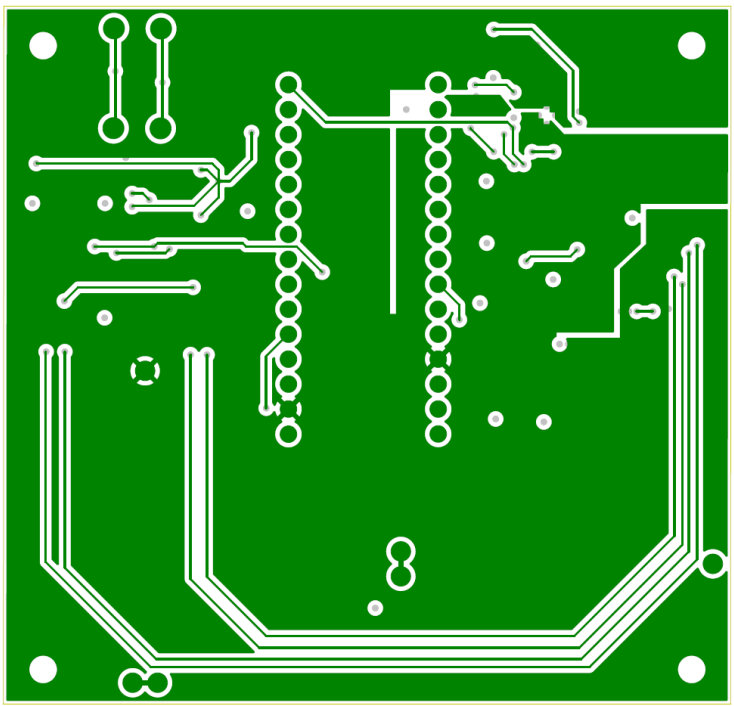


Figure 20: Bottom layer.

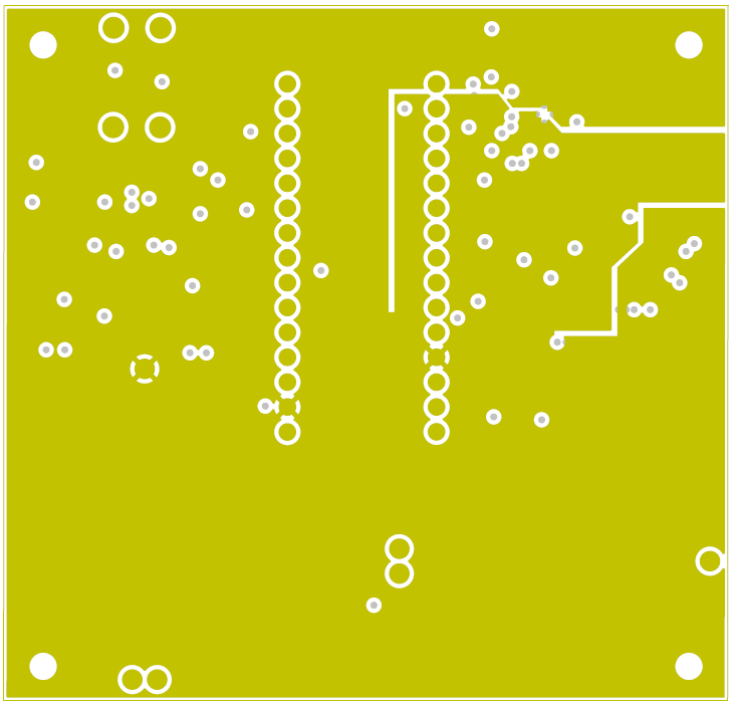


Figure 21: Second layer: ground power plane.

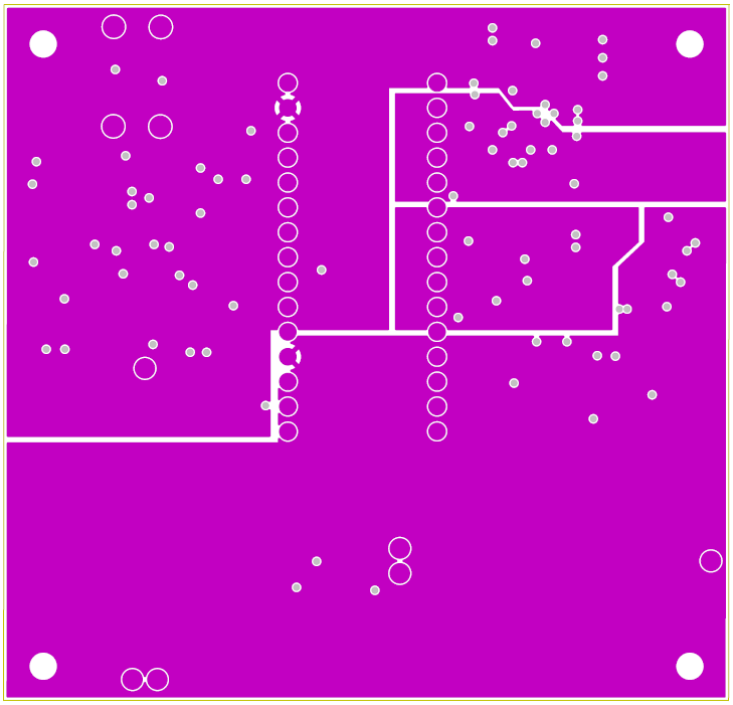


Figure 22: Third layer: segmented power plane.

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