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ACTIVE FILTER FOR DC-LINK LOW FREQUENCY RIPPLE FILTERING AND PASSIVE COMPONENTS REDUCTION

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Abstract

Contemporary Alternating Current to Direct Current converters (AC-DC) and Direct Current to Alternating Current converters (DC-AC) include a DC-link with a relative big DC-link capacitor to filter the ripple. AC-DC converters represent a fundamental component of battery chargers for battery energy storage systems since they allow to charge and possibly discharge the battery. The main drawbacks of AC-DC converters or more in detail of conventional battery chargers are the dimension and the weight, but also the durability over the years. Essentially a battery charger that works using grid power is composed by a Power Factor correction (PFC) bridgeless rectifier that rectifies the current from alternating to direct, in order to charge the battery. This stage is often equipped with a bulk filter made of electrolytic capacitors connected in parallel to the DC-link, in order to smooth out the double line frequency current ripple and obtain a direct current. A Direct Current to Direct Current converter (DC-DC) then regulates voltage and current levels according to the specific requirements of the battery.

The main drawback of conventional battery chargers are the capacitors that, apart from the size and weight, because of being electrolytic, are not so well suited for long time and safety critical application.

This study aims to analyse a new concept of DC-link filter and, in particular, an active buck topology filter that uses Film capacitors. Simulation and analysis using PLECS are conducted in order to verify the functionality of the proposed filter.

In addition, a physical prototype will be implemented in order to validate the obtained simulation results and confirm the feasibility of this kind of filter.

Contents

1. Introduction

1.1 Objectives and structure of the study

This study undertakes a comprehensive examination of a novel battery charger topology designed for energy storage systems, with particular emphasis on mitigating the challenges associated with large DC-link electrolytic capacitance required in AC-DC bridgeless rectifiers. The primary objective is to achieve a battery charger that is more compact, lighter, and possesses an extended lifespan. To address the issue of large DC-link electrolytic capacitance, an active filter will be developed and simulated for the purpose of minimizing ripple effects in the DC-link. The aim is to assess the feasibility of the proposed battery charger through the designed active filter.

A conventional battery charger is usually made by three stages: a PFC stage, a DC-link and a DCDC. The first stage is typically a rectifier, often presented as a PFC bridgeless rectifier, responsible for converting current from alternating to direct. It also strives to maintain a power factor as close as possible to 1, ensuring the absorption of only active power from the grid. Connected to the rectifier, a bulk capacitor, composed of several electrolytic capacitors arranged in series and parallel, is conventionally placed on the DC-link. Those capacitors serve the purpose of filtering out the double line frequency ripple generated by the rectifier, typically occurring at 100Hz or 120Hz. The objective is to achieve a nearly constant current with minimal residual ripple.

A DC-DC converter is then used to transform the rectified voltage from the PFC rectifier, adjusting it to a voltage level suitable for charging the battery. Various DC-DC converter topologies can be employed, but the use of an LLC resonant converter is common due to its notable attributes, such as high efficiency and bidirectional capability. For this reason, an important feature of battery chargers pertains to the direction of the power flow, with the capacity for unidirectional operation, dedicated solely to battery charging, or bidirectional functionality. Currently, only a part of the battery chargers on the market are bidirectional but the trend is moving toward bidirectionality in order to support the grid and enable new commercial scenarios. Focusing on the primary issue within traditional chargers topology, it becomes evident that the capacitance requirement of the DC-link capacitor, essential for minimizing DC-link ripple, may be very high depending on the power demand. Consequently, a considerable quantity of electrolytic capacitors is employed for this purpose. The principal drawback associated with the use of electrolytic capacitors lies in their limited lifespan, which can be very short in worst case scenarios, ranging from 2000 to 3000 hours. In cases where prolonged operational longevity is required, such as energy storage applications, the utilization

of electrolytic capacitors proves to be an unsuitable option.

As it will be explained in following chapters, the most challenging scenario during charging from the grid occurs in the American single-phase configuration. This configuration can deliver up to 19.2kW in the split phase setup, becoming a critical case due to the RMS current drawn from the grid, which is approximately 80A. After rectification, if the DC-link voltage is 600V or lower, the resulting current flow will be around 32A or higher. In order to obtain minimal current ripple at the output a significantly large DC-link capacitance is required.

Regarding this issue, extensive research has been conducted, and many solutions have been proposed in the literature. A predominant approach involves the use of active power decoupling filters employing various topologies such as buck, boost, buck-boost, and others. This strategy optimizes the utilization of energy stored in the capacitor, leading to a substantial reduction in the required capacity. The primary concept underlying active filter involves the decoupling of capacitor voltage from the DC-link voltage, allowing for flexibility where the capacitor voltage can either be lower or higher than the DC-link voltage. This configuration enables the comprehensive utilization of capacitor's energy, allowing for near-complete charge and discharge cycles. In contrast, conventional DC-link passive filters maintain a considerably high stored energy in the capacitor, but only a fraction of it is effectively employed.

The adoption of active filters, therefore, offer the advantage of mitigating the capacitance requirements, thereby facilitating the utilization of Film or ceramic capacitors. Despite having lower energy density, these capacitors exhibit increased durability throughout operational lifespan, and typically feature lower equivalent series resistance (ESR), resulting in minimized energy losses.

The primary objective of this study is to evaluate and validate the effectiveness of active filters in mitigating DC-link current ripple. This reduction consequently leads to a reduction in the size and weight of DC-link capacitor filters and the overall battery charger. Significantly, the study seeks to extend the lifespan of the charger, thereby minimizing the probability of operational failures.

The initial chapters of this research involve an examination of the conventional battery charger structure, encompassing an evaluation of the required capacitance for filtering output ripple and exploring regulations specifying permissible DC ripple limits. Subsequently, a comprehensive literature review delves into active filters specifically designed for ripple mitigation. The investigation includes an in-depth analysis of a buck active topology filter through simulation utilizing PLECS software. Moreover, a practical implementation involves the design and

assembly of a tangible prototype of an active filter to validate both the simulation results and the functional effectiveness of the filter.

1.2 Specification of the project

The goal of this study is to realize an active filter for DC-link low frequency ripple filtering in a battery charger for an energy storage system. The active filter will be designed to work as expected also in the worst possible case configuration that is represented by the split phase US configuration, in which the power absorbed from the grid can be as high as 19.2kW. In this specific case, the battery charger will be able to charge the battery with a maximum power of 15kW. Regarding the battery voltage, the maximum allowed voltage that the charger is able to sustain is between 600V and 1000V.

In the following table, the specification of the battery charger are reported.

Parameter	Value
Vin single phase	240 V_{rms}
Vin three phase	480 V_{rms}
Iin max	64 A_{rms}
Pin	15000 W
Vbat min	600 V
Vbat max	1000 V
Switching frequency	100kHz

Table 1 - Battery charger maximum ratings

All the calculations and design choices that will be described in the following chapters, will be based on these data.

1.3 Power distribution grid in the world

The power distribution grid for private homes is different according to the region or country. As shown in Figure 1 [1] there are three main power distribution systems in the world that are United States (US), Europe and China.

Starting from Europe and China, these two countries exhibit remarkable similarities in both single and three-phase scenarios. The frequency is fixed at 50Hz, but also the voltage is similar, 220V and 230V in single phase, and 380V and 400V in three phase.

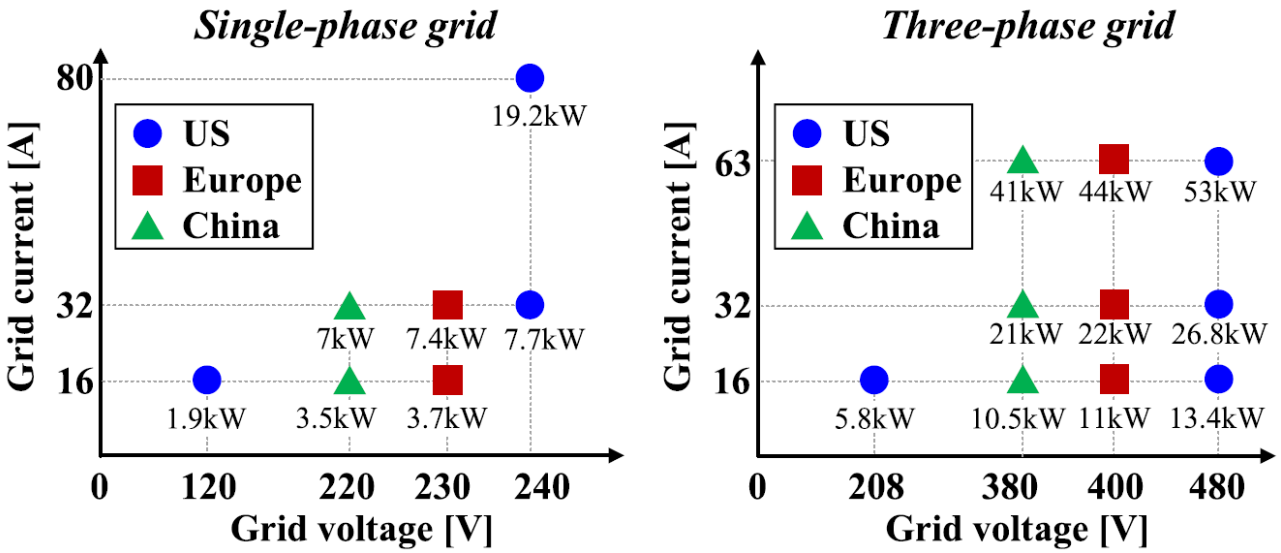

Figure 1 - Power grid in the world

Focusing on US region instead, it is quite different, both in three phase and single-phase configuration respect to the previous case. First of all, the frequency is different and fixed at 60Hz. Moreover, also the voltage in three phase is different, because it can be 208V or 480V. However, the most important difference is related to the single phase case, in which there are two configurations, the normal one that uses only one phase and provides up to 1.9kW of power at 120V, and the split phase configuration that can provide up to 19.2kW of power at 240V. Regarding the three phase grid configuration, it will not be analysed deeply, since it is not a big problem for what concerns the low frequency DC-link ripple. This is related to how a three-phase system distributes power over the three phases. Indeed, having three phases shifted of 120° between each other, implies to already have a constant output power and obviously zero ripple power, because the three-phase system is balanced, and if a PFC rectifier is used, a constant output power will be obtained.

The only problem that remains in three phase is that since mosfet switches are used in the rectifier part, some switching ripple at the output of the rectifier will be present. For this reason, despite having a constant output power, there will be a superimposed switching ripple, that is

highly dependent on the working load, and on the input phase inductance value. In the case under examination, it will be a 100kHz ripple since the PFC works at that frequency. For this reason, a small DC-link capacitor is added, but more about this in the next chapters.

Referring to Figure 1 it is evident that in the single-phase grid case, the worst-case scenario is the split phase case of US grid, where the voltage is fixed at 240V and the current that can be absorbed is up to 80A, resulting in an absorbed power of 19.2 kW. This case is particularly critical because the ripple without any DC-link capacitor can be really high, at a relatively low frequency of 120Hz that is double the fundamental frequency of 60Hz in US. The main problem of this configuration is the high absorbed current that has a Root Mean Square value (RMS) of 80A. In this specific case if normal electrolytic capacitors are employed, the overall volume of the battery charger will increase a lot, but besides the volume, the main problem is the lifetime duration that in an energy storage system application is not enough. This because in the worst-case scenario the capacitors will last no more than 2000-3000h.

1.4 Regulations regarding maximum allowed DC-link ripple in battery charger

For what concerns the regulations, since this work is not focused on the study of a complete battery charger, all the regulations regarding the harmonics levels on the input current will be neglected and the main focus will be given to the standards that regulate the maximum allowed ripple on the battery side.

Different standards on maximum allowed ripple are present depending on the application, but in this study, the standard for electric vehicle onboard chargers will be followed.

For what concerns the regulations regarding DC-link ripple in automotive onboard-chargers, the only one that talks about this topic is the Chinese GB/T 40432-2021 [2] of the National Standard of the People's Republic of China that talks about: "Conductive on-board chargers for electric vehicles".

The norm under consideration deals with the technical requirements and test methods for conductive on-board chargers for electric vehicles.

The paragraph 4.2.8 talks specifically about the "Output voltage ripple factor" and sets the maximum output voltage ripple factor to 5% in voltage-limiting output state.

Moreover, at paragraph 5.3.7 it exposes the exact methods and procedure for testing the DC output voltage error.

The only interesting thing that could be taken from this regulation is the maximum output voltage ripple factor that must be less than 5%. For this reason, all the design of the filter has been done following this value as target.

1.5 Traditional battery charger structure

In this chapter, a brief look at what is a battery charger, and its conventional structure will be exposed, analysing every component that is present.

Primarily, there are two main topologies of battery charger: single-phase and three-phase. However, it is common to find a unified solution where a single charger encompasses both configurations.

The second important characteristic of a charger is the power flow direction, that can be unidirectional, or bidirectional. Unidirectional chargers can only charge the battery, therefore deliver power only in one direction. Bidirectional chargers can be used both for charging the battery, but also for using the energy storage as a source of power for different kind of applications such as battery to grid or battery to home appliance.

In Figure 2 a simple architecture of a traditional single phase battery charger is shown.

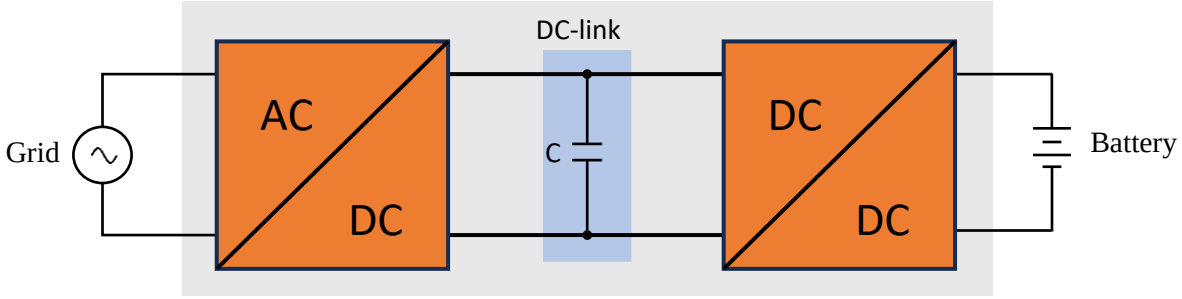

Figure 2 - Traditional battery charger

Talking about the structure, as shown in the previous picture, it is normally composed of three main parts:

- **AC-DC Rectifier.** This part of the component is in charge of converting alternating current coming from the grid to direct current (DC). It can be achieved in various ways, depending on the target of efficiency and power factor, but the simplest way is a diode bridge rectifier that is only composed of diodes. The main drawback of this solution, neglecting the efficiency, is that it has no control on the power factor, that depends only by the load. This means that in most of the cases, a distorted and out of phase signal that is not a pure sinewave is absorbed from the grid leading to a power factor that is far from 1. A solution to this problem is to introduce a bridgeless power factor corrector rectifier, that is normally composed by all mosfets, or some mosfets and some diodes depending on the configuration. In this way thanks to the mosfets it is possible to control the power factor and try to maintain it as close as possible to 1. At the output of this component, a perfectly rectified sinewave can be found, but this will be really far from being constant, at least in the single-phase case.

- **DC-link capacitor.** For obtaining a nearly constant or at least ripple limited current, normally a big capacitor is attached at the output of the AC-DC rectifier and has the scope of taking the rectified sinewave and absorbing and releasing energy when needed in order to obtain a nearly constant current.
- **DC-DC converter.** The last stage of a battery charger is normally the DC-DC converter. In most of the cases, the AC-DC rectifier, works at a constant voltage setpoint that depends mainly on the voltage of the grid. This means that in some way this voltage must be adapted to the voltage of the battery that changes during the charging cycle. For this reason, a DC-DC converter is introduced, and has the objective of adapting the rectified voltage to the one of the battery. This converter normally has also another task that is to electrically isolate the grid from the battery. This is normally done by employing transformers. For this reason, a common topology that is used is a resonant converter. It has the double advantage of being able to adapt the voltage, with a really high efficiency, but also provide the electrical isolation, since to work it uses a transformer.

1.6 DC-link capacitor analysis for passive filter

In the following chapters a complete analysis will be carried out in order to calculate the needs in terms of DC-link capacitance, in the two possible working modes of a battery charger that are single phase and three phase configurations.

1.6.1 Three phase case

The first working mode that is analysed is the three-phase case that is shown in Figure 3. In this configuration, the battery charger is connected to the three-phase grid socket. In particular due to how the three-phase distribution grid is made, having a look at how the power is distributed over the three phases, it will be clear that at the output of the rectifier a perfectly constant power will be present.

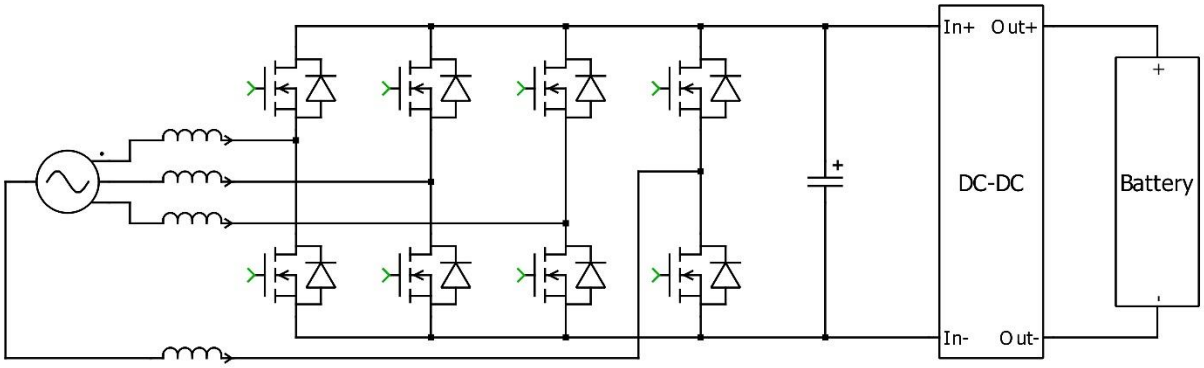

Figure 3 - Three phase battery charger

Indeed, it is possible to calculate the power by summing the contributions of the three phases, and assuming that current and voltage are perfectly in phase the following equation is obtained:

$$P_{3phase} = VI\sin^2(\omega t) + VI\sin^2\left(\omega t + \frac{2}{3}\pi\right) + VI\sin^2\left(\omega t - \frac{2}{3}\pi\right)$$

Eq. 1

where P_{3phase} is the total power of a three-phase system, V is the phase rms voltage, I is the phase rms current and ω is the angular frequency equal to $\omega = 2\pi f$.

The previous equation simplifies to:

$$P_{3phase} = 3VI$$

Eq. 2

that is a constant power. Thanks to this fact, if a bridgeless power factor corrector rectifier is used, there will be no ripple on the DC-link battery side.

However, in case a diode bridge rectifier is employed, it won't be possible to get a constant

output, but the signal at the output will have a DC component, and some harmonic components at 360 Hz and multiples.

On the other hand, in the PFC case, in a real world case scenario, the only residual ripple that remains is due to the switching of the PFC that is basically a bridgeless rectifier controlled in order to generate a sinusoidal current and obtain a power factor of 1. For this reason, a parallel capacitor must be placed in parallel on the DC-link in order to compensate for the high frequency ripple and filter it out.

In order to design the capacitor that must be put on the DC-link for reaching a target residual ripple in the three-phase working mode, the following simple equation can be used:

$$C = \frac{\sqrt{3} \cdot \left(1 - \frac{V_{LL}}{V_{DC}}\right) \cdot \frac{V_{LL}}{V_{DC}} \cdot I_{RMS}}{\sqrt{2} \cdot f_{sw} \cdot \Delta V_{PP}}$$

Eq. 3

where V_{LL} is the line-to-line grid voltage, V_{DC} is the DC-link voltage, I_{RMS} is the phase current, f_{sw} is the switching frequency of the rectifier, and ΔV_{PP} is the peak to peak DC-link voltage ripple.

In the worst case, the battery charger will work with 600Vdc on the DC bus, with an RMS current of 32A for phase, at 100 kHz switching frequency. If the residual voltage ripple target is of 1%, using Eq. 3, a parallel DC capacitor of 17uF must be placed. However, taking a safety margin of 1.5 the capacitor needs to be around 25uF.

1.6.2 Single phase case

As said in the previous sections, the worst possible working scenario is present when the battery charger works in the US split phase configuration as shown in Figure 5, where the voltage is 240Vrms and the phase current can go up to 80Arms (in the specific case the charger under exam will support up to 64Arms).

Moreover, since the system is working in single phase, for sure the power will not be constant as the three phase case analysed before, but in the best case after the rectifier, a perfectly rectified sinewave will be obtained as it can be seen in Figure 4. In addition to this rectified wave, there is a superimposed 100kHz ripple that is due to the switching of the PFC rectifier and depends on the working load and on the input inductance and can be perfectly seen in Figure 6.

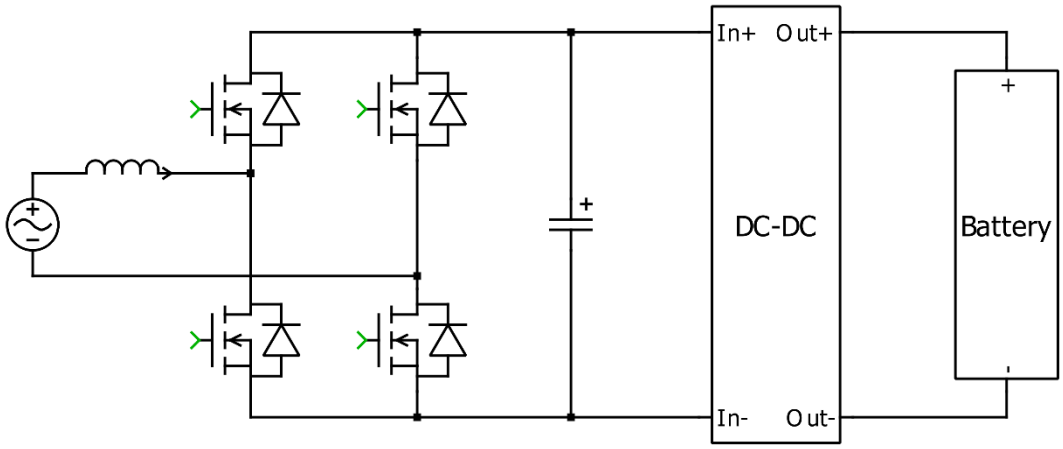

Figure 5 - Single phase configuration Battery-Charger

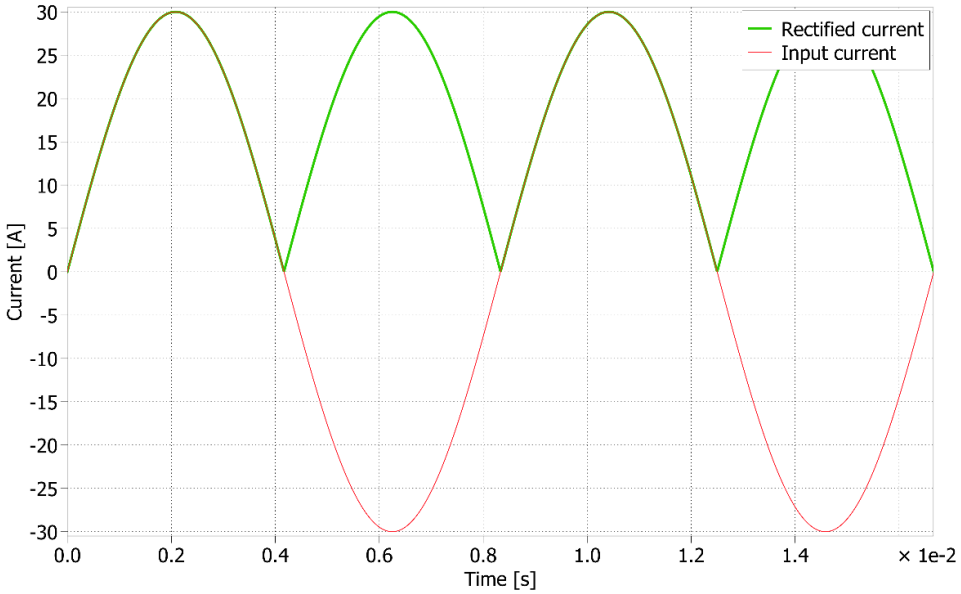

Figure 4 - Ideal input current and rectified current

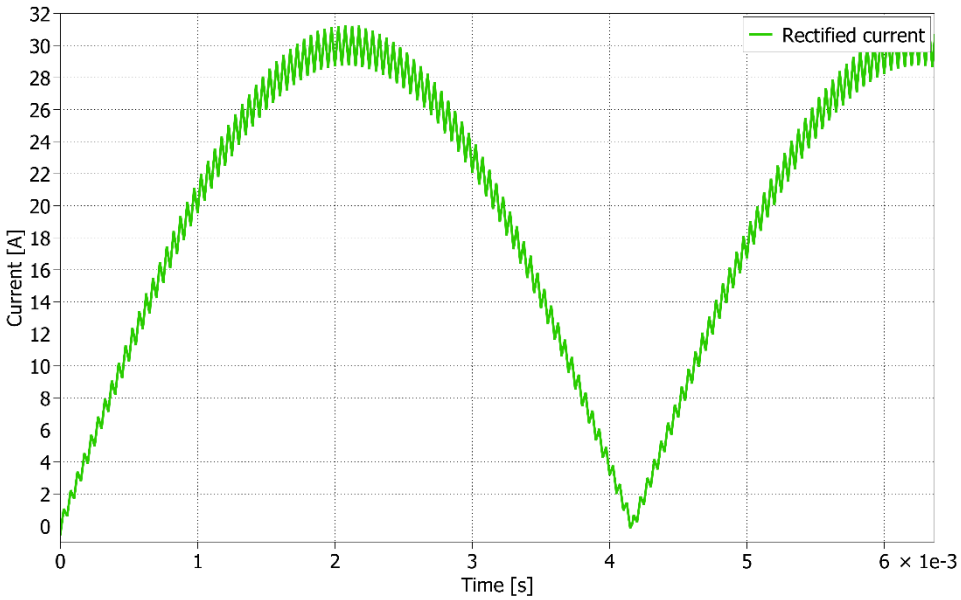

Figure 6 - Rectified current detail

In this specific case, the capacitance needed in order to filter out the double line frequency ripple and the switching ripple is not small as the three-phase case analysed before. Indeed, if a current ripple lower or equal to 5% wants to be reached, larger capacitance is needed. Following the steps done in [3] it is possible to obtain the minimum capacitance needed to filter out the DC-link current ripple. The first step is to start by calculating the power absorbed by the load knowing that the AC power supply voltage v_s and current i_s are assumed to be sinusoidal, as shown in the following equations:

$$v_s(t) = V_s \sin \omega t$$

Eq. 4

$$i_s(t) = I_s \sin(\omega t - \varphi)$$

Eq. 5

where V_s and I_s are the voltage and current peak values, respectively, φ is the angle between the supply voltage and current and ω is the supply angular frequency. The supply power from the ac source can be expressed as follows:

$$P_{in} = v_s(t) i_s(t) = \frac{V_s I_s}{2} \cos \varphi - \frac{V_s I_s}{2} \cos(2\omega t - \varphi)$$

Eq. 6

The energy of the input inductor can be expressed as:

$$E_L = \frac{1}{2} L i_s^2(t) = \frac{1}{2} L I_s sin^2(\omega t - \varphi)$$

Eq. 7

where L is the input inductor inductance. The corresponding power is:

$$P_L = \omega L I_s^2 \sin(\omega t - \varphi) \cos(\omega t - \varphi)$$

Eq. 8

The input power of the rectifier after the input inductor can be obtained by subtracting Eq. 6 and Eq. 8 as:

$$P_{in} = \frac{V_s I_s}{2} \cos \varphi - \left(\frac{V_s I_s}{2} \cos(2\omega t - \varphi) + \frac{\omega L I_s^2}{2} \sin(2\omega t - 2\varphi) \right) = P_o + P_r$$

Eq. 9

The constant power P_o feeds the DC load:

$$P_o = \frac{V_s I_s}{2} \cos \varphi$$

Eq. 10

The ripple power P_r is a second-order harmonic power:

$$P_r = -\left(\frac{V_s I_s}{2} \cos(2\omega t - \varphi) + \frac{\omega L I_s^2}{2} \sin(2\omega t - 2\varphi)\right)$$

Eq. 11

By using the ripple peak power P_{r_peak} and peak current, the ripple energy E_r can be determined as:

$$E_r = \frac{P_{r\_peak}}{\omega} = \frac{\sqrt{P_o^2 + \left[\frac{2\omega L P_o^2}{V_s^2 cos^2 \varphi} - P_o \left(\frac{sin\varphi}{cos\varphi}\right)\right]^2}}{\omega}$$

Eq. 12

With the derived single-phase ripple energy requirement and the voltage ripple requirement ΔV_d, the DC bus capacitance needed can be calculated as:

$$C_b = \frac{\sqrt{P_o^2 + (\frac{2\omega L P_o^2}{V_s^2 cos^2 \varphi} - P_o \left(\frac{sin\varphi}{cos\varphi}\right))^2}}{V_d \Delta V_d \omega}$$

Eq. 13

where V_d is the DC-link voltage and ΔV_d is the allowed DC-link voltage ripple.
The corresponding current rating of the capacitor is then given by:

$$i_{cb\_rms} = \frac{P_{r\_peak}}{\sqrt{2} V_d}$$

Eq. 14

Using Eq. 13 and the following data that represent the worst-case scenario:

Parameter	Value
Vac peak [V]	340.00
Max out. power [W]	15000
Frequency [Hz]	60
DC link voltage [V]	600
Δv Ripple %	5
Δv Ripple voltage [V]	29.5
Input inductor [H]	0.001

Table 2 - Worst case scenario

it is possible to calculate the value of the capacitor and the rms current rating as:

$$C_b = 2.2\ mF$$

$$i_{cb\_rms} = 18.06A$$

As it can be noticed, for a 15kW battery charger working at 600V, a very large DC-link capacitor is needed in order to obtain a maximum voltage ripple of 5%.

1.7 Capacitor technology analysis

In this chapter, a brief discussion about the different DC-link capacitor technologies that are present on the market nowadays, and the main advantages and disadvantages of each of them will be carried out. This will be done following some important results present in [4].

The three main capacitor technology used nowadays as DC-link capacitor filter are Aluminum Electrolytic Capacitors (Al-Caps), Metallized Polypropylene Film Capacitors (MPPF-Caps) and high capacitance Multi-Layer Ceramic Capacitors (MLC-Caps).

For representing a real capacitor, an equivaled lumped model can be realized as in Figure 7.

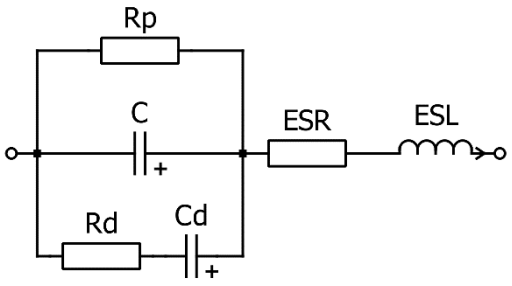

Figure 7 - Equivalent capacitor model

In the figure above *C*, *Rs*, and *Ls* are the capacitance, the equivalent series resistance (ESR) and the equivalent series inductance (ESL), respectively. Then *Rp* is the insulation resistance, *Rd* is the dielectric loss due to dielectric absorption and molecular polarization and *Cd* is the inherent dielectric absorption.

Since the previous model is quite complex and requires a lot of components, usually a simplified model is used and is represented as in Figure 8:

Figure 8 - Simplified capacitor

This model is composed by only three elements *C*, *Rs*, and *Ls*. They represent the capacitance, the equivalent series resistance and the equivalent series inductance. This model is a good approximation of a real capacitor.

In Figure 9 a comparison between the three technologies available for DC-link capacitor is depicted in order to point out the performance of each of them regarding different parameters. As it can be seen, for what concerns the energy density, the Aluminum capacitors offer the highest energy density possible, and the Film ones, are the worst type. Instead looking at the ESR resistance, it will be clear that the Aluminum capacitors have the highest resistance, whereas the Film capacitors have the lowest resistance. Moreover, an interesting thing about Film capacitor and Ceramic capacitor is the reliability that is really high respect to the Aluminum ones.

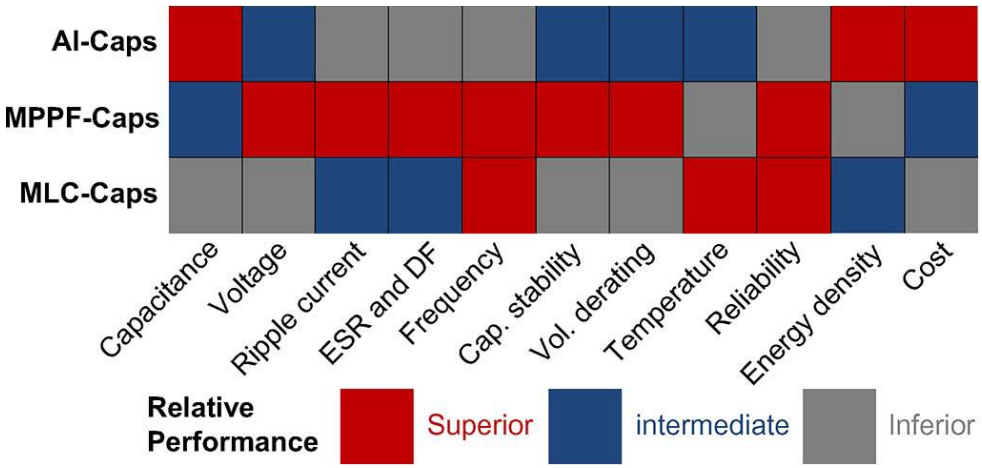

Figure 9 - Capacitor main characteristics

Another important thing to take into consideration is the failure modes that the capacitors could face. The possible failures and the factors that cause stress on the capacitor are shown in Figure 10. As it can be seen in the figure above the most critical things that can stress and damage the capacitors are temperature, voltage, current and humidity. This is quite similar for all the types of capacitors. An interesting thing to point out is that the dominant failure mechanism of Aluminum capacitor is the electrolyte vaporization that can happen for different reasons. On the other hand, for what concerns the Film capacitors, the dominant failure mechanism is represented by the dielectric loss.

For all the things mentioned before, Film capacitors are better in terms of lifetime, reliability,

and also for voltage and current rating. Obviously, they have a lower capacitance and energy density respect to the Aluminum ones, but this is compensated by all the advantages previously mentioned. Also ceramic capacitor are a good choice for DC-link ripple filtering, but they are not so cheap, and they have low voltage rating, meaning that a lot of capacitor in series must be placed, for reaching the desired voltage rating.

	Al-Caps	MPPF-Caps	MLCC-Caps
Dominant failure modes	wear out		
	open circuit	open circuit	short circuit
Dominant failure mechanisms	electrolyte vaporization; electrochemical reaction	moisture corrosion; dielectric loss	insulation degradation; flex cracking
Most critical stressors	T_a, V_C, i_C	T_a, V_C, humidity	T_a, V_C, vibration
Self-healing capability	moderate	good	no

Figure 10 - Possible failure modes

1.8 Proposed battery charger structure

In this chapter the proposed battery charger structure will be described and analysed in deep, in order to understand all the components it contains inside, with a special focus on the active filter. As it can be seen in Figure 11, where the proposed battery charged structure is shown, the structure is quite similar to the traditional ones. Nevertheless, taking a deeper look inside all the components, it will be clear that there is a big difference especially in the DC-DC converter.

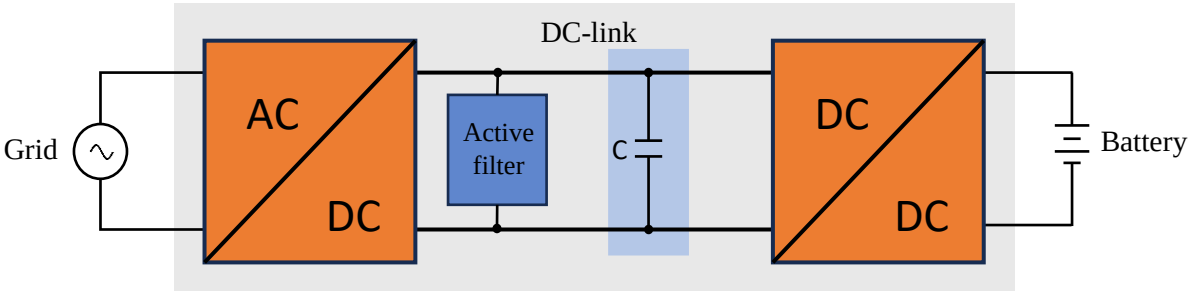

Figure 11 - Proposed battery charger structure

At first sight, it seems to be the same as the traditional battery charger, where normally an LLC resonant converter is present with the scope of adapting the voltage of the AC-DC rectifier, to the one of the battery, having a variable conversion ratio depending on the rectifier and battery voltage. However, in this case, the DC-DC converter is a 1 to 1 isolation transformer, hence it has always a constant conversion ratio of 1. This has a big implication in the voltage of the AC-DC rectifier side, because this component will see exactly the voltage of the battery since the DC-DC converter is almost transparent, at least up to a certain frequency depending on the passband width.

Another difference of this topology is that, since the DC-DC converter has a fixed ratio of 1, the AC-DC rectifier will see the battery voltage. For this reason, the rectifier, will not be able to generate and impose a certain voltage, but it will experience the voltage imposed by the battery. This means that the rectifier will work with only a current target that depends on the requested charging power, and not a voltage target.

The last component added in this topology is the active filter that is attached on the DC-link between the rectifier and the DC-DC converter. Apart for the intention of reducing the dimension of the DC-link capacitance, this kind of filter is needed for the same reason explained before, that is the fixed conversion ratio DC-DC converter. Since the voltage of the DC-link is imposed by the battery, only a small 100kHz switching ripple will be present on the DC-link. The 120Hz ripple will not affect the voltage, but only the current that flows to the battery.

For this reason, the capacitors attached in parallel on the DC-link will not be able to filter the 120Hz ripple, but only the 100kHz one. This implication is strictly related to how a capacitor works and especially how the current flows through a capacitor. Taking a closer look at Eq. 15 it is clear that the current $i(t)$ that flow across a capacitor is proportional to the capacitance value C multiplied by the variation of the voltage $v(t)$ on the capacitor.

$$i(t) = C\frac{dv(t)}{dt}$$

Eq. 15

This means that if the voltage of a capacitor is constant, no current will flow through it. For the reason explained before, the voltage on the DC-link is almost constant, it has only a 100kHz ripple component, but it has no 120Hz ripple voltage.

The capacitor attached to the DC-link is used only to filter the 100kHz component, but the 120Hz ripple cannot be filtered by a passive capacitor as in the traditional topology. Instead of a passive capacitor, an active filter that is able to compensate the 120Hz ripple current must be placed in parallel to the DC-link. The filter will have two working modes depending on the current that flows through the DC-link. When the current is above the average value, the filter will absorb the ripple power and store it in the active filter capacitor. Instead, when the current is under the average value, it will inject current on the DC-link by releasing the energy stored in the filter capacitor.

Everything said until now can be confirmed by looking at Figure 12, Figure 13 and Figure 14. In particular, in Figure 12 all the waveforms related to the grid side are plotted. The voltage and the current represent the grid side voltage, and the grid side current absorbed by the charger,

assuming an ideal power factor of 1 and no harmonic distortion. Multiplying those two quantities it is possible to obtain the grid absorbed power. This power, as it can be noticed has a constant component, and a sinusoidal component that represent the ripple power.

Analysing the waveforms values on the DC-link side, for what concerns the traditional topology, they will result as in Figure 13. It can be seen that both the current and voltage represent a perfectly rectified sinewave, with a frequency that is double the one of the grid. Multiplying those two quantities it is possible to obtain the power that flows on the DC-link. This power, as it can be noticed has a constant component, and a sinusoidal component that represent the ripple power, which is obviously at double the line frequency.

Regarding the waveforms values on the DC-link side, for what concerns the proposed topology, they will result as in Figure 14.

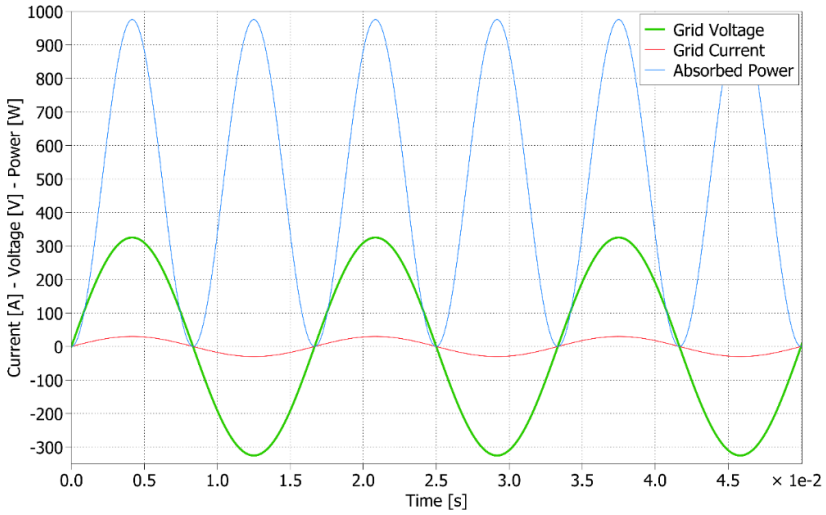

Figure 12 - Grid side waveforms

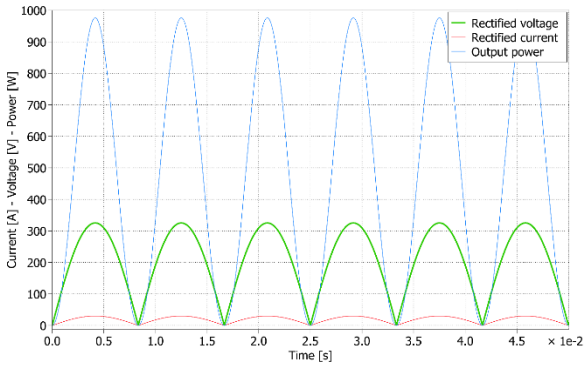

Figure 13 - Traditional charger case

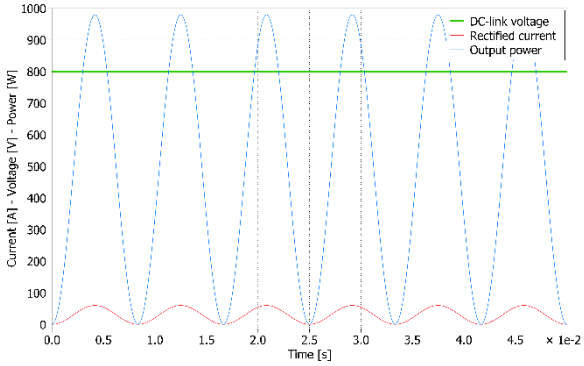

Figure 14 - Proposed charger case

In this case, since the battery voltage imposes the voltage of the DC-link, the voltage will be constant. Instead, the current will be different from the previous case, since it will be a pure sinewave, translated up of the amplitude of the sinewave itself obtaining a signal that is always higher or equal to 0. Multiplying the voltage and the current, it is possible to obtain the power

that flows on the DC-link. This will be exactly the same as in the case before.
More information and details regarding the existing active filter topology and their working principle is given in the following section.

2. Active filter topology literature analysis

In this chapter an analysis of the main active filter topology for double line frequency ripple present in literature will be exposed, pointing out all the pros and cons for every topology. In addition, the capacitor ratings in terms of capacity, voltage and current will be calculated in order to make a comparison between all the topologies as done by [3].
First of all, as shown in Figure 15 the different types of filter can be divided and characterized by four different parameters that are:

- The type of storage element
- The topology
- The type of control
- The number of stages

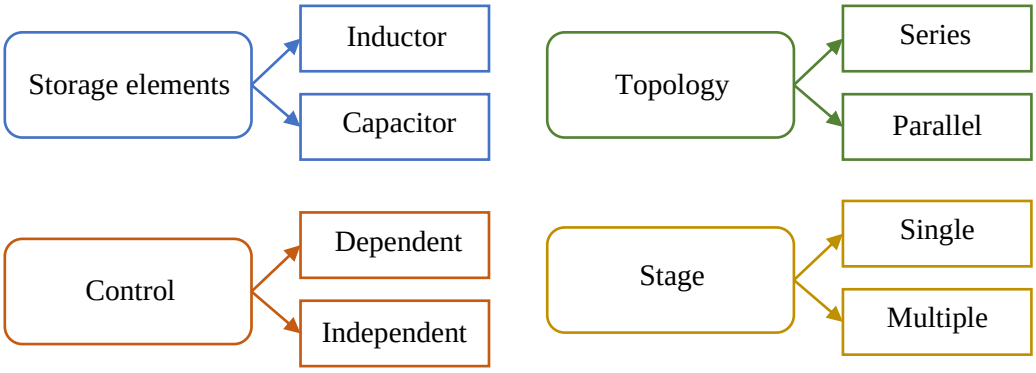

Figure 15 - Different characteristics of the filters

Starting from the storage element type, the ripple energy can be stored in inductors or capacitors. If an inductor is used, the energy is stored in the form of magnetic field energy while if a capacitor is used, the energy is stored in the form of electric field energy. Both solutions have pros and cons, but in general capacitors are better suitable for energy storing respect to inductors.
For what concerns the topology, series and parallel connection can be found. As the name already says, series filters are attached in series on the DC-link after the single-phase PWM rectifier, while the parallel filters are attached in parallel on the DC-link.
Both of the precedent topologies can present a single stage or multi-stage filter. This means that more filters can be placed in parallel or series in order to sum up the contributes an also

introduce some additional techniques as the interleaving.

The last important parameter relates to the type of control employed for the filter. This control can be independent or dependent respect to the one of the single-phase PWM rectifier. Both of them have different pros and cons, but normally it is better to have independent controls, especially for the fact that in this way is possible to turn off the filter when the charger is working in three phase configuration, or for any other reasons.

In this specific case, a parallel active filter will be analysed, but all the assumption that will be made are really similar for series active filters.

As shown in Figure 16 the power that enters the DC-link has a sinusoidal component, that represents the ripple part, but also a constant DC component.

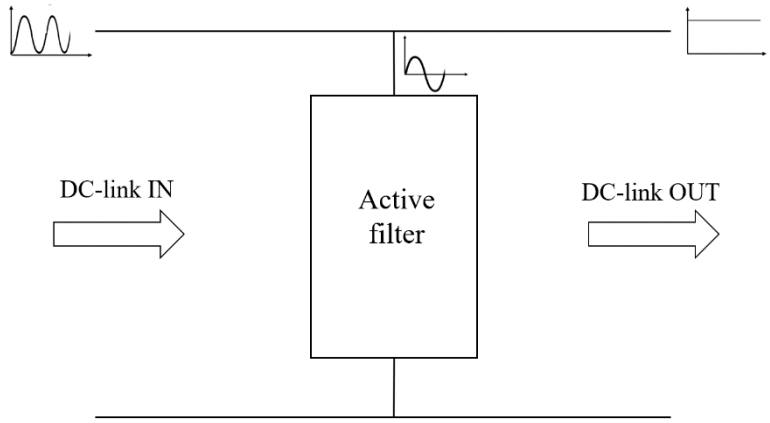

Figure 16 - Parallel active filter

At the output of the DC-link instead, a constant power with only a residual ripple is present. This is true thanks to the introduction of the active filter, that absorbs and releases a power that is opposite in sign with respect to the ripple power that flows through the DC-link. In this way it is able to compensate for that sinusoidal power leading to an almost constant output that will enter the battery.

This can be perfectly seen in Figure 17 where two phases can be identified: the first is the absorption phase in which the filter absorbs energy and stores it in the capacitor, since the ripple energy on the DC-link is in the positive half-wave. The second phase is the release phase, in which the filter releases the energy stored in the capacitor and compensates for the negative ripple half-wave.

The main advantage of active filters is that the capacitor voltage is independent from the DC-link voltage. This means that is possible to charge and discharge the capacitor in a more efficient way taking advantage of the full capacity. Indeed, theoretically the capacitor could be charged and discharged completely at every cycle, but in reality a small safe margin must be taken.

In the following sections a complete analysis of the main topologies of active filters that can be found in literature will be exposed, pointing out all the advantages and disadvantages of each of them.

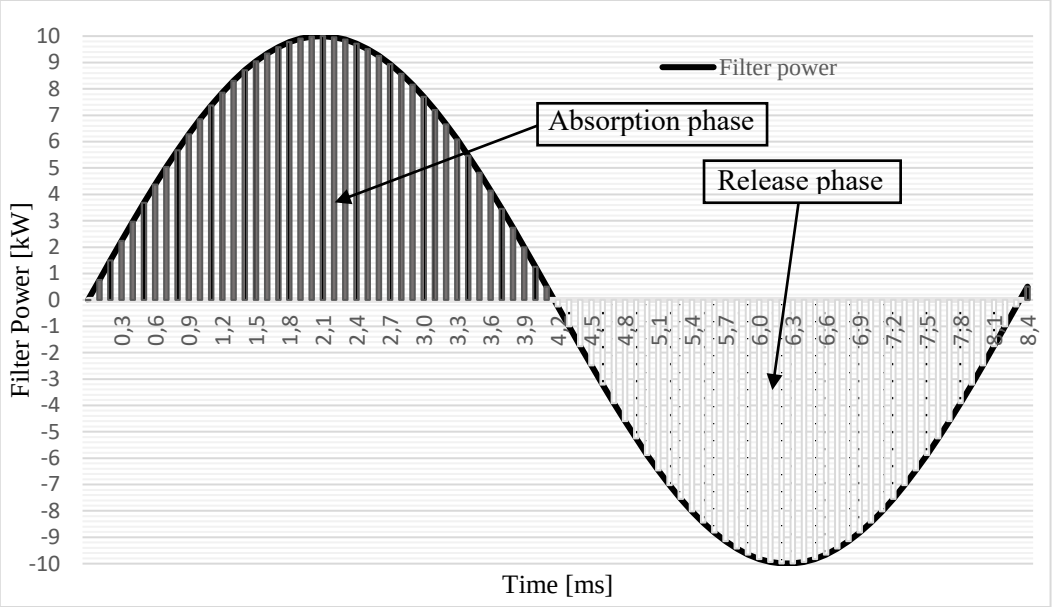

Figure 17 - Active filter energy flow

2.1 Buck

The first filter topology analysed is the Buck topology [3]. As shown in Figure 18 the auxiliary filter is a parallel topology since it is connected in parallel on the DC-link. The scheme represents exactly a synchronous bidirectional buck converter and in this case the energy storage element is a capacitor.

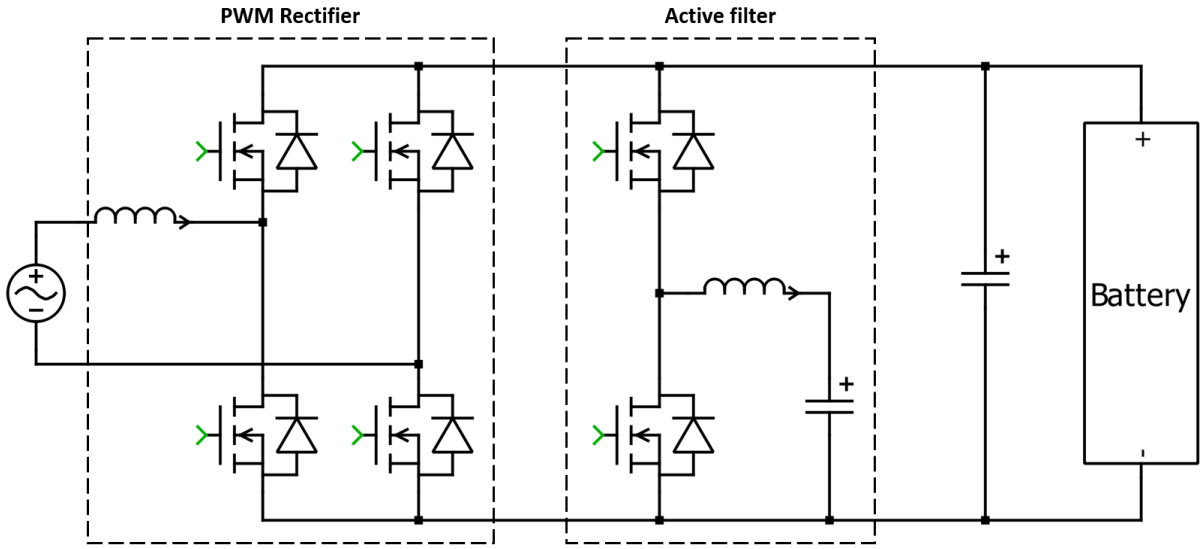

Figure 18 - Buck filter topology

For what concerns the working principle, the filter has two working modes, the buck mode and the boost mode. When the current on the DC-link is higher than the DC value, the filter works as a buck converter, lowering the voltage from the DC-link value to a certain specified value. Doing this, a current is absorbed from the DC-link and the auxiliary capacitor is charged.

When the current on the DC-link is lower than the DC value, the filter works as a boost converter, boosting up the voltage of the capacitor to the one of the DC-link. Doing this, a current flow from the capacitor to the DC-link, discharging the auxiliary capacitor. In this way the filter is able to compensate the ripple energy by continuously absorbing and releasing energy from the filter capacitor.

For the buck active topology, in order to calculate the minimum necessary capacity C_s to eliminate the ripple the following equation can be used:

$$C_s \geq \frac{2P_{r\_peak}}{V_{c\_peak}^2 \omega}$$

Eq. 16

where P_{r_peak} is the ripple peak power, V_{c_peak} is the peak voltage on the active filter capacitor and ω is the grid angular frequency.

In this case there is the assumption that the auxiliary capacitor, completely charges and discharges every cycle and the voltage goes from 0 to a peak value called V_{c_peak}.

For calculating the voltage variation V_{cs} in time on the capacitor filter the following equation can be used:

$$V_{cs} = \sqrt{\frac{P_{r\_peak}}{C_s \omega}(\mathrm{k} - \cos 2\omega t)}$$

Eq. 17

where k is:

$$k = \frac{V_{cs\_max}^2 C_s \omega}{P_{r\_peak}} - 1, \qquad k \geq 1$$

Eq. 18

and V_{cs_max} is the maximum capacitor voltage.

The theoretical minimum capacitor needed to filter out the ripple energy derived from the rectification of the current is:

$$C_s = 320\mu F$$

In this case the capacitor charges and discharges completely from the maximum admissible voltage that is assumed to be 500V to 0V. This can be easily seen in Figure 19 and represent a borderline case. Increasing by little steps the capacitor value, it will be clear that the capacitor no longer discharges from 500V to 0V, but it goes from 500V to a certain value that can be 100V, 150V and so on. In all this cases the capacitor is not used completely, since a residual energy is always present in it.

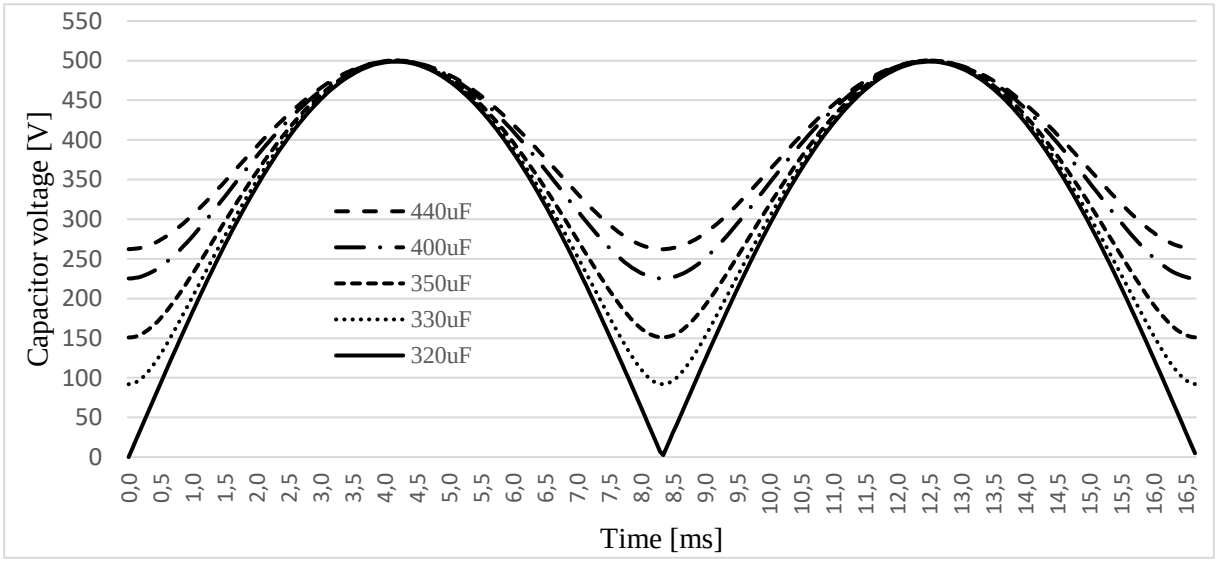

Figure 19 - Capacitor voltage depending on capacitance value

Starting from Eq. 16 a more complete equation that takes into account the minimum and maximum voltage of the auxiliary capacitor V_{c_min} and V_{c_max} can be derived as:

$$C_s \geq \frac{2P_{r\_peak}}{(V_{c\_max}^2 - V_{c\_min}^2)\omega}$$

Eq. 19

As it can be noticed from Eq. 19 and especially in Figure 19 the larger the swing that the capacitor can have the lower the capacitance needed. Obviously a too high swing especially with low voltage makes the buck work with a high conversion ratio, leading to lower efficiency, thus there is a trade-off between capacitor voltage swing and energy utilization.

Another parameter that must be set is the capacitor maximum voltage V_{c_max}. In this case since a buck converter is employed, this voltage must be always lower than the minimum voltage that the DC-link can assume, and also a small safety margin must be taken.

Talking about the current i_{cs} that flows through the capacitor and inductor, this can be calculated as:

$$i_{cs} = \frac{P_{r\_peak} \sin 2\omega t}{\sqrt{\frac{P_{r_{peak}}}{C_s\omega}(k - \cos 2\omega t)}}$$

Eq. 20

In Figure 20 the current that flows through the capacitor in time is shown. The borderline case is the one with the smallest possible capacitance (320uF) that charges and discharges completely. In this it can be seen that every period the current passes from -60A to +60A instantly. On the other hand, increasing the capacitor dimension, the current will no longer have instantaneous sign changes, but will follow a more sinusoidal trend. In addition, the bigger the capacitance, the lower the current that flows in it.

If the RMS current of the auxiliary capacitor wants to be evaluated, the following equation can be used:

$$i_{cs\_rms} = \frac{\sqrt{2}P_{r\_peak}}{V_{c\_peak}}$$

Eq. 21

where V_{c_peak} is the peak capacitor voltage.

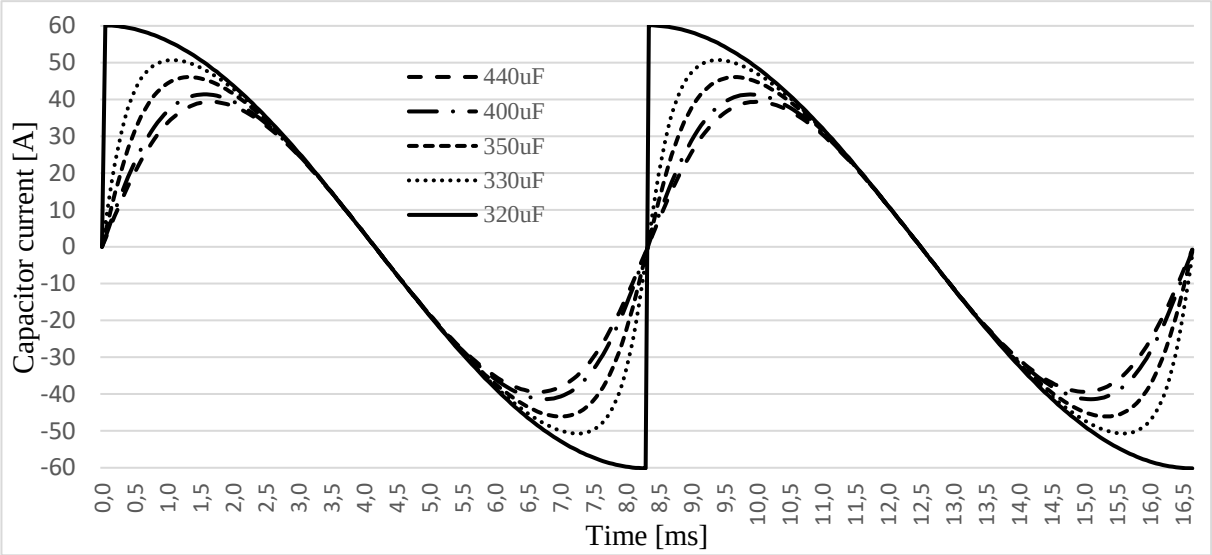

Figure 20 - Capacitor current depending on the capacitor value

For what concern the inductor selection there are two possible working modes: Continuous Conduction Mode (CCM) or Discontinuous Conduction Mode (DCM) mode. In DCM mode the inductor selection can be done following Eq. 22 and Eq. 23 as:

$$L \geq \frac{2 \cdot \bar{\imath}_{cs} \cdot T_s}{I_{peak}^2} \frac{V_d V_{cs} - V_{cs}^2}{V_d}$$

Eq. 22

$$L \leq \frac{T_s}{2 \cdot \bar{\imath}_{cs}} \frac{V_d V_{cs} - V_{cs}^2}{V_d}$$

Eq. 23

where V_d is the DC-link voltage, $\bar{\imath}_{cs}$ is the average inductor current, V_{cs} is the capacitor voltage, T_s is the switching period, and L is the inductance of the buck inductor.
Instead, working in CCM mode [5], the inductor dimension can be evaluated as:

$$L_f = \frac{V_{cf}\left(V_{dc} - V_{cf}\right)}{\Delta I_{Lf,hf} V_{dc} f_s}$$

Eq. 24

where V_{cf} is the average voltage over the auxiliary capacitor, $\Delta I_{Lf,hf}$ is the desired high frequency inductor current ripple and f_s is the switching frequency of the filter.
In the end, the main advantage of this topology is that the capacitor works at lower voltages respect to the DC-link, making possible to use low voltage, high-capacity capacitors like Film or Ceralink. Also the voltage stress on the switches is the same as the bridge rectifier, therefore no higher rating switches are needed for the filter.

2.2 Boost

Another commonly used topology that is analysed is the Boost topology [6] [7]. As shown in Figure 21 the auxiliary filter is a parallel topology since it is connected in parallel on the DC-link. The scheme is exactly a synchronous bidirectional Boost converter and in this case the energy storage element is a capacitor.

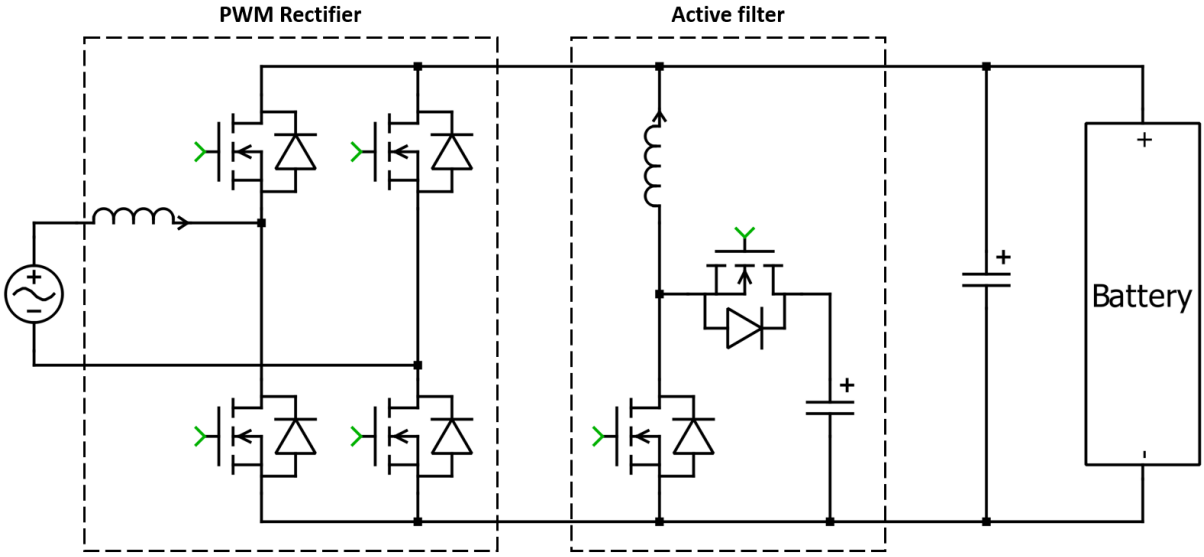

Figure 21 - Boost filter topology

For what concerns the working principle, the filter has two working modes, the boost mode and the buck mode. When the current on the DC-link is higher than its mean value, the filter works as a boost converter, boosting up the voltage from the DC-link value to a certain specified value. Doing this, a current is absorbed from the DC-link and the auxiliary capacitor is charged. When the current on the DC-link is lower than its mean value, the filter works as a buck converter, lowering the voltage of the capacitor to the one of the DC-link. Doing this, a current flow from the capacitor to the DC-link, therefore the auxiliary capacitor is discharged. In this way the filter is able to compensate the ripple energy by continuously absorbing and releasing energy from the filter capacitor.

In the boost converter topology, the capacitance needed in order to eliminate the current ripple of the DC-link is calculated as follows:

$$C_s \geq \frac{2P_{r\_peak}}{\left(V_{c\_max}^2 - V_{c\_min}^2\right)\omega}$$

Eq. 25

where V_{c_max} and V_{c_min} are the maximum and the minimum capacitor voltage, ω is the angular frequency, and P_{r_peak} is the ripple peak power.

Differently from the buck topology, where V_{c_max} must be lower than the DC-link voltage, in the boost topology V_{c_min} must be higher than the DC-link voltage.

The theoretical minimum capacity depends on the maximum voltage admissible on the auxiliary capacitor, but assuming for example that the capacitor can swing between 950V and 1200V, the needed capacitance is:

$$C_s = 146\mu F$$

In this configuration, the working voltage of the auxiliary capacitor is always higher than the one of the DC-link, therefore in this case there is almost no choice on the capacitor technology and only Film capacitors can be used.

As in the buck converter topology, in order to have a smaller auxiliary capacitor, the voltage range must be increased. But increasing too much the upper value of the voltage, will result in high values of conversion ratio that means lower boost efficiency.

The advantage of this topology is that the capacitor works at higher voltages respect to the DC-link, therefore high voltage, low-capacity capacitors can be used, gaining energy storage capability. This is due to how a capacitor stores energy, because looking at Eq. 26 the energy stored in a capacitor is proportional to the capacitance, hence lower capacitance means lower energy, but it also have a quadratic proportionality respect to the voltage, therefore working at higher voltages gives high advantages in terms of energy storage capability.

$$E = \frac{1}{2} CV^2$$

Eq. 26

On the other hand, one drawback that arise is related to the switches of the filter, that since the capacitor works at higher voltage respect to the one of the DC-link, they will require a higher voltage rating respect to the rectifier ones. This implies to have different switches ratings in the battery charger that from an industrialization point of view could be not the best choice.

2.3 Buck-Boost

Another commonly used topology that is analysed is the Buck-Boost topology [8] [9]. As shown in Figure 22 the auxiliary filter is a parallel topology since it is connected in parallel on the DC-link. The scheme is exactly a synchronous bidirectional Buck-Boost converter and in this case the energy storage element is a capacitor.

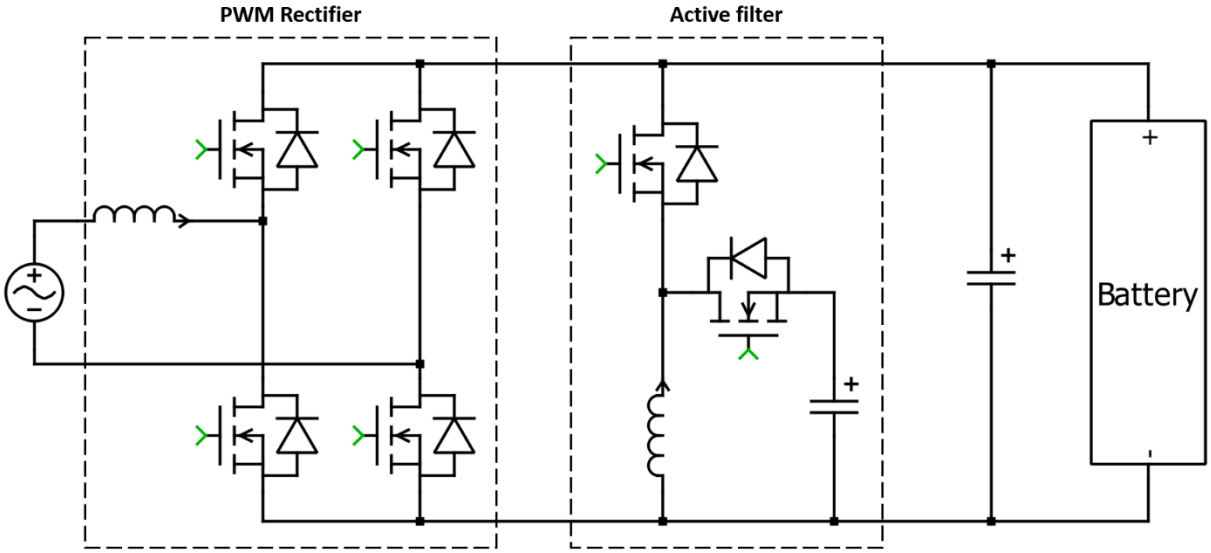

Figure 22 - Buck-Boost filter topology

For what concerns the working principle, it is basically the same as the one of the Buck and the Boost filters, hence it has the boost mode and the buck mode.

The filter will work in buck or boost mode depending on the voltage of the capacitor respect to the voltage of the DC-link. In this way the filter is able to compensate the ripple energy by continuously absorbing and releasing energy from the filter capacitor.

In the Buck-Boost converter topology the capacitance needed in order to eliminate the ripple can be calculated as:

$$C_s \geq \frac{2P_{r\_peak}}{(V_{c\_max}^2 - V_{c\_min}^2)\omega}$$

Eq. 27

where V_{c_max} and V_{c_min} are the maximum and the minimum capacitor voltage, ω is the angular frequency, and P_{r_peak} is the ripple peak power.

Differently from the buck and the boost topology, here V_{c_min} and V_{c_max} can be lower or higher than the DC-link voltage, therefore the voltage range in which the capacitor will work can be freely chosen without particular constraints.

The theoretical minimum capacity depends on the minimum and maximum voltage

admissible on the auxiliary capacitor, and assuming that the capacitor can swing between 600V and 900V, the needed capacitance is:

$$C_s = 173\mu F$$

In this configuration, since the working voltage of the auxiliary capacitor can be lower or higher than the one of the DC-link, the most suitable capacitor technology between Film and ceramic can be chosen.

The advantage of this topology is that the capacitor can work at lower or higher voltages respect to the DC-link, making possible to take advantage of a larger voltage swing of the capacitor. On the other hand, the main drawback is the voltage stress on the switches that is not the same as the bridge rectifier, since working in the boost mode, leads to higher voltages, therefore higher stress on the switches.

2.4 H-bridge Flying capacitor

Another commonly used topology that is analysed is the H-bridge Flying capacitor topology [10]. As shown in Figure 23 the auxiliary filter is a parallel topology since it is connected in parallel on the DC-link. The scheme is composed of an half bridge and a two capacitors leg connected by an inductor.

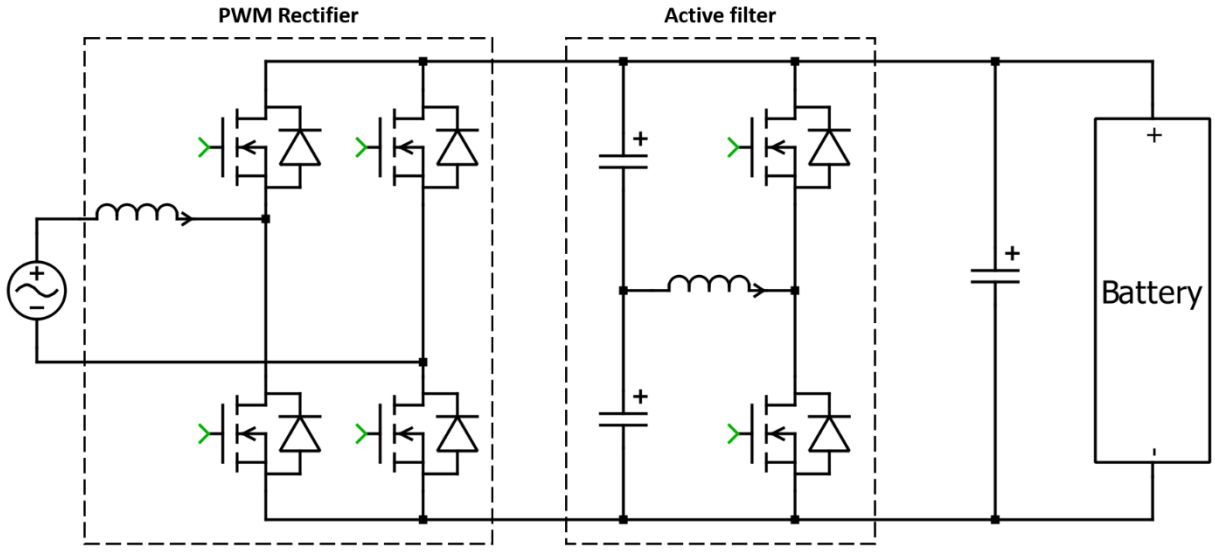

Figure 23 - H-bridge Flying capacitor topology

For what concerns the working principle, it is all based on the voltage of the two capacitors. The two capacitors are connected in series to reach the DC-link voltage and the central point is connected to the central point of the half bridge leg.

Using the two mosfets, the voltage on the central point between the two capacitor is changed in a sinusoidal way. When the lower capacitor charges, the other discharges, and vice versa.

In this way as all the other topologies the filter is able to compensate the ripple energy by continuously absorbing and releasing energy from the two capacitors.
For the H-bridge flying capacitor active topology, in order to calculate the minimum necessary capacity to eliminate the ripple the following equation can be used:

$$C_s = \frac{4P_{r\_peak}}{V_{c\_peak}^2 \omega}$$

Eq. 28

where V_{c_peak} is the peak capacitor voltage, ω is the angular frequency, and P_{r_peak} is the ripple peak power.
With Eq. 28 it is possible to calculate the total needed capacity, therefore the sum of the two capacitors. In this case it is assumed that the two auxiliary capacitors, completely charges and discharges every cycle and the voltage goes from 0 to a peak value called V_{c_peak}. In this configuration, the theoretical minimum capacity is:

$$C_s = 640\mu F$$

The main advantage of this topology is that the capacitors can work also if the active filter is disabled. This because they are directly connected to the DC-link in parallel and there are no switches in series. On the other hand, it can be seen that this topology is not so efficient for what concerns the capacitor requirements, since the smallest value of the capacity needed is normally 2 times larger than the theoretical minimum of the buck type.

2.5 Series stacked capacitor

Another commonly used topology that is analysed is the Series-Stacked capacitor topology [11]. As shown in Figure 24 the auxiliary filter is a parallel topology since it is connected in parallel on the DC-link. The scheme is composed of four mosfet that works as a bidirectional inverter that absorbs and releases the energy stored in the auxiliary capacitor in order to create a voltage swing on the series stacked capacitor.

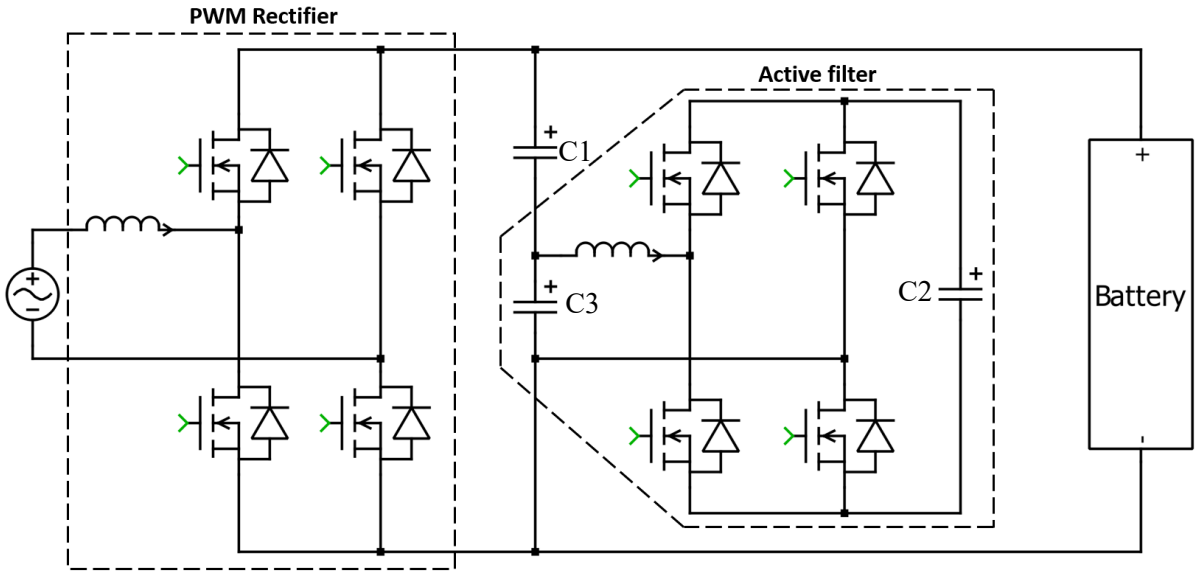

Figure 24 - Series stacked capacitor filter

The main focus of this topology is to use in a more intelligent way the capacitor C1. The idea is that, normally for having a low value of the ripple voltage on the DC-link, a big capacitor is needed, but is not fully utilized, only a small percentage of capacity is used. A solution is to make the capacitor be able to have a larger voltage swing (in the order of 20-30%). This is done by generating on C3 a voltage v_{ab} that is opposite respect to the one of the capacitor C1, hence this capacitor is free to oscillate of a certain value.

In this topology, different parameters must be chosen: *C*1, *C*2 that are the capacitance of the two capacitors and *Q*2,*init* that is the initial charge of capacitor *C*2. Therefore, the design constraint on the value of *C*1, *C*2 and *Q*2,*init* is:

$$\begin{cases} \left| \dfrac{-Q_{2,init} + \sqrt{Q_{2,init}^2 - 4\Delta q_1^2 \dfrac{C2}{C1}}}{2\Delta q_1} \right| < 1 \\ Q_{2,init}^2 - -4\Delta q_1^2 \dfrac{C2}{C1} > 0 \end{cases}$$

Eq. 29

Simplifying the second equation results in:

$$\frac{1}{2}C_2V_{C2,init}^2 > 4 \cdot \frac{1}{2}C_1\Delta v_{C1,max}^2$$

Eq. 30

This result indicates that the auxiliary capacitor *C*2 needs to have enough initial energy at the beginning of each cycle such that it is larger than 4 times the maximum energy change on *C*1 (determined by the load current) within a cycle. This can be ensured by sufficient capacitance of *C*2 and proper precharge during system startup.

Simplifying the first equation results in:

$$\frac{C2}{C1 + C2}V_{C2,init} > |\Delta v_{C1,max}| = |\Delta v_{C3,max}|$$

Eq. 31

This means that the smallest value of v_{C2} has to be larger than the maximum ripple of v_{C3}.

To simplify calculation the two equations above can be simplified as:

$$\sqrt{C_1C_2}V_{C2,init} \geq 2|\Delta q_{1,max}|$$

Eq. 32

$$\frac{C_1C_2}{C_1 + C_2}V_{C2,init} > |\Delta q_{1,max}|$$

Eq. 33

where $\Delta q_{1,max}$ is a known and determined by the load. The parameters *C*1, *C*2, and $V_{2,init}$ need to be selected taking into account the previous constraints in the design. Indeed, it can be derived that the first equation holds as long as the second equation is satisfied and in practice:

$$\frac{C_1C_2}{C_1 + C_2}V_{C2,init} > |\Delta q_{1,max}|$$

Eq. 34

is a sufficient design constraint for the design of the parameters.

The main advantage of this topology is that the series-stacked capacitor blocks the majority of the DC bus voltage leading to a reduction on the voltage stress on the buffer converter. This means that lower voltage rating mosfets can be used leading to a higher efficiency.

Moreover, the series passive capacitor compensates most of the ripple power since it can have a large voltage swing. In this way only a small portion of the ripple will be processed by the active filter leading to a reduction in volume and an increased efficiency.

2.6 Series capacitor

Another commonly used topology that is analysed is the series capacitor filter [12] [13]. As shown in Figure 25 the auxiliary filter is a series topology since it is connected in series on the DC-link. The scheme is composed of four mosfet that works as a bidirectional inverter that absorbs and releases the energy stored in the auxiliary capacitor to create a voltage swing on the series capacitor.

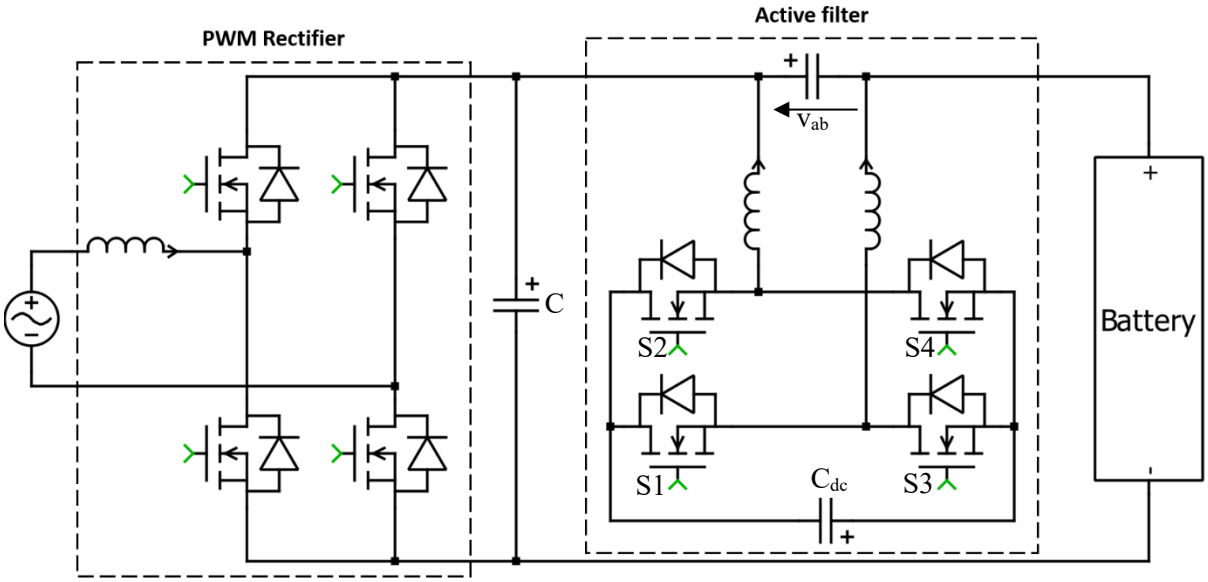

Figure 25 - Series capacitor

In the series active buffer filter the scope is to divert all the ripple energy into the capacitor by means of a full bridge inverter. In this case, since it is in series, only the residual ripple voltage that remains after the DC-link capacitor filtration must be compensated. Since the system is a voltage generator that generates a voltage V_{ab} across the series capacitor, in the best case, it is necessary to charge and discharge the auxiliary capacitor with a voltage that is exactly equal to the ripple voltage of the DC-link. Normally a safety margin is set in order to withstand possible load changes, and also to increase the hold-up time.

The design of the DC-link capacitance C is a compromise between the allowable voltage level of the average capacitor voltage, and the stress on the auxiliary capacitor and the mosfets S1-S4. A smaller value of C requires higher voltage ratings of C_{dc} and S1-S4.

In order to calculate the necessary capacitance $C_{dc,min}$ needed to eliminate the ripple voltage on the DC-link bus, the following formula can be used:

$$C_{dc,min} = \frac{I_s S_b}{2\omega^2 C_{dc} V_{b,0}^2 V_{dc,0}}$$

Eq. 35

where $V_{dc,0}$ is the RMS value of the DC-link voltage, $V_{b,0}$ is the RMS value of the bias voltage applied to the buffer capacitor, S_b is the apparent power, I_s is the DC-link current and ω is the angular frequency of the grid.

An important parameter to take into consideration when dimensioning the capacitance is the modulation index of the full bridge inverter that in some papers is maintained between 0.35 and 0.65.

For everything said before, this kind of topology is quite complex, both from the control point of view, but also regarding the number of components employed.

2.7 Selected topology comparison

In Table 3 a complete comparison between all the selected topology is done [14].

The first parameter taken into consideration is the topology of the filter, that can be series, series stacked, or shunt (parallel).

Then the number of components needed for the active filter is analysed pointing out the number of mosfets, the number of capacitors and the number of inductors.

Another parameter analysed is the device stress where for device it is intended the mosfets, capacitor and inductors. If the voltage stress is equal to $V_{DC\text{-}link}$ the mosfets has the same rating of the rectifier switches, and the capacitor work at lower voltage respect to the DC-link voltage. On the contrary if the voltage stress is higher than $V_{DC\text{-}link}$ both the mosfets and the capacitors must have higher voltage rating respect to the rectifier switches. Lastly if the voltage rating is lower than $V_{DC\text{-}link}$ all the components work at lower voltage respect to the DC-link.

Regarding the device current stress, this indicates the current that flows through the filter. In all the parallel or series stacked topologies, the only current that flows is the ripple one. On the other hand, in the series topologies, since they are connected as shunt, both ripple current and DC current will flow through them leading to a lower efficiency.

Filter topology	**Type**	**Number of mosfets**	**Number of capacitors**	**Number of inductors**	**Device stress**	
					Voltage	**Current**
Buck	Shunt	2	1	1	$V_{DC\text{-}link}$	$i_{2\omega}$
Boost	Shunt	2	1	1	$> V_{DC\text{-}link}$	$i_{2\omega}$
Buck-Boost	Shunt	2	1	1	$> V_{DC\text{-}link}$	$i_{2\omega}$
H-bridge Flying capacitor	Shunt	2	2	1	$V_{DC\text{-}link}$	$i_{2\omega}$
Series stacked capacitor	Series stacked	4	2	1	$< V_{DC\text{-}link}$	$i_{2\omega}$
Series capacitor	Series	4	2	2	$< V_{DC\text{-}link}$	$I_{dc} + i_{2\omega}C_{ab}/C_f$

Table 3 – Selected topology comparison

3. Proposed filter structure

After a deep analysis of all the topologies present in literature, the choice has fallen on the buck topology. For this reason, a brief introduction with some considerations about the boost topology, that was the second choice after the buck converter will be held in the next section.

3.1 Boost topology considerations

A first analysis has been done on the boost converter since on paper, due to the topology it seems a good candidate. The main advantage that emerges is the position of the inductor filter. Indeed as it can be seen in Figure 26 the inductor is directly connected to the DC-link, and there are no mosfets between them. This means that the current is always filtered from the inductor, leading to a lower switching ripple on it.

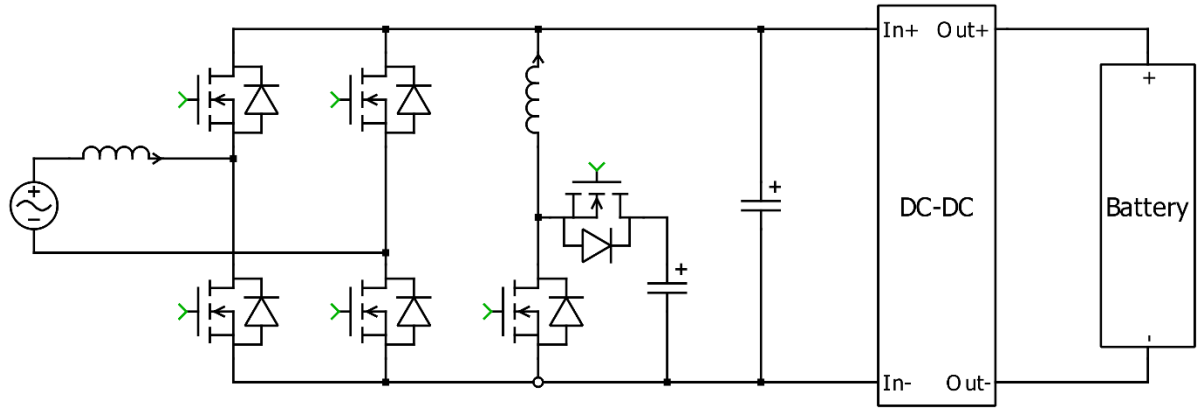

Figure 26 - Battery charger with boost topology filter

On the other hand, there are a lot of drawbacks related to this topology. The first one is that since it is a boost converter, it will work at a higher voltage respect to the one of the DC-link. This leads to the need of a higher voltage rating of the mosfets of the filter.

In addition, also the filter capacitor needs to have a high rating in terms of voltage, and in most cases this is an advantage in terms of energy density, but limits the filter to use Film capacitors and not ceramic capacitors due to the low voltage rating.

Another big problem is related to how the leg of the power module is attached to the DC-link. As it can be seen in Figure 26 the leg is not directly connected on the DC-link as the other legs of the rectifier, but is connected on one side, and the other side is connected to a capacitor. This is not the best thing from the industrialization point of view for two reasons: the first one is related to the loop inductance that is not optimized in this topology. The second and more important one is that since different power modules are needed a specific cooling must be designed leading to a complexity increase.

The last bad aspect of the boost topology is related to the gain. Eq. 36 shows the gain of the two

filter topologies and as it can be seen, the buck gain has a linear relation with respect to the duty cycle. On the other hand, the boost gain has a completely different response that is not linear.

$$G_{buck} = d \qquad G_{boost} = \frac{1}{1-d}$$

Eq. 36

This is confirmed by looking at Figure 27 where the buck and the boost ideal gain are plotted. In the buck case the gain is perfectly linear and starts at 0 when the duty cycle is 0 and ends at 1 when the duty cycle is 1.

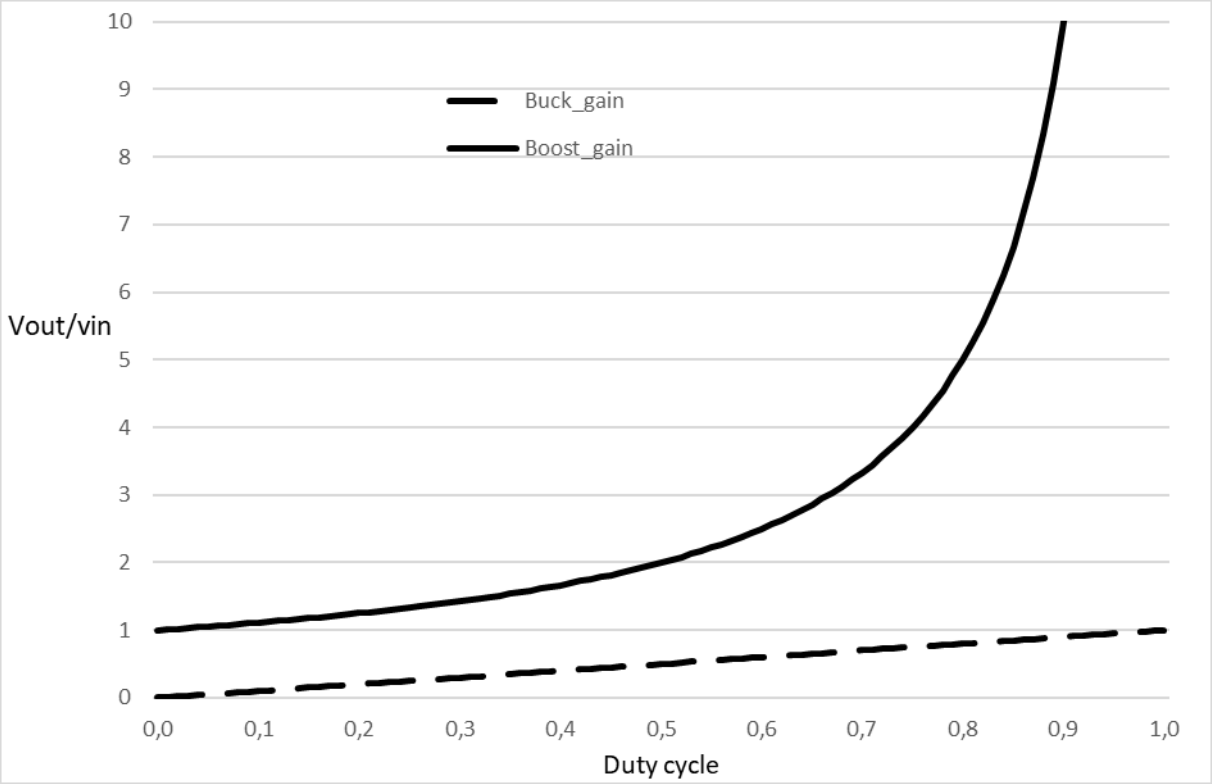

Figure 27 - Ideal buck and boost converter gain

Instead, the boost converter has a diverging behaviour, since when the duty cycle tends to 1, the gain tends to infinite. All those considerations are done for the ideal boost, hence if a real boost is considered, the gain will not be able to go to infinite, but it will surely grow a lot. This means that the boost topology is an unstable topology itself, and an error in the control of the duty cycle could lead to really high voltage on the filter capacitor.

For all the reasons previously mentioned, the buck topology has been preferred over the boost one. More information regarding the buck topology are given in the following sections.

3.2 Buck consideration and analysis

The reasons for which the buck topology has been selected will be deeply discussed below. The first important consideration that can be done is regarding the filter mosfets rating. Indeed, since the buck lowers the voltage of the DC-link, the mosfets of the filter will be exactly equal to the ones of the rectifier. This means that all the battery charger could be constructed with the same power modules and this has an advantage especially in terms of industrialization since it simplifies the overall circuit. In addition, also from the cooling point of view there are advantages. Indeed, having all the power modules equal leads to a uniform design, and the cooling system could be created for both the rectifier and the filter.

A further advantage that this topology introduces is a low loop inductance. Indeed, as shown in Figure 28 where the complete battery charger is present, the three legs of the battery charger, two from the rectifier and one from the filter are exactly equal, hence they could be placed really near to each other minimizing the loop inductance.

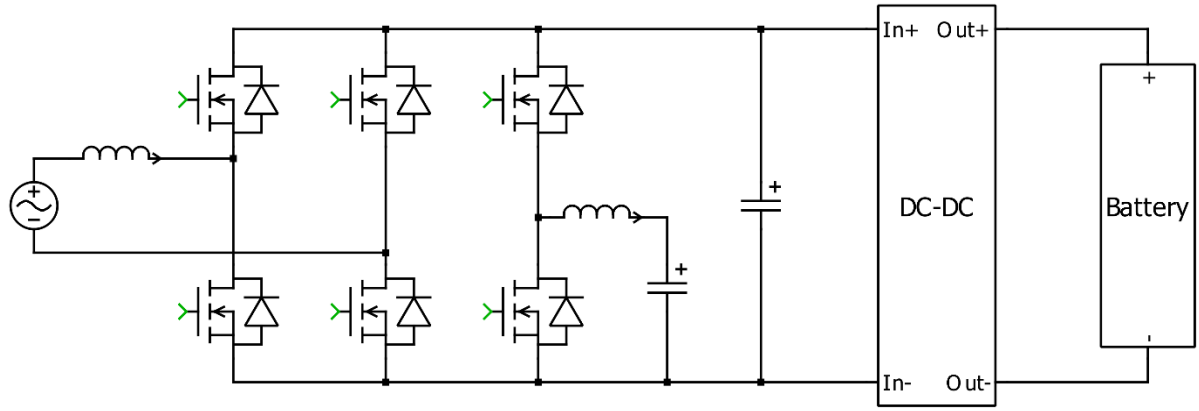

Figure 28 - Battery charger with buck filter topology

Another advantage of this topology is the voltage rating of the filter capacitor that since it is essentially a buck converter, the voltage on the filter will always be lower respect to the voltage of the DC-link. This implies that both Film capacitors and ceramic capacitors can be used. The last advantage respect to the boost topology is the open loop stability of this filter. As already mentioned before and as shown in Figure 27 the buck topology is stable itself also without control. This is a big implication, since all the duty cycle can be fully utilized without any instabilities.

For what concerns the working principle of the buck filter topology in Figure 29 and in Figure 30, the filter and the current are showed. As it can be seen, the filter is connected in parallel on the DC-link and in the top part a current node is present. There are three currents, an input current, a filter current and an output current. Those three currents are plotted in Figure 29. It can be seen that the input current I_{in} is the current that comes from the rectifier circuit. This

current is a pure sine with an offset equal to its amplitude. In this way it has a mean value equal to its amplitude, and it goes from 0 to a peak value. The second current shown is the filter current I_{fil} that is the current generated by the buck filter. Also this current is a pure sinusoid with an average value equal to 0 and an amplitude equal to the average of the input current. If the two currents I_{in} and I_{fil} are summed, the current I_{out} is obtained. In theory the output current is a perfectly constant value equal to the average of the input current.

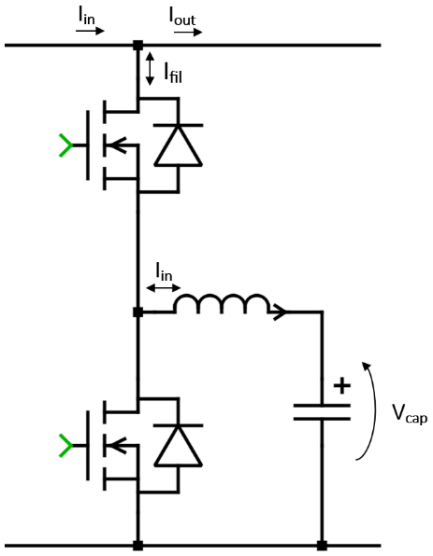

Figure 30 - Buck filter currents

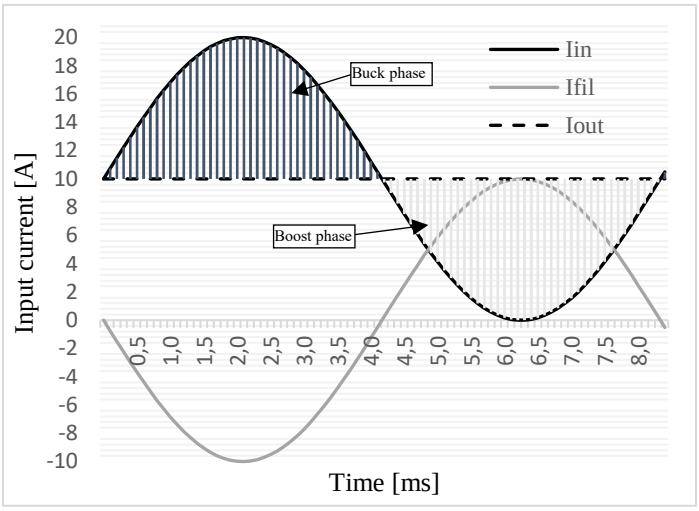

Figure 29 - Current analysis

From all the consideration done above, and as showed in Figure 29 it can be understood that the filter has two working modes, a buck and a boost mode. In the buck mode it lowers down the voltage from the DC-link value to the target value and absorbs current (energy) from the DC-link charging the auxiliary capacitor. In the boost mode, it boosts up the voltage of the capacitor to the voltage of the DC-link and injects current and releasing the energy stored in the capacitor. Doing this, the ripple power that comes from the rectifier is completely compensated by the active filter with a really high efficiency. The only losses that the filter has are represented by the switching and conduction losses of the mosfets and the losses related to the equivalent series resistance of the capacitor and inductor.

3.3 Power module dimensioning

The power module dimensioning is a challenging task to perform. This because a lot of different factors must be taken into consideration, such as RMS current that flows through the leg, the voltage rating, the switching frequency and the cooling system. Also the technology of the module must be chosen.

Starting from the technology and the voltage rating, since the filter will work up to 900V that is the maximum voltage of the DC-link, a perfect choice is to use a 1200V SiC power module.

The choice falls on SiC especially due to the high switching frequency, that is of 100kHz in this application.

Regarding the current rating, it is more difficult to give a precise value since it depends on a lot of factors such as RMS current and cooling type. Since this is still a prototype, and it could vary a lot in the future developments, a good rule of thumb is to pick a module with a current rating that is double the RMS current. In the case in exam, the current is in the order of $30A_{RMS}$. If the 2 times current rule is used, the rating must be of at least 60A. However, if also the peak current is taken into consideration, the module must withstand $120A_{peak.}$

In depth analysis should be done in order to optimize the power module, by analysing the switching and conduction losses of the module and the used cooling in order to understand how much power could be dissipated. However, it is not on interest of this work since the main scope is to verify the working principle of the active filter, and not to optimize it.

For all the previous considerations, the ratings of the used mosfet are summed up in the table below.

Feature	Value
Voltage rating	1200 V
Current rating	60 A_{RMS}
Peak current	120 A_{peak}
Working frequency	100 kHz
Technology	SiC

Table 4 - Power module ratings

3.4 Inductor dimensioning

The design of the inductor is an important task since it is a critical component of the filter. Depending on its value, the filter will work in CCM or DCM.

In the case of the proposed filter, it has been decided to work in a particular mode, that is really similar to the CCM mode. Indeed as shown in Figure 32 and in Figure 33 it could be noticed that the current flows continuously through the inductor, hence it could be thought as CCM, but the current is never only negative or only positive as in a normal CCM mode, but it changes sign continuously. This is due to the fact that the filter is a synchronous buck, and for this reason also the negative current that goes back can be controlled. This specific choice of working mode has been done in order to move away as much as possible the resonant peak that the LC filter of the buck have.

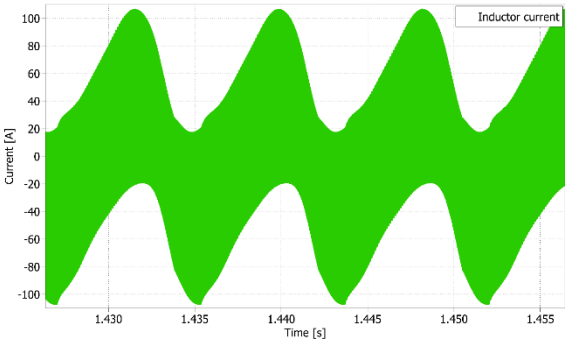

Figure 32 - Inductor current

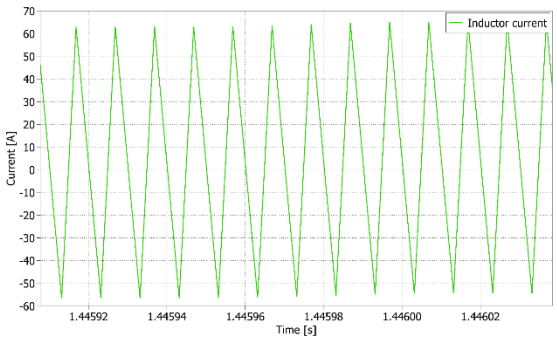

Figure 33 - Inductor current detail

This can be appreciated in Figure *31* where different magnitude and phase response are plotted varying the filter inductance L between 15uH and 75uH. In particular, it is quite clear that increasing the inductance value, the resonance peak moves to the left, thus it gets close to the working point of the filter, since the ripple harmonics that the filter must compensate are at 120Hz and multiple of it.

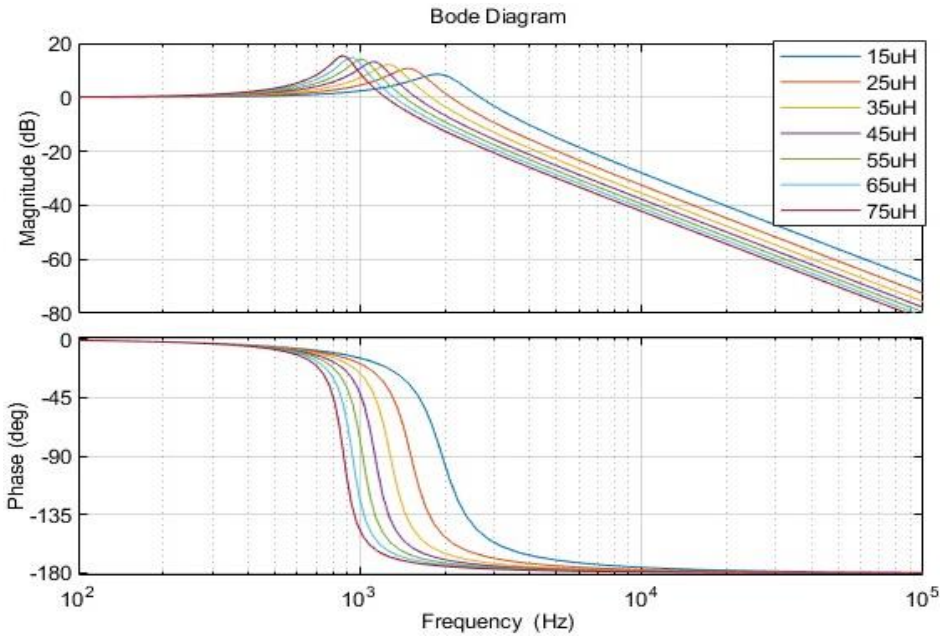

Figure 31 - Bode plot of LC filter response

As it can be seen in Figure *31*, choosing a big inductance around 75uH, means to have a resonance peak of the LC filter centred at 870Hz. This is close to the working point of the filter since in works at 120Hz, 240Hz and so on until around 720Hz. Working near to the resonance peak, implies to have an instable filter response since it is hard to create a controller that is able to compensate for that resonance. On the other hand, having a big inductance means to have smaller switching ripple current, leading to a better DC-link ripple elimination.

Choosing a small inductor of 15uH, the resonance peak moves to the right and it is centred at around 1.9kHz. This means that the filter works quite away from the resonance peak leading to

a better controller response. On the other hand, a smaller inductor leads to a higher switching ripple current.

All the problems related to the resonance, are amplified if the dead time on the two mosfets of the leg is introduced. For this reason, the best trade-off between stability of the filter and switching ripple current has been found by selecting as inductance value a 15uH inductor. If a solution for compensating the dead time is found, a bigger inductor can be selected, making possible to work in CCM, thus reducing the current ripple leading to lower stress on all the components of the filter.

3.5 Capacitor dimensioning

The capacitor dimensioning is a really important task since from this component depends the overall volume of the filter. The choice of the capacitance value depends on different parameters such as current, voltage, temperature rating and life duration.

Starting from the current, depending on the choice of the capacitance value, the current will vary as in Figure 20. This implies that the larger the capacitor the lower the current. If the 400uF case is analysed, it is clear that the maximum current is around 40A, and it has a more sinusoidal trend. Talking about the voltage, the lower the average voltage value on the capacitor, the larger will be the voltage swing on the capacitor since it will charge and discharge more. It has been chosen to work at about 370V in order to optimize the problems related to the dead time that will be explained later.

Depending on the value of the capacitor, the larger the capacitor the lower will be the voltage swing if the peak voltage is maintained constant, and this can be appreciated in Figure 19.

As before, if the 400uF capacitor is analysed, it can be seen that it has a good compromise between voltage swing and capacitance value.

For all the previous consideration it has been decided to take at least for the prototype, a capacitor of 400uF with a voltage rating of 550-600V.

Talking about the technology of the capacitor, the only possible choice in order to withstand the requirements in terms of life duration are Film and ceramic capacitors. Those two types of capacitors have also quite good behaviour at high temperature.

For the prototype, Film capacitors have been chosen mostly for assembly reasons and lower cost.

3.6 Active filter control scheme

In this chapter the proposed control scheme for the active filter is exposed and analysed in all his components.

A lot of different control scheme are present in literature. They differ between each other in terms of the controller type, that can be a Proportional Integral (PI), a Proportional Resonant (PR) a repetitive control and so on, for the measured parameters on which the controller is based and for the duty cycle generation technique. Two of them are particularly interesting [15] [5], because both are based on proportional resonant controllers.

An overview of the proposed control is present in Figure 34. As it can be seen, there are three main components: the DC offset block, the PR block and the PI block.

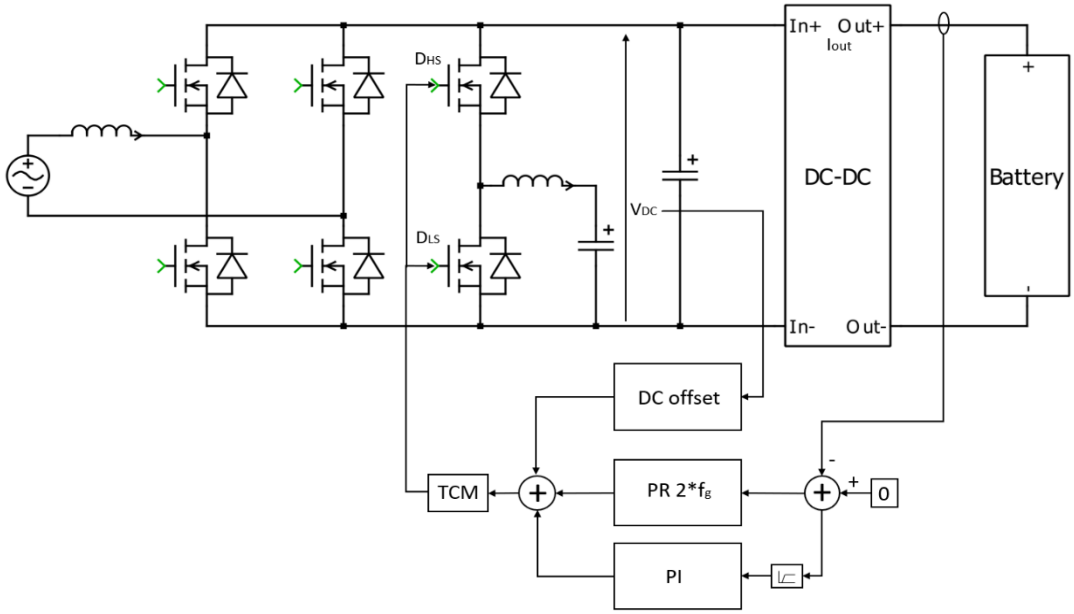

Figure 34 - Proposed control scheme.

For what concerns the measurements needed for the controller, those are two and consist of the measure of the voltage and the current of the DC-link. The measurement of the current is done by inserting a series hall effect sensor in the output of the DC-link before the battery. The measurement of the voltage instead is done by measuring with a voltage divider the DC-link voltage.

3.6.1 DC offset calculation block

Talking about the blocks that compose the controller, if the first DC offset calculator block is analysed, it will be easy to understand that is a simple duty cycle calculator. For doing this a simple division is performed as in Figure 35.

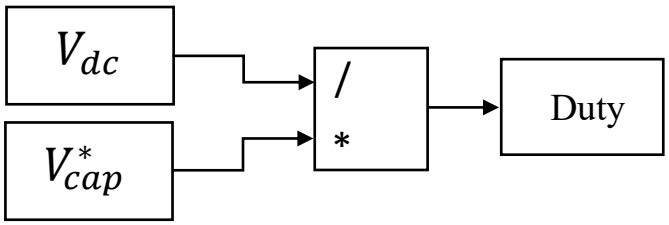

Figure 35 - DC offset duty calculator

The offset signal is used in order to guarantee a constant average voltage on the auxiliary capacitor. The target average voltage is V_{cap}^* that in study will be around 370V. A division is performed as:

$$Duty\ offset = \frac{V_{cap}^*}{V_{dc}}$$

Eq. 37

This is exactly equal to the buck duty cycle formula. In this way a static duty cycle is calculated and given to the buck filter.

The exposed structure is really simple and require only a division, but it has a limitation because there isn't any feedback control on the real average voltage of the auxiliary capacitor. A more complex control could be created by measuring the voltage of the capacitor and controlling it using a PI controller. The PI will be feed by an error that is the difference between the averaged measured capacitor voltage and the reference capacitor voltage. Doing this, the capacitor average voltage is perfectly tracked and set to the desired value. The main drawback respect to the previous control is related to the computational complexity that in this case is obviously higher.

3.6.2 PR controller

The PR block is composed by multiple PR controller that run in parallel and are tuned at different resonant frequencies.

In the case under examination, the controller must compensate a double line frequency ripple, that is a sinusoidal signal. The PR controllers are perfect choices when a sinusoidal signal must be tracked and compensated. The transfer function of a continuous time PR controller is shown in Eq. 38:

$$G_s(s) = \frac{2K_i\omega_{cut}s}{s^2 + 2\omega_{cut}s + \omega_0^2}$$

Eq. 38

As it can be seen from the previous equation, the parameter that must be set are ω_0, K_i and ω_{cut}. ω_0 sets the resonant frequency at which the controller works, and in this case, it is the double line frequency of 120Hz. For what concerns K_i, this represents the gain of the controller, and varying it, the magnitude will change as in Figure 36 [16].

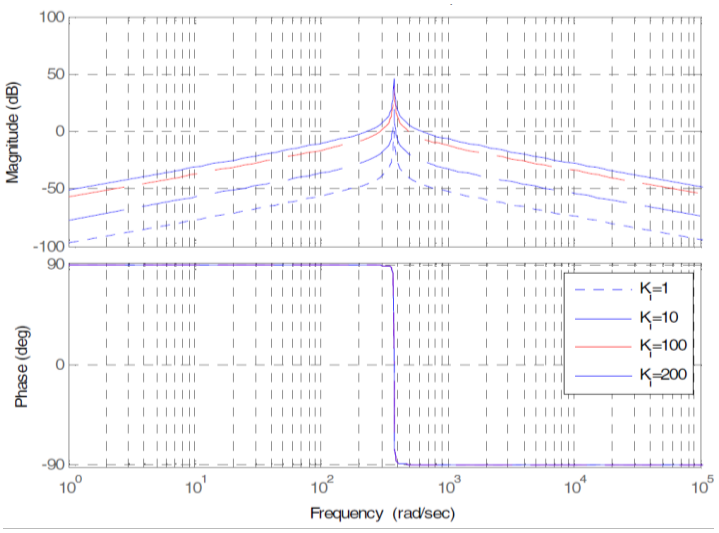

Figure 36 - Frequency response when K_i changes

Regarding ω_{cut}, this parameter sets the bandwidth of the controller at resonance frequency. Increasing ω_{cut} will increase the bandwidth of the controller, and the results are shown in Figure 37 [16].

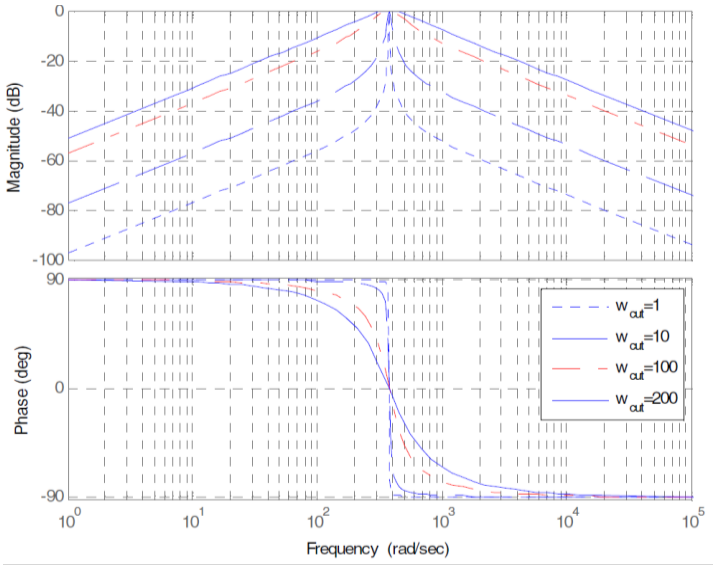

Figure 37 - Frequency response when ω_{cut} changes

The structure of the PR block is shown in Figure 38. The first step that is performed by this block, is to generate the signal that must be compensated by subtracting the DC-link current from the reference ripple current value, that is 0. Then a gain of -1 is present only to invert the sign of the signal to be tracked.

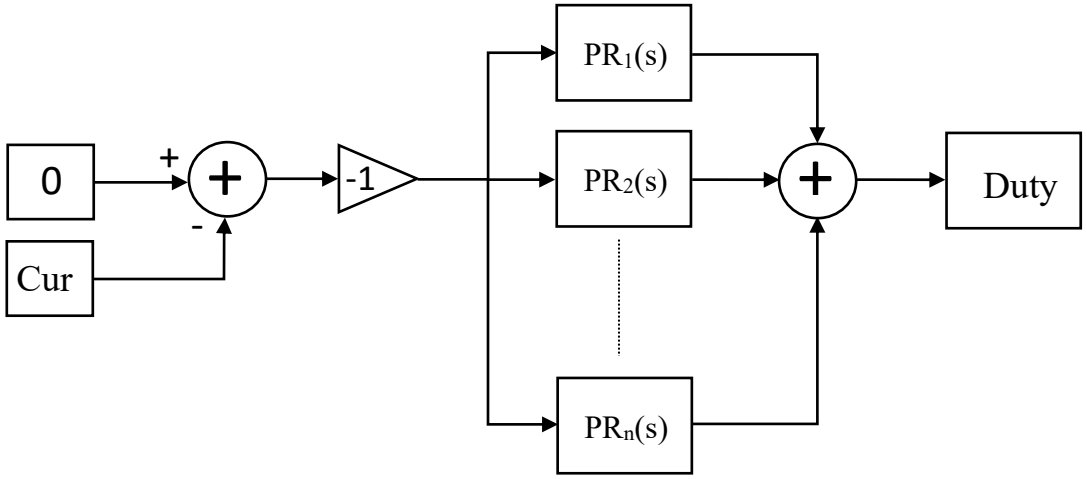

Figure 38 - PR block

A high pass filter that takes away the continuous time signal is not needed since the PR controller is a passband filter itself and will cut away automatically the continuous component of the signal. After that, the signal that must be compensated goes to different PR controllers that are connected in parallel. Each of them is tuned at a multiple of the double line frequency, Therefore the first one is at $1 \cdot 2\omega$ (that in the case under exam is 120Hz) the second one at $2 \cdot 2\omega$ (that is at 240Hz) and so on.

For what concerns the use of the PR controller, this choice has been done since it is one of the best controllers in terms of performance when dealing with sinusoidal signals. Indeed, if a PI controller was used instead, the performance were not the same. This because the PI controller is not created to track and control a specific frequency band but has a larger bandwidth and slower response.

3.6.3 PI controller

The PI block implements a PI controller that in this case is used in order to compensate for the harmonics introduced by the dead time. Indeed, in the ideal case in which the two mosfet of the filter behaves in an ideal way, switching ideally without a dead time between the two, this block is useless since no harmonics are present. But in real case, when dealing with dead time, this introduces higher order harmonics that the PR block is not able to compensate. For this reason, this block has been implemented.

As it can be seen in Figure 39 the first thing that this block does is to generate the error that must be compensated by the PI. This is done by firstly taking away the continuous time component from the DC-link current using a low pass filter. Then it generates the real error that must be compensated by subtracting the obtained signal from the reference value that is 0 since the scope is to put the ripple to 0. Then a gain of -1 is present only for changing the sign of the

signal. The generated signal is then feed to the PI controller that will generate the desired duty cycle.

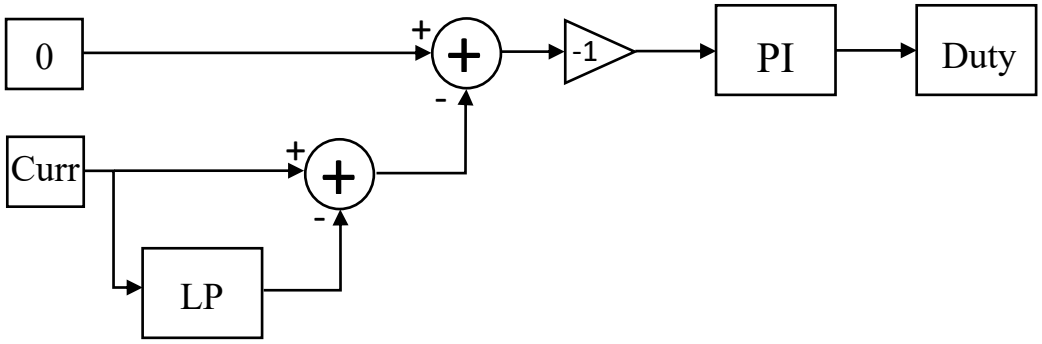

Figure 39 - PI controller

4. Software simulator

For what concerns the simulator, since the scope of this study is only to validate the functionality of the active filter, as simulation software it has been chosen PLECS from Plexim. For this reason, a complete simulator of the battery charger has been built in order to verify the working principle of the filter from a qualitative point of view.

The only component that has not been implemented is the PFC rectifier, since it was not of interest in this project.

4.1 Buck active filter simulator (DT)

All the simulator has been designed to run in discrete time in order to be as similar as possible to the real physical battery charger. The simulation step is fixed to $10^{-6}\ s$.

In Figure 40 the complete battery charger is shown with all the blocks that compose it. Starting from the right, the first block represent the PFC rectifier, that as it will be explained later, it is not a real rectifier, but is only a reproduction of the signal of a rectifier.

Then the active filter is connected in parallel on the DC-link, together with the passive DC-link capacitor.

After those two components, the fixed ratio DC-DC converter is present and is connected in series on the DC-link.

The last component is represented by the battery. This block reproduces a simplified model of a lithium battery.

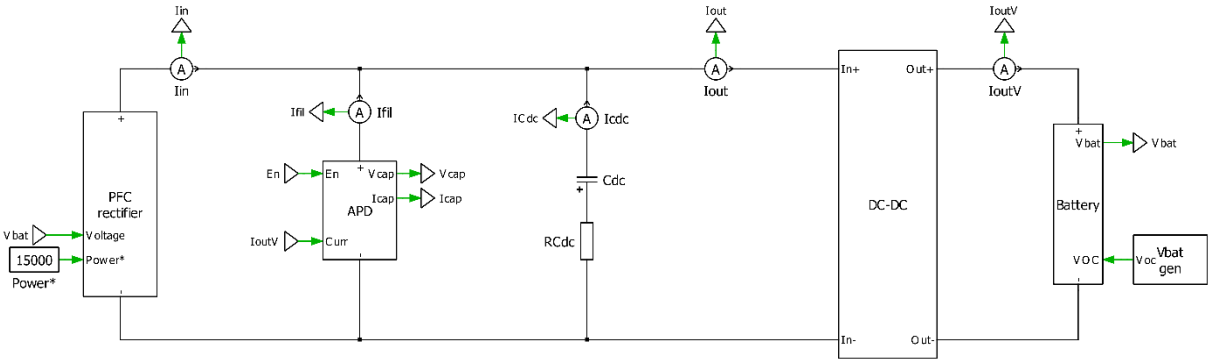

Figure 40 - Complete battery charger simulator

4.1.1 PFC rectifier

As mentioned before, since it is not in the interest of this study, and in order to simplify the simulator, the PFC rectifier part has not been implemented in real terms using switching elements and a controller, but it has been done by reproducing the waveform generated by a PFC rectifier as in Figure 41.

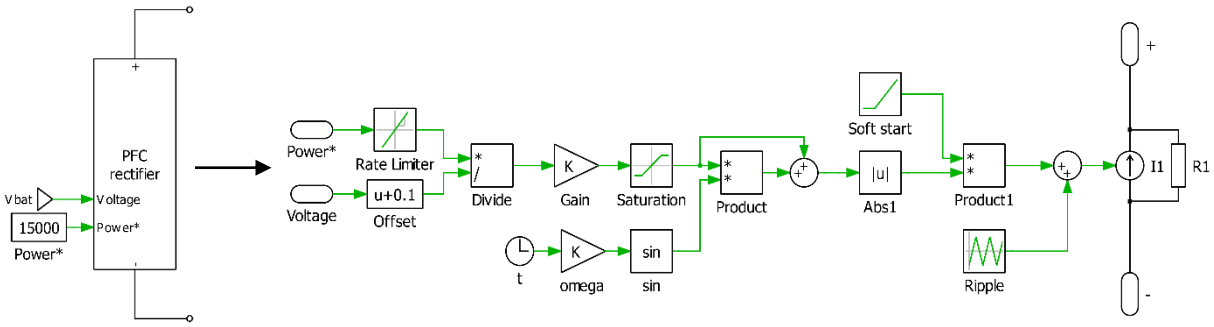

Figure 41 - PFC rectifier block

As explained in previous chapters the PFC rectifier will not have a target on the voltage, since it is directly connected to the battery, therefore the battery will impose the voltage. The rectifier will only have a target on the current that it must generate as output. The current target depends on the power value at which the battery must be charged, and in the simulator this power is set as a variable. From the target power and from the voltage value of the DC-link, that as said before is imposed by the battery, the block in Figure 41 calculates the amplitude value of the current that the rectifier must produce.

At the end, there is a controlled current source generator that will give as output the reconstructed current signal that a real PFC rectifier would give. This can be seen in Figure 42 and in Figure 43 and as it can be noticed it is a sinewave with an offset equal to half the amplitude, hence it goes from 0 to the peak value. In addition, a switching ripple can be added in order to simulate the ripple introduced by the 100kHz switching rectifier.

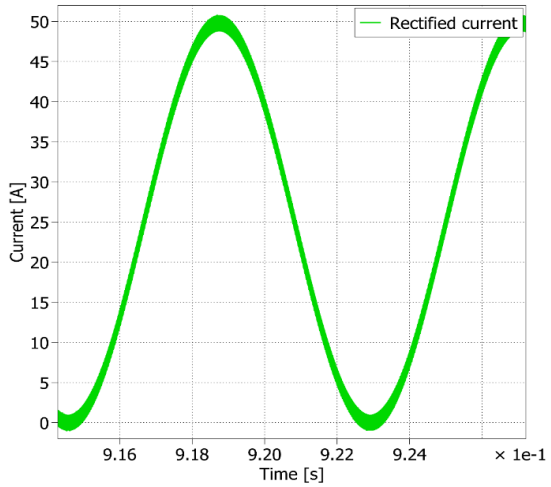

Figure 42 - Rectified current

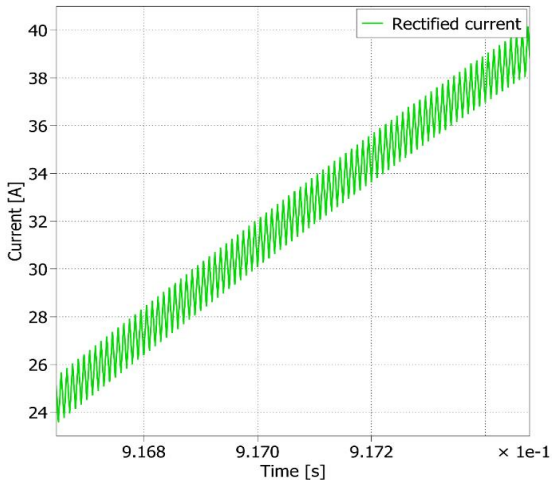

Figure 43 - Rectified current detail

4.1.2 Battery

The battery block of the simulator shown in Figure 44 reproduces a High Voltage (HV) lithium battery pack that has a minimum voltage of 600V and a maximum voltage of 900V.

It is created by using a controlled voltage source that can be changed manually and a series resistance that reproduces the internal resistance of the battery. The voltage of the battery can be changed manually by setting it as a constant. In addition, a rate limiter is added in order to avoid making step voltage changes.

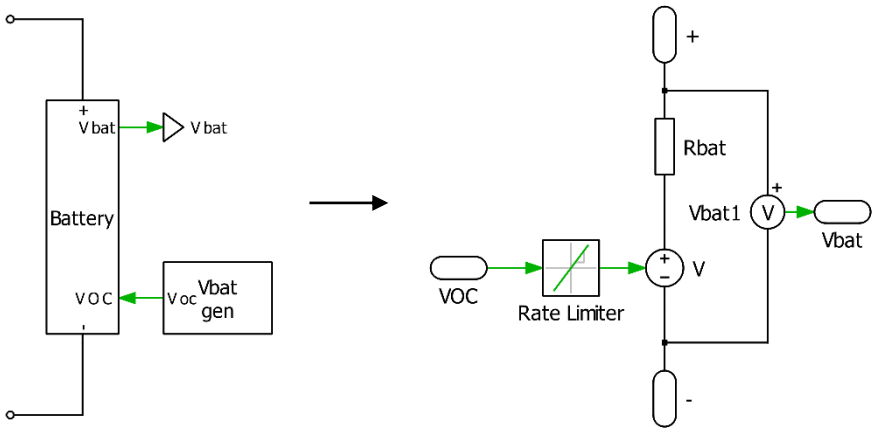

Figure 44 - Battery block

4.1.3 DCDC Converter

As for the PFC rectifier, also the DC-DC converter is not of interest in this work. For this reason, it has not been reproduced in a real way using switching elements and a controller, but it has been modelled as a simple LC low pass filter as shown in Figure 45. This has been possible since in reality the DC-DC converter is a 1 to 1 converter with a passband width of around 150kHz. Therefore, the LC filter reproduces the bandwidth of the filter. Obviously, this is a simplification, but this doesn't change the behaviour of the active filter.

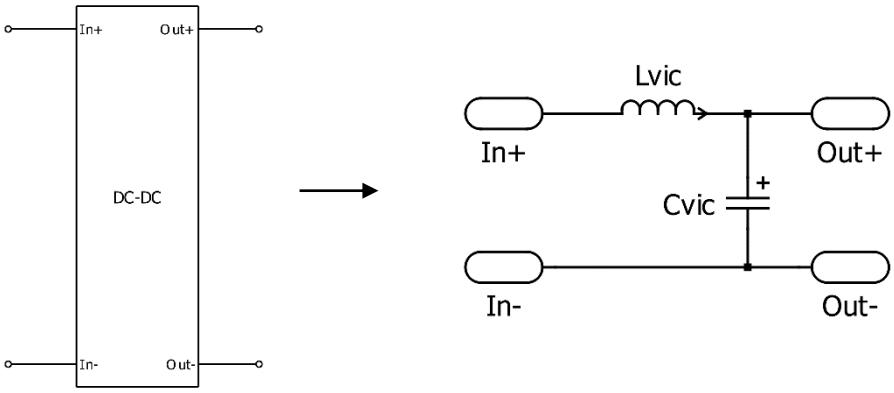

Figure 45 - DCDC converter block

4.1.4 Active filter

This subsystem is the core of all the simulator because it reproduces the active ripple eliminator filter. As shown in Figure 46 it is connected in parallel to the DC-link and is positioned between the PFC rectifier and the DC-DC converter. In this case the filter reproduces a Buck topology.

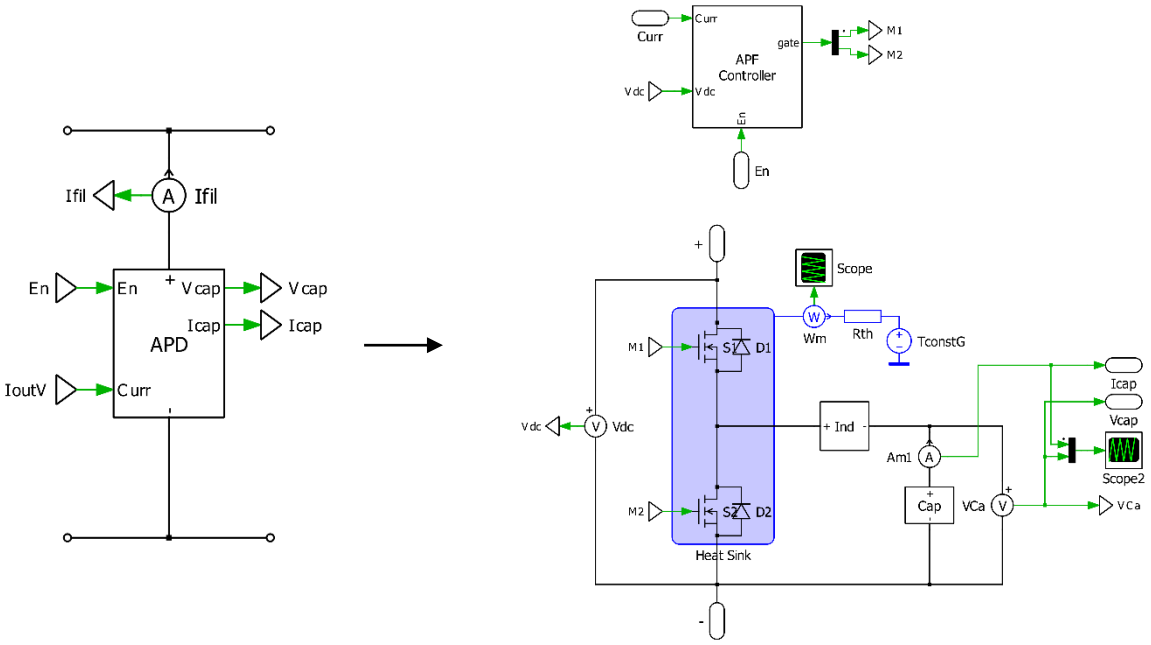

Figure 46 - Active filter block

It can be seen that there are two mosfet connected in series appended to the DC-link, and on the midpoint of the leg, an inductor and a capacitor are connected in series.

All the passive components have been simulated reproducing a real model of them. For example, the capacitor is composed by a capacitor, a series resistance and a series inductance. Also the two mosfet have the real model integrated in the component, hence the switching losses and the conduction losses are evaluated.

4.1.5 Capacitor and inductor

The capacitor has been modelled as a real capacitor. This has been possible since the real physical capacitor has been analysed with an impedance analyser. Indeed, thanks to the instrument, it has been possible to extract an equivalent circuit with all the parameters that characterize it. For this reason, since four capacitors connected in parallel are present, in the simulator four different capacitors have been modelled. In order to reproduce a real capacitor response, each capacitor has been modelled as a capacitor with an inductor and resistor in series. For what concerns the inductor, also in this case it has been modelled as a real inductor, hence a resistor has been added in series to the inductance in order to model the losses in the inductor. The result is shown in Figure 47 and in Figure 48.

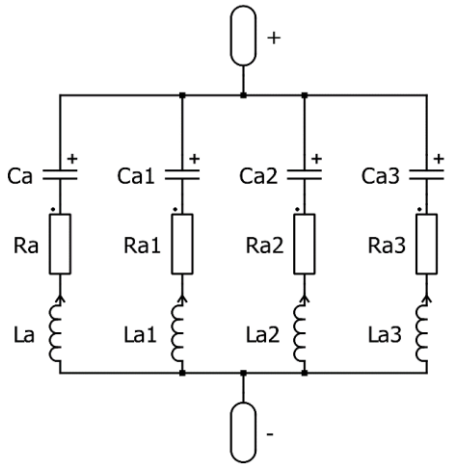

Figure 47 - Real capacitor model

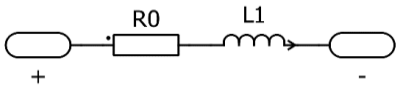

Figure 48 - Real inductor model

4.1.6 Control scheme

This is the main block that incorporates all the controllers of the active filter in order to generate the PWM signals for both the mosfets.

In order to work, it gets as input the DC-link current, the DC-link voltage, and an enable signal that is used to enable and disable the PR controllers and the PI controller.

As shown in Figure 49 inside this block, two main blocks that are triggered systems are present. The first one called *DC calc,* is in charge of calculating the DC offset duty cycle needed in order to maintain a constant DC voltage on the capacitor of the active filter.

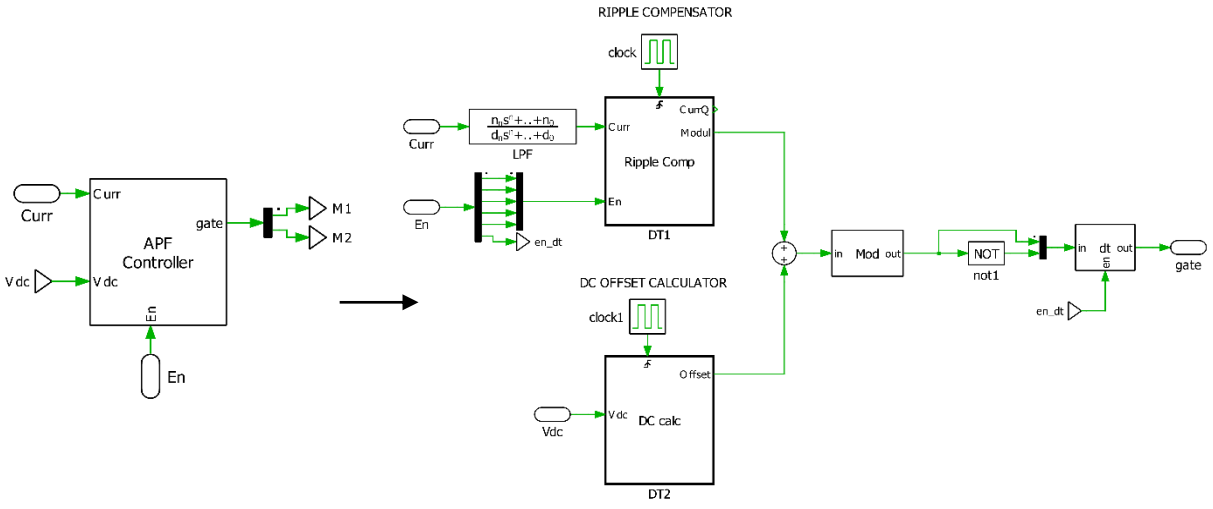

Figure 49 - Control scheme

The second block called *Ripple comp* is in charge of calculating the duty cycle for compensating the ripple on the DC-link. To get a deeper view, in Figure 50 the contents of the *Ripple comp* block are shown.

Two main blocks are present, the PR block, that contains the PR controllers, and the PI block that contains a PI controller in order to compensate the residual remaining ripple.

Using both controllers, this block generates a modulation signal and consequently a PWM

signal for controlling the two mosfets of the active filter.

More information about the *Ripple calc* block and the *DC calc* block will be given in the following sections.

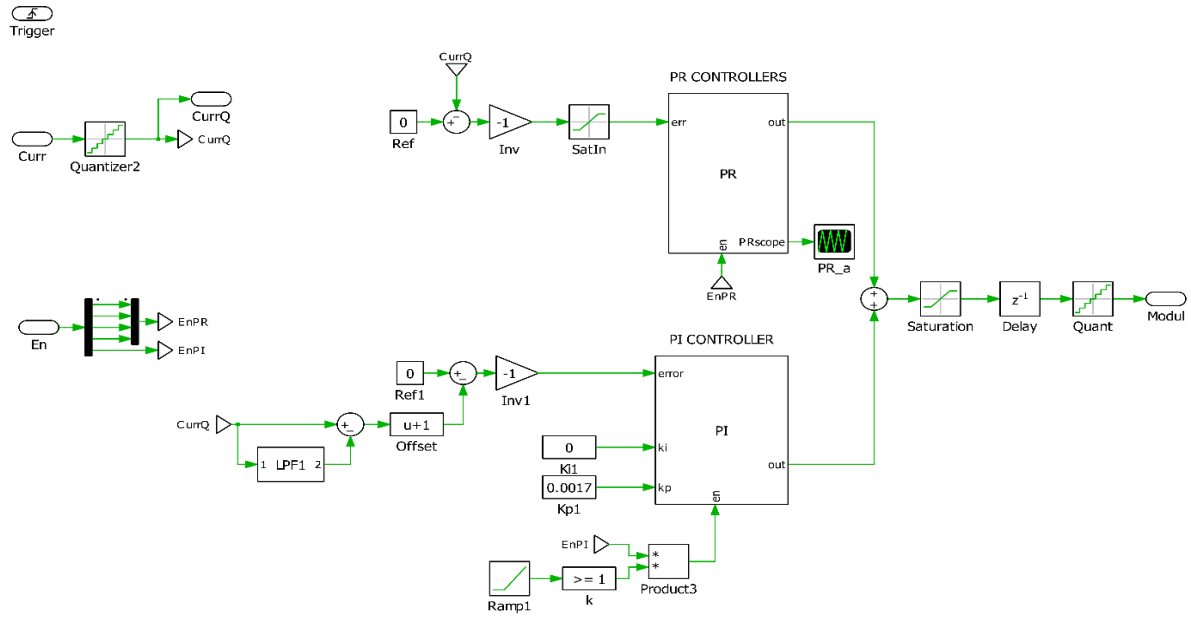

Figure 50 - Ripple comp block

4.1.7 PR controller

Inside the *Ripple comp* block the first part that can be found is the PR controller block. This block, since it is inside of the Ripple comp block, is scheduled and executed at 100kHz. Inside this block, as shown in Figure 51 different PR controllers are present. Each of them is tuned at a different frequency, for example 120Hz, 240Hz and so on. Each block inside contains a discretized version of a continuous time PR controller. The discretization has been executed following the steps done from [17].

The different controllers are all fed by the DC-link current and are then summed together in order to generate the modulation signal that will then go to the modulator.

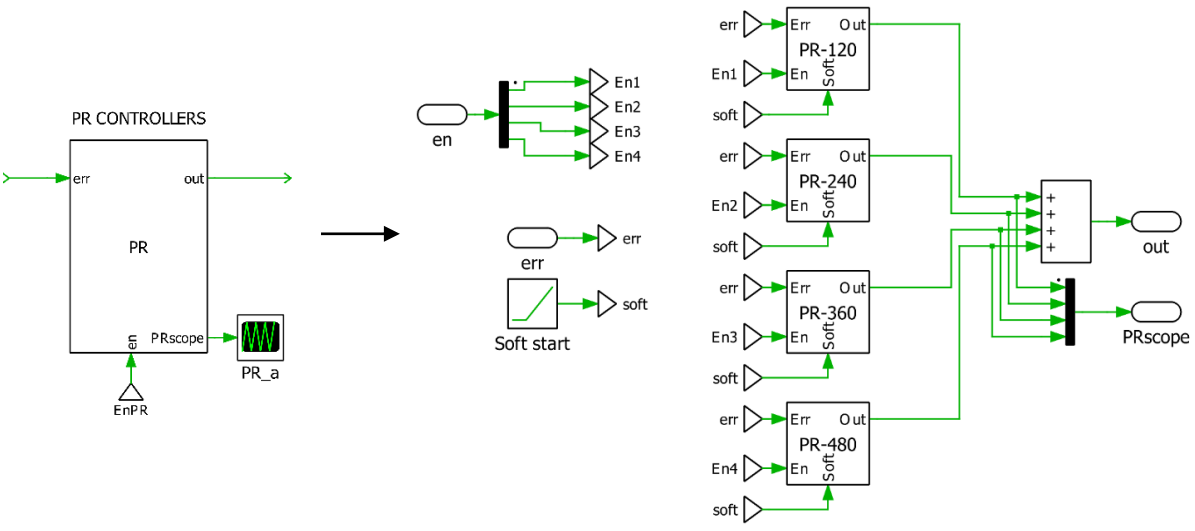

Figure 51 - PR controller block

Each of the PR block can be singularly enabled or disabled, in order to make the filter work with more or less controllers and see the results on the DC-link ripple. In addition, a soft start procedure is added in order to let the filter start working in a controlled way.

4.1.8 PI controller

This is the second part of the *Ripple comp* block and it is scheduled as the PR block at 100kHz. As shown in Figure 52 this block takes as input the error that must be compensated, and gives as output the modulation signal needed to control the two mosfets.

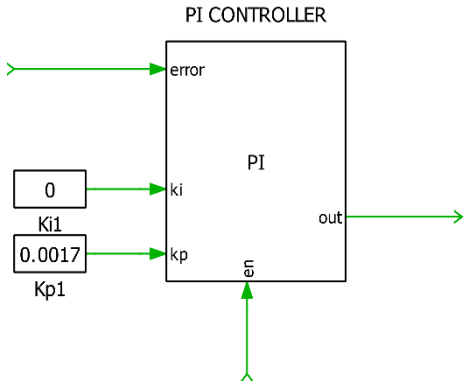

Figure 52 - PI controller block

For doing this, inside this block a discretized version of a PI controller is present.

This block is in charge of compensating all the residual ripple that the PR controller is not able to filter out. As the previously mentioned block, also for this one it is possible to enable or disable it in order to appreciate in deep the contribute that it does on the DC-link ripple filtering.

4.1.9 DC Calculator

Differently from the previously analysed blocks, this block is scheduled and executed at 5kHz since the dynamics that has to follow are really slow.

As shown in Figure 53 this is a really simple block that is in charge of generating the modulation DC component part in order to maintain a constant average voltage on the active filter capacitor. As explained in the previous chapters, the DC modulation is calculated by dividing the capacitor voltage reference for the DC-link voltage.

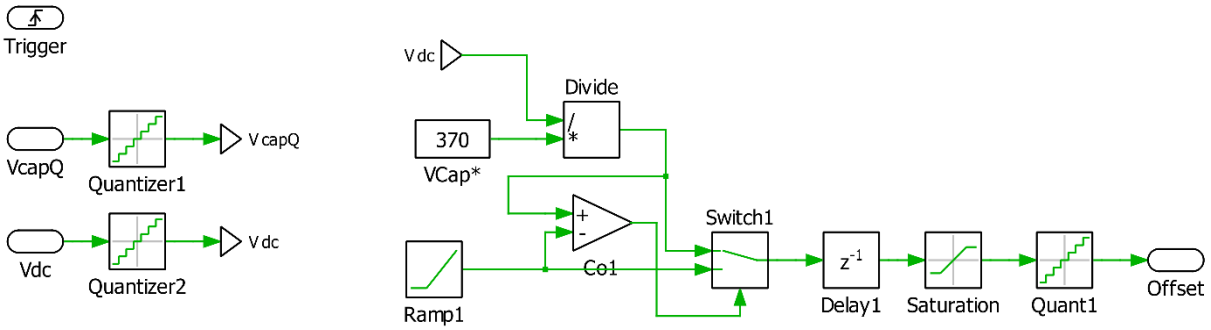

Figure 53 - Dc calculator block

In addition, a soft start procedure is implemented. This is fundamental since using a predefined ramp, it charges up the capacitor until the desired average voltage in a stable and controlled way. Indeed, if this particular procedure is not done at each startup of the filter, there is nothing that limits the current that flows in the capacitor apart from the inductor, and a huge inrush current will flow through it possibly damaging it permanently.

4.2 Simulation results

In this chapter, all the simulations that have been performed will be explained in detail, pointing out all the obtained results and the problems that raised.

4.2.1 Active filter simulation

In this section, some simulations of the active filter will be exposed pointing out all the interesting parts, such as the soft start of the filter, the DC-link current ripple results, and all the interesting signals of the active filter.

The first interesting thing to point out is the soft start procedure. Every time the filter is turned on, therefore every time the battery charger starts charging the battery, the active filter must be turned on with a soft start procedure. This is particularly important, since if no soft start is present, and the filter starts working without a precharge procedure, the current that flow through the mosfets could reach very high values, leading to a possible permanent capacitor damage.

Indeed, as shown in Figure 54, when the upper mosfet is closed, the configuration becomes a short circuit between the DC-link and the capacitor and inductor in series.

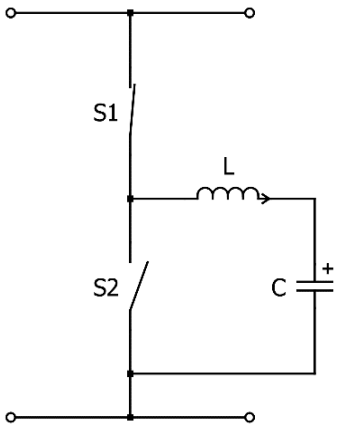

Figure 54 - Active filter startup procedure

For this reason, during startup, a particular soft start procedure has been implemented. This is done by the control system, which limits the current that flows through the filter by modulating the duty cycle of the two mosfets.

This leads to a slowly increasing ramp for what concerns the capacitor voltage. Obviously, also the capacitor current increases slowly until the DC voltage of the active filter capacitor is reached. After that instant, the filter starts working by activating the PR controllers still in a soft and controlled way. This is particularly clear watching Figure 55 where, from the starting of the

simulation until 200ms, the voltage on the filter increases with a controlled slope, and after that a predefined average voltage reference is followed.

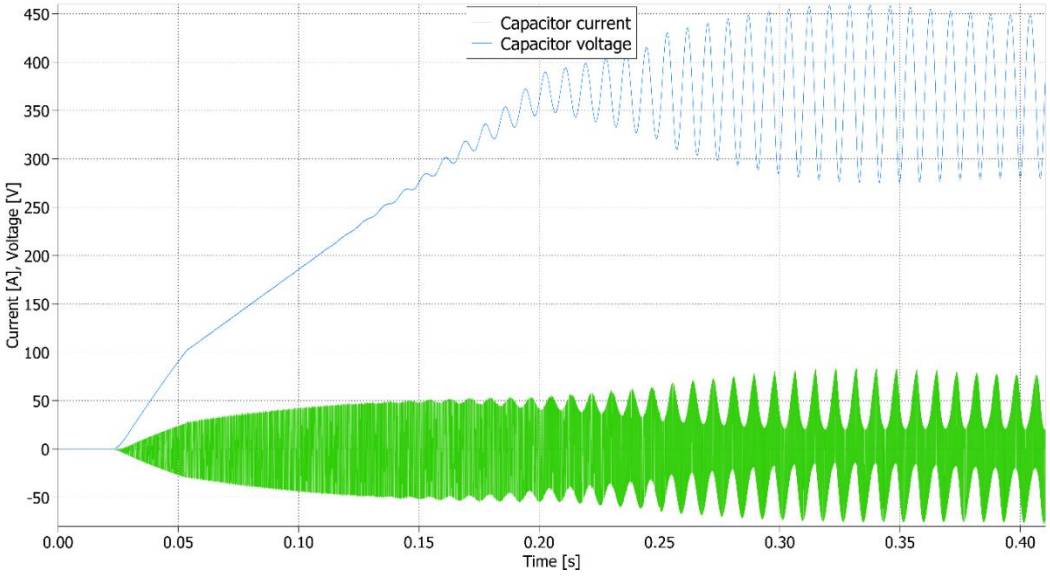

Figure 55 - Active filter soft start

A lot of simulations have been performed to confirm that the filter works as expected. Among all simulations, the most interesting are the ones performed in the worst-case scenario.

15kW CHARGING SCENARIO

The first configuration that has been analysed is exposed in Table 5.

Parameter	Value
DC-link voltage	600 V
Charging power	15 kW
Dead time values	800 ns

Table 5 - Simulation setup

In this specific configuration, the capacitor voltage and current behave as in Figure 56. It is possible to observe that the current and the voltage are out of phase of 90 degrees. This is related to the presence of an inductor between the capacitor and the DC-link, that leads to a delay in the current of 90 degrees.

Another interesting thing to point out is represented by the active filter capacitor voltage that behaves as a 120Hz sinewave. Indeed, in Figure 56 the capacitor voltage oscillates between 250V and 500V in a sinusoidal way in order to store and release the ripple energy depending on the magnitude of the rectified current.

The average value of the capacitor voltage is fixed at 370 by the control system, thanks to the DC-offset block exposed in chapter 3.6.1. This is done in order to always maintain a residual

energy margin and not let the capacitor discharge completely.

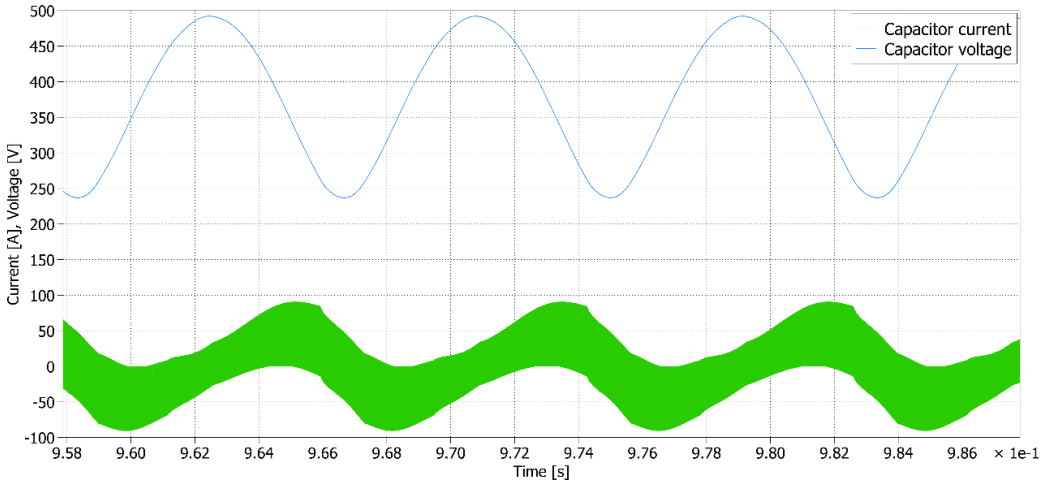

Figure 56 - Filter capacitor current and voltage

In Figure 57, all the currents that act on the DC-link are plotted. The first current, represented in green, is the rectified input current that comes from the PFC rectifier. Then, the red current is the active filter current contribute. The last current, the blue one, is the output current on the DC-link after the active filter.

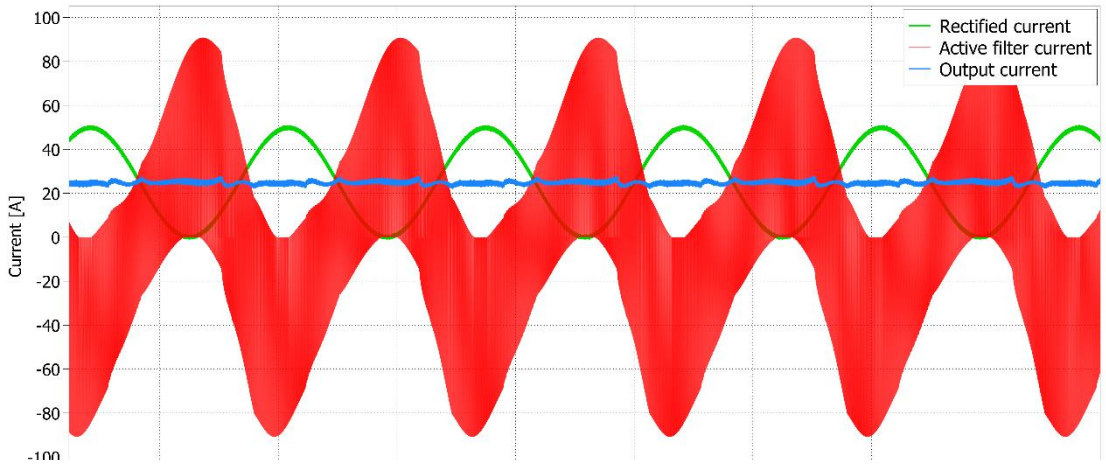

Figure 57 - Current components

It is easy to see that the filter current is out of phase of 180 degrees with respect to the input rectified current. For this reason, summing them will result in an almost constant DC current that have low harmonic content. This is confirmed by looking at Figure 58 where the Fast Fourier Transform is plotted. It can be seen that the active filter has a 120Hz harmonic that has the same magnitude of the input rectified current, but has a 180 degrees phase, therefore those two currents cancel out. All the other higher harmonic currents are very small, but not zero. This is the result of the dead time contribution that will be deeply explained in section 4.1.1. The last thing to point out is that some 100kHz ripple component remains on the output DC-link current. This is due to the switching ripple of the active filter and depends on the value of

the filter inductance. Increasing it will lead to a more filtered current, thus lower high frequency ripple. As explained in the previous sections, this has some implications on the stability of the filter and, for this reason, it has been decided to work in this configuration and not increase the inductor value.

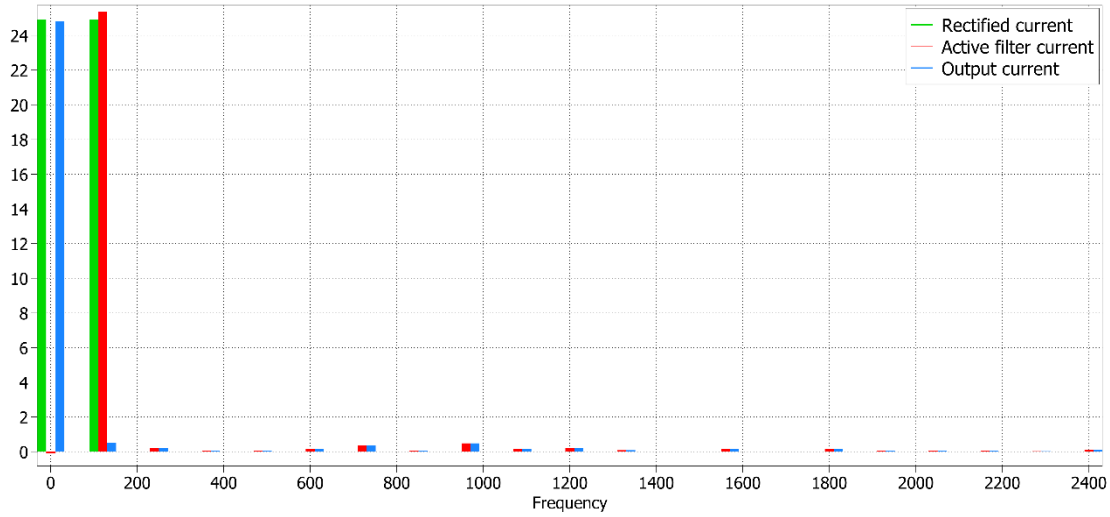

Figure 58 - FFT of current components

The resultant ripple, in this particular case, is of 11%. This is way too high respect to the design target fixed to 5%. This high value is only due to the dead time contribution, that, in this case, is fixed at 800ns. More information about the dead time problems will be given in the next section.

Frequency [Hz]									**Ripple [A]**	**Ripple [%]**
DC	**120**	**240**	**360**	**480**	**600**	**720**	**840**	**960**		
24,82	0,5183	0,1919	0,0755	0,0366	0,1513	0,3698	0,0627	0,4802	2,72	11,0

Table 6 - FFT transform of 15kW charging scenario

7kW CHARGING SCENARIO

The second analysed simulation scenario is very similar to the previous one, apart from the charging power that, in this case, is fixed at 7kW. The precise parameters of this simulation are exposed in Table 7:

Parameter	Value
DC-link voltage	600 V
Charging power	7 kW
Dead time values	800ns

Table 7 - Simulation setup

An interesting thing to point out is the current and voltage of the active filter capacitor. Indeed, respect to the previous analysed case, as shown in Figure 59, since the battery charger is providing only 7kW, the capacitor voltage oscillation is lower than the previous case, since the ripple energy that has to absorb and release is lower than before. In addition, the current flowing through the filter inductor and capacitor is quite different, since the peak values are lower, because the fundamental harmonic at 120Hz is lower, but the ripple at 100kHz is almost equal, therefore, as it will be explained in the following chapters, the efficiency at lower power charging rates is lower.

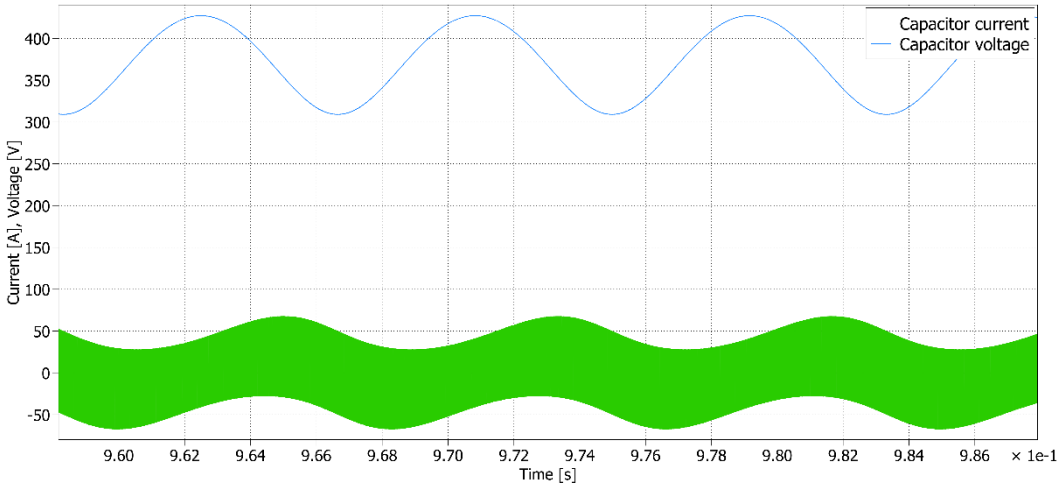

Figure 59 - Active filter capacitor current and voltage

In Figure 60, all the currents that act on the DC-link are plotted. The first current, represented in green, is the rectified input current that comes from the PFC rectifier. Then, the red current is the active filter current contribute. The last current, the blue one, is the output current on the DC-link after the active filter.

It is easy to see that the filter current is out of phase of 180 degrees with respect to the input rectified current. For this reason, summing them will result in an almost constant DC current

that have low harmonic content. This is confirmed by looking at Figure 61 where the Fast Fourier Transform is plotted. It can be seen that the active filter has a 120Hz harmonic that has the same magnitude of the input rectified current, but has a 180 degrees phase, therefore those two currents cancel out. All the other higher harmonic currents are almost negligible in this case, since the effect of the dead time is not present as in the previous case.

The last thing to point out is that some 100kHz ripple component remains on the output DC-link current. This is due to the switching ripple of the active filter and depends on the value of the filter inductance.

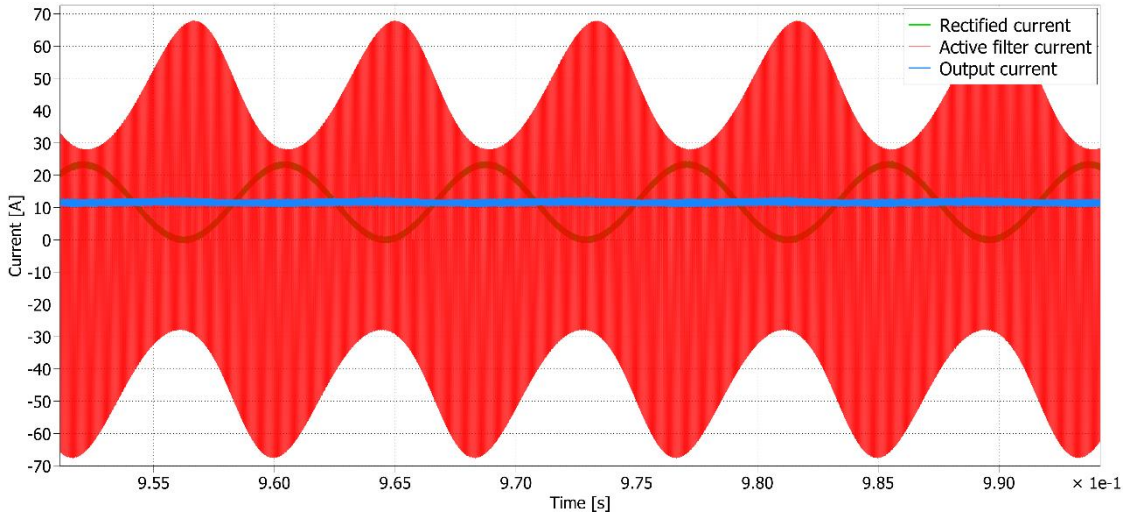

Figure 60 - Current components

For what concerns the magnitude of the DC-link ripple current, as it can be seen in Figure 61 and in Table 8, the ripple component at 120Hz is quite small in this specific case, around 2.3% of the DC component, and all the higher harmonics are almost negligible.

The overall ripple current is of 3% that is lower than the design target of 5%.

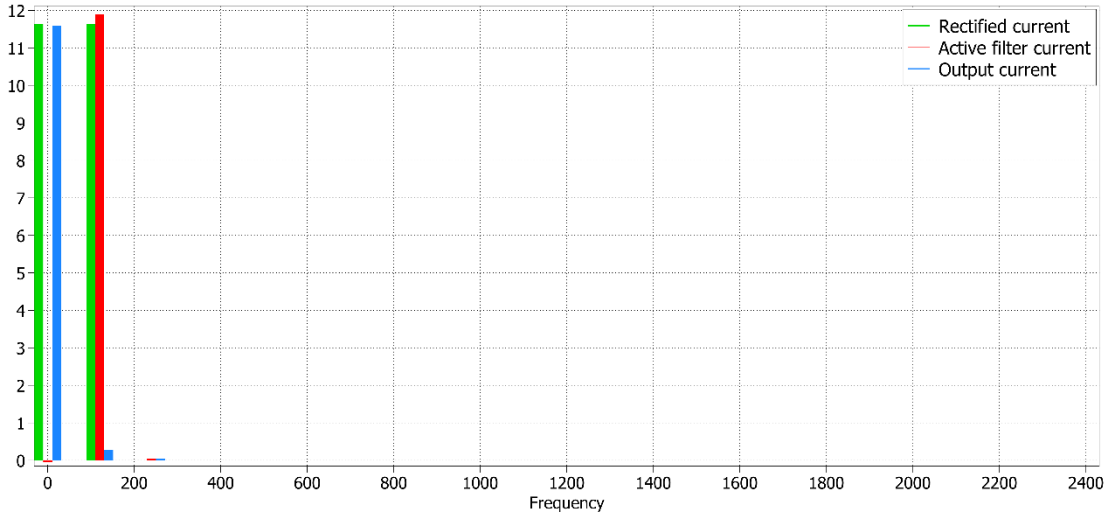

Figure 61 - FFT of current components

Frequency [Hz]								Ripple [A]	Ripple %
DC	120	240	360	480	600	720	840		
11,59	0,2748	0,0434	0,0023	0,0004	0,0011	0,009	0,0021	0,0009	0,35

Table 8 - FFT transform of 7kW charging scenario

4.1.1 Dead time analysis

Within this section, an analysis will be conducted to point out the effects introduced by the dead time of the two mosfets on the active filter.

All the considerations that will be exposed in the following section are done taking into consideration the worst-case scenario, represented by the configuration exposed in Table 9.

Parameter	Value
DC-link voltage	600 V
Charging power	15 kW
Dead time values	0ns - 500ns – 800ns

Table 9 - Simulation parameters

As shown in Figure 62, the DC-link current ripple changes, depending on the dead time. Starting from the case in which the dead time is 0ns, therefore an ideal case, the current is quite smooth and has no spikes, and only some high frequency ripple at 100kHz is present due to the switching ripple.

Taking into consideration the second case, in which the dead time is fixed at 500ns, some spikes start to appear, leading to a not perfectly constant current.

The third analysed case is the one with 800ns dead time. In this case, a lot of spikes at low frequency are present, which leads to a dirty signal with a lot of low frequency harmonic content.

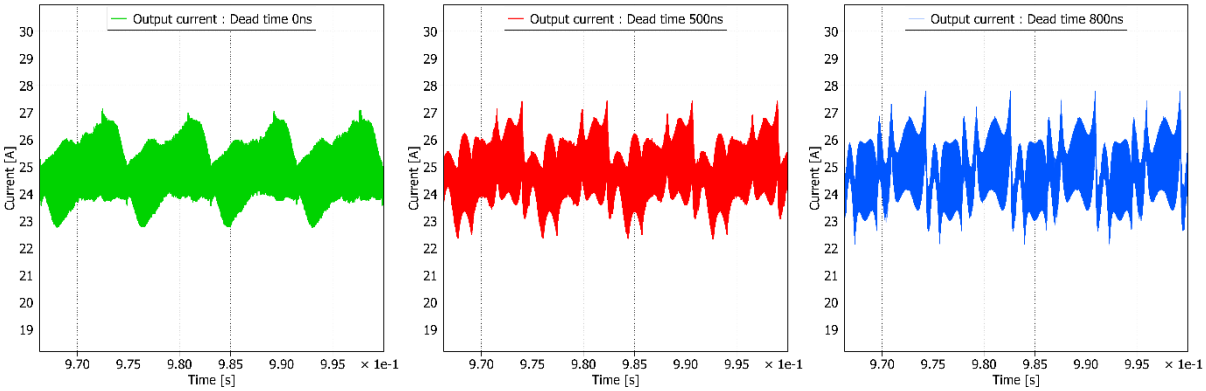

Figure 62 - Dead time effect on DC-link current

The differences that the dead time introduces are particularly visible looking at the Fast Fourier Transform present in Figure 63. Starting from the 0ns dead time case, only some residual ripple

at 120Hz and 240Hz is present, all the higher order harmonics are almost negligible. In the 500ns case, the harmonic content is higher, especially in the range 360Hz-960Hz. The last case, with 800ns dead time, present the highest harmonic content at all the low frequencies.

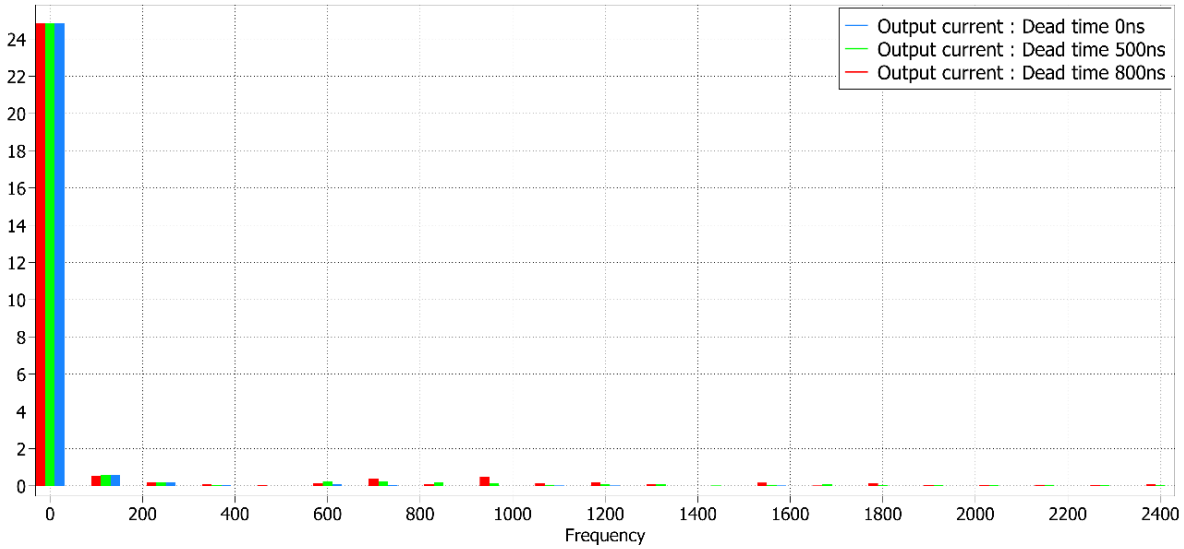

Figure 63 - FFT of DC-link current with different dead time values

Dead Time	Frequency [Hz]									Ripple [A]	Ripple %
	DC	120	240	360	480	600	720	840	960		
0ns DT	24,83	0,5838	0,2032	0,0297	0,0071	0,0632	0,0299	0,0096	0,0053	0,93	3,8
500ns DT	24,82	0,5695	0,1948	0,0413	0,0084	0,2265	0,2464	0,1777	0,1339	2,09	8,4
800ns DT	24,82	0,5183	0,1919	0,0755	0,0366	0,1513	0,3698	0,0627	0,4802	2,72	11,0

Table 10 - FFT of DC-link current

Looking at Table 10, the exact harmonic content is shown, together with the percentage of ripple current. In the 0ns dead time case, the ripple is in the order of 3.8%, that is under the 5% target. Changing the dead time to 500ns brings the current ripple to 8,4%, that is slightly over the target ripple. In the third case, when the dead time is fixed at 800ns, the ripple gets larger and reaches 11%, way over the project target.

All these problems arise because the dead time weights a lot with respect to the switching period. This happens due to the fact that the switching period is 10us and the dead time is 8% respect to that period. For this reason, in case the duty cycle is in the order of 30%, that is 3us on and 7us off, after the application of the dead time, the real duty cycle becomes 22%, therefore 2.2us respect to the requested 3us, losing 26% of the on time. This implies that the controller of the filter is convinced that is applying a certain duty cycle, but the real duty is way smaller due to the dead time.

The only solution to this problem is to integrate some kind of dead time compensation in the controller of the active filter.

4.1.2 DC-link current sampling

A big problem encountered during the simulation, and especially during the transition from a continuous time to a discrete time simulator, has been the DC-link current sampling.

Indeed, until the model runs in continuous time, no problem arises since everything is working in an ideal way and all the signals are continuous.

After passing to a discretized system that can run on a microcontroller, some problems related to the sampling of the signal arise. This can be perfectly seen in Figure 64 where the currents before and after the Analog to Digital Converter (ADC) sampling are plotted.

Taking a closer look at the currents plotted, the green line represents the continuous time DC-link current that has to be measured in order to make the system work. Then, the blue line represents the DC-link current sampled and quantized at 100kHz without any filter.

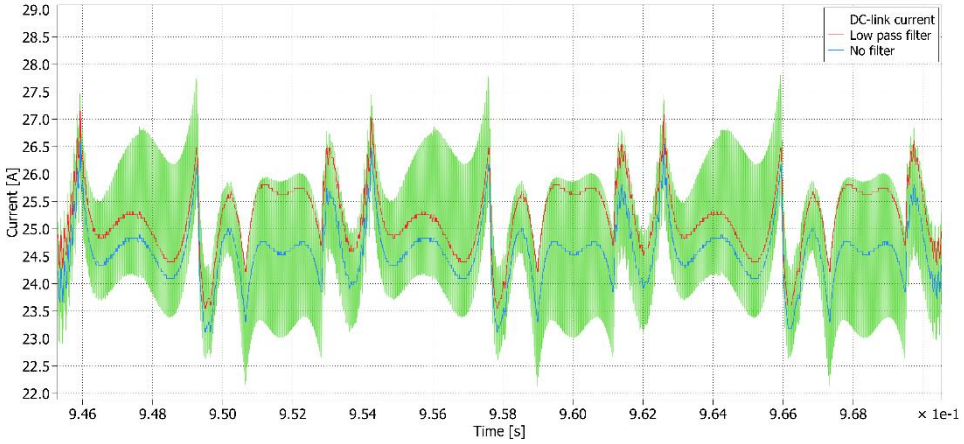

Figure 64 - DC-link current sampling

Since the signal that has to be compensated is at low frequency, all the 100kHz ripple is not of interest for the active filter, therefore the scope is to give to the controller a sampled version of the current that represent a filtered version of the continuous time current. It is quite clear that the blue signal is very different from the green one, at least for the low frequency harmonic content. This is clearly shown in Figure 65, where the Fast Fourier Transform of the signals is performed. For this reason, a low pass filter, with cut-off frequency centred around 30kHz, has been placed before the sampling of the current. In the real world, this could be implemented in hardware using a simple Resistor Capacitor (RC) filter circuit.

Looking again at the Fast Fourier Transform figure, it can be seen that the filtered and sampled version of the continuous time signal, identified in the red one, has almost the same harmonic content of the continuous one. For this reason, for the simulations, a first order low pass filter

has been placed in order to generate a good reference signal for the controller of the active filter.

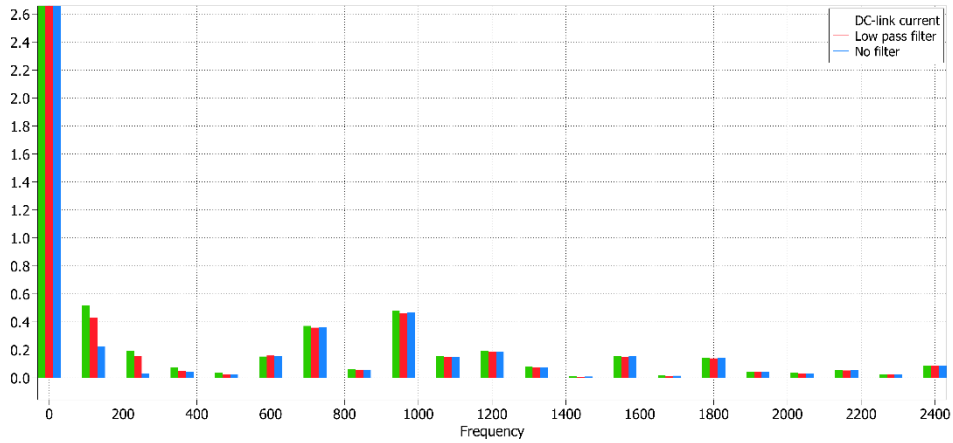

Figure 65 - FFT of DC-link current

4.1.3 System efficiency

In this section, an analysis regarding the active filter overall efficiency and all the losses contributions is done.

The first case taken into consideration is a charging procedure at 7kW in single phase configuration. As it can be seen in Figure 66, the losses sources are represented by the two mosfets, the filter capacitor and the filter inductor.

The inductor and the capacitor contribute with only little losses in the order of 5-10W for the inductor, and 10-20W for the capacitor. The exact value depends on the voltage of the DC-link, indeed increasing it, the losses increase.

Regarding the mosfet losses, the one plotted in Figure 66 represents the overall losses of a mosfet, therefore the switching losses and the conduction losses. These represent the main component of the overall filter power losses.

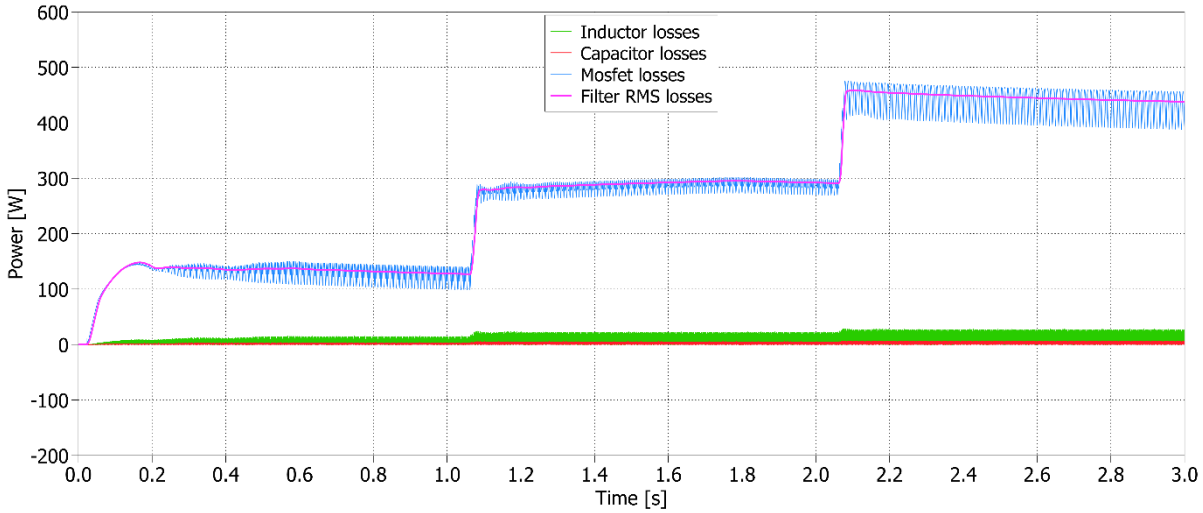

Figure 66 - Filter losses at different DC-link voltage values (7kW case)

As shown in Table 11, the filter efficiency at 7kW charging rate varies between 93.6% and 97.9%, depending on the DC-link voltage value.

DC-link voltage [V]	RMS losses [W]	Filter efficiency [%]
600	145	97.9
770	270	96.1
900	450	93.6

Table 11 – Filter efficiency (7kW case)

The second case analysed is the worst-case scenario that is the maximum charging rate the battery charger is able to give, hence 15kW power.

For what concerns the losses, as shown in Figure 67, the filter losses are slightly bigger than in the previous analysed case. These are shown in Table 12.

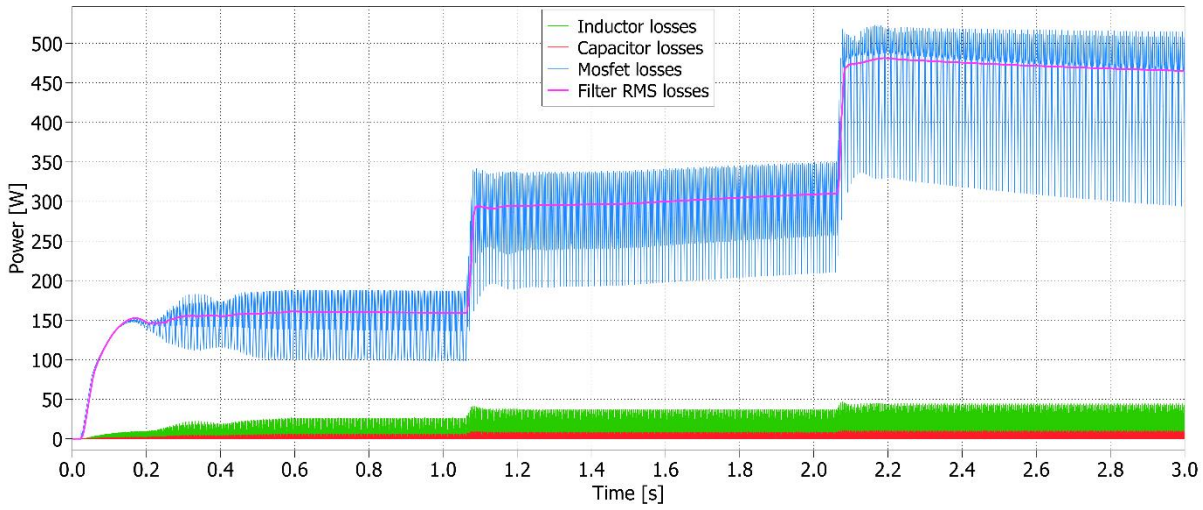

Figure 67 - Filter losses at different DC-link voltage values (15kW case)

It can be seen that the efficiency is higher than the previous case and it is in the range of 96.9% to 98.9%, depending on the DC-link voltage.

DC-link voltage [V]	RMS losses [W]	Filter efficiency [%]
600	160	98.9
770	300	98.0
900	460	96.9

Table 12 – Filter efficiency (15 kW case)

5. Prototype design

In this chapter, the design and assembly of the prototype will be exposed pointing out all the components that has been selected during this phase.

5.1 Capacitor Part number selection

The capacitor dimensioning and selection is quite a complex task to perform, but, after figuring out all the requirements it should have, as explained in chapter 3.5, the C4AQCEW6110A3AJ Film capacitor from Kemet shown in Figure 68 [18] has been selected. Since it has only 110uF of capacity, four of them are needed in parallel in order to reach the 400uF design target.

Figure 68 - C4AQCEW6110A3AJ capacitor

5.2 Inductor design and testing

As already mentioned before, the inductor dimensioning and design is a very challenging task to perform, however, starting from the ratings defined in chapter 3.4, a ferromagnetic core has been selected. In particular, the 0076726A7 Magnetics Kool Mμ Hf core has been chosen as candidate for the prototype. After the core selection, Litz wire has been wounded around the core doing 10 turns in order to reach the required 15uH inductance, resulting in the inductor present in Figure 69.

In the end, an impedance analysis has been performed using an impedance analyser to verify the real inductance of the inductor and also to evaluate its series resistance. The obtained results are shown in Figure 70.

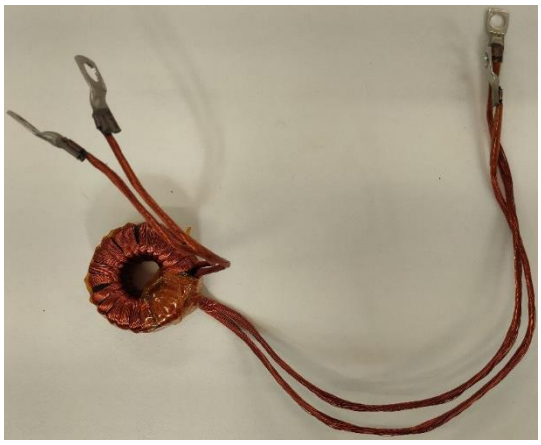

Figure 69 - Assembled inductor

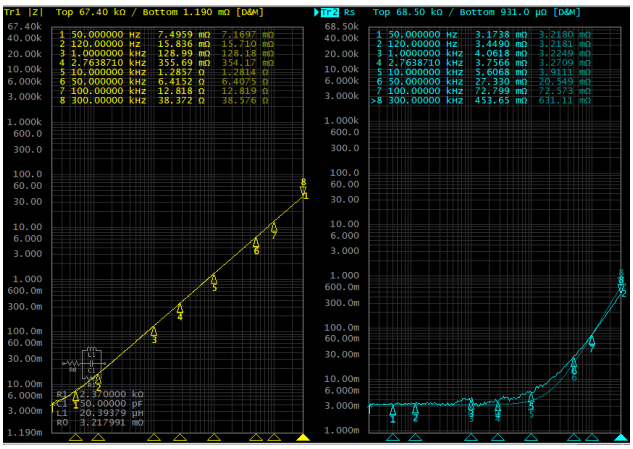

Figure 70 - Impedance analysis of inductor

5.3 Power module selection

For what concerns the power module selection, after the requirement analysis performed in chapter 3.3, it has been decided to work with the CAB450M12XM3 Wolfspeed power module shown in Figure 71 [19]. This is a 1200V SiC module that can withstand high currents and, for this reason, is a perfect candidate for the prototype.

It has been chosen to work with such a high-performance power module since, during the prototype testing, faults as overcurrent and high impulse current could happen due to software control errors. Therefore, it has been oversized in order to not stress too much the power module.

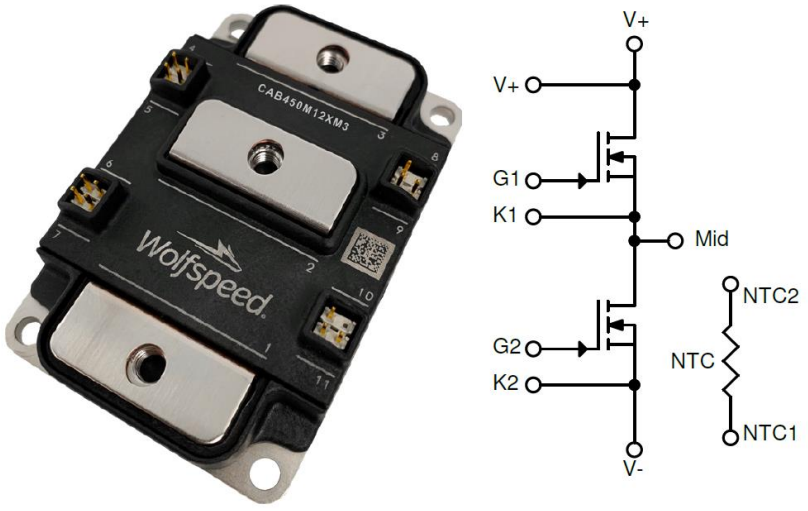

Figure 71 - CAB450M12XM3 Wolfspeed power module

5.4 PCB design

For building a prototype of the filter, some Printed Circuit Board (PCB) for interfacing the Wolfspeed module gate driver, and the control logic has been designed.

The first PCB designed is the one shown in Figure *73*. The main scope of this circuit is to make a simple interface for controlling the Wolfspeed gate driver CGD1700HB2P-XM3, which has a differential interface.

The second PCB that has been designed is shown in Figure *72*. It is a fiber optic interface that is used to control the gate driver. It has been decided to adopt the fiber optics since, when dealing with power modules control, a lot of common mode noise can be generated by the power module and the gate driver, leading to problems in the control logic board. For this reason, between the logic board and the gate driver, the connection is made by using 3m long fiber optic cables.

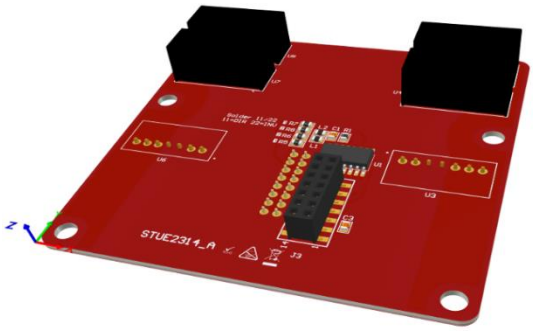

Figure 73 - Gate driver interface

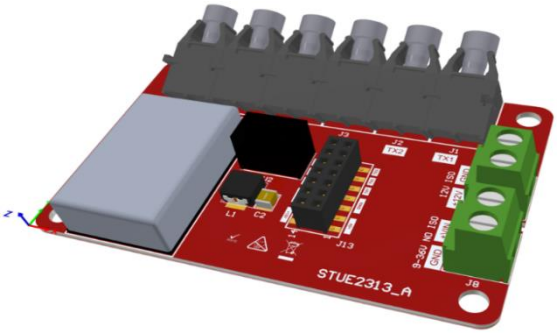

Figure 72 - Optical fiber interface

The last PCB that has been designed and assembled is shown in Figure 74 and represents the real core of the active filter.

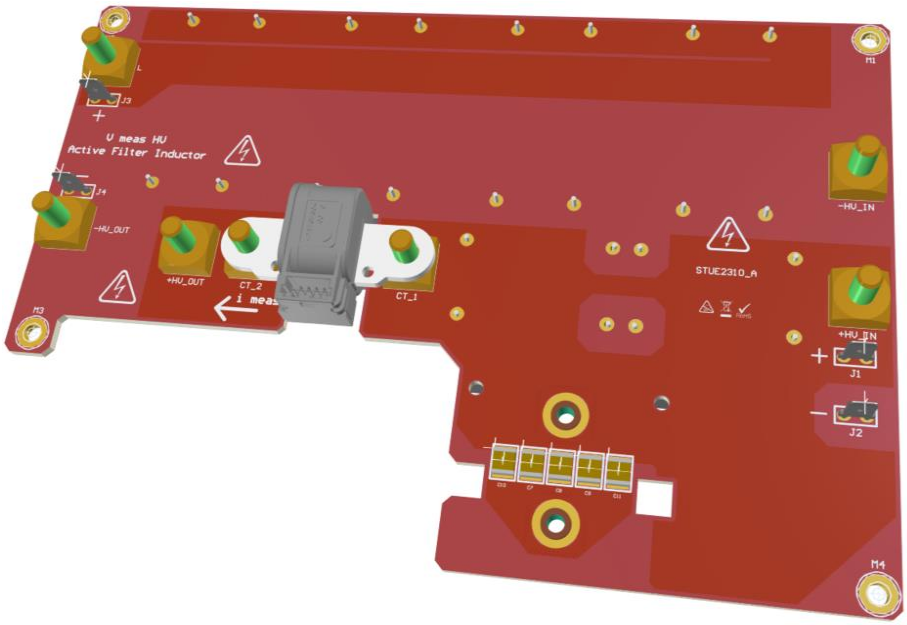

Figure 74 - Active filter capacitor and inductor PCB

Indeed, this board hosts the DC-link current sensor, that is a hall effect sensor, all the active filter capacitor that are mounted and soldered under the board, but also all the connections for the power module and for the inductor of the filter.

5.5 Structure and cooling

For combining and assembling all the components and all the boards together, a 3D printed support structure has been designed and printed. The result can be seen in Figure 75.

An additional function of this structure is to cool down the power module using liquid cooling. Indeed, a cooling system is present and is designed in order to host the power module and, by means of an inlet and an outlet, is able to cool it down using direct liquid cooling on the case of the module.

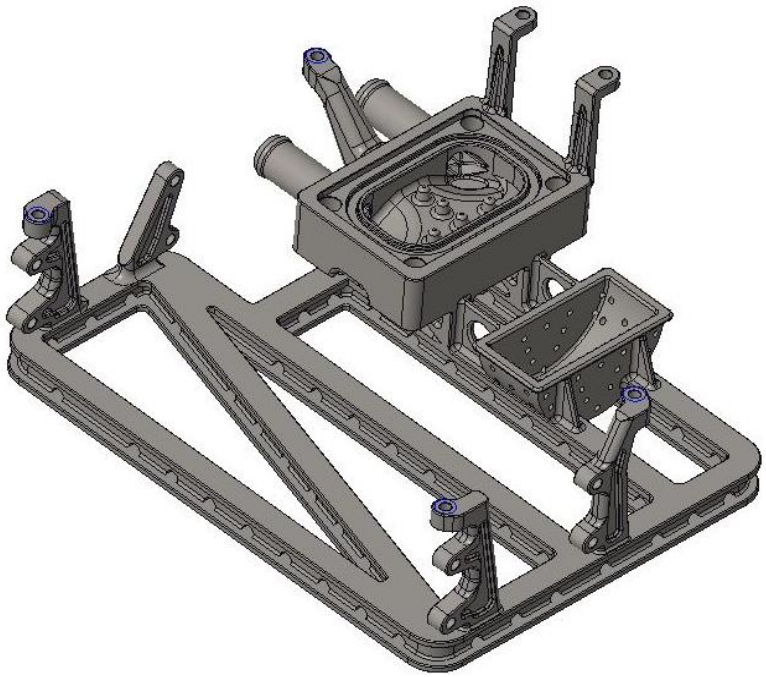

Figure 75 - Support structure and power module cooling

For this reason, some tests have been performed in order to assess the behaviour of the cooling system under high pressure. Up to 2 bar of pressure, the results were extremely satisfactory since the pressure leakage was very low.

The previous test has been performed also at 50°C temperature, in order to assess the behaviour of the cooling system under a higher temperature. Also, in this condition the pressure leakage was very low and acceptable.

The proposed cooling system is clearly not designed and optimized for high pressure and high temperature, but can represent a good choice for a fast and easy prototyping, like in this work.

5.6 Complete prototype

In the end, all the previously described components have been assembled together in order to form the complete prototype. The power module has been mounted on the cooling system, together with the inductor and all the printed circuit boards.

The obtained result is shown in Figure 76, Figure 77 and Figure 78, where the rendering and the real assembled prototype are present.

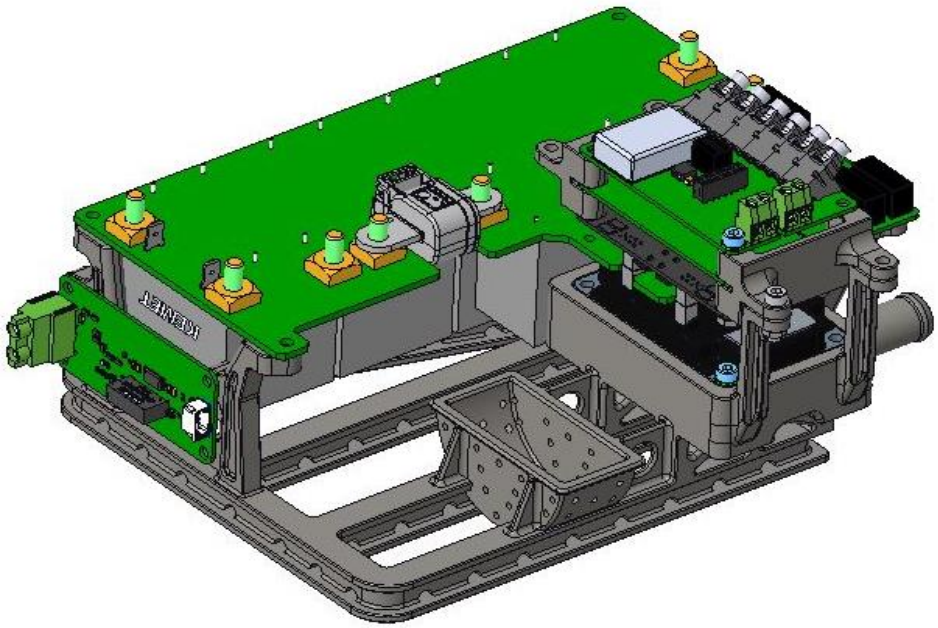

Figure 76 - Rendering of the assembled prototype

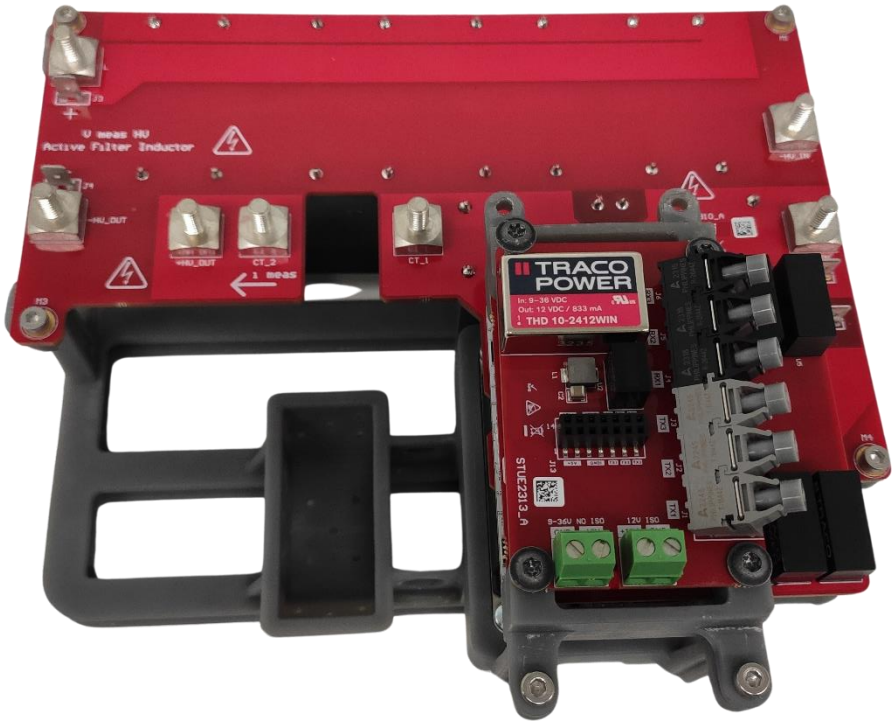

Figure 77 - Real assembled prototype

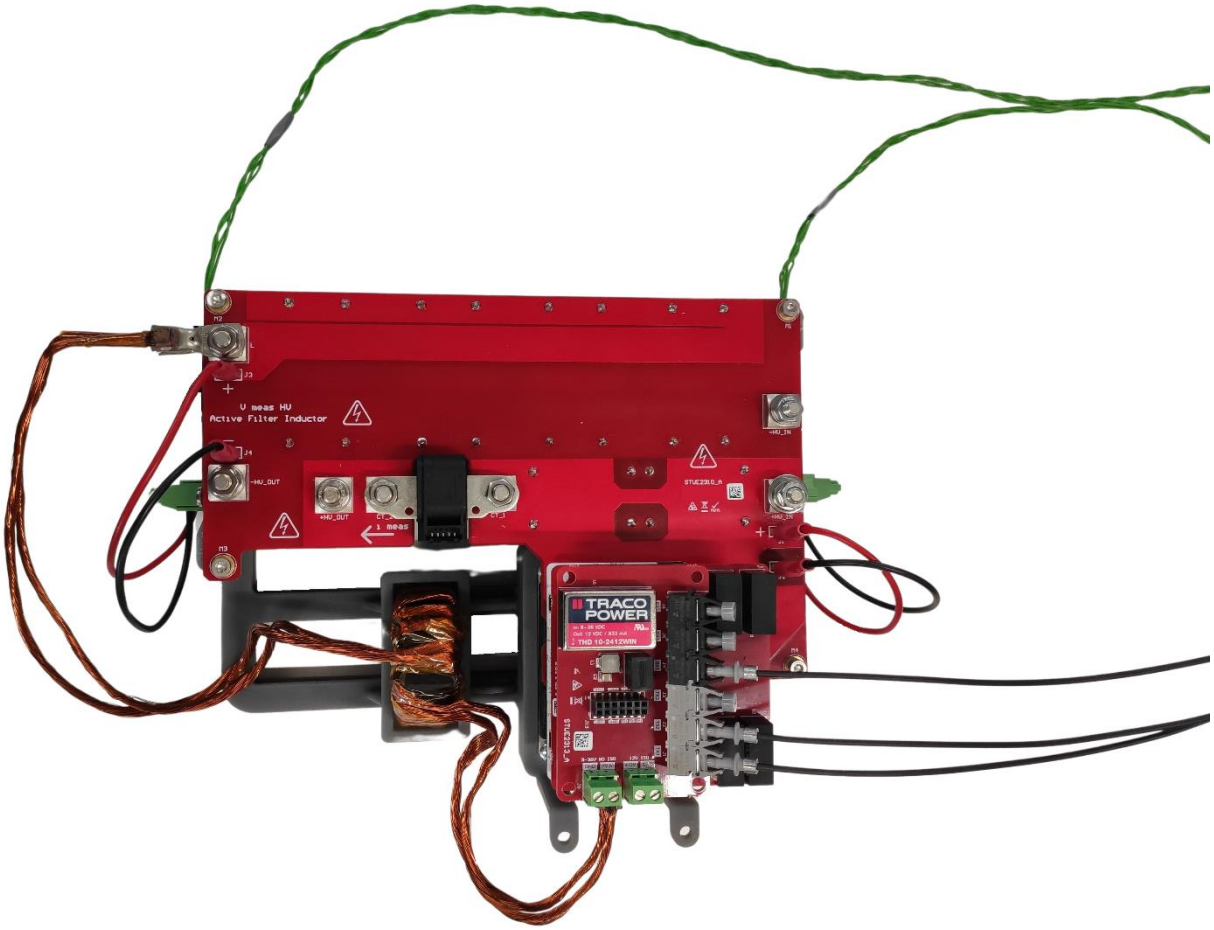

Figure 78 - Assembled prototype with cables and fiber optics

6. Weight and volume evaluation

In this chapter, a brief evaluation of the volume and the weight of the different approaches is done in order to point out the differences and the advantages of each topology.
In particular, three approaches are exposed:

- Passive solution using electrolytic capacitors.
  For this solution, the TDK B43652A5687M05 electrolytic capacitors have been selected, since they represent the best possible solution on the market in terms of volume and weight. On the other hand, they are not so good in terms of lifetime duration, since in the worst case they last 3000h.
- Passive solution using Film capacitors.
  For this solution, the KEMET C4AQIBW5300A3LJ capacitors has been selected, since they represent one of the best possible solution on the market in terms of volume and weight. In addition, they have a very long lifetime duration.
- Active filter solution using Film capacitors.
  The active filter is built with all the components that have been already explained in the previous sections.

6.1 Weight respect to traditional approach

Starting from the passive electrolytic approach, 14 capacitors are needed in order to reach the requirements in terms of voltage rating of 900V and 2300uF capacitance. Each of them has a weight of 56 grams, therefore the overall total weight is 784 grams.
Talking about the second approach, the passive Film capacitor solution needs around 76 capacitors in order to reach the 2300uF capacitance target. Each of them has a weight of 64 grams, hence the overall total weight is 4864 grams.
The last solution analysed is the active filter topology that uses Film capacitors. In this case, the overall weight of this approach, that takes into consideration also all the other components respect to the capacitors, therefore the inductor, the power module, the cooling system and all the PCBs, is around 2122 grams.
The weight of an active solution is surely higher than an electrolytic passive solution, since a lot of additional components are needed. On the other hand, it brings a big advantage represented by the increased lifetime duration and reliability.
In addition, the proposed solution is only a simple prototype that has the scope of verifying the working principle of the active filter and is surely not optimized for what concerns the

weight. For this reason, lower weight values can be reached optimizing every single component.

In the end, as shown in Figure 79, the lowest weight solution is the passive electrolytic one. The second one is the active filter with Film capacitors, and the heaviest one is the passive Film solution. However, the active filter has a lot of margin of weight reduction and it is reasonable to assume that is possible to reach a lower weight, comparable with the one of the passive electrolytic solution.

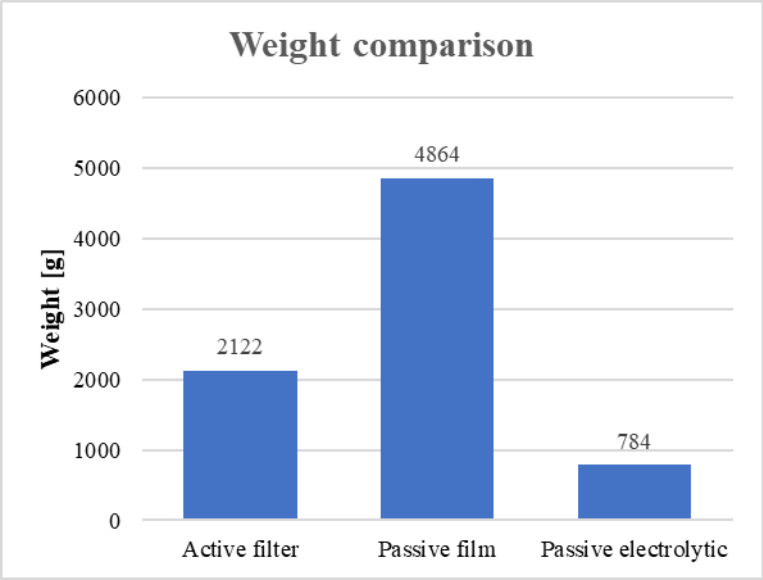

Figure 79 - Weight comparison

6.2 Volume of the filter

In Figure 80, the overall dimensions of the proposed active filter prototype are shown. From those dimensions, the total occupied volume is 5.02 litres. Obviously, since it represents only a prototype, it is not optimized for what concerns the arrangement of the components and the overall structure. If the only volume of all the components is taken into consideration, the total volume of the filter is around 1.25 litres.

In the end, in Figure 81 the complete volume comparison between the three proposed approaches is shown. As it can be seen, in all the three approaches most of the volume is occupied by the capacitors.

The lowest volume solution is represented by the passive electrolytic approach with 0.66 litres. Then, the active filter approach has a volume of 1.25 litres and, in the end, the volume of the passive Film solution is 4.6 litres.

As for the weight, also the volume of the active filter solution can be optimized and reduced, since the proposed solution represents only a prototype. For this reason, using an active filter is

possible to obtain a comparable volume respect to the passive electrolytic solution, but with a higher reliability since only Film or ceramic capacitors are employed.

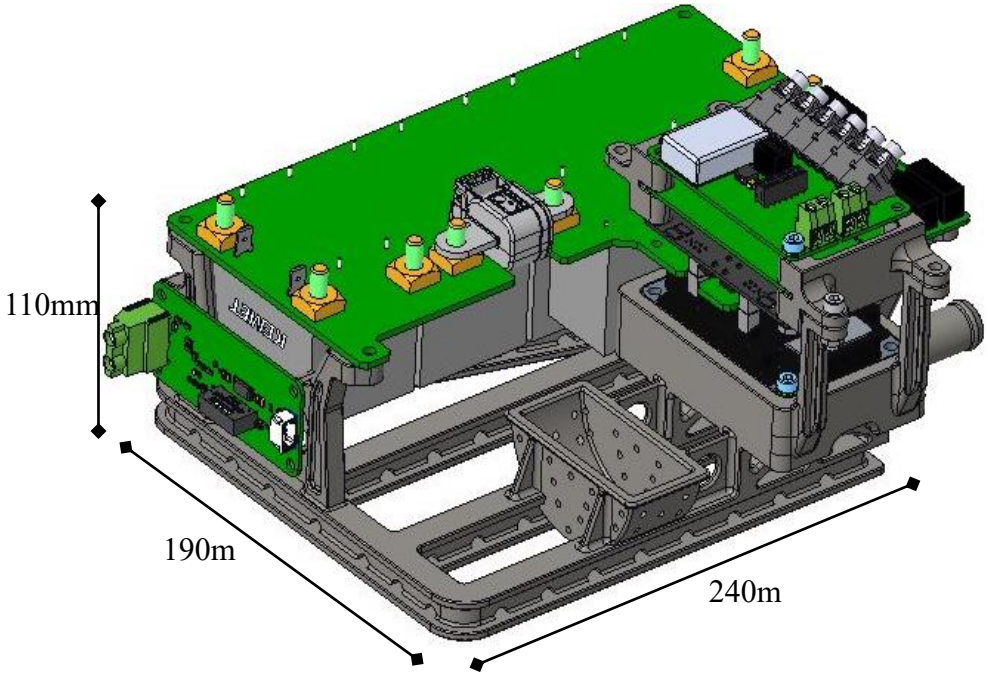

Figure 80 - Dimensions of the proposed prototype

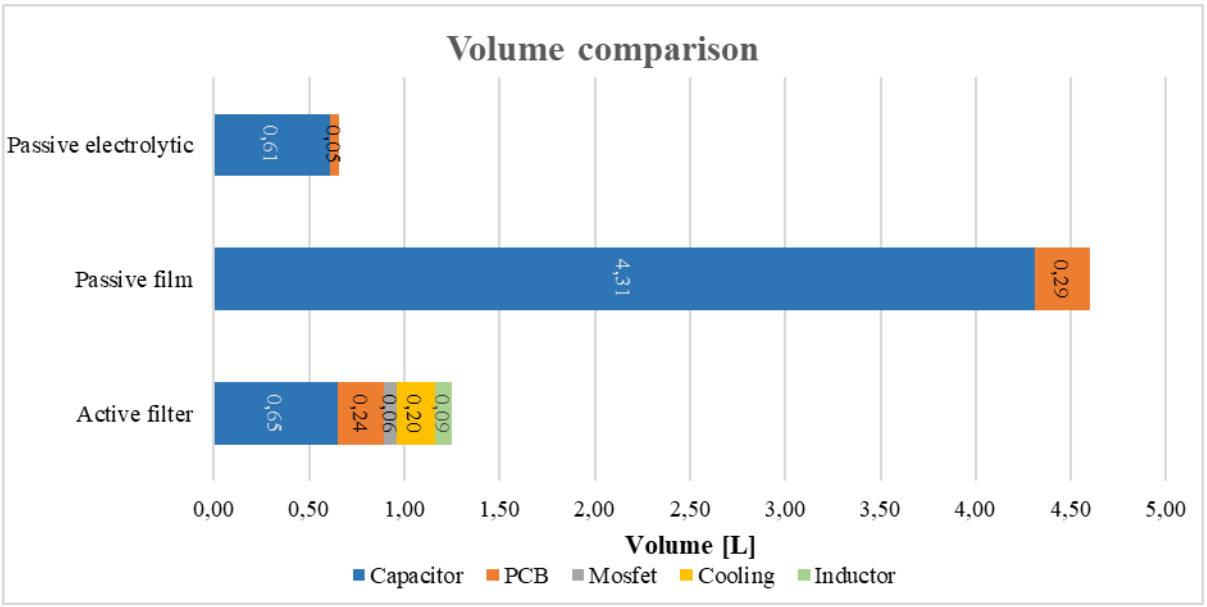

Figure 81 - Volume comparison

7. Conclusions and future work

This study dealt with the design and simulation of an active filter intended to reduce the size of DC-link bulk capacitor of battery charger.

The obtained results are well aligned with both theoretical expectation and simulations. Additionally, a prototype has been designed and assembled to prove the feasibility of the proposed concept. Further tests will follow to validate the thermal behaviour of the unit.

The prototype also served to highlight some aspects that can be potentially improved with a specific design. The selected capacitors are, for example, commercial grade off-the-shelf pieces: their energy density is far from being optimized. The inductor core has been selected between available part numbers, but a custom design driven by Finite Element Method (FEM) analysis can lead to a reduced size solution.

Moreover, both capacitors and inductor can benefit in terms of size from being cooled as power module. From this point of view, the potential of the active filter solution in terms of size reduction is particularly high compared to traditional structures.

On the control algorithm side, the main challenge comes from the compensation of current distortions introduced by dead time and a reduction of its effects can in fact lead to further reduction in DC-link ripple.

Additionally, Proportional-Resonant (PR) controllers require the grid frequency value to be known. Because of the fact grid frequency actually fluctuates around its nominal frequency, this implies that, for proper implementation of PR, parameters should be re-calculated and updated online. This poses some stringent requirements on software architecture and available computational power.

On the other hand, the versatility of this filter topology makes it applicable to various contexts, including automotive systems, such as On-Board Chargers (OBC) and inverters, replacing passive capacitors. This study not only introduces novel perspectives in energy management, but also suggests potential directions for further development and optimization.

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