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Calibration of Switched Capacitor Arrays for time measurements with picosecond resolution for the LHCb Upgrade II

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Abstract

L'esperimento LHCb ha lo scopo di ricercare fisica oltre il Modello Standard tramite misure di precisione nell'ambito della fisica del sapore, in particolare nel settore degli adroni contenenti *q*uark *b*eauty e *c*harm. La presenza di fisica oltre il Modello Standard può essere responsabile, ad esempio, per la modifica delle osservabili di violazione della simmetria di *CP*, per l'aumento dei rapporti di diramazione di decadimenti rari o addirittura proibiti, o per la violazione dell'universalità leptonica nei decadimenti di adroni contenenti *b*eauty e *c*harm. Una deviazione delle misure di tali quantità rispetto alle previsioni del Modello Standard, sarebbe una chiara indicazione della presenza di nuove particelle o interazioni non previste. Fino ad ora l'esperimento ha ottenuto grandi risultati sfruttando l'enorme quantità di adroni contenenti *q*uark *b*eauty e *c*harm prodotti al Large Hadron Collider del CERN, ma senza evidenziare discostamenti rilevanti rispetto alle previsioni del Modello Standard. Al fine di portare la precisione delle misure al loro limite estremo, negli ultimi anni si sta discutendo la possibilità di un ulteriore aggiornamento dell'esperimento che lo renda in grado di operare a una luminosità istantanea circa un fattore 30 maggiore rispetto alla versione originale, raccogliendo un campione totale corrispondente a circa 300 fb^{-1} di luminosità integrata, rispetto ai circa 9 fb^{-1} attuali. Una delle sfide che tali condizioni impongono è quella di distinguere l'elevato numero di interazioni primarie in un evento. Una delle chiavi di volta per la risoluzione di tale problema è quella di dotare i rivelatori della capacità di misurare il tempo di arrivo delle particelle con precisioni dell'ordine di poche decine di picosecondi. Tali precisioni temporali richiedono l'utilizzo di schede di acquisizione capaci di contribuire alla risoluzione temporale totale per non più di pochi picosecondi. Molto convincenti in questa direzione sono le schede basate su SCA (Switched Capacitor Array), di cui il chip DRS4 è un esempio, che permettono di raggiungere le precisioni richieste a fronte di costi ridotti. L'obiettivo di questa tesi è di descrivere il metodo di calibrazione di una specifica scheda, la V1742, progettata e realizzata da CAEN, e di valutarne il contributo alla risoluzione temporale totale dell'apparato sperimentale. Per farlo viene implementato un metodo di calibrazione proposto da S.Ritt *et al.*. Dopo aver applicato la calibrazione, le prestazioni della scheda sono state misurate ottenendo ottimi risultati e raggiungendo una precisione di circa 2.5 ps, che rappresenta un miglioramento di un intero ordine di grandezza rispetto all'utilizzo della scheda non calibrata. Inoltre, un confronto con la risoluzione temporale ottenuta utlizzando la calibrazione di fabbrica, fornita da CAEN, mostra un miglioramento di circa un fattore 4.

Contents

Introduction

The LHCb [1] (*Large Hadrons Collider beauty*) experiment is a single-arm forward spectrometer located at the Large Hadron Collider (LHC) at CERN. Its purpose is to search for new physics through the study of *CP* violation and rare decays in the sector of quarks *beauty* and *charm*. In the last years the experiment reached remarkable results, like: the first observation of the rare decay $B_s^0 \to \mu^+\mu^-$, the first observation of *CP* violation in the decays of the B^+, B_s^0 and D^0 mesons, and the first observations for exotic states compatible with being *tetraquark* and *pentaquark*. However, the results obtained in Heavy Flavour Physics are, so far, fully consistent with the Standard Model, but the level of *CP* violation in the weak interaction cannot explain the imbalance between matter and antimatter in the universe [2]. During the Run 1 (from 2010 to 2012) and the Run 2 (from 2015 to 2018) of the LHC, the experiment ran at a capacity of low luminosity of 2×10^{32} cm^{-2} s^{-1}. Running at this level of luminosity has some advantages: the majority of events are characterized by a single *pp* interaction per bunch crossing, which makes the data much simpler to analyze than those with multiple primary *pp* interactions, and the radiation damage is considerably reduced. This detector will be described in Chapter 1. A first upgrade of the detector [3] has been installed during the Long Shutdown 2 (LS2) of the LHC (from 2019 to 2020) and will operate until the end of Run 4. The new detector will collect data at the instantaneous luminosity of 4×10^{33} cm^{-2} s^{-1} aiming to collect a total integrated luminosity of 50 fb^{-1} of *pp* collisions at a centre-of-mass energy of $\sqrt{s} = 13.6$ TeV. A brief description of the changes with respect to the previous detector will be given. In addition, the LHCb collaboration already started to work on a proposal for the next upgrade of the detector, LHCb Upgrade II [4], to be built during Long Shutdown 4 (LS4). The aim is to increase the peak instantaneous luminosity up to 1.5×10^{34} cm^{-2} s^{-1}, and to collect a total integrated luminosity of 300 fb^{-1} by the end of the Run 6 of the HL-LHC. A summary of the proposed future detector will be also discussed. To cope with the numerous *pp* collisions occurring per bunch crossing, achieving precise time measurements for all the subdetectors is of paramount importance for the forthcoming LHCb Upgrade II. Physics studies [4] show that time resolutions of few tents of picoseconds are mandatory to distinguish between the multiple primary *pp* interactions and guarantee the necessary detection performances. To achieve these level of precision, all the components of the detectors must be optimised, including the electronic boards used to acquire the signals from the detectors. Technological advancements in this direction have yielded potential solutions, such as digitisers based on Switched Capacitor Arrays (SCAs), like the DRS4 chip, developed at the Paul Scherrer Institute (PSI) in Zurich. These SCAs have shown the capability to provide very precise time determination of electrical pulses, together with a relatively reduced cost. They operate by utilizing an array of capacitors in a sample-and-hold mode. Upon commencing data acquisition, they continuously cycle

in a circular fashion until a trigger signal halts the ongoing process, effectively freezing the data stored in the sampling capacitors. This stored data can later be read out at a significantly reduced speed. This approach offers the advantage of minimizing dead times between the 1024 cells, albeit at the expense of introducing additional dead time during the read-out phase. The operational principles of these devices will be widely discussed in Chapter 2. The objective of this thesis is to implement a calibration procedure for acquisition boards based on SCAs that would allow very small contribution to the overall time resolution to be achieved. The study is performed using a specific acquisition board, the V1742, which is manufactured by CAEN, described as well in Chapter 2. Chapter 3 is dedicated to the description of the calibration methodology employed and the resultant findings. A notably innovative calibration approach, as proposed by S. Ritt *et al.* [5] has been implemented and employed in this thesis. This method encompasses a Voltage Calibration, that adjust for any incorrect measurement of the amplitude of acquired signals, and a Time Calibration, that precisely determine the time difference between consecutive samples of the incoming electrical signals. Finally, a comparative analysis is performed to determine the contribution to the time resolution due to the calibration of the acquisition board. The time resolution of the board is evaluated using a split-signal method before any calibration, using the calibration provided by the manufacturer of the board and the calibration performed in this thesis.

Chapter 1

The LHCb experiment

1.1 The Large Hadron Collider

The LHCb experiment hosts the most energetic hadron collisions ever generated within an accelerator machine. This unparalleled capability is made possible by the Large Hadron Collider (LHC), a two-ring superconducting hadron accelerator and collider located within a pre-existing 26.7 km tunnel. This tunnel was initially constructed between 1984 and 1989 to house the CERN LEP machine (Large Electron-Positron Collider) [6]. Situated approximately 100 meters beneath the earth's surface, the LHC straddles the border between France and Switzerland, near Geneva. The LHC primarily employs protons as its hadronic projectiles, enabling collisions with a center-of-mass energy that can reach by design an astounding 14 TeV. The luminosity[1] of the LHC surpasses 10^{34} $\mathrm{cm}^{-2}\,\mathrm{s}^{-1}$. The LHC serves as the concluding component of a comprehensive accelerator complex, depicted in Figure 1.1. A particle's journey to reach the LHC encompasses several stages. The linear accelerator Linac2 accelerates protons from a state of relative rest to an energy of 50 MeV. These protons are subsequently injected into the Proton Synchrotron Booster (PSB), where their energy is increased to 1.4 GeV. The proton beam advances to the Proton Synchrotron (PS), where it is organized into bunches, each containing approximately 10^{11} protons. Here, the energy is elevated to 25 GeV. The final stage of acceleration before the injection into the LHC occurs within the Super Proton Synchrotron (SPS), propelling the protons to an energy of 450 GeV. These accelerated proton bunches are then introduced into the dual rings of the LHC, where they circulate in opposite directions. Within the LHC, the two rings converge at four interaction points, constituting the locations where the principal CERN experiments (ATLAS, CMS, LHCb, and ALICE) are strategically positioned.

1.2 The LHCb Detector

The most evident difference between the LHCb and the other main experiments at the LHC is that, instead of surrounding the entire collision point with an enclosed detector, it uses a series of subdetectors arranged along the beam line to reveal mainly particles produced in the forward direction [1]. The choice of such detector geometry is justified by

[1] Luminosity (L) is the ratio of the number of events detected (dN) in a certain period of time (dt) to the cross-section (σ): $L = \frac{dN}{\sigma dt}$

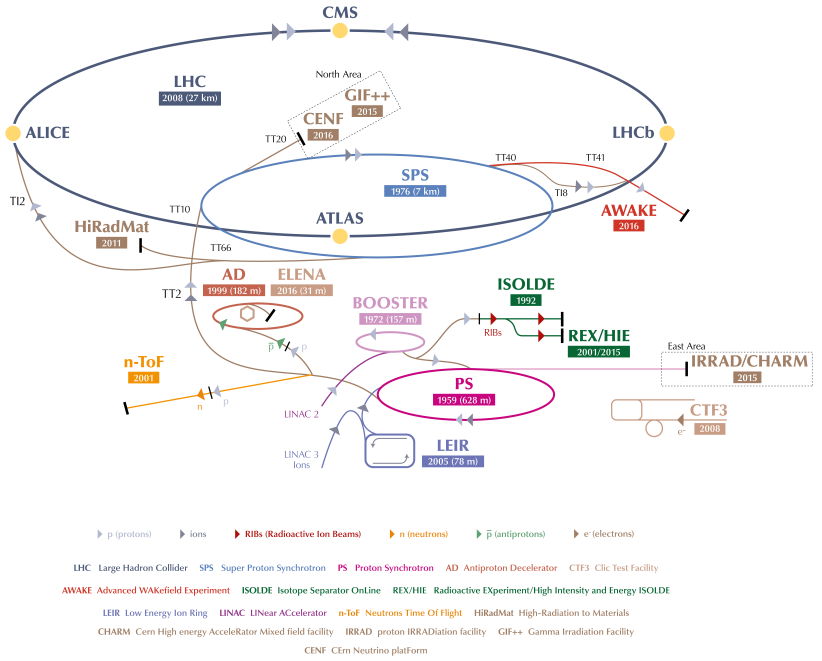

Figure 1.1: Schematic picture of the CERN accelerator complex [7].

the fact that, at high energies, both the b- and $\bar{b}$-hadrons are predominantly produced in the same forward or backward cone. The layout of the LHCb spectrometer is shown in Figure 1.2.

1.2.1 Tracking system

Reconstructing the tracks of the charged particles and measuring their momentum are, of course, very important tasks for this experiment. A distinctive feature of b-hadrons is that they travel about 1 cm inside the detector before decaying. The LHCb Tracking system consists of the VErtex LOcator system (VELO), the Tracker Turincesis (TT), a Magnet and three Tracking Stations (T1-T3). Both VELO and TT use silicon microstrip detectors, while the Tracking stations uses both silicon detectors and straw-tube detectors.

VELO

The VErtex LOcator is the sub-detector located closest to the interaction point and provides precise measurement of track coordinates, which are used to identify the secondary vertices, displaced with respect to the primary pp interaction point, that are a distinctive feature of b- and c-hadron decays. The detector is schematically illustrated in Figure 1.3. It consists of a series of 23 modules placed orthogonal to the beam and mounted in a vessel that maintains the vacuum around them. Each module is composed of two different kinds of silicon-strip sensors with high radiation tolerance: one for the radial coordinate (r) and the other one for azimuthal angle (ϕ) of the hits produced by charged particles.

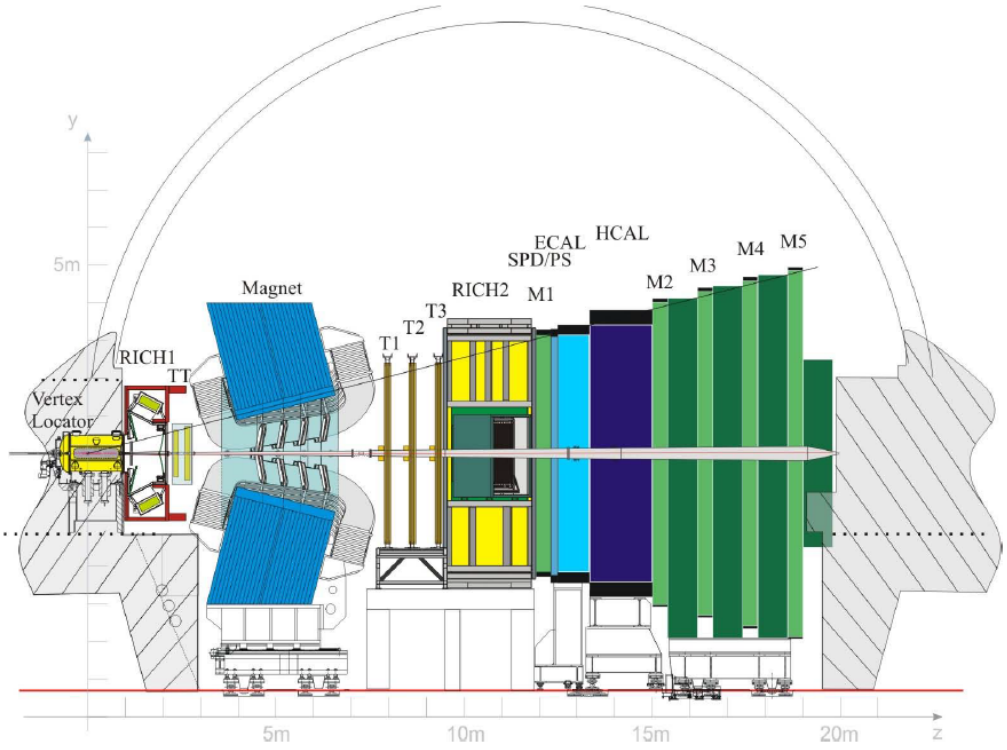

Figure 1.2: The LHCb detector. Starting from left, the following subcomponents are visible: Vertex Locator (VELO), ring imaging Cherenkov detector RICH1, Tracker Turicensis (TT), dipole magnet, tracking stations (T1-T3), RICH2, first muon station (M1), electromagnetic calorimeter (ECAL), hadronic calorimeter (HCAL), final muon stations (M2-M5) [1].

The VELO is split in a left and a right part, during the LHC injection they are maintained at a safety distance of 3 cm, but during the data taking they are closed at 7 mm from the beam axis.

Silicon Tracker

The Silicon Tracker (ST) includes two different detectors: the Tracker Turicensis (TT) and the Inner Tracker (IT). They both use silicon microstrip sensors arranged in four detection layers each.

The TT is a 150 cm wide and 130 cm high planar detector located 2.4 m far from the interaction region, between the RICH1 and the magnet. Its purpose is to match the tracks reconstructed in the VELO to the segments in the Tracking Stations downstream of the magnet. It is made of four detection layers with silicon microstrips. These strips are vertical in the first and in the fourth layer, while in the second and the third they are tilted by +5° and -5°, respectively. The resolution of the TT on the single hit is approximately 60 µm and it helps reducing the number of fake tracks, also called *g*host tracks.

The IT detector instruments the innermost region (that closest to the beampipe) of the three Tracking Stations situated right after the magnet. Each of them consists of four

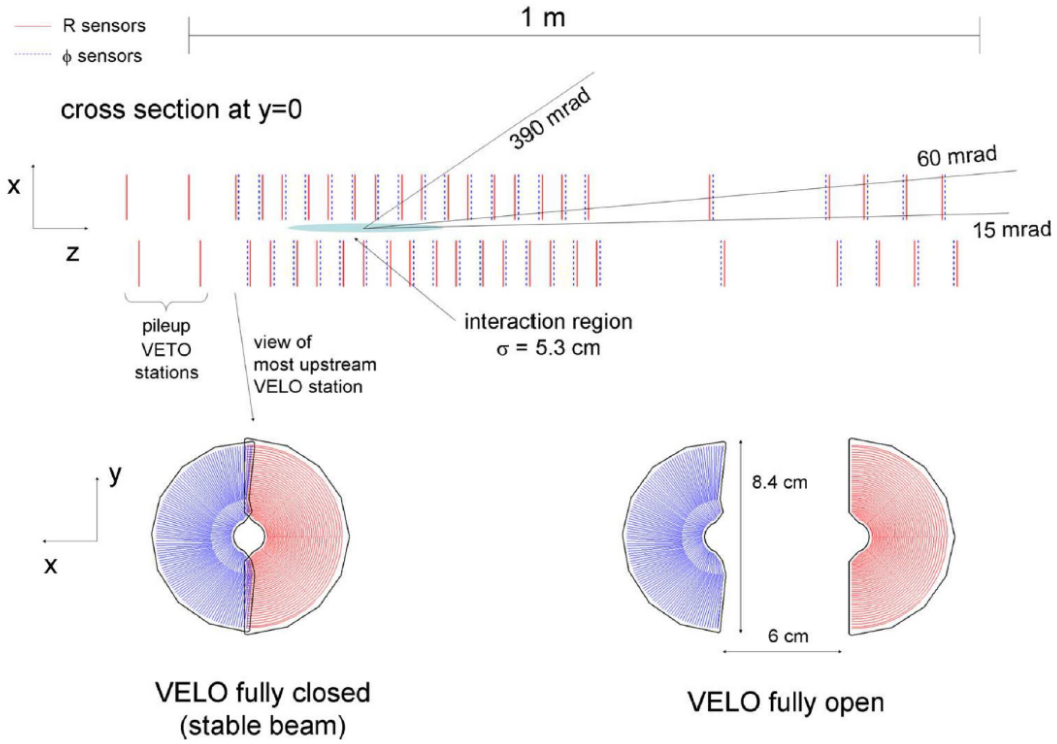

Figure 1.3: Top: sketch of the VELO module arrangement from a top view. Bottom: frontal view sketch of a VELO module in (left) open and (rigth) closed position. The two pile-up veto stations are located upstream of the VELO sensors. The radial sensors are represented in red, the azimuthal ones in blue [1].

individual detector boxes that are arranged around the beampipe. Each detector box contains four silicon detection layers, arranged as in the TT, and each of them is made of seven detector modules.

In both TT and IT, all four detection layers are maintained below the temperature of 5° C and are continuously flushed with nitrogen to avoid condensation on the cold surface.

Magnet

A warm dipole magnet is positioned between the TT and the Tracking Stations. Its aim is to bend the trajectory of the charged particles in order to measure their momentum. It is formed by two identical saddle-shaped coils, mounted inside an iron yoke (as shown in Figure 1.4). The total weight of the yoke is 1500 tons and that of the two coils is 54 tons. The maximum circulating current is 6.6 kA for an integrated bending power of 4 Tm. The direction of the magnetic field is vertical, along the vertical y-axis, therefore the charged particles are bent in the horizontal plane (x, z).[1] Of course, positive and negative particles are deflected to opposite sides, thus any detection efficiency variation between the left and the right component of the detector might affect CP-asymmetry measurements. To

[1]The system of coordinates used by LHCb is defined as a right-handed cartesian system, with the z axis along the beam direction toward the end of the detector, and the y axis pointing away from the Earth centre.

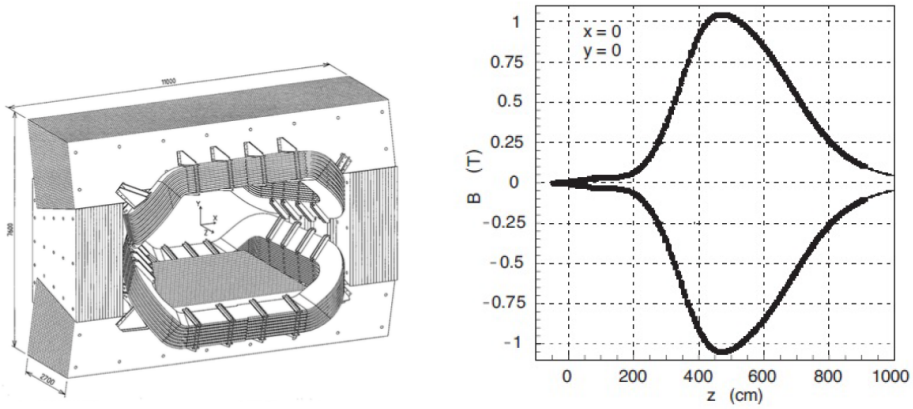

Figure 1.4: Left: schematic view of the LHCb dipole magnet. Right: magnetic field intensity along the y axis [1].

minimize this systematic effect, every few weeks of data taking the orientation of the magnetic field is inverted.

Outer Tracker

The LHCb Outer Tracker (OT) is a drift-time detector, equipping the outer part of the Tracking Stations. It is fundamental for the tracking of charged particles and the measurement of their momentum over a large acceptance area. The OT is designed as an array of three individual gas-tight straw-tube modules. Each one of those contains two staggered layers of drift-tubes with inner diameters of 4.9 mm and is filled with a mixture of Argon (70%) and CO_2 (30%) in order to guarantee a drift time below 50 ns. The detector modules together with those of IT, assemble the stations T1, T2, T3. The final resolution of these detectors is 200 μm per hit.

1.2.2 Particle Identification System

Distinguishing between different particle species is a fundamental objective of the LHCb experiment, crucial for achieving its scientific goals. Three distinct physics mechanisms are harnessed to accomplish this task.

1. **Cherenkov Emission**:

   Charged particles traversing a medium with a velocity surpassing that of light in the medium emit Cherenkov photons at a specific angle. This angle is contingent upon the medium's refractive index (n) and the particle's velocity relative to the speed of light in a vacuum (βc, where c is the speed of light in the vacuum). The Cherenkov angle (θ_c) can be expressed as $\cos\theta_c = 1/(n\beta)$. Subdetectors designed to harness Cherenkov light are denoted as Ring Imaging CHerenkov detectors (RICH).

2. **Particle Absorption**:

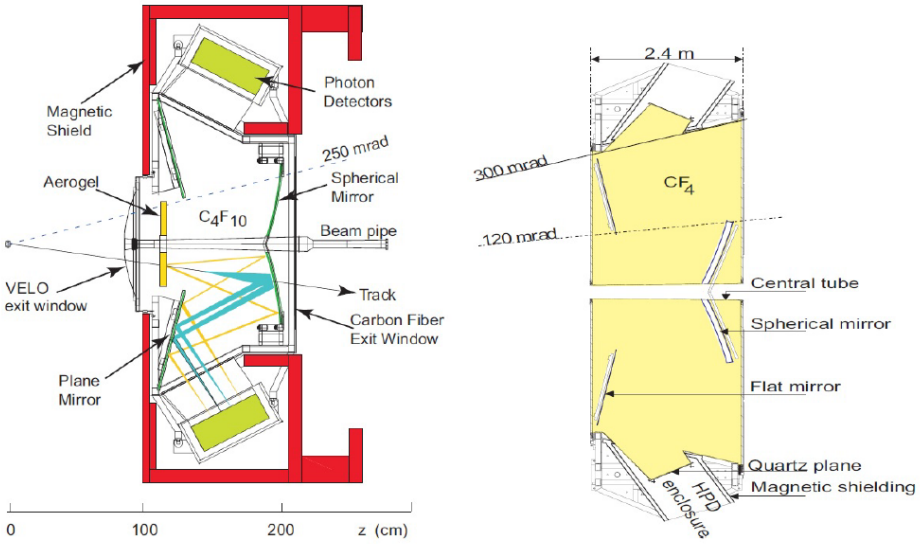

Figure 1.5: Sketches of the (left) RICH1 and (right) RICH2, sectioned along the vertical and horizontal plane, respectively [1].

Particle absorption constitutes another strategy utilized for particle species differentiation. This approach proves particularly significant for tasks such as photon identification and the distinction between electrons and pions. The task of particle absorption is entrusted to the calorimeter system.

3. **Muon Penetration**:

   The distinctive property of muons, characterized by their high penetration capabilities, serves as the basis for a specialized strategy. Specialized devices, the Muon Stations, leverage this trait to identify and differentiate muons from other particles.

Collectively, these strategies enable LHCb to distinguish between various particle species effectively. The RICH detectors, the calorimeter system, and the Muon Stations all contribute to the comprehensive and accurate identification of particles within the experimental context.

RICH

In order to cover the full momentum range of the particles under study (from few GeV/c up to 100 GeV/c and beyond), LHCb counts two RICH detectors. The first one is situated between the VELO and the TT, while the second one is placed between the tracking station and the first station of the muon detector. Both detectors are depicted in Figure 1.5. In both RICH detectors, the focusing of Cherenkov light is achieved through a combination of spherical and flat mirrors. These mirrors direct the light out of the spectrometer's acceptance region, where photodetectors are located within a shield to counteract the influence of any residual magnetic field. Notably, RICH1 employs a vertical optical layout, while RICH2 utilizes a horizontal optical layout. This configuration ensures optimal

performance and effective utilization of the Cherenkov emission phenomenon for particle species identification within the LHCb experiment.

Hybrid Photon Detectors (HPD) are used to detect single Cherenkov photons, in a range of wavelengths between 200 and 600 nm. When these photons impinge upon the photocathode, they prompt the emission of photoelectrons. Subsequently, these photoelectrons undergo multiplication, leading to the generation of an electric signal that can be detected.

The adopted pattern recognition strategy operates as follow: utilizing information about the positions and directions of all particle tracks, the probability of observing a specific pattern on the HPD plane can be computed. Naturally, this outcome is contingent upon the assigned mass hypothesis for each particle. Following this method, the challenge is addressed by identifying the mass-hypothesis association that maximizes the likelihood between the predicted pattern and the actual pattern observed on the HPD planes.

Calorimeters

The LHCb calorimeter system, positioned between the first (M1) and second (M2) Muon Stations, comprises several key components: an electromagnetic calorimeter (ECAL), accompanied by a Pre-Shower (PS) and a Scintillating-Pad Detector (SPD) positioned in front of it, as well as a hadronic calorimeter (HCAL). This system serves multiple crucial functions within the experiment. The system is instrumental in selecting candidates for hadrons, electrons, and photons based on their transverse energy, particularly at the trigger level.[2] Additionally, it performs the essential tasks of identifying electrons, photons, and hadrons, while also accurately measuring their energies and positions. The fundamental operational principle remains consistent across all calorimeters: scintillation light, produced by the charged component of electromagnetic and hadronic showers, is conveyed to a MultiAnode PhotoMultiplier (MAPMT) through wavelength-shifting (WLS) fibers. The MAPMT subsequently generates the readout signal. The ECAL (as depicted in Figure 1.6) is an electromagnetic calorimeter based on shashlik[3] technology. Its cells consist of 66 lead slices, each with a thickness of 2 mm, sandwiched between two polystyrene-based scintillator plates, each with a thickness of 4 mm. The size of the cells varies to accommodate for different occupancies going farther from the beampipe. In the innermost region, where the occupancy is higher, their size is 4×4 cm^2, then it becomes 6×6 cm^2 in the middle region, and finally 12×12 cm^2 in the outermost region. These layers incorporate hole patterns to accommodate the aforementioned WLS fibers. The ECAL's overall dimensions are 7.8 m in width and 6.3 m in height. The PS and SPD serve as auxiliary systems located in front of the ECAL. The SPD enhances the discrimination between charged and neutral particles by detecting light emitted in the scintillator for the former, but not for the latter. Conversely, the PS helps in distinguishing between electrons, which typically initiate their showers earlier, and photons, which are more penetrating. The HCAL (as depicted in Figure 1.7) comprises scintillator planes that are 4 mm thick and alternated with iron plates that are 16 mm thick. The arrangement of

[2]As transverse energy it is meant the product $E_{\mathrm{T}} = E \sin\theta$, where θ is the angle between the beamline and the particle direction.

[3]In high-energy physics detectors, it denotes a specific arrangement employed in sampling calorimeters. It involves a configuration characterized by the stacking of alternating layers comprising absorber materials (such as lead or brass) and scintillator materials (crystal or plastic). Crucially, this assembly is traversed

Figure 1.6: Left: downstream view of the ECAL installed (but not completely closed). Right: outer, middle and inner type of ECAL modules [1].

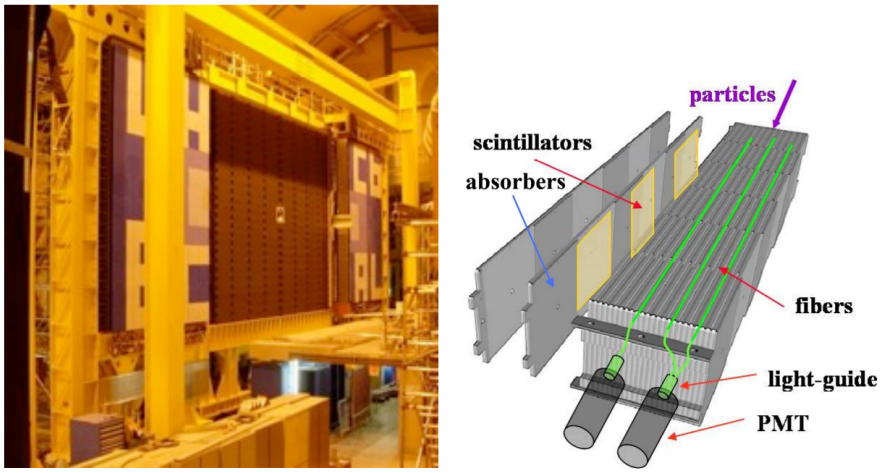

Figure 1.7: Left: view from upstream of the HCAL detector installed behind the two retracted ECAL halves. Right: Sketch of the internal cell structure of HCAL [1].

tiles is parallel to the beam direction. The primary utility of the HCAL is to provide trigger information that doesn't necessitate precise energy measurements.

Muon Stations

The Muon Stations, depicted in Figure 1.8, comprise a set of five rectangular stations denoted as M1 through M5, positioned along the beam axis. This comprehensive system encompasses a total of 1380 multiwire proportional chambers, collectively spanning an area of 435 m^2. The space between M1 and M2 accommodates the calorimeter system, while the regions between M2 and M5 are interspersed with 80 cm thick iron absorbers. The primary objective of the muon stations is to detect muons as they traverse through them. The absorbers serve the purpose of sequentially selecting more penetrating particles at each stage. For a muon to successfully traverse all five stations, it generally requires a minimum momentum of around 6 GeV/c. The design of these stations enables them

by wavelength-shifting fibers that run perpendicular to the absorber and scintillator tiles.

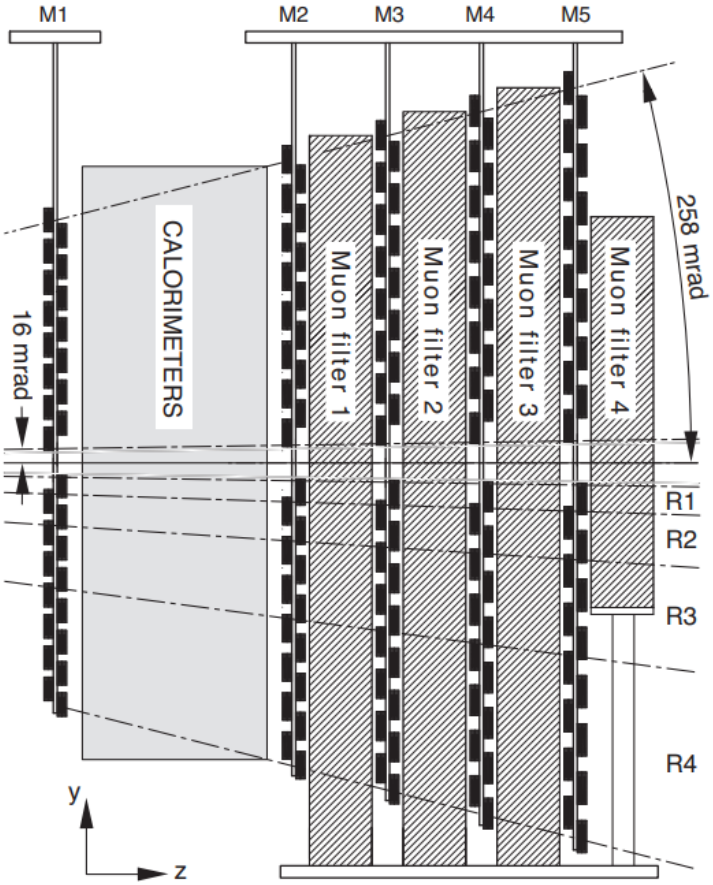

Figure 1.8: Schematic view of the Muon Stations [1].

to handle a particle rate of up to 500 kHz/ cm^2 of charged particles. The initial three stations (M1-M3) are particularly adept at enhancing the transverse momentum resolution, which is facilitated by their high spatial resolution. Conversely, the latter two stations (M4-M5) exhibit more limited spatial resolution, as their primary role is to effectively identify highly penetrating particles. The LHCb detector boasts remarkable efficiency in identifying muons with a momentum above 10 GeV/c. It attains an identification efficiency surpassing 90%, coupled with a mis-identification rate below 1%.

1.2.3 Trigger

The LHCb detector generates an extensive volume of data that requires careful management. To tackle this challenge, the trigger system responsible for data acquisition and reduction operates across three distinct levels. The first level, referred to as L0, is hardware-based and synchronized with the LHC's bunch crossing rate of 40 MHz. The subsequent two levels, termed High Level Trigger 1 and 2 (HLT1 and HLT2), employ software algorithms and save their resultant data to mass storage.

The L0 level leverages the characteristic exhibited by the decay products of b- and

c-hadrons, namely a higher transverse momentum compared to the average particles produced in a pp collision. The L0 is subdivided into three sub-systems, each linked to different sub-detectors: L0 pile-up, L0 calorimeter and L0 muon. These subsystems aggregate relevant information, which is then conveyed to a decision unit (DU). The DU ultimately determines whether the event should be accepted or rejected. This process is completed in approximately 4 µs.

The HLT1 level of the trigger system undertakes an initial phase of event reconstruction by utilizing information derived from the tracking system. Throughout the reconstruction process, successive criteria are applied to effectively filter out irrelevant events. The procedure commences with the VELO, where tracks segments and primary vertices (PVs) are constructed. These tracks and vertices are subsequently correlated with hits registered on the TT, enabling an initial estimation of their charge and momentum. Subsequently, minimum momentum (p) and transverse momentum (p_{T}) thresholds are enforced, and the input from other tracking stations is incorporated to refine the reconstruction process. The HLT2 level, on the other hand, executes a more accurate and complete event reconstruction that capitalizes on information derived also from RICH detectors and calorimeters. This enhanced reconstruction process ensures a more comprehensive analysis of the event, contributing to a refined understanding of the data and facilitating the identification of relevant events for further analysis.

1.3 The LHCb Upgrade I

During the period from 2018 to 2022, the LHC underwent its second Long Shutdown (LS2), as shown in Figure 1.9, that was used also for the first major upgrade of the LHCb experiment, that goes under the name of LHCb Upgrade I [3]. The LHCb Upgrade I is currently operating in the Run 3 of the LHC and will continue his work in Run 4 at an instantaneous luminosity of $L = 2 \times 10^{33}\ \mathrm{cm}^{-2}\,\mathrm{s}^{-1}$ which is an increase of a factor 5 with respect to Run 2. As a consequence the detector has to be able to process a much higher data rate and withstand the radiation damage of the higher track multiplicity. Consequently a comprehensive replacement of the tracking system was carried out. This included an upgraded VELO, the introduction of the Upstream Tracker (UT) upstream of the magnet as a replacement for the TT, and the implementation of the Scintillating Fibre Tracker (SciFi) as the primary tracking detector downstream of the magnet in lieu of the IT and OT. Furthermore, substantial modifications were made to the trigger system, a key aspect of the experiment. The upgraded VELO was engineered to manage the heightened track multiplicity and radiation dose stemming from the augmented luminosity, while sustaining or even improving upon the physics performance of its predecessor. To achieve this, the silicon-strip based modules were entirely replaced with modules based on silicon pixels. This change in design not only enhanced granularity but also incorporated a custom read-out ASIC named VeloPix. The Upstream Tracker (UT) succeeded the previous TT as the tracking system positioned upstream of the LHCb dipole magnet. This silicon-based detector was optimized for the LHCb upgrade, featuring increased granularity, particularly in proximity to the beam pipe, to accommodate the amplified track multiplicity. A notable alteration in the trigger system was the removal of the L0 hardware trigger stage, previously described in Section 1.2.3. This decision stemmed from the pronounced L0 trigger inefficiencies observed for numerous decay modes central to

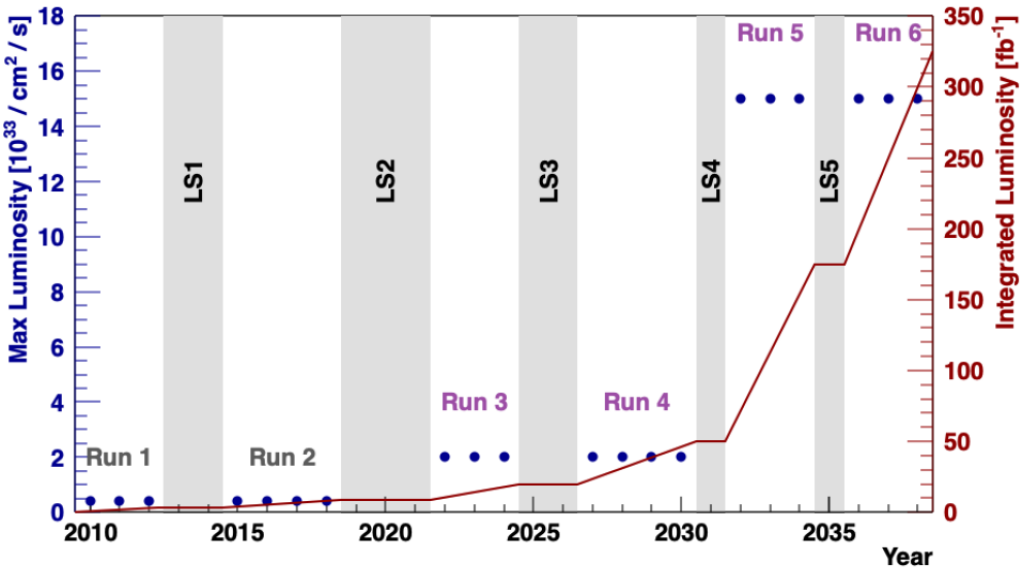

Figure 1.9: Integrated luminosity profile for the original LHCb, LHCb Upgrade I and LHCb Upgrade II experiments. Blue points are the anticipated maximum instantaneous luminosity, whilst red lines are the accumulated integrated luminosity.

the LHCb physics programme, particularly for those with fully hadronic final states. By the end of LHC Run 4, in 2030, the experiment will have accumulated a data sample of around 50 fb^{-1}. Further data taking with the Upgrade I detector will not be interesting, as adding little statistics to the already collected one. In addition, beyond this date many of its components will have reached the end of their natural life span in terms of radiation exposure. In conclusion then, the LHCb Upgrade I, will improve the sensitivity of many flavour studies but the precision of the measurements will still be limited by statistics. That's why there is strong motivation to further upgrade the detector and to build LHCb Upgrade II.

1.4 The LHCb Upgrade II

Experimental studies over the past several decades cemented the Standard Model (SM) as a formidable theory of particle interactions. The ultimate proof has been the results from the first two runs of the LHC, both in the Higgs sector at ATLAS and CMS and the flavour sector in LHCb, where there is no deviation from SM prediction, so far. Nonetheless, there is a multitude of observed phenomena that the SM does not predict and struggles to explain, including the matter-antimatter discrepancy in the Universe, neutrino masses and dark matter. All these factors provide a convincing case for the existence of new physics (NP) beyond the SM. This is what is behind the proposal, presented in 2017 [8], of the LHCb Upgrade II experiment, which is intended to take full advantage of the flavour-physics opportunities at the High Luminosity LHC (HL-LHC). Ideally, the detector will be installed during the Long Shutdown 4 of the LHC (LS4), and it will start taking data during Run 5, currently scheduled for 2032. It will be able to operate at

the peak luminosity of 1.5×10^{34} cm^{-2} s^{-1}. Similarly to the past, its physics programme will include flavour-physics measurements, spectroscopy studies, QCD and electroweak physics, heavy ion and fixed target opportunities, and long-lived particle searches [9]. In Figure 1.9 one can appreciate the integrated luminosity profile during the full lifetime of the experiment and the expected period for the start of the LHCb Upgrade II project.

1.4.1 Detector challenges

The LHCb Upgrade II data sample will be significantly larger than that of any other flavour-physics experiment, either existing or planned, and will lead to improvements in the precision of a large number of observables. The challenges of performing precision flavour physics at the high luminosities under consideration are daunting. The expected mean number of interactions per pp bunch-crossing is around 40, which leads to much higher particle multiplicities and rates than in the previous runs. This is, of course, good from a statistical point of view but makes data difficult to handle and radiation damage becomes a great concern for all sub-detectors too. Despite that, the exploitation of the LHCb Upgrade II physics programme assumes that the current detector performance is maintained, and even improved in certain specific domains. For this reason, developments of sensors and computing beyond the state-of-the-art is needed. Indeed, an essential attribute, not present in the Upgrade I version of the detector, will be *p*recision timing. Being able to time-tag particles with a resolution of few tens of ps will allow charged tracks and photons to be associated with the correct interaction vertex, thereby suppressing combinatorial background [4].

1.4.2 Detector changes

In the new project [4], the existing footprint of the spectrometer remains unaltered, together with the current sub-detectors arrangement. However there are a few new features, for instance, the magnet's side walls will be covered by additional tracking stations, the hadron calorimeter (HCAL), in front of the muon detector, will be replaced by additional shielding and, ahead of the RICH2, a time-of-flight detector (TORCH) will be added. Nevertheless significant technical improvements in existing sub-detectors are needed.

The VELO upgrade is probably the most important, indeed, as the new detector must be able to both efficiently and precisely reconstruct the trajectories of charged particles and also correctly assign them to the primary or secondary vertices in which they were produced. In addition, it has to overcome a huge amount of radiation without letting them affect its performance. In order to achieve this, the idea is to increase the detector granularity and add timing information with a precision of better than 50 ps per single hit, transforming the VELO to a true 4D-tracking detector. This new time information is highly useful and can be employed in many ways. For example, a powerful new handle to ensure the correct assignment of tracks to PVs is to exploit the spread in time of the vertices of approximately 180 ps, as illustrated in Figure 1.10, which shows how a reduced subset of vertices can be selected by applying requirements on the track timestamps. In Figure 1.11, the comparison between the performance of the VELO Upgrade I operating at the Upgrade I and Upgrade II conditions, respectively, is illustrated. It can be seen that, with no timing information, the efficiency drops

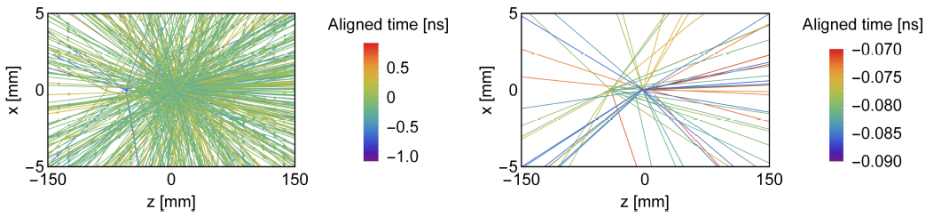

Figure 1.10: Illustration of the track density generated by 42 collisions spread over a bunch crossing. On the left the whole bunch crossing time period is considered (≈ 1 ns), while on the right a time cut of 20 ps is applied [4].

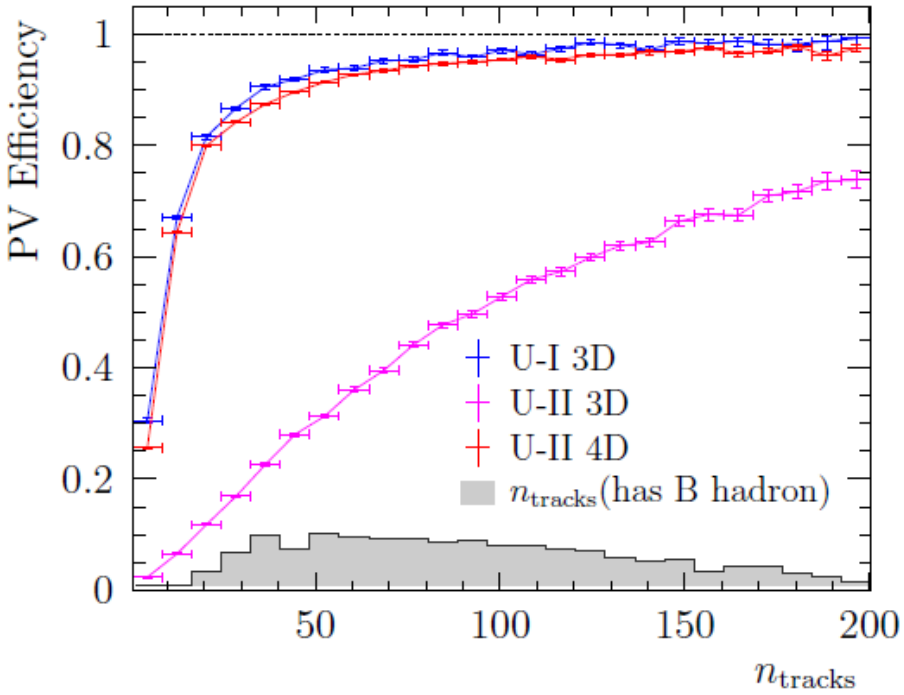

Figure 1.11: Reconstruction efficiency against the number of tracks per primary vertex, comparing the Upgrade I 3D reconstruction in the Upgrade I and Upgrade II conditions, with the Upgrade II detector in Upgrade II conditions using time information (4D). The grey solid area shows the distribution of the number of tracks per primary vertex [10].

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dramatically at the higher occupancies, but, the VELO Upgrade I performance can be recovered with the addition of time information.

Chapter 2

Acquisition board

After the introduction of the LHCb experiment and its upgrades in the first chapter, in this one the instrumentation identified as suitable for the digitisation and acquisition of signal pulses will be described. Hereafter the equipment used in this study is introduced: the acquisition board, how it's made, how it works and the other devices needed for the calibration of the digitised pulses registered by the board itself. In Section 2.1 the DRS4 chip [11], at the basis of the acquisition board used in this study, is described. In Section 2.2 is presented the actual board, CAEN V1742, and finally, in Section 2.3 a brief overview of the waveform generator used in the calibration of the CAEN V1742 board is given.

2.1 The Domino Ring Sampler

The Domino Ring Sampler (DRS), of which a schematic rappresentation is given in Figure 2.1, is a Switched Capacitor Array (SCA) capable of sampling 9 differential input channels at a sampling speed varying from 700 Mega Sample Per Second (MSPS) up to 5 Giga Sample Per Second (GSPS). It was developed in Switzerland at the Paul Scherrer Institut (PSI), fabricated on an advanced CMOS process in a radiation hard design. The working principle of the DRS is to use an array of capacitors in sample-and-hold mode. A fast sequence of write pulses allows the recording of analog wave forms in these capacitors, which can later be read out and digitized at a much lower speed; of course, this brings the disadvantage that the time required to read out the capacitor cells causes dead time. The chip's domain of application is centered around scenarios where a low trigger rate is encountered, coupled with a demand for exceptional time resolution and effective pile-up rejection. The model used in this work is the DRS4 [11], designed in 2007 with an increased bandwidth of 950 MHz and fixing some flaws of the previous model (DRS3). The analog waveform is stored in 1024 sampling cells per channel, and can be read out via a shift register clocked at 33MHz. The write signal for the sampling cells is generated by a chain of inverters (domino principle). The domino wave is running continuously until stopped by a trigger. A read shift register clocks the contents of the sampling cells either to a multiplexed or to individual outputs, where it can be digitized with an external ADC. It is possible to read out only a part of the waveform to reduce the digitization time. Notable applications encompass particle physics within the intensity frontier, for instance: Cherenkov telescopes employed in gamma-ray astronomy, time-of-flight (TOF) implementations, and neutrino physics. Additionally, the application scope extends to

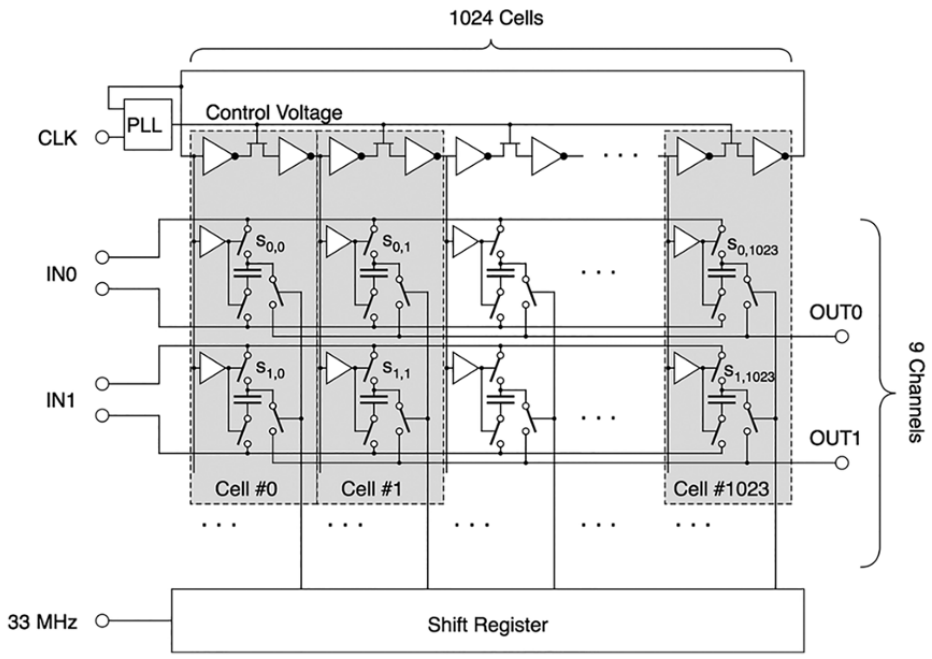

Figure 2.1: Simplified schematics of the DRS4 chip [5].

medical imaging, particularly positron emission tomography (PET), wherein time-of-flight assumes a pivotal role. In such contexts, SCAs emerge as promising candidates for future utilization.

2.1.1 Operation principles

The DRS4 [12] consists of an on-chip inverter chain generating a sampling frequency up to 6 GHz. This signal opens write switches in all 9 sampling channels, where the differential input signal is sampled in small (150 fF) capacitors. After being started, the domino wave runs continuously in a circular fashion until de-coupled from the write switches by a trigger signal, which freezes the currently stored signal in the sampling capacitors. The signal is then read out via a read shift register for external digitization. In the next subsections the most important components of the chip, such as Domino Wave Circuit, Phase-Locked Loop, aperture jitter, analog input, registers and waveform readout, are briefly described.

Domino Wave Circuit

The domino wave circuit is basically a series of 1024 double inverters. Upon elevating the DENABLE signal, a propagating wave courses through these inverters, culminating in the generation of the write signal intended for the sampling cells. The simplified schematic presented in Figure 2.2 elucidates the configuration of two double inverter blocks. The first inverter is actually a NAND gate. This allows the domino wave to be enabled and stopped at any time via the DENABLE signal. The NAND gate is connected to the following inverter via an NMOS transistor operating as a voltage controlled resistor. Since the

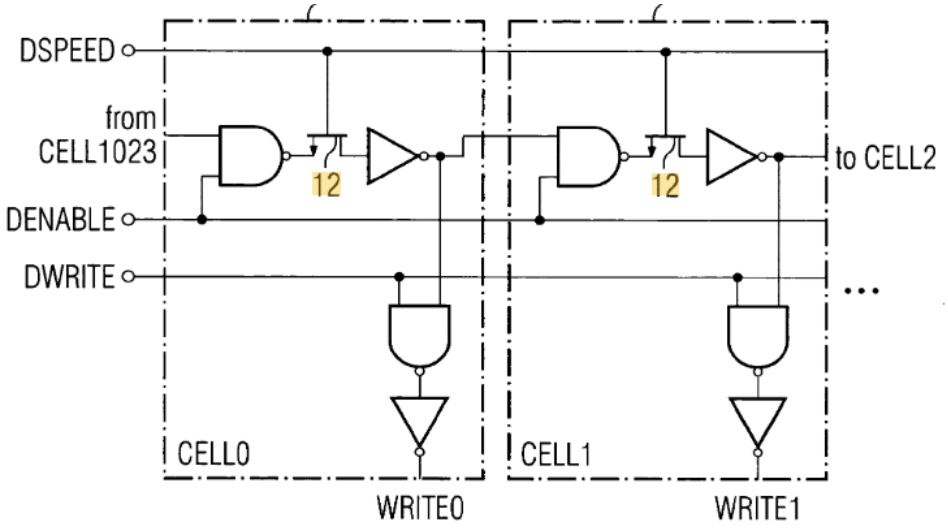

Figure 2.2: Simplified schematics of two out of 1024 double inverter blocks forming the domino wave circuit [11].

actual domino wave speed depends on the power supply voltage and the temperature, some stabilization is necessary to ensure steady operation. A widely adopted strategy involves the implementation of a phase-locked loop (PLL) mechanism, serving to synchronize the sampling frequency with an external clock.

Phased-Lock Loop

A Phase-Locked Loop (PLL) is a control system that generates an output signal whose phase is related to the phase of an input signal. One of the most basic type of PLL is an electronic circuit consisting of a variable frequency oscillator and a phase detector in a feedback loop. By manipulating the applied voltage, one can exert control over both the phase and frequency of the oscillator, hence the nomenclature "Voltage-Controlled Oscillator" (VCO). Within this arrangement, the VCO operates as a creator of periodic signals with predetermined frequencies. Subsequently, the phase detector evaluates the phase alignment between this VCO-generated signal and the phase of the input periodic signal. This feedback loop serves the pivotal role of continually adjusting the VCO's frequency to uphold phase synchronization. This endeavor of sustaining alignment between input and output phases is concomitant with the preservation of congruent input and output frequencies. Incorporating a phase-locked loop facilitates not only signal synchronization but also the capacity to track an input frequency or generate a frequency that stands as a multiple of the input frequency. Consequently, the phase-locked loop stands as a versatile tool encompassing a spectrum of applications, from signal synchronization to frequency generation and multiplication.

Aperture Jitter

A minor timing jitter emerges amid the double inverter blocks, which subsequently leads to non-uniform time intervals for the sampling process. This phenomenon engenders what

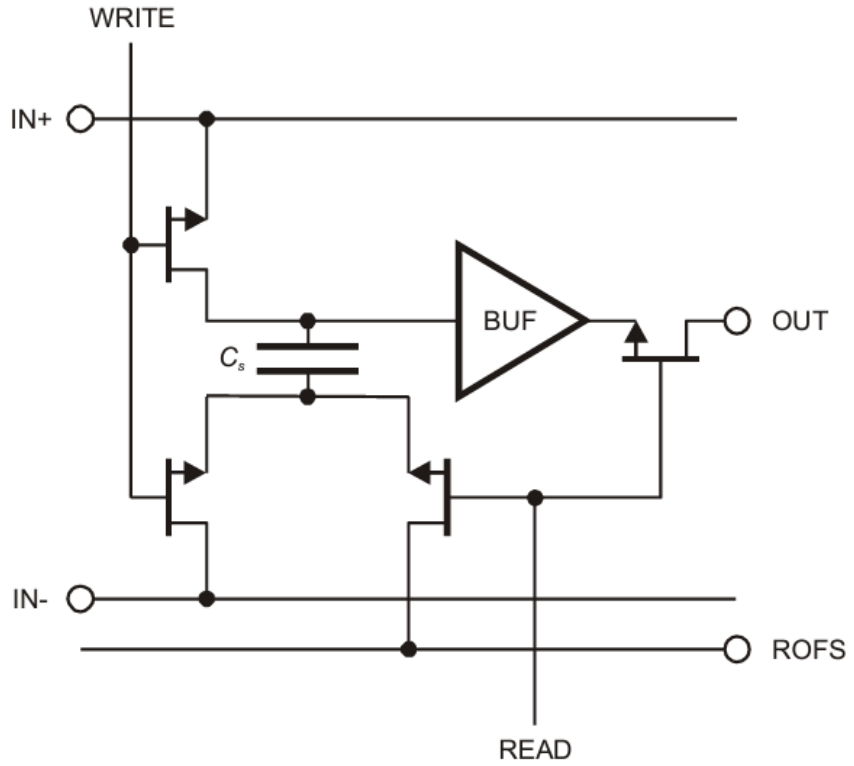

Figure 2.3: Simplified schematics of one sampling cell [12].

is termed an "aperture jitter" when sampling an analog input signal. This aperture jitter encompasses two distinct components: a consistent deviation for each cell known as the "fixed pattern aperture jitter," stemming from transistor mismatch within each cell, and a variable term inherent to each domino wave revolution termed the "random aperture jitter." Despite the implementation of a PLL to stabilize the average sampling frequency, as discussed earlier, variations between individual cells persist. If applications require high timing accuracy, the fixed pattern jitter can be calibrated and corrected and this is exactly the purpose of this thesis. In general accuracy of few picoseconds can be achieved.

Analog Input

Each sampling cell consists of a sampling capacitor with $C_s = 150$ fF connected to the IN+ and IN- inputs via two NMOS transistors, as illustrated in Figure 2.3. Ensuring that the signal source exhibits sufficient driving capability to provide the necessary current for charging these capacitors is a critical consideration. For instance, when operating at a sampling speed of 6 GHz, it becomes imperative to have an input current of approximately 1 mA to adequately charge the capacitors, especially in scenarios involving a 1 V signal. After the sampling cycle, the capacitors store the voltage.

$$U_s = U_{IN+} - U_{IN-}$$

It's essential to bear in mind that the charge accumulated within the sampling capacitor gradually dissipates over time due to charge leakage. Consequently, to counteract this

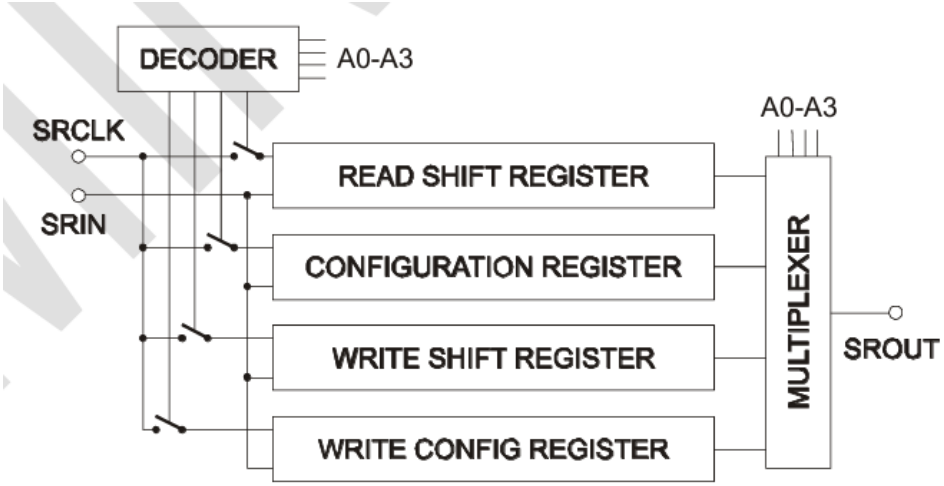

Figure 2.4: Sharing of shift register signals [12].

phenomenon, the readout of a cell must be executed promptly (< 1 ms) subsequent to the completion of the sampling phase. This expeditious readout timeframe is crucial to mitigate the impact of charge leakage, maintaining data integrity and accurate representations of the input signal.

Registers

The DRS4 chip is equipped with four distinct shift registers, which are crucially accessed for configuration purposes and during the readout process. In a strategic move to limit the requisite number of package pins, a shared interface approach utilizing the three signals, namely the SRIN, SRCLK, and SROUT, has been adopted. This interface is supplemented by an addressing schema employing four bits, comprising a decoder and a multiplexer, as depicted in Figure 2.4. The address inputs A3-A0 contribute to this addressing mechanism. While the SRIN signal is directly connected to all shift registers, the SRCLK is enabled only for a certain shift register if it is addressed. Similarly, the SROUT signal is multiplexed between the outputs of the four shift registers.. Depending on the bit settings the chip assume different configurations. For example, with the configuration 0010 Channel 2 is selected by the multiplexer (MUX), while with 1111 all output drivers are disabled and the internal bias generators are switched off to minimize power dissipation (Standby mode).

Waveform Readout

Once sampling has been stopped by either setting the corresponding command signals low, the waveform can be readout via the shift register. There are two possible modes for readout. The "Full Readout Mode" reads all 1024 cells while the "Region-of-Interest Readout mode" only reads a certain window of the waveform reducing dead time. This mode accomplish one of the design goal for SCA which is to minimize the readout time. Indeed, particle detectors produce normally only short pulses, so most of the sampling cells usually contain "baseline" values. The contents of the 9 DRS4 channels can either be

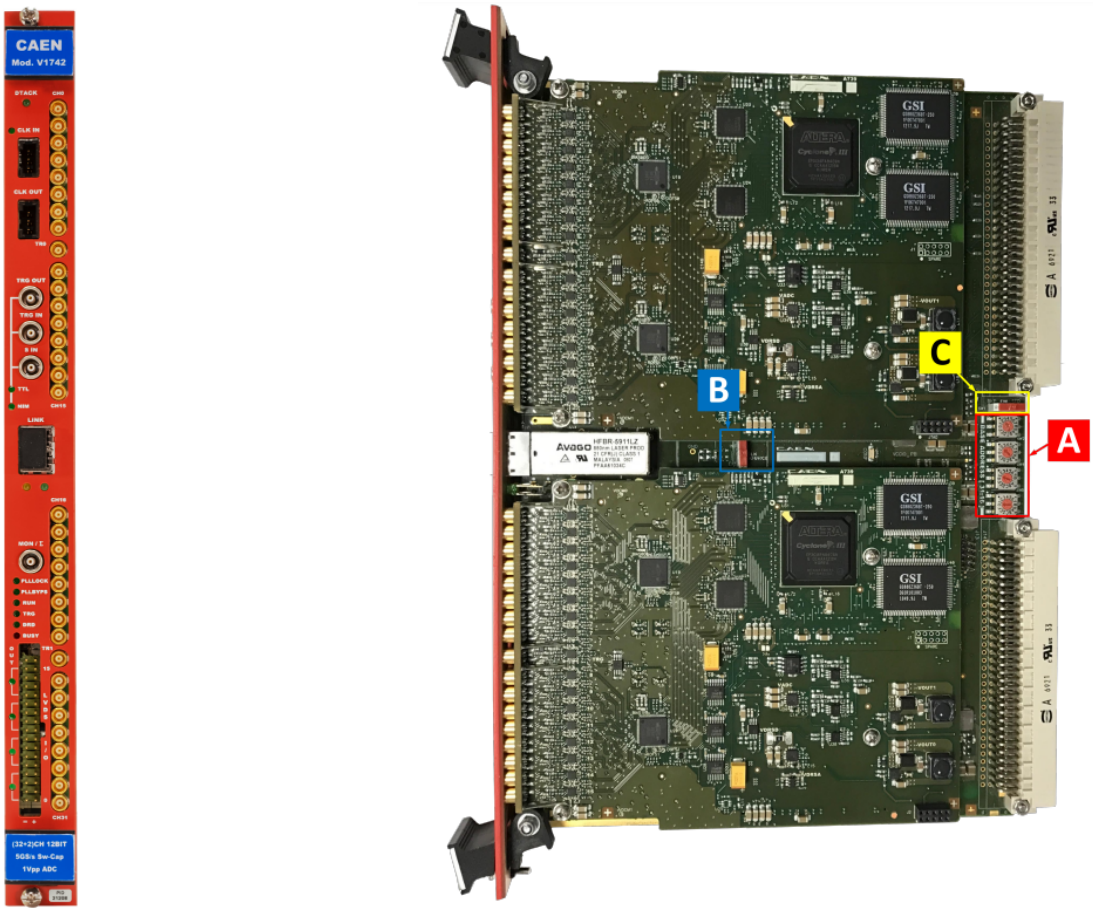

Figure 2.5: Left: front panel view of the CAEN V1742 digitisier. Right: electronical components of the CAEN V1742 digitiser viewed from above [13].

digitized with a single external ADC using the internal multiplexer, or with eight external ADCs in parallel to reduce dead time.

2.2 Waveform digitiser CAEN V1742

Now that we have described the general type of technology used, we can delve into more specifics and particularly see which measuring instrument was the object of our calibration work. The acquisition board that we have been using is the model V1742 developed by CAEN ELS [13], equipped with four DRS4 chips for a total of 32+2 channels, each one digitised with 12-bit ADC, and a sampling frequency up to 5 GSPS. In addition the 9th channel of the first and second chips are coupled to the same input, as well as the 9th channel for the third and fourth chips.

2.2.1 Overview

The analog input signal is continuously sampled by the 1024 capacitive cells of the DRS4 in a circular way, at a frequency that is software selectable amongst 5 GHz, 2.5 GHz, 1 GHz, and 750 MHz. In line with the chip upon which it is based, the analog to digital

conversion is not simultaneous with the chip sampling phase, and it starts as soon as the trigger condition is met. When the trigger stops the DRS4 chip sampling (holding phase), the analog memory buffer is frozen, and the cell content is made available to the 12 bit ADC for the digital conversion. The chip functioning has two major consequences:

- there is an unavoidable dead-time when the DRS4 chip stops its acquisition and the ADC converts the capacitances (about 110 µs);
- the acquisition window is fixed to 1024 samples, that in case of 5 GHz corresponds to a maximum of about 200 ns.

Moreover, the trigger processing introduces a latency between the trigger arrival and the DRS4 holding phase that varies according to the trigger source. There are four possible trigger sources available:[1]

1. *Software Trigger*, common to all enabled groups, mainly intended for debug purposes.
2. *External Trigger*, trigger on TRG-IN connector, common to all enabled groups.
3. *Fast (Low Latency) Local Trigger*, trigger on TR0 and TR1 connectors, common to pairs of 8-channels groups. This mode is called "Fast" or "Low Latency" since the trigger latency is reduced with respect to the external trigger.
4. *Self-trigger*, common to couples of 8-channels groups.

2.2.2 Functional Description

Analog Input

The default input dynamic of the V1742 CAEN digitiser is 1 V_{pp}[2] on a single-ended MCX coaxial connector with impedance $Z_{in} = 50\ \Omega$. In order to preserve the full dynamic range according to the polarity of the input signal (bipolar, positive unipolar, negative unipolar), it is possible to add a DC offset by means of a 16-bit DAC, which is up to ±1 V DC. The input bandwidth ranges from DC to 500 MHz. The additional channels available for the TRn ($n = 0, /, 1$) connector, and dedicated to the low latency triggers, other than acting as a fast trigger can also be digitized and saved into memory. The TRn appears as the 9^{th} channel of each group in the final readout. The input dynamics is then attenuated by a factor of 2 to make it compliant with the 1 V_{pp} dynamics of the other channels.

Domino Ring Sampling

The analog input signals undergo a continuous sampling process facilitated by the DRS4 (Domino Ring Sampler) chip. This chip is equipped with an on-chip inverter chain, capable of generating a maximum sampling frequency of 5 GSPS. Furthermore, programming allows for alternative frequencies of 2.5 GSPS, 1 GSPS, and 750 MSPS. Within the board configuration, each group features one chip, and within each chip, there exist 1024 capacitor cells per channel, responsible for the high-frequency analog sampling of the input signal. The record length of an acquisition is inherently tied to the count of these

[1] For our purposes, only the first two configurations have been used.

[2] With V_{pp} is meant the voltage difference between maximum and minimum value (peak-to-peak voltage).

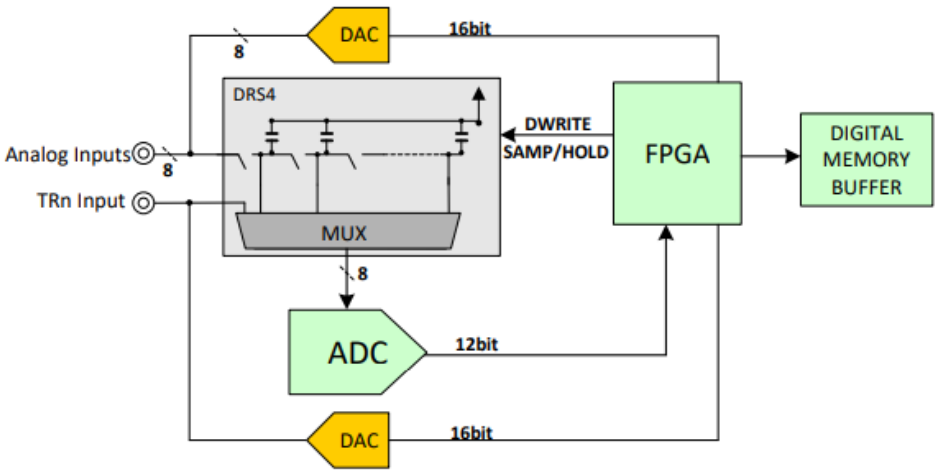

Figure 2.6: Input diagram of the DRS4 chip [11].

capacitor cells, mandating a fixed length of 1024 samples. While options allowing 512, 256, and 136 samples can be chosen through software, with the intent of reducing data transfer volume, it's important to note that all 1024 cells undergo conversion regardless. This implies that, while the options reduce the transferred data volume, they do not lead to dead-time reduction. Functionally, the DRS4 chip maintains a continuous circular sampling of the input signal, repeatedly overwriting the samples until the acquisition is halted by a trigger signal, a phase termed the "holding phase." Upon cessation, the cells release their stored charges at a readout frequency under the control of the FPGA (Output Mode). To perform the subsequent digitization process, the analog samples are subjected to digitization through a 12-bit ADC, operating at a frequency of 29.296 MHz; this constitutes the low-frequency digital sampling phase. The output from the ADC is stored in the Digital Memory Buffer by the FPGA, subsequently rendering the data accessible for readout. The complete workflow is illustrated in Figure 2.6.

TR0 and TR1 Inputs

The module features two fast trigger inputs TR0 and TR1 with extended level amplitude; TR0 is common to group 0 (ch[7..0]) and group 1 (ch[15..8]), TR1 to group 2 (ch[23..16]) and group 3 (ch[31..24]). TRn signal can be used as external trigger. Moreover, they can be also sampled into the DRS4s analog memory buffers for applications where high resolution timing and time analysis with a common reference signal (like a trigger or system clock) is required.

2.2.3 CAEN WaveDump

CAEN provides software tools to interact with their digitizers. The one that has been used in our laboratory is WaveDump, a basic console application, with no graphics, supporting only CAEN digitizers running the waveform recording firmware. It allows the user to program a single board (according to a text configuration file containing a list of parameters and instructions), to start/stop the acquisition, read the data, display the

readout and trigger rate, apply some post-processing, save data to a file and also plot the waveforms using Gnuplot, a third-party graphing utility. WaveDump is a very helpful example of C code demonstrating the use of libraries and methods for an efficient readout and data analysis.

2.2.4 Data Correction

As repeatedly mentioned before, the purpose of this work is to calibrate the V1742 board such that its contribution to the total time resolution for the acquisition system is small when compared to the final required resolution (that means below 5 ps). Indeed, the DRS4 chip needs data corrections due to the unavoidable differences in the chip construction process. Of course, the manufacturing company provides its own calibration service, which will be interesting and useful to compare with the one carried out by us, as can be observed in Chapter 3. The corrections are managed at software level, while the firmware on-board retrieves the raw data. There are three available corrections:

1. **Cell Index Offset correction**, which compensates the signal offset for the differences in cell amplitudes.

2. **Sample Index Offset correction**,which corrects the signal offset for a noise over the last 30 samples.

3. **Time correction**, which compensates the differences of the delay line of the chips.

The default correction tables are provided by CAEN in the memory flash of the board. WaveDump software then can retrieve the tables and make the appropriate corrections. The user can leave the software automatically apply all the corrections, or decide which correction applies to which group through the CORRECTION_LEVEL function of WaveDump.

2.3 Waveform Generator

As will be clear from the calibration procedure described in Chapter 3, the calibration process necessitates the use of a waveform generator. The one that has been chosen for this task is the model 33622A, produced by Keysight Technologies [14]. It is based on Trueform signal generation technology, which offers more capability, fidelity and flexibility than previous generation Direct Digital Synthesis (DDS) generators.

All the specification about this tool can be found in his data sheet [14]. Here are only the relevant information for our purpose, which will be used in Chapter 3. This precision instrument has two channels, and is capable to generate different types of waveform. In particular it is able to generate DC signals with high stability, fundamental to calibrate the amplitude registered by the V1742 board. In addition, it is able to generate sine waveform with frequency up to 120 MHz, that will be crucial to calibrate the time correction of each of the 1024 samples of the V1742 board. Finally this waveform generator is capable of producing stepping-function waveform with a very steep rising time of 2.9 ns over 1 V_{pp}.

Figure 2.7: Waveform generator Keysight 33622A [14].

Chapter 3

Calibration procedure and results

As we have seen previously, the DRS4 chip (and all the Switched Capcitor Arrays ASICs[1] in general) are full of strengths, but they of course have also some disadvantages. Probably, the most concerning ones are that they suffer from the fact that their sampling bins are not equidistant in time, given by limitations of the chip manufacturing, and that the time required to read out the capacitor cells causes dead time. In the past, the first issue has limited time measurements of optimal signals to standard deviations (σ) of $\mathcal{O}(10)$ ps in accuracy for the split pulse test, depending on the specific chip [11]. However, a novel calibration method, introduced by Stricker-Shaver, Ritt and Pichler [5], permits to improve the time resolution to about 1 or 2 ps. This latter method, that will be summarised in the following sections, is the one employed in this thesis.

3.1 Determination of time measurements and its limitations

Even with precise time calibration, the accuracy of time measurements using an SCA chip remains constrained by the residual random jitter present in the transition times of the inverter chain. This is due to the inherent nature of each inverter, which operates based on a voltage threshold at its input. When this threshold is crossed, the inverter switches either to a high or low state. Despite the stability of this threshold, any noise present in the input signal can introduce fluctuations in the inverter's transition time, resulting in time jitter. In modern SCA chips, the inverter chain's time jitter is typically maintained below 1 ps. This reduction is achieved through careful engineering that curbs noise to a minimum level. For applications like measuring the arrival time of an electrical pulse, particularly in fields like particle physics, the pulse time is usually extracted from the first rising or falling edge of the waveform, depending on the pulse's polarity. A straightforward approach involves employing a single threshold discriminator. In situations involving waveform digitization, a digital counterpart can be achieved by comparing the digitized voltage of sampling points with a fixed value. As depicted in Figure 3.1(a), an interpolated line derived from an ideal signal intersects a designated threshold at time t_1, illustrated as an open square. It is important to already note that the precise knowledge of the timing of the two samples before and after t_1 is fundamental for a precise determination of t_1 itself. Conversely, Figure 3.1(b) portrays a real-world scenario incorporating voltage noise,

[1] ASIC stands for Application Specific Integrated Circuit.

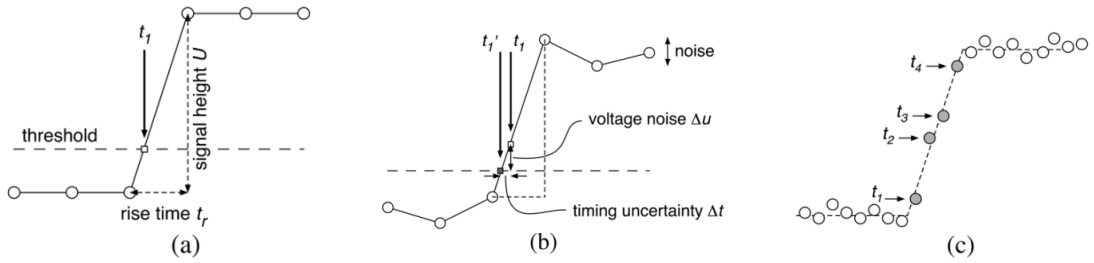

Figure 3.1: Time estimations for a leading edge in the ideal case (a), in the presence of noise (b) and for several sampling points lying on the edge (c) [5].

leading to time jitter. If the signal experiences a voltage noise perturbation of magnitude Δu, the linearly interpolated line intersects the same threshold at a different time t_1', as indicated by the grey square.

From Figure 3.1(b), one can easily derive the formula for the time accuracy Δt as

$$\frac{\Delta u}{\Delta t} = \frac{U}{t_r}, \tag{3.1}$$

where U is the signal height, t_r the rise time and Δu the voltage noise. The time resolution can be improved by sampling the signal at a higher frequency. Figure 3.1(c) shows the same signal sampled with four times higher sampling rate. The sampled points scatter around the signal indicated by the dashed line. Now several points lie on the signal edge, shown as grey circles. If the voltage noise of these points is statistically independent, each point allows a separate measurement of the edge time, and thus reduces the time uncertainty of the edge by $\sqrt{n}$ where n is the number of points lying on the edge. The value of n is also determined by the product of sampling frequency f_s and the signal rise time t_r. Adopting this to Equation (3.1) and solving for Δt gives

$$\Delta t = \frac{\Delta u}{U} \cdot t_r \cdot \frac{1}{\sqrt{n}} = \frac{\Delta u}{U} \frac{t_r}{\sqrt{t_r] \cdot f_s}} = \frac{\Delta u}{U} \cdot \frac{\sqrt{t_r}}{\sqrt{f_s}}. \tag{3.2}$$

From Equation (3.2) it becomes clear that not only a high sampling frequency is important for a precise time measurement, but also the Signal-to-Noise ratio and a short rise time.

3.1.1 Constant Fraction Discrimination

Constant fraction discrimination (CFD) represents a technique employed to furnish amplitude-independent insights into the timing of an event's occurrence. At its core, CFD aims to identify a discriminative point within the analog signal where the sum of signals preceding and succeeding the discrimination point equates to a fixed fraction of the pulse's maximum amplitude. This approach departs from the conventional reliance on the pulse's maximum amplitude and instead seeks a position within the signal where a consistent portion of the maximum amplitude is attained. Certain signals, characterized by notably swift rise times t_r, lack a distinct maximum amplitude but instead possess very short rise times. A prime example of such input signals encompasses pulses originating from scintillators or silicon detectors. These pulses share uniform rise times that

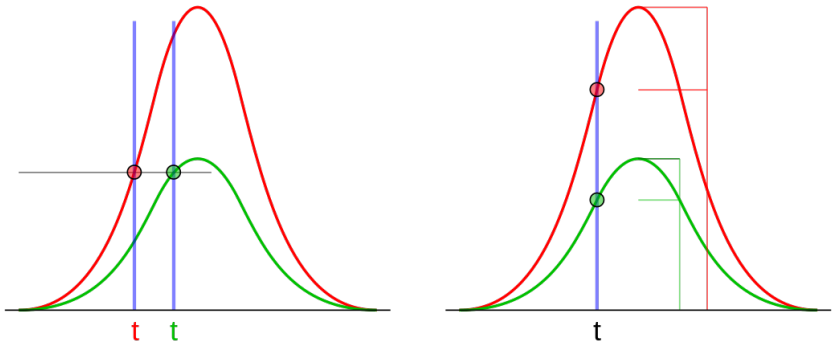

Figure 3.2: Schematic comparison between (left) threshold triggering (left) and (right) constant fraction triggering. As explained in the text it is evident how the former method is affected by a time-walk effect.

considerably exceed the intended temporal resolution. Consequently, straightforward threshold triggering becomes impractical, as it would result in a temporal dependence of the trigger time on the signal's peak height, a phenomenon dubbed "time walk." The uniform rise times and peak shapes exhibited by these signals allow for triggering not at a predetermined threshold, but rather at a constant fraction of the overall peak height. This approach culminates in trigger times that remain unaffected by variations in peak heights, as vividly depicted in Figure 3.2. To sum up, in order to get the correct and coherent time value of a digitised pulse, one has to intercept the point of the slope corresponding to a given fraction of the pulse height, trace the orthogonal line to the time axis that intersects that point and that is the correct time value. The best fraction to be used depends on several factors connected on how the pulses are generated and collected in each particular detector. For the purposes of this thesis, it has been found that using a 50% discrimination is a good choice.

3.2 Voltage Calibration

Given the inherent correlation between voltage errors and time errors, the necessity arises to rectify any voltage discrepancies prior to conducting an accurate time calibration. This corrective process entails two distinct adjustments. Primarily, the stored waveform's voltages exhibit minor variations in offsets and gains across each sampling cell. In the context of the DRS4 chip, this variability mainly stems from the fact that individual sampling capacitors are read out by separate buffers, each characterized by a random offset typically spanning 10-20 mV. To address this, the offsets can be quantified by connecting the input to a DC voltage source and subsequently subtracting these offsets during measurements, thereby effecting an offset correction. Subsequently, a time-dependent readout offset correction is implemented to counteract slight supply voltage fluctuations encountered when transitioning the DRS4 chip from sampling to readout mode. The differential power consumption of the DRS4 chip in these operational modes leads to a small dip in the power supply voltage, not fully mitigated by linear regulators or blocking

capacitors. This dip manifests as an approximate 2 mV shift in the DRS4 output for approximately 10 µs post cessation. Of paramount importance is executing the offset correction at the precise voltage level adopted for subsequent time measurements. This precautionary measure stems from the non-linear nature of the gain's behavior. In addition to the aforementioned adjustments, certain SCA chips are plagued by an issue wherein traces of previously stored signals distort the last sampled waveform. In the case of the DRS3 chip, this phenomenon is dubbed "ghost-pulses" and can result in waveform distortion of about 2-5%, contingent on the sampling speed. Encouragingly, this concern has been resolved for the DRS4 chip by initiating a clear cycle before writing to a storage cell. This process effectively grounds both sides of the storage capacitor via supplementary analog switches for a brief period in the nanosecond range prior to each write cycle, efficiently eliminating any residual charge from previous storage.

In order to calibrate the voltage output produced by the digitiser, 10000 waveforms have been collected for each of the DC voltages −300 mV, 0 mV and +300 mV. The value of the DC voltage is ensured by connecting the output of the Keysight waveform generator to each of the 8 input channels of the group 1 of the digitiser. In the case of the TR0 channel, two additional samples have been collected, one with DC set at −600 mV and one with DC set at +600 mV. The reason for this difference is that, as described in Section 2.2, the input to this channel is attenuated by a factor 2. Hence, in order to cover the same dynamic range of the ADC, a larger range of input voltages must be used.

The voltage calibration consists of two consecutive phases. In the first the offset registered by each cell with respect to the input voltage is calibrated. To do that, for each of the 1024 cells in each channel, the average of the ADC counts over the 10000 acquired waveform is computed and is associated to the voltage at which the waveforms have been acquired. Then, a first order polynomial is fit to the three points corresponding to the three different DC voltages −300 mV, 0 mV and +300 mV. The first order polynomial used in the fit is parameterised as

$$V(x_{\mathrm{ADC}}) = p_0 + p_1 \left(x_{\mathrm{ADC}} - \hat{x}_{\mathrm{ADC}}\right), \tag{3.3}$$

where $V(x_{\mathrm{ADC}})$ is the voltage corresponding to the ADC count x_{ADC}, $\hat{x}_{\mathrm{ADC}}$ is the average of the 10000 ADC counts acquired at 0 mV, and p_0 and p_1 are the free parameters to be determined by the fit. The second phase of the calibration serves to guarantee a uniform behaviour of the ADC over all the 1024 conversions it has to perform. In fact differences may arise when a cell is readout by the ADC as first after the trigger signal or in another of the 1024 points of the acquired waveform. To calibrate this effect, the same data used in the first step are analysed. First, all the ADC counts are converted into voltages according to the calibration parameters p_0, p_1 and $\hat{x}_{\mathrm{ADC}}$ determined in the first phase. Then an average over the 10000 acquired waveform of the readout voltages of all the cells in the first position after the trigger is computed. The same average is performed for all the cells in the second, third... 1024^{th} position, respectively, after the trigger. At this point it is possible to build a correspondence between the averages of the 1024 positions after the trigger and the voltages in input to the chip channels, as in the first phase of the calibration. A linear fit to the three points corresponding the DC voltages −300 mV,

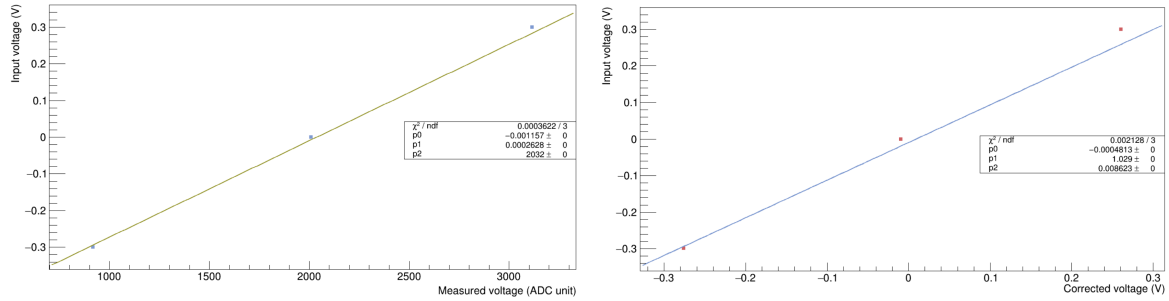

Figure 3.3: Example of the linear fits performed to calibrate the voltage response of (left) the first cell and (right) the first ADC conversion of channel 0.

0 mV and +300 mV,[2] is performed adapting the function

$$V' = q_0 + q_1 \left(V - V_0\right), \tag{3.4}$$

where V' is the final voltage of the calibration procedure, V is the voltage as obtained from Equation (3.3) for the first phase, and V_0 is the voltage obtained from the first phase of the calibration when measuring a DC voltage of 0 mV. As an example, in Figure 3.3 the two linear fits to the three points performed to determine the calibration parameters of the first cell and the first ADC readout, respectively, are shown. In the end, the voltage calibration produces 6 parameters (p_0, p_1, $\hat{x}_{\mathrm{ADC}}$, q_0, q_1 and V_0) for each sampled voltage value, that allow the conversion of the ADC counts registered by the board into actual voltage measurements, by simply sequentially applying Equations (3.3) and (3.4). In order to visualise how much the calibration parameters can vary over the 1024 cells of a channel, in Figure 3.4 the distributions of p_0, p_1, $\hat{x}_{\mathrm{ADC}}$, q_0, q_1 and V_0 are shown. The effect of the voltage calibration can be visualised by simply plotting the voltages measured by the 1024 cells of each channel when a DC voltage is given in input the the digitiser. This is shown in Figure 3.5, where the acquired waveform corresponding to a DC voltage of 0.5 V is shown with and without applying the voltage calibration. The quality of the calibration can be quantified by evaluating the spread of the 1024 voltages, since they should correspond all to the same value. In Figure 3.6 the distribution of these 1024 voltages is shown before and after the application of the voltage calibration. In addition, the same distribution is also shown when the calibration provided by the manufacturer is applied. It is important to note that the voltage calibration returns an ADC count already converted in volts. On the contrary, the output of the data acquired before the calibration procedure or with the manufacturer calibration expresses the voltages as an ADC count on a 12-bit scale, hence from 0 to 4095. In the corresponding plots in Figure 3.6, the output ADC voltages have been converted using the information that the total dynamic range of the digitiser is 1 V, hence each ADC count corresponds to $1/4096 \approx 0.244$ mV. In this way the three plots contain comparable information. The root mean square (RMS) in the three cases are 7.95 mV, 0.36 mV, and 0.33 mV, respectively. As discernible from the plots and their corresponding root mean square (RMS) values, the precision of the acquisition without any calibration proved to be less accurate. However, with the

[2]As in the first phase, for the TR0 trigger channel, the DC voltages −600 mV, 0 mV and +600 mV are used.

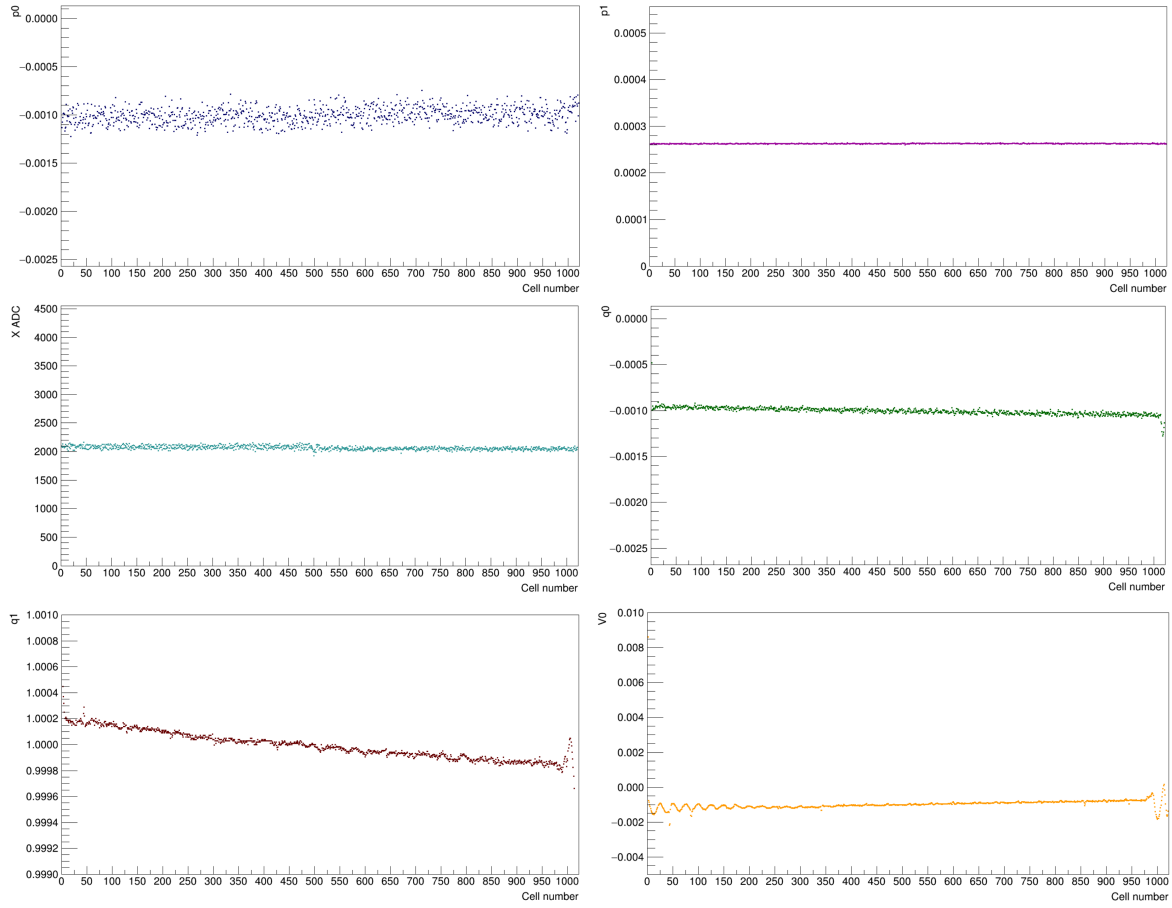

Figure 3.4: From top left to bottom right the values, as a function of the cell number, of the calibration parameters p_0, p_1, $\hat{x}_{\mathrm{ADC}}$, q_0, q_1 and V_0, described in the text, are shown.

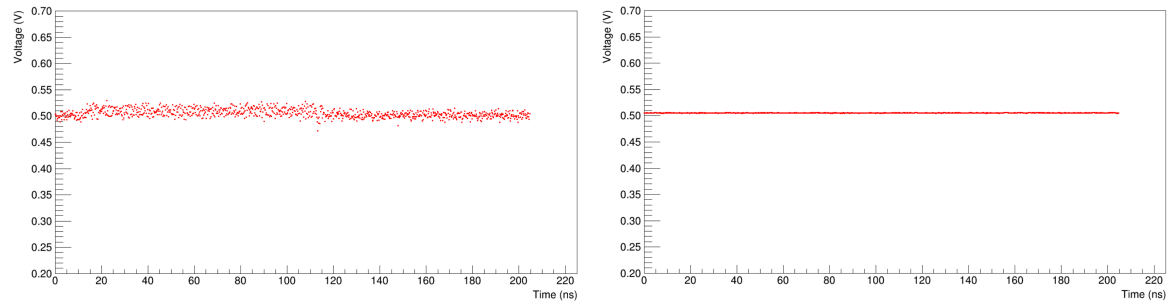

Figure 3.5: Example of an acquired waveform corresponding to a DC voltage of 0.5 V (left) before and (right) after the application of the voltage calibration described in the text. In this example the channel 0 of the first group of the digitiser is used.

incorporation of voltage correction, a noticeable enhancement is observed. At this stage of the process, the manufacturing calibration method exhibits a slight advantage, yielding a reduction of 0.03 mV in standard deviation, with respect to the method presented in this thesis. Nevertheless, it's worth noting that they remain closely comparable, and the Time Calibration phase is yet to be executed.

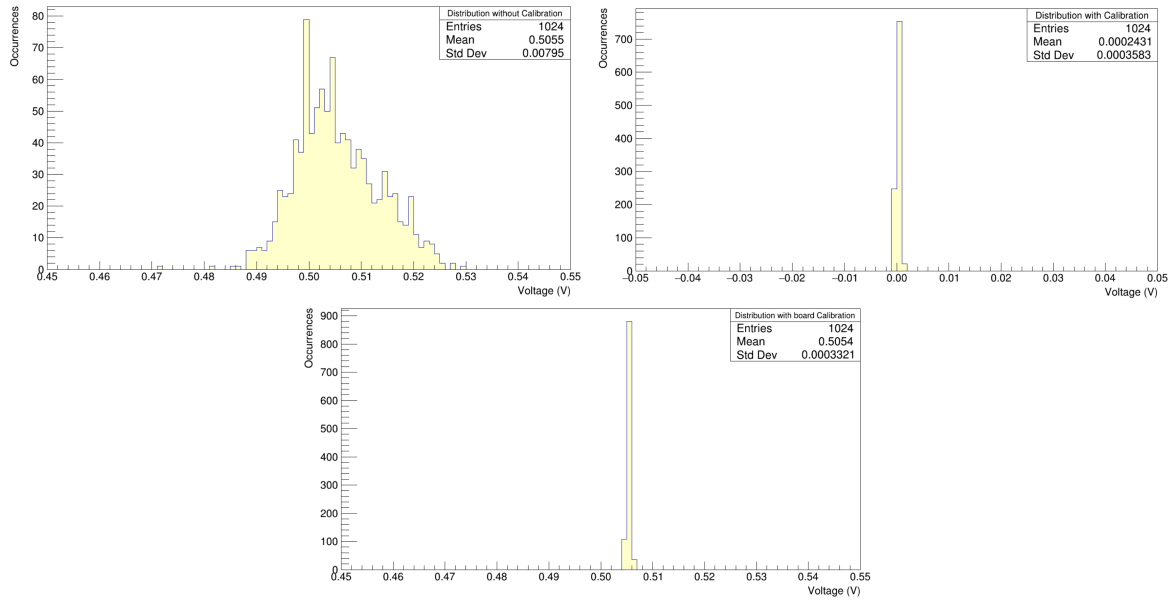

Figure 3.6: Distribution of the voltages registered by the 1024 cells of channel 0 when given in input a DC voltage of 0 mV (or 500 mV). The distribution is shown (left) before and (right) after applying the voltage calibration described in the text, and (below) after the application of the voltage calibration provided by the manufacturer of the digitiser.

3.3 Time Calibration

The sampling intervals of the DRS4 chip are not equidistant, but constant over time. This means the DRS4 has to be calibrated before a precise time measurement can be made. In the following description we will use Δt_i as the effective sampling interval between cell i and cell $i+1$. Δt_i is defined as the time difference between the opening of the analogue switched $S_{0,i}$ and time point $S_{0,i+1}$ as illustrated in Figure 3.1. From this follows that the integrated or "global" time difference between cell k and cell q is given by:

$$\Delta t_{k,q} = \sum_{i=k}^{(q-1)} \Delta t_i \tag{3.5}$$

As an anticipation, in Figure 3.7, the distribution of the time width Δt_i for the 1024 cells of channel 0 is presented, as obtained from the calibration procedure. It is evident that they do not exhibit uniform time intervals, hence requiring a thorough calibration. However, the most intriguing observation pertains to the presence of two distinct peaks in the plot. This phenomenon can be attributed to the design and construction techniques employed, as even and odd cells display subtle variations, resulting in differing time widths. In order to perform the time calibration one has to digitize a known sine wave. The frequency of this sine wave f_{TC} should be adjusted according to the sampling speed range of the SCA. This calibration method works in the frequency ranges:

$$f_{TC} \in \left[\frac{2}{n} \cdot f_{SCA},\ \ \frac{1}{20} \cdot f_{SCA}\right] \tag{3.6}$$

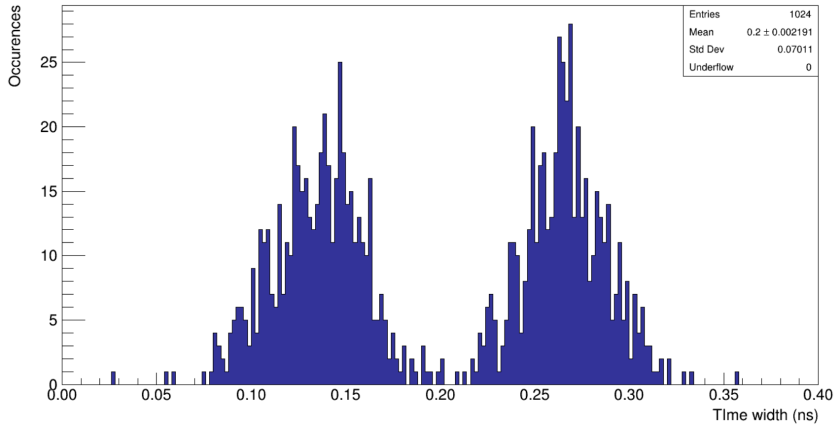

Figure 3.7: Time width distribution of the 1024 cells of channel 0. Each point represents the time width, in ns, between cell i and cell $i+1$.

where f_{SCA} is the nominal sampling frequency of the SCA and n stands for the number of its cells. This time calibration approach is structured in two distinct components. The initial segment focuses on estimating the effective sampling intervals Δt_i through the measurement of voltage disparities between adjacent cells and is aptly labeled the "local" time calibration (TC) phase. Subsequently, the second component fine-tunes the sampling intervals by gauging time differences across cells positioned at significant distances, leading to its designation as the "global" TC phase. The local TC phase adeptly rectifies any non-linearity in differential time by effectively compensating for it. Meanwhile, the global TC component addresses integral time non-linearity.

3.3.1 Local time calibration

The idea behind the local time calibration is that Δt_i is proportional to the measured voltage difference between neighboring cells when applying a linear increasing or decreasing signal, such as a saw-tooth waveform for example. This correlation is given by the *intercept theorem*:

$$\frac{\Delta t_i}{\Delta U_i} = \frac{\sum \Delta t_i}{\sum \Delta U_i} \tag{3.7}$$

where ΔU_i is the voltage difference between cells i and $i+1$, and is graphically illustrated in Figure 3.8. For an SCA with n cells we know:

$$\sum_{i=1}^{n} \Delta t_i = \frac{n}{f_{SCA}}. \tag{3.8}$$

When combining Equation (3.7) and Equation (3.8), one can calculate all n time intervals Δt_i as:

$$\Delta t_i = \frac{\Delta U_i \cdot \frac{n}{f_{SCA}}}{\sum \Delta U_i}. \tag{3.9}$$

Using rising and falling edges of the TC signal will result in two calibrations. Averaging over these two calibrations will cancel any residual voltage offset

$$\Delta t_i = (\Delta t_{i,falling} + \Delta t_{i,rising}) \cdot \frac{1}{2} \tag{3.10}$$

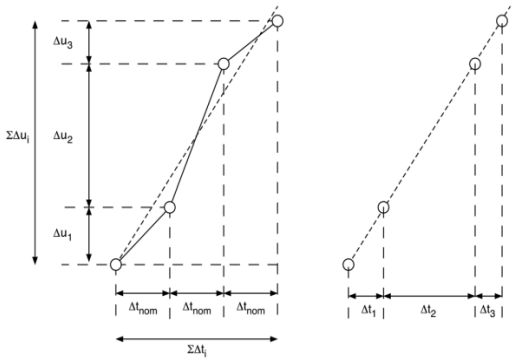

Figure 3.8: Correlation between voltage differences ΔU_i and time differences Δt_i of a rising edge can be used for the local TC of an SCA chip [5].

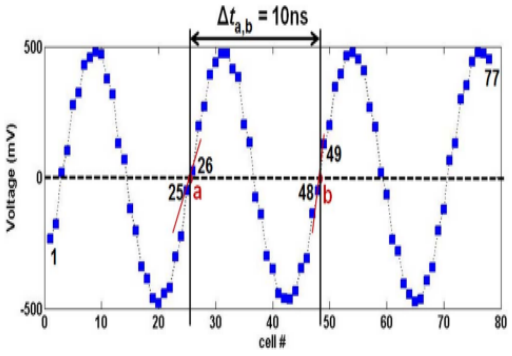

Figure 3.9: First 77 cells of the 1024 cell array of a DRS4 sampling a 100 MHz sine wave at a sampling speed of 2.5 GSPS. This signal is used for the local TC and the global TC [5].

where $\Delta t_{i,falling}$ and $\Delta t_{i,rising}$ stand for the time differences calculated by the falling and rising edges, respectively. Within a digitized waveform, it becomes feasible to ascertain solely the Δt_i values for cells positioned along the slopes of the sine wave. Consequently, it becomes imperative to iterate this process across multiple sine waves, each featuring a random phase with respect to the SCA clock. To achieve a reliable outcome for the local time calibration, it is recommended to perform this procedure across at least 1000 digitised sine waves, relying on the arithmetic mean values for the requisite adjustments. The local time calibration makes use of sinusoidal waveforms with a total amplitude of 1 V, in order to exploit as much as possible the dynamic range of the digitiser. Since it is necessary to assume a linear correlation between cell time width and voltage variation, only the regions where the sine function can be approximated as linear are used in the calibration. It has been found that restricting to the range between -300 mV and +300 mV the approximation is sufficiently accurate. The frequency of the sine function is set at 50 MHz. With these parameters, there are approximately 30 cells in the linear region of the rising front of the sine, as well as 30 cells on the falling front, that can be used for the local calibration. A final note is that the acquisition is triggered out of synchronisation with respect to the sine waveform, in order to have the zero crossing points of the sine function in different places each time and cover all the 1024 cells. A total of 100000 sine waveforms have been acquired for each channel of the digitiser in order to guarantee a sufficient statistics. In Figure 3.10 one of the acquired waveforms is shown, after the application of the voltage calibration described in Section 3.2.

3.3.2 Global time calibration

The global time calibration entails measuring one or more complete periods of the 100 MHz sine wave. To establish the period, a linear interpolation approach is employed by considering sampling points both below and above 0 V. The procedure involves gauging the time span between the points where the interpolated lines intersect the zero line, as exemplified in Figure 3.9. In the illustrated scenario, the zero crossings, represented by the artificial points a and b, occur between cells #25 and #26, as well as between cells

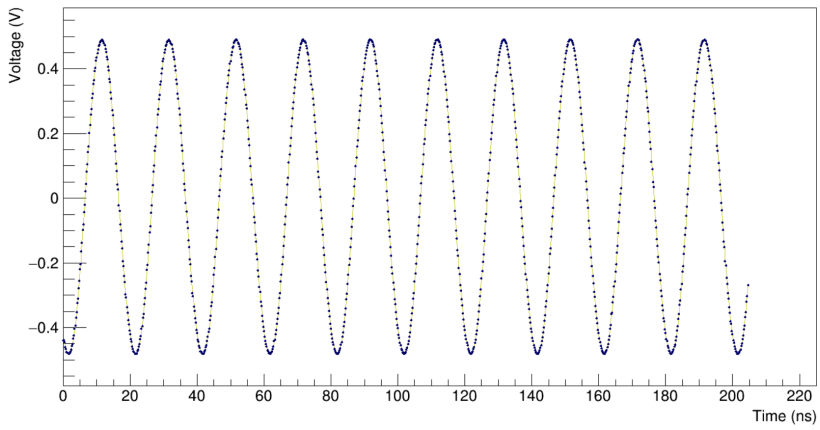

Figure 3.10: Example of a sine waveform acquired to perform the local time calibration described in the text. The readout voltages are already calibrated using the procedure described in Section 3.2.

#48 and #49, thereby necessitating two distinct correction factors, one for a and one for b. The time of a and b can be determined as

$$t_a = t_{26} - \frac{U_{26}}{\Delta U_{25}} \Delta t_{25}, \tag{3.11}$$

$$t_b = t_{48} + \frac{U_{48}}{\Delta U_{48}} \Delta t_{48}. \tag{3.12}$$

Hence, the difference $t_a - t_b$ corresponding to m periods of the calibration sine wave can be written as

$$t_b - t_a = m \frac{1}{f_{TC}} = t_{26,48} + t_{cor}, \tag{3.13}$$

where

$$t_{26,48} = t_{48} - t_{26}, \quad t_{cor} = \frac{U_{26}}{\Delta U_{25}} \Delta t_{25} - \frac{U_{48}}{\Delta U_{48}} \Delta t_{48}. \tag{3.14}$$

As a consequence, Equation (3.13) can be used to correct the time difference between cell #26 and cell #48, by applying the correction factor

$$u_{cor} = \frac{m}{f_{TC}(t_{26,48} + t_{cor})}, \tag{3.15}$$

such that the corrected time intervals are $\Delta t_i^{cor} = u_{cor} \Delta t_i$, where $i = \{26, 27, ..., 47\}$. The procedure can be generalised between any pair of cells k and q close to the zero crossing points of the calibration sine wave. In Reference [5] an iterative procedure has been used to find the final global correction factor. In this thesis, instead, an average of u_{cor} factors is determined over a large number of events and for all the possible values of m present in the calibration data. In addition, to improve the robustness of the procedure, the global correction factor is determined from the arithmetic mean of the u_{cor}, obtained analysing the raising and falling zero-crossing points. The effectiveness of the global TC rests upon two underlying factors. Firstly, the local TC inherently harbors imperfections owing to

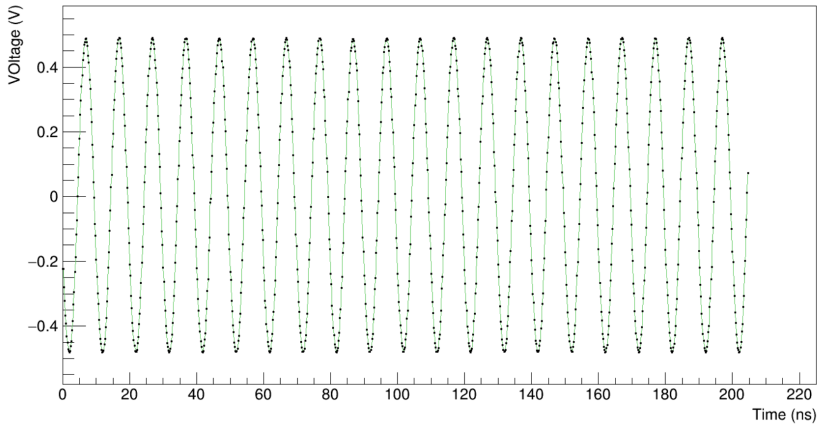

Figure 3.11: Example of a sine waveform acquired to perform the global time calibration described in the text. The readout voltages are already calibrated using the procedure described in Section 3.2.

the statistical errors inherent in any measurement. Over time, these errors accumulate as measurements are integrated. Secondly, the diverse SCA cells exhibit varying effective analog bandwidths across the chip. Cells in proximity to the input pin experience a lesser resistance in the signal bus within the chip compared to those situated farther from the input pin. This discrepancy gives rise to slight variations in rise times for the calibration sine wave across different cells. As a consequence, a systematic error materializes in the context of the local TC, which the global TC systematically rectifies.

The global time calibration uses the timing information provided by the zero-voltage crossing point of a sine waveform. In this case, a sine waveform with 100 MHz frequency is utilised, that guarantees about 20 zero-crossing points over the entire 204.8 ns width of the acquisition window. The sine amplitude is still fixed at 1 V and a total of 20000 waveforms are acquired for each channel. In Figure 3.11 an example of the used waveform is shown as acquired by the digitiser and after the application of the voltage calibration described in Section 3.2.

3.4 Performance of the calibration procedure

In order to determine the goodness of the calibration procedure, the difference between the time-stamps of two stepping-function waveforms, each acquired by one of the digitiser channels, is measured. The Keysight waveform generator is equipped with two output channel that can be synchronised, but given the target precision of this study, any jitter between the two channel would bias the performance determination. Hence the output of a single channel is split with a T connector, and the two split waveforms are sent to two different channels. An example of the used stepping-function waveform is shown in Figure 3.12, as registered by the digitiser and after the application of both the voltage and time calibration described in the previous Sections. The used waveform has a maximum amplitude of 800 mV and the rising time of the step is set to the minimum possible for the waveform generator, corresponding to 2.9 ns. The time stamp of each digitised waveform is determined using a constant fraction discrimination at 50% of the waveform height.

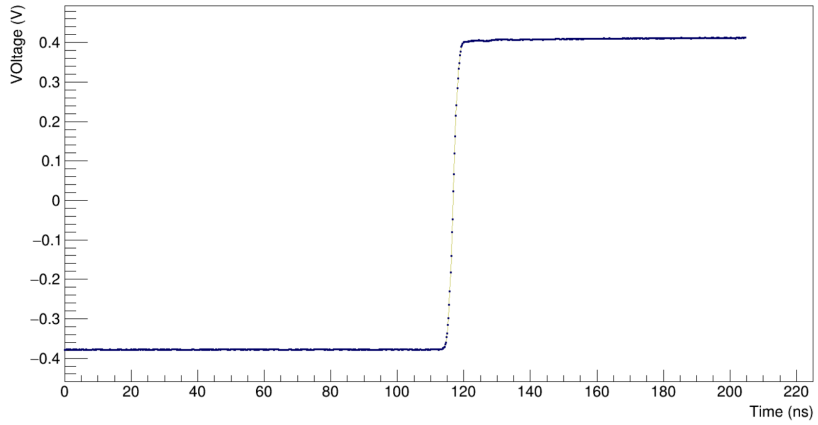

Figure 3.12: Example of a stepping-function waveform used to determine the performance of the calibration procedure as described in the text. The readout voltages and timing are already corrected using the calibration described in this thesis.

The steps of the procedure are:

- the baseline voltage, V_{B}, of the stepping-function waveform is determined by averaging the voltages registered by the cells in the first 20 ns of the acquisition window;
- the maximum voltage, V_{M}, of the waveform is determined as the maximum voltage registered by any cell;
- the value of the 50% threshold is determined as $V_{50} = 0.5\,(V_{\mathrm{B}} + V_{\mathrm{M}})$;
- the two cells, i and j, registering the voltages just below and just above V_{50} are identified;
- a linear interpolation between the measurements of cells i and j is performed to determine the time corresponding to V_{50},

$$t_{50} = t_i + \frac{t_j - t_i}{V_j - V_i}\,(V_{50} - V_i)\,, \tag{3.16}$$

  where V_i and V_j (t_i, t_j) are the voltages (times) corresponding to cells i and j, respectively.

The difference between the time stamps t_{50} of the two channels fed with the split stepping-function waveform is computed for about 10000 acquired samples. In Figure 3.13, the distributions of these time differences, between channel 0 and channel 1, are shown as determined without applying any calibration, after applying the manufacturer calibration and after applying the calibration determined in this thesis. The corresponding RMS of the distributions are good measurements of the contribution of the digitiser to the final time resolution and correspond to 26.8 ps, 10.2 ps and 2.5 ps, respectively. It is important to note that the time resolutions determined in this way include also the contribution from the unavoidable electronic noise. According to Equation (3.2) and given

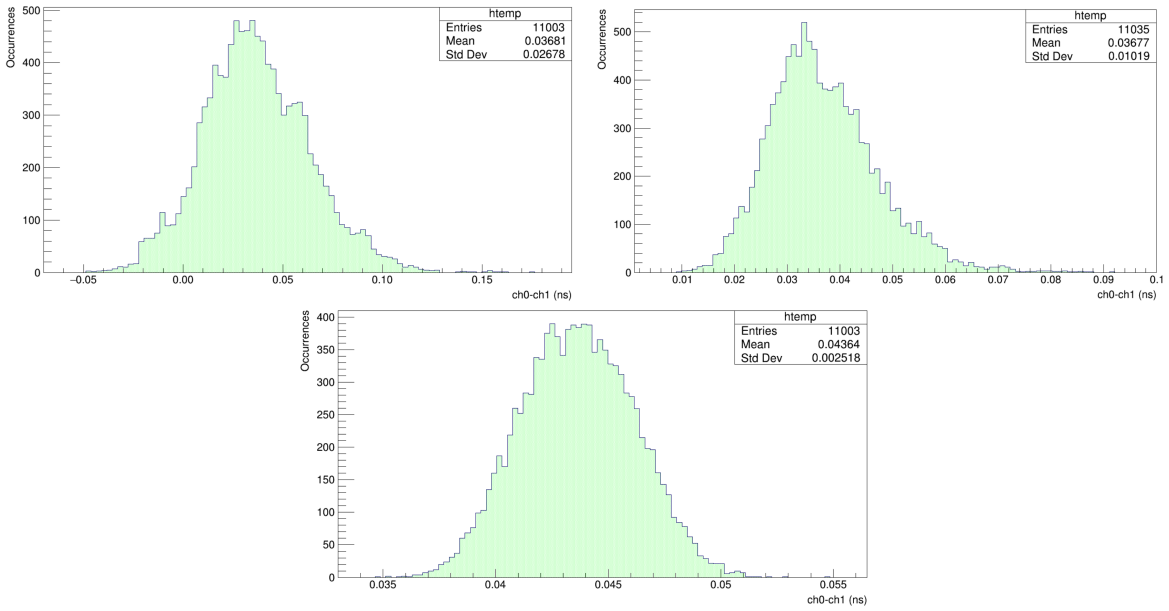

Figure 3.13: Distribution of time differences between channel 0 and channel 1 of the digitiser, over about 10000 acquired waveforms. The time difference is computed (left) without applying any calibration, (right) using the manufacturer calibration and (below) applying the calibration described in this thesis.

the parameter of the used stepping-function waveform, this component can be estimated to be in the range 1-2 ps. The obtained results align with our expectations. Specifically, the intrinsic precision of the chip, devoid of any calibration, is relatively modest. The calibration provided by the manufacturing company, while an improvement, does not attain an exceptional level of accuracy. Conversely, the calibration method expounded upon in this thesis offers a substantial enhancement in precision, achieving an order of magnitude improvement in time accuracy.

Conclusion

In this thesis the LHCb experiment and its upgrades [1, 3, 4] have been introduced. The LHCb detector is designed to exploit the unprecedented cross-section of b- and c-quarks production in pp collisions at the Large Hadron Collider (LHC) at CERN, to perform precision measurements in the sector of flavour physics. Despite the success of the experiment, with first observations of rare decays and world-leading measurements of CP-violating quantities, all the results from LHCb are in very good agreement with the predictions of the Standard Model. However, the current experimental landscape still allows room for the presence of physics beyond the Standard Model, but relevant improvements in the precision of many measurements are required to establish it. To chase the ultimate precision in the quark-flavour sector, the LHCb collaboration is planning a further upgrade of its detector, to make it capable of operating at a peak instantaneous luminosity of 1.5×10^{34} $\mathrm{cm}^{-2}\,\mathrm{s}^{-1}$, about a factor 30 higher than the original design, and hence increase the total statistics by a corresponding factor. In these conditions the LHCb Upgrade II detector will have to face a very crowded environment with a large increase of the pile-up up to 40 visible primary pp interactions per bunch crossing. The most promising solution to control such an increase in the pile-up is to equip the sub detectors with the capability to measure the time-of-arrival of particles with about 10-20 picoseconds of resolution. In this way it will be possible to associate the particles producing the hits to the corresponding primary interaction, exploiting the time spread of pp collisions in a bunch crossing of about 180 ps.

In order to achieve the required time resolution, all the components of the detector must be optimised accordingly, notably including the electronic boards used to digitise and acquire the electrical signals produced by the detectors. The so-called Switched-Capacitor Array (SCA) technology is currently one of the viable solutions to achieve fast and precise digitisation of electrical signals at a reasonable cost. Nevertheless, acquisition boards based on SCA still need a very thorough calibration in order to guarantee a minimal contribution to the total time resolution. In this thesis, the design and operational principles of the SCA technology have been presented and discussed, referring in particular to the DRS4 chip [11, 12], developed at the Paul Scherrer Institute (PSI) in Zurich. Then the general calibration procedure proposed in Reference [5] is implemented and applied to the particular case of the CAEN V1742 digitiser [13]. The V1742 board is equipped with four DRS4 chip, for a total of 32 input channels plus 2 dedicated to fast triggering, with an analog input bandwidth of 500 MHz and a maximum sampling frequency of 5 GSPS. The calibration methodology entails a voltage calibration, aiming at correcting the determination of the voltage of input electrical signals, followed by a time calibration, aiming at the precise determination of the time passing between two consecutive sampling of the incoming signals. Throughout the calibration process, we

have underscored the critical importance of calibration in elevating the precision and accuracy of data acquisition systems. The split-signal test has been used to determine the intrinsic time resolution of the studied acquisition board. A comparative analysis has been performed as well, encompassing the cases of using no calibration, the calibration provided by the manufacturer and the calibration implemented in this thesis. The analysis revealed a substantial enhancement in accuracy when applying the calibration implemented in this thesis, particularly regarding the time resolution. The not-calibrated board achieved a time resolution of almost 27 ps, while the calibration provided by the manufacturer allowed an improvement in precision down to about 10 ps. These values are clearly not satisfactory for the purposes of the LHCb Upgrade II experiment, as the contribution to the total time resolution coming just from the acquisition board would equal the final target. Instead, the application of the calibration implemented in this thesis allowed the remarkable time resolution of 2.5 ps to be achieved, signifying an enhancement of an entire order of magnitude compared to the not-calibrated board, and a fourfold improvement over the calibration provided by the manufacturer.

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