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Study of high-quality ALD gate dielectrics in radiation sensitive oxide field effect transistors

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Abstract

Radiation dosimetry is crucial in many fields, where the exposure of ionizing radiation must be precisely controlled to avoid health and environmental safety issues. Radiotherapy and radioprotection are two examples in which fast and reliable detectors are needed. Compact and large area wearable detectors are being developed to address real-life radiation dosimetry applications, their ideal properties include flexibility, lightness, and low-cost.

This thesis contributed to the development of Radiation sensitive OXide Field Effect Transistors (ROXFETs), which are detectors able to provide fast and real-time radiation read out. ROXFETs are based on thin film transistors fabricated with high-mobility amorphous oxide semiconductor, making them compatible with large area, flexible, and low cost production over plastic substrates. The gate dielectric material has high dielectric constant and high atomic number, which results in high performances and high radiation sensitivity, respectively.

The aim of this work was to establish a stable and reliable fabrication process for ROXFETs made with atomic layer deposited gate dielectric. A study on the effect of gate dielectric materials was performed, focusing the attention on the properties of the dielectric-semiconductor interface. Single and multi layer dielectric structures were compared during this work. Furthermore, the effect of annealing temperature was studied. The device performances were tested to understand the underlying physical processes. In this way, it was possible to determine a reliable fabrication procedure and an optimal structure for ROXFETs. An outstanding sensitivity of $(65 \pm 3)\mathrm{V/Gy}$ was measured in detectors with a bi-layer $Ta_2O_5-Al_2O_3$ gate dielectric with low temperature annealing performed at 180°C.

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Introduction

Nowadays, the precise control of the dose of ionizing radiation is required in a wide range of fields, spanning from radiotherapy to nuclear waste management, industrial processes, and space missions. Wearable detectors can be useful to address radioprotection issues and the development of personal medicine. Their ideal properties include flexibility, lightness, and low cost, as well as low-power consumption for battery operations.

Recently, researchers from University of Bologna (Italy) and NOVA University of Lisbon (Portugal) have developed promising Radiation sensitive OXide Field Effect Transistors (ROXFETs). The devices are based on amorphous materials deposited at low temperatures, thus they can be fabricated over plastic flexible substrates. The devices consist in thin film transistors based on high-mobility amorphous indium-gallium-zinc oxide semiconductor, which is suitable for dosimetry applications as it shows great radiation hardness. The gate dielectric of ROXFETs is based on materials with high dielectric constant and high atomic number. These properties guarantee high performing transistors and high sensitivity to ionizing radiation, respectively.

In this thesis, atomic layer deposition was used to deposit high-quality gate dielectric, in order to improve the properties of similar devices previously fabricated with sputtered dielectric. At CENIMAT clean room facilities present at NOVA University of Lisbon, several batches were fabricated varying the gate dielectric layer structure, from monolayers, to bi-layers and tri-layers. The role of two annealing temperatures (180°C and 300°C) was tested for each batch. Moreover, the material of the source and drain layer was studied. The samples were characterized electrically with standard transistor characterization. The stability was assessed with positive gate bias stress measurements and measuring the threshold shift in no-stress conditions. The x-ray response was measured at University of Bologna facilities. Radiation sensitivity tests were performed. Moreover, capacitance-voltage measurements were also performed to evaluate the change of semiconductor sub-bandgap density of states upon irradiation.

Chapter 1 contains a general introduction about thin film transistors. Their structure and working principles are explained in detail, and the electrical properties of transistors are enunciated. Then, the chapter focuses on the advantages of thin film transistors based on high-mobility amorphous oxide semiconductors. Finally, the working principles of radiation detecting field effect transistors are presented and compared with the distinctive

features of ROXFETs.

Chapter 2 focuses on the devices fabrication process. First, the techniques employed in this thesis are explained from a theoretical point of view. Then, the fabrication process is described step-by-step, also providing the parameters used.

Chapter 3 describes the characterization methods employed to assess the performances of the fabricated devices: current-voltage characteristics, positive gate bias stress tests, x-ray sensitivity measurements, and capacitance-voltage measurements for the extraction of the sub-bandgap density of state.

Chapter 4 presents the results obtained in this thesis. The fabrication procedure is assessed by optical and electrical measurements. The transport properties are assessed through current-voltage characterization. The stability is tested with bias stress measurements and measuring the threshold shift in no-stress conditions. Finally, the x-ray sensitivity of the devices is tested, and the behavior of the semiconductor sub-bandgap density of states upon irradiation is observed.

Chapter 1

Thin-film transistors for x-ray detection

1.1 Thin-film transistors

Thin-film transistors (TFTs) are three terminal field-effect devices. The current flowing between the source and the drain electrodes through a semiconductor layer is modulated by the voltage applied to a transversal electrode, the gate. A dielectric material is positioned between the semiconductor layer and the gate, forming a parallel plate capacitor structure. When a sufficient gate voltage V_G is applied, a conductive channel forms in the semiconductor close to the dielectric interface by capacitive injection of carriers, allowing the passage of a current I_D between the source and the drain. Figure 1.1 shows a schematic diagram of a TFT and its working principle.

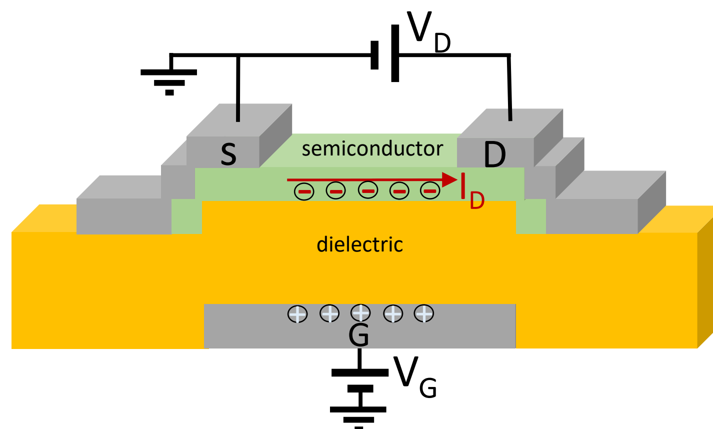


Figure 1.1: Schematic diagram of the main components of a TFT, where S, D and G are the source, drain and gate electrodes, respectively. The operation mode shown in the diagram refers to a TFT with n-type semiconductor.

The working principle of field-effect transistor can be investigated looking at the band energy diagram (Figure 1.2). The semiconductor channel is modulated by the gate voltage. This allows to distinguish three regions of operation, with respect to the amount of charges present in the semiconductor channel [1]. In the following, the polarity of the bias refers to an n-type semiconductor.

Equilibrium ($V_G = 0$ V). When no bias is applied, the metal work function is equal to the semiconductor work function. Therefore, their Fermi level is aligned and no band bending is present.

Depletion ($V_G < 0$ V). The Fermi level of the gate is higher than the one of the semiconductor, inducing an upward bending of the semiconductor energy bands. Physically, the negative charge at the gate pushes away the electrons from the semiconductor. The absence of electrons creates a depletion region, which prevents current flow between the source and drain. Under this condition the transistor is said to be in the *off state*.

Accumulation ($V_G > 0$ V). When the gate is positively charged, the Fermi energy of the gate is lowered, leading to a downward bending of the bands of the semiconductor. Therefore, the electrons accumulate in the channel close to the dielectric interface. The current can flow between the source-drain electrodes and the transistor is in the *on state*.

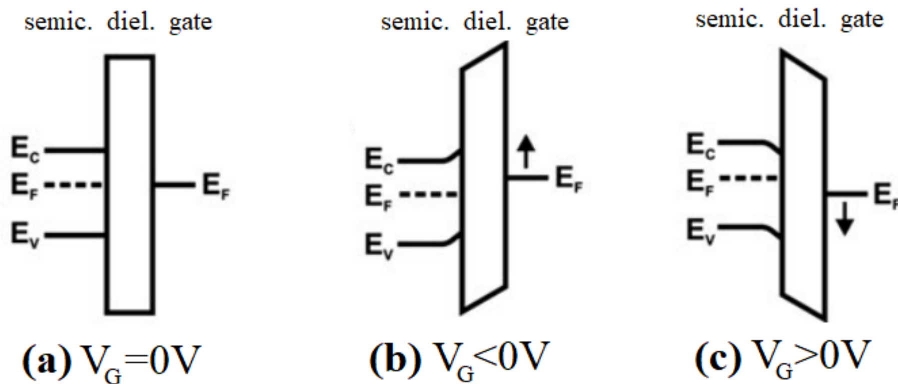


Figure 1.2: Band diagram of the three regions of operation of a FET. Adapted from [1]

The TFTs can be classified based on their structures, as shown in Figure 1.3. The configuration is called coplanar if the source-drain and the gate electrodes lay on the same side of the semiconductor layer; otherwise it is said to be staggered. Depending on the gate position, a further distinction can be made between devices with the gate below the structure or above it, called respectively bottom-gate or top-gate. Each configuration

has its own specificity, which makes it suitable for a certain purpose [2]. In bottom gate structures the semiconductor surface is exposed to air, which can lead to undesirable instabilities, but it can be exploited as well to modify the semiconductor properties for example during annealing or plasma treatment. This structure is often covered by an insulating passivation layer, which acts as a chemical and mechanical protection.

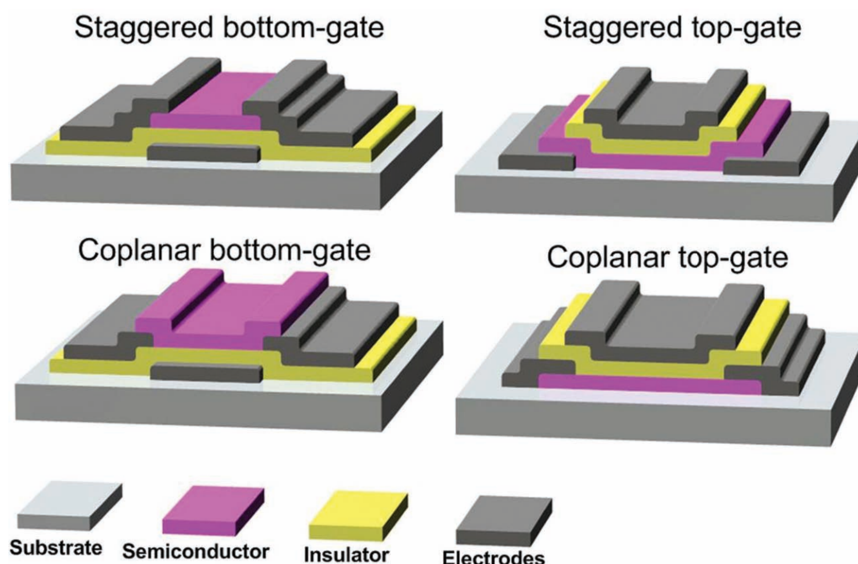


Figure 1.3: Schematics of the possible TFT configurations [2].

The working principle of TFTs is similar to other field effect devices (FETs), such as metal-oxide-semiconductor FETs (MOSFETs), as they both rely on field effects to modulate the conductance of the semiconductor at the interface with the dielectric.

However, some basic differences between MOSFETs and TFTs are present. First of all, TFTs are fabricated over an insulating substrate which only acts as a support. The substrate is typically glass or plastic; this characteristic makes TFTs suitable to produce transparent and/or flexible electronics. On the other hand, MOSFETs are fabricated on silicon wafers which act both as a substrate and the semiconducting layer. The crystalline nature of the silicon wafer guarantees higher electrical performances of MOSFETs compared to TFTs. Other differences include the processing temperature, which can be as high as 1000°C in MOSFETs, while in TFT the substrate softening point (for glass ∼650°C) sets a limiting point. Moreover, only MOSFETs have a p-n junction at the source-drain interface with the dielectric. MOSFETs work in depletion mode, which implies an inversion region close to the dielectric interface. On the contrary, in TFTs the field effect causes an accumulation layer.

1.1.1 Electrical behavior

The behavior of a TFT depends on the voltage applied to the electrodes:

- For $V_D < V_G - V_{th}$ the transistors show a linear regime described by

$$I_D = \frac{W}{L} c\mu_{FE} \left[(V_G - V_{th})V_D - \frac{1}{2}V_D^2 \right], \tag{1.1}$$

  where W and L are the channel width and length respectively, c is the capacitance per unit area of the gate dielectric, and μ_{FE} is the field effect mobility. For very low V_D, the quadratic term can be neglected, resulting in an approximately linear relation between I_D and V_D. In this situation the charges are uniformly distributed throughout the channel.

- For higher V_D ($V_D \geq V_G - V_{th}$) the channel is said to be pinched-off as it becomes depleted of charges close to the drain region. This results in the saturation of I_D, and the so-called saturation regime is described by

$$I_D = \frac{W}{2L} c\mu_{sat}(V_G - V_{th})^2, \tag{1.2}$$

  where μ_{sat} is the saturation mobility.

The most important figures of merit to assess the electrical characteristics of a TFT are illustrated in the following paragraphs [2].

On/off ratio (I_{on}/I_{off}): ratio between the drain current flowing in accumulation (on) and depletion (off) regime. I_{on} depends on the semiconductor material and on the effectiveness of capacitive injection by the field effect, while I_{off} is generally due to the leakage gate current or the instrumental sensitivity.

Threshold voltage (V_{th}) and **onset voltage** (V_{on}): V_{th} is the minimum V_G leading to the formation of the conductive channel in the semiconducting layer. It is usually calculated by linear extrapolation of the $I_D - V_G$ plot for low V_D, or of the $\sqrt{I_D} - V_G$ one for high V_D. Similarly, V_{on} is defined as the minimum V_G necessary to fully turn-on the transistor and it is calculated in a log $I_D - V_G$ plot. It is often used in literature due to the lower variability in its determination compared to V_{th}.

Subthreshold swing (S): S is the V_G needed to increase I_D by one decade and describes the transistor switching behavior. Specifically, it is the inverse of the maximum slope of the transfer characteristic

$$S = \left(\left. \frac{d \log I_D}{dV_G} \right|_{max} \right)^{-1}. \tag{1.3}$$

Small values indicate high working speeds and low power consumption.
The subthreshold swing can be linked to the trap density (N_t) at the dielectric-semiconductor interface according to the equation [3]

$$N_t = \left[S \frac{log(e)}{k_B T / q_0} - 1 \right] \frac{c}{q_0}, \tag{1.4}$$

where k_B is the Boltzmann's constant, T the temperature, e the base of natural logarithm and q_0 the unitary charge.

Mobility (μ): mobility measures the ability of a material to transport carriers. In general, mobility is affected by several scattering mechanisms such as lattice vibrations, ionized impurities, grain boundaries, and other structural defects. In TFTs the conducting channel is located close to the dielectric/semiconductor interface. Therefore, besides normal scattering mechanisms, mobility is also affected by Coulomb scattering from dielectric charges and interface states, as well as scattering due to surface roughness [2]. Mobility can be calculated following different methodologies.
In linear regime:

- Effective mobility (μ_{eff}): obtained by the conductance $g_d = I_D/V_G$

$$\mu_{eff} = \frac{g_d}{c \frac{W}{L} (V_G - V_{th})}, \tag{1.5}$$

- Field effect mobility (μ_{FE}): obtained by the transconductance $g_m = \partial I_D / \partial V_G$

$$\mu_{FE} = \frac{g_m}{c \frac{W}{L} V_D} \tag{1.6}$$

While in saturation regime:

- Saturation mobility (μ_{eff}):

$$\mu_{sat} = \left(\frac{d\sqrt{I_D}}{dV_G} \right)^2 \frac{2L}{cW}, \tag{1.7}$$

Mobility calculated at low V_D has the disadvantage to be affected by the contact resistance. Moreover, μ_{eff} requires the determination of V_{th}, while μ_{FE} is more extensively used, as it easily calculated by the derivative of the transfer characteristic. Saturation mobility does not require V_{th} and is not so sensitive to contact resistance, however in saturation the channel is pinched-off, which means that its effective channel length is shorter than L.

1.2 High mobility amorphous oxide semiconductor TFTs

High mobility Amorphous Oxide Semiconductors (AOS) are a class of materials attractive for large area, flexible electronics.

AOS deposition is extremely versatile [4]: in the first place, AOS are compatible with low processing temperature, obtaining good performing devices fabricated at room temperature. At the same time the processing temperature window is large, as the crystallization temperature can be above 500°C, which allows to choose an appropriate temperature to modify the transistor characteristics. AOS are compatible with large-area mass production deposition methods such as sputtering and wet processing. In general, the deposited films have good short range uniformity and great surface flatness, owning to the amorphous nature of the material.

AOS guarantee some interesting electrical properties in TFTs, which will be presented in the following [4]. AOS TFTs have large electron mobility of more than 10 cm^2/Vs. The great transport properties of the amorphous structure arise from the strong ionicity of the oxides, which stabilizes the electronic structure by raising the electronic levels in cations and lowering the ones in anions. As a result, the conduction band minimum (CBM) is formed by unoccupied s orbitals and the valence band maximum (VBM) by fully occupied $2p$ oxygen orbitals. The spherical shape of the s orbitals composing the CBM guarantees an overlap among neighboring metal cations regardless of the spatial orientation. The amorphous nature does not affect the transport properties, as the CBMs are insensitive to local randomness. On the contrary, in covalent semiconductors such as silicon, the bonds are made of the sp^3 and p orbitals, which have strong spatial orientation. In amorphous structures the chemical bonds are strained, resulting in deep and high-density localized states, which cause charge trapping. This results in a huge decrease in mobility when going from the crystalline phase (μ ≈100 cm^2/Vs) to the amorphous phase ($\mu \approx 1$ cm^2/Vs) of silicon [5]. A comparison of the chemical bonds of AOS and covalent semiconductors is shown in Figure 1.4.

Moreover, thanks to the highly ionic nature of the chemical bonds, oxides form less defects states in the band gap compared to traditional covalent semiconductors such as silicon. The low defect density results in low operation voltage (< 5 V) and small subthreshold swing $S \approx 0.1$ V/decade.

For AOS TFTs in depletion regime, the concentration of holes do not exceed that of the electrons near the semiconductor-dielectric interface [6]. This means that AOS TFTs also have the advantage that they do not exhibit inversion p-channel operation and consequent increase of the off current, as opposed to traditional silicon-based MOSFETs. The latter require a p-n junction for the source and drain electrodes to avoid inversion operation, while in AOS TFTs a metallic junction is sufficient [4].

Indium, gallium, zinc, and tin are good candidates to compose transparent AOS, as their unoccupied s orbitals can form the isotropic electron transport path. One of the most investigated high-mobility AOS is amorphous indium-gallium-zinc oxide (IGZO),

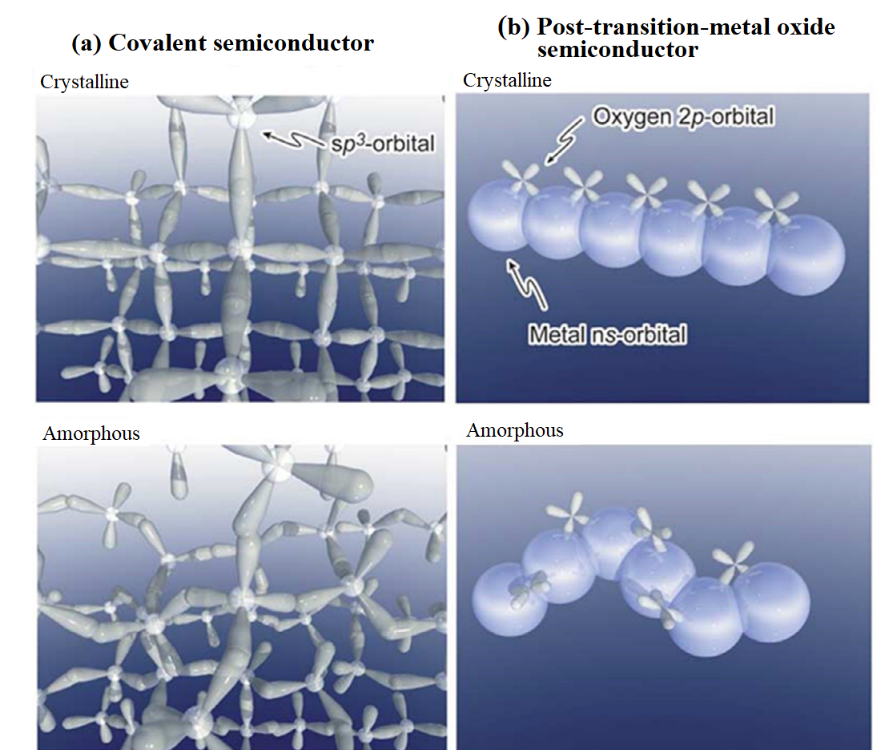


Figure 1.4: Chemical bonds of **(a)** Covalent semiconductors as for example silicon and **(b)** Post-transition-metal oxide semiconductors [4].

which was first reported by Nomura *et al.* [7] in 2004. It is amorphous when deposited at room temperature and it has a energy gap of ∼4.5 eV.

1.3 Radiation Sensitive OXide Field Effect Transistors (ROXFETs)

The effects of ionizing radiation on human beings is crucial in many fields such as health-care, nuclear, high energy physics, avionics, and space applications [8]. Monitoring the radiations absorbed by the bodies of professionals working in these fields is required to ensure safety and prevent health hazards.

The energy deposited on a unit mass of matter by the ionizing radiation is called the radiation dose, which is measured in Grays (1 Gy = 1 J/kg).

Real-time radiation detection is traditionally performed with ionization chambers and calorimeters. However, they are voluminous and operate with high voltages. To date, the necessity of compact and spatially resolved devices has been addressed mainly solid state detectors based on traditional silicon technology, consisting in diodes or transistor

structures. In particular, Radiation Sensitive Field-Effect Transistors (RADFETs) are sensitive in a dose range of several orders of magnitude, from µGy to MGy [8].

The basic physic principles of RADFETs (Fig. 1.5) can be explained as follow. The high energy radiation impinging on the device transfers its energy during the interaction with matter. The energy transfer results in the excitation of electrons, thus creating electron-hole pairs. When this happens in conductors or semiconductors, the free charges will recombine or mobilize by drift or diffusion [8]. When the ionized charges are generated in the insulating layer the outcome is different. Electrons have higher mobility, therefore in presence of an electric field they can rapidly diffuse out of the dielectric through the gate. The holes migrate slowly towards the semiconductor interface through thermally activated hopping. The accumulation of positive ionization charge in the dielectric results in a shift of the threshold voltage towards negative values. The value of the shift is proportional to the irradiated dose and the sensitivity of the device is measured as the threshold shift per unit dose dV_{th}/dGy.

Typical silicon-based RADFET sensitivities range between $0.05-0.30$ V/Gy, depending on oxide thickness and photon energy. This value refers to passive mode operation, where no bias is applied to the gate electrode of the device. However, larger sensitivities can be achieved applying a positive bias to the gate, as the electric field improves the exciton dissociation [8].

The accumulated positive charge over time often results in other unwanted effects, such as increase of leakage current and increased flicker noise, which deteriorate the device behavior [8].

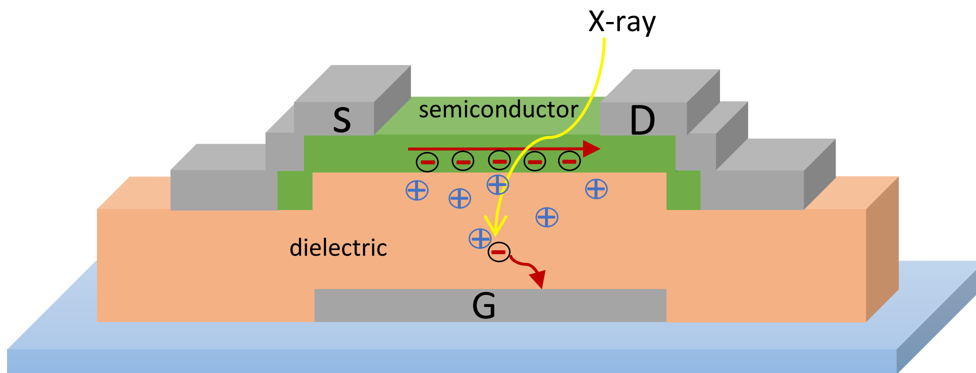


Figure 1.5: Schematic of RADFET interaction with radiation.

A downside of RADFETs is that they have limited sensitivity to ionizing radiation due to the low dielectric constant (k) of silicon oxide used as insulating layer.

Recently, researchers from University of Bologna (Italy) and CENIMAT laboratories at NOVA University of Lisbon (Portugal) have developed a promising Radiation sensitive OXide Field Effect Transistor (ROXFET), which is a TFT based on high mobility amorphous oxide semiconductor, and high-k dielectric [9, 10].

The devices are made of amorphous IGZO semiconductor, which shows great radiation hardness [9]. The gate dielectric layer is based on the high-k and high atomic number Z tantalum oxide (Ta_2O_5), which gives high sensitivity to ionizing radiation. The first version of ROXFET devices was made with a sputtered dielectric with Ta_2O_5/SiO_2 and SiO_2 multi-layer stack [10]. Last year, during a master thesis project [11], ROXFETs with atomic layer deposited bi-layer $Ta_2O_5-Al_2O_3$ were studied to improve the properties of the existing devices. The results seemed promising, but it was not possible to establish a reproducible fabrication process and the majority of the fabricated devices were broken. The aim of this thesis work is to solve the fabrication issues in order to obtain a reproducible and stable procedure for ROXFETs based on atomic layer deposited gate dielectric.

ROXFETs combine the high sensitivity to ionizing radiation with the compatibility with high integration density, large-area production, low cost, and flexibility, as they can be produced on flexible plastic substrates. This makes ROXFETs compatible with the requirements of wearable sensors, which need to be light-weight, able to bend according to the body movements, and should cause no harm to humans when touching the body [12].

The appeal of ROXFETs lies in the following characteristics [10]:

- **High sensitivity**. The sensitivity is calculated as the threshold voltage shift per unit dose. In ROXFETs the reported sensitivity of (3.4±0.2) V/Gy [10] corresponds to an order of magnitude increase with respect to the typical Si-based RADFETs in passive mode.

- **Radiation hardness**. The oxide semiconductor properties show great radiation hardness, meaning that no other transistor parameters, such as subthreshold slope or mobility, are affected.

- **Stable measurements**. The device response to impinging radiation is in the order of second. After exposure the threshold voltage tends to return to the initial value. The relaxation happens on much longer timescales.

- **Device resettability**. It is possible to increase the charges annealing rate by increasing the temperature or by applying strong electric fields. In this way it is possible to easily reset the device to its initial state to reuse it.

- **Real-time, remote measurement**. The positive charge accumulation in the dielectric induces a change in the channel impedance. The impedance can be passively probed by a RFID chip remotely controlled wireless by a RFID reader. The change of impedance will be directly proportional to the received radiation dose.

1.3.1 Dielectric layer

AOS TFTs have been demonstrated to have good operation characteristics with a large variety of gate dielectrics [4]. The optimization of the gate dielectric is crucial to increase the TFT performances, as well as the radiation sensitivity. Indeed, the radiation response is given by the positive charge accumulation in the dielectric.

Dielectrics deposited at low temperatures with amorphous structures has been demonstrated to be the best choice for oxide TFTs [6]. Indeed, amorphous dielectrics do not have grain boundaries, which are known to act as preferential paths for impurity diffusion and leakage current. Moreover, amorphous layers have smoother surfaces than polycrystalline ones, thus improving the interface properties.

The structure composed by the gate electrode, the insulator, and the semiconductor can be considered as a parallel plates capacitor. The capacitance is directly proportional to the dielectric constant of the insulator k and the channel area, and inversely proportional to its thickness. High capacitance improves the TFTs performances decreasing the operating voltage. A larger capacitance can be obtained either by decreasing the gate dielectric thickness or by using high-k dielectrics.

In radiation detectors, the gate dielectric thickness can not be decreased excessively because the absolute value of the threshold voltage shift is proportional to the gate dielectric thickness squared d^2 [8]. Therefore, high-k gate dielectrics are an optimal choice to increase the capacitance in radiation sensitive transistors.

However, materials with very high k present some drawbacks, such as increased parasitic capacitance and low energy gap [6]. Dielectrics with low band gap cause an increase of undesirable gate leakage. The band gap is not the only parameter to be considered in this framework: another requirement is that the offsets of the dielectric's VBM (in a p-type transistor) and the CBM (in a n-type transistor) should be at least 1 eV relative to those of the semiconductor [6]. AOS-based TFT are unipolar n-type devices, so only the offset between the dielectric and semiconductor CBM have to be taken into account. Other problems of high-k dielectrics are related to threshold-voltage control [13] and the presence of high charge trap density [14].

The ideal dielectric for x-ray detectors should have high ionizing radiation cross section. As the X-ray interaction with matter occurs mainly via photoelectric effect, the interaction probability is directly proportional to Z^n, where Z is the atomic number of the material and n is a coefficient varying between 3 and 4 [15]. Tantalum has high atomic number $Z = 73$, compared to traditional CMOS technology where silicon has $Z = 14$.

In this thesis, tantalum oxide (Ta_2O_5) and aluminum oxide (Al_2O_3) were used as gate dielectric materials. A study on the properties of a single-layer of Ta_2O_5 and various multi-layer $Ta_2O_5{-}Al_2O_3$ is performed.

The multi-layer dielectric stack allows to combine the advantages of two high k dielectrics while minimizing the individual disadvantages [3]. For instance, Ta_2O_5 has a

high dielectric constant ($k \approx 25$), but also a relatively high leakage current due to relatively small band-gap energy (4.5 eV). On the other hand, Al_2O_3 has a dielectric constant $k \approx 9$ and a band gap of 8 eV [16]. Even if it has a lower dielectric constant compared to Ta_2O_5, it guarantees a low leakage current thanks to larger band gap, as well as low interface trap density with the oxide semiconductor [16].

Chapter 2

Device fabrication

This chapter presents the fabrication procedure performed during this thesis to obtain the ROXFET devices.

Each layer composing the TFTs must be deposited and patterned. Section 2.1 will give an overview of the two deposition methods used for this project: sputtering and atomic layer deposition. Concerning the pattering of the layers, Section 2.2 explains the steps needed to perform optical lithography, Section 2.3 outlines the principles of etching, and Section 2.4 compares traditional lithography with lift-off lithography.

Finally, Section 2.5 explains how the methods presented in the previous sections were applied for the fabrication of the ROXFETs. In this section the fabrication parameters are reported and the structure of the samples is explained in detail.

2.1 Deposition methods

2.1.1 Sputtering

In physical vapor deposition (PVD) methods, atoms of a chosen material are ejected from a solid target, transported in vacuum, and deposited on a substrate. There are various ways to eject atoms from the target: resistive heating, electron beam heating, laser ablation, or ion bombardment. Among these methods, the latter is the most used one and is known as sputtering [17]. Ion bombardment is performed using ionized inert gas plasma. The gas used is usually argon due to its low cost and high cross-section.

To explain sputtering phenomenon, it is appropriate to start from the simplest sputtering apparatus, the DC diode (Fig. 2.1). It consists of two plates kept at high potential difference, placed in a high-vacuum chamber. When the sputtering gas is introduced in the chamber at a pressure in the millitorr range and the voltage is applied to the plates, a plasma discharge is created under appropriate conditions. The plasma is created as follows: a high potential difference between two electrodes accelerates free electrons nat-

urally present in the atmosphere. Energetic electrons collide with the neutral gas atoms present in the chamber, exciting or ionizing them. If the first process happens, the excited gas eventually returns to its ground state emitting the characteristic glow discharge. Instead, if the gas gets ionized, positive ions are generated. In the plasma, free electrons are lighter than ions, and therefore they have higher velocities. This results in a layer depleted from electrons close to the cathode, called sheath layer, where most of the potential drop happens [18]. The positive ions composing the plasma are drawn to the cathode and accelerated through the sheath layer. A target with the material to be sputtered is placed at the cathode. When ions knock the negatively biased target several processes can happen [19]: sputtering, emission of secondary electrons, ion implantation, ion reflection, or heat generation. The atoms sputtered from the target travel in the vacuum chamber and then deposit on the substrate, as well as on the chamber walls. The secondary electron emission is also an essential process in sputtering. Indeed, secondary electrons emitted from the cathode surface are accelerated away from it through the sheath layer, gaining enough energy to ionize more gas atoms, allowing for a self-sustaining plasma [18].

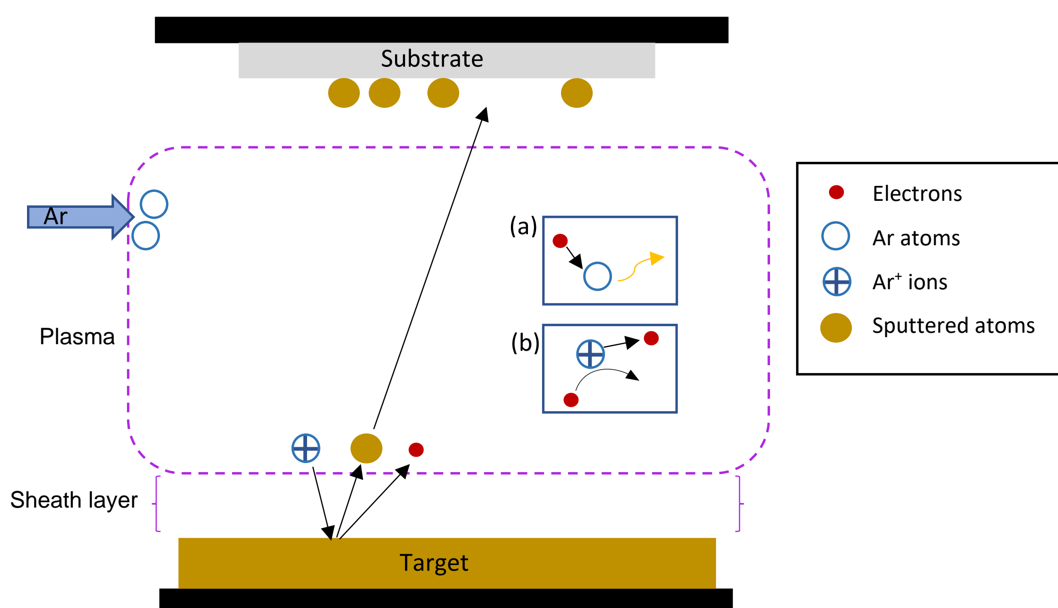


Figure 2.1: Schematics of the sputtering process. Two possible mechanisms happening in the plasma are shown: (a) excitation of Ar atoms which decay emitting a photon; (b) ionization of Ar atoms.

The removal rate of atoms from the target can be measured by the sputtering yield, defined as the ratio between the number of atoms ejected from the target due to sputtering and the number of incident ions. The sputtering yield is influenced by many

factors, such as energy of incident particles, target material, incident angle of particles, and crystal structure of the target surface [19].

DC diodes have some major limitations. First, the aforementioned process works only for a metal cathode. Indeed, if the target is an insulating material, the glow discharge can not be sustained, as the positive ions on the target surface will cause a buildup of charges, which reduces the bombardment [19]. Secondly, the deposition rates are extremely low due to low levels of gas ionization and sputtering of the cathode.

Radio frequency (RF) diode sputtering solves the problems of traditional DC diode sputtering. It uses an alternating RF diode, which couples the electron motion in the plasma. The electrons manage to stay longer in the plasma, resulting in higher collisional ionization and higher plasma density. RF sputtering allows the deposition of insulating materials, as the alternated potential prevents the buildup of charges on the target surface. Besides overcoming the problems of DC diode sputtering, the alternating potential applied to the sample placed at the anode allows for sputter-cleaning and planarization via resputtering of the deposited film from ion bombardment [18].

Sputtering systems used nowadays are mainly based on magnetron sputtering. It uses strong magnetic fields to keep secondary electrons spatially confined close to the target surface. The secondary electrons are accelerated perpendicularly to it through the cathode fall potential. On the other hand, the magnetic field is usually set up so that the field lines are parallel to the target surface. The resulting Lorentz force on the electrons confines them in cycloidal orbits parallel to the target surface. This increases the ionization of the sputter-gas atoms, resulting in denser plasma and higher deposition rates [18]. In current magnetron sputtering systems, a permanent magnet is mounted behind the target in a motor-driven mechanism performing circular orbits [18]. The motion of the magnet is necessary to avoid high non-uniform local erosion of the target, which would result in non-uniform deposition on the sample.

A variant of traditional sputtering is the so-called reactive sputtering. This method consists in the addition of reactive gas to the sputtering atmosphere, which will react with the material from the target to form composites. For example, adding oxygen it is possible to form oxide films and adding nitrogen nitrites can be formed.

2.1.2 Atomic layer deposition

Atomic layer deposition (ALD) is a chemical vapor deposition (CVD) method. In all CVD methods, the materials are deposited by chemical reaction between two or more source materials in the gas phase and the substrate surface. The gaseous reactants (precursors) are brought into the deposition chamber, where the chemical reaction that forms the film is enabled usually by heating or plasma; afterwards, the by-products are desorbed and pumped away.

ALD works in pulsed mode, introducing one precursor at a time in the reaction chamber separated by inert gas purging (usually nitrogen) to avoid uncontrolled homo-

geneous reactions in the gas phase between precursors. Figure 2.2 shows a schematic of the working principle of ALD deposition. During each pulse, the precursor saturates the surface, leaving a monolayer of material. The purge then removes the excess gas and the reaction byproducts. As long as the precursor dose is large enough to saturate all the available surface sites, the process is self-limiting and the film is deposited in a layer-by-layer fashion. This allows for superb uniformity and thickness control of the deposited layer, making ALD a perfect technique to deposit high quality films also over large areas. The obtained film is generally dense, continuous, and homogeneous [20].

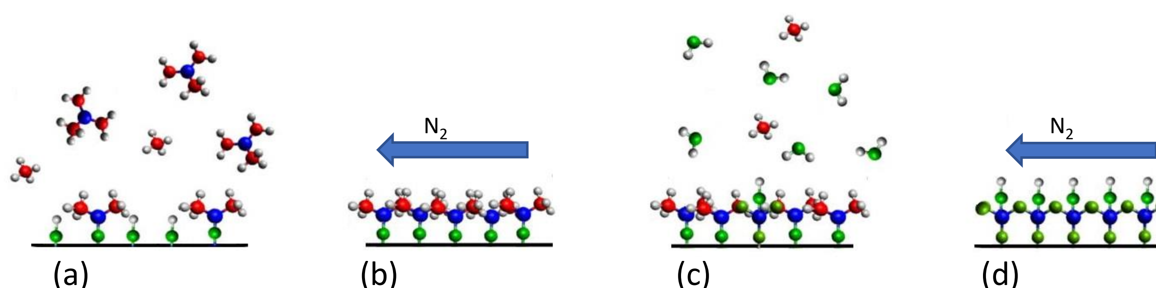


Figure 2.2: Steps performed for one cycle of the ALD deposition of aluminum oxide. (a) the precursor (TMA) is pulsed inside the chamber, TMA reacts with available reaction sites on the surface (OH groups); (b) a TMA mono-layer is deposited, then excess precursor and by-products are purged away with N_2 flow; (c) H_2O is pulsed in the chamber, it reacts with the TMA layer; (d) excess H_2O and by-products are purged away with N_2 flow. Adapted from [21]

.

The deposition rates in CVD methods depends on the process chemistry, and therefore they are strongly dependent on temperature, but in general they are of the order of 0.1-10 nm/s. In ALD the actual deposition rates have to take into account also the inert purging between the cycles, resulting in slower deposition rates of few nanometers per minute [17].

It must be noted that actual ALD deposition present some non-idealities related to the process. The first cycles can show problems in nucleation due to a lack of reactive sites on the starting surface, resulting in imperfections in case of ultrathin films. Moreover, the growth rate can vary between the first cycles, in which the precursor molecules are deposited on the starting surface, and the following ones, in which the growth occurs on the film material itself. Usually, the growth rate is slower at the beginning, during the nucleation period. In order to obtain a linear correlation between the film thickness and the number of ALD cycles it is necessary to consider a large enough number of cycles [20]. Another non-ideal phenomenon is the growth of sub-monolayers, which is due to the so called *steric hindrance* [17]. Indeed, large precursor molecules can prevent other precursor molecules from reaching close-by reactive sites, leaving them unreacted.

2.2 Photolithography

Photolithography techniques imply the use of a polymer called photoresist, which is able to change its properties upon exposure to UV light. To this aim all the photolithography processes must be performed in a dedicated room with yellow light, as photoresists are sensitive to light with wavelength below 450 nm [17].

2.2.1 Photoresist spincoating

Spincoating is the most common method to coat substrates with photoresist, providing high homogeneity and throughput [22]. A few milliliters of soluted photoresist are deposited on the substrate, which is then spun according to an optimized recipe, typically at a rotational speed of several 1000 rpm (rotations per minute). The photoresist spreads thanks to centrifugal force, forming a uniform film, and the excess photoresist is spun off the edges of the substrate. At the same time part of the solvent evaporates form the film. Evaporation of the solvent ensures that the resulting film is sufficiently stable to remain on the sample during handling after coating.

Spincoating is a fairly fast coating method. The films deposited in this way are smooth and with easily controllable thickness. On circular substrates the layer is generally very homogeneous, while on squared substrates there can be significant accumulations of resist in the corner regions of the sample. On textured substrates, the thickness homogeneity of the resist is negatively affected, as there can be unintentional accumulation of resist in spaces and holes during the spinning.

2.2.2 Pre-exposure bake

After the spincoating, the resist film has a residual solvent concentration of 20-40% which is usually desorbed during a baking step (*soft bake* or *pre-exposure bake*). Typically the bake leaves between 3% and 10% residual solvent, which is sufficiently small to keep the film stable during subsequent lithographic processing [23].

Removing the excess from the photoresist film results in the following major effects: photoresist film thickness is reduced, development properties are changed, and adhesion is improved [23].

Typical baking temperatures are in the range 90-120°C. The temperature must be carefully optimized, because a too high temperature will decompose the photoactive compound, leading to lower sensitivity to exposing radiation [17].

2.2.3 Patterning by light exposure

The exposure of the photoresist upon UV light changes its chemical properties, resulting in increased (positive resist) or decreased (negative resist) solubility in the developer.

Different methods to imprint the pattern on the sample exist. They can be divided in two groups, depending on whether the design is patterned using a mask which is irradiated, or if the pattern is directly written on the sample without the use of any mask.

Mask exposure

A photomask is the stencil used to reproduce a desired pattern on film of photoresist. It is composed of transparent features in the regions that have to be exposed and dark features in the regions that must be covered from exposure. Commercial-grade masks are usually made by glass plate with a thick (> 100 nm) chromium layer deposited on it [17]. Optical lithography with a mask is historically the first method used and it is still the most common patterning technology [17]. The photomask is placed above the photoresist-coated surface. Usually, the sample and the mask are inserted in a mask aligner in order to align the pattern already present on the sample with the new pattern. Perfect overlay of the layer stack is a critical factor for successful lithography. Once the alignment is performed, the system is irradiated with UV light. A mercury lamp is often used, as it provides strong spectral peaks at wavelength of 436 nm, 405 nm, and 365 nm. The needed exposure energy is typically in the range of 100 mJ/Cm^2, leading to exposure times of the order of a few seconds [17].

It is possible to distinguish different lithography methods (Fig. 2.3):

- **Contact lithography**. It is the simplest and most used lithography technique. The photomask and the sample are brought into close contact and exposed. Resolution is determined by the pattern dimension on the mask. Vacuum contact can be used for extremely small patterns, but in this case the resist is more prone to stick to the mask, which can get dirty.

- **Proximity lithography**. In proximity lithography a small gap (up to few tens of micrometers) is left between the mask and the sample. It can be done in the same machine as contact lithography. Proximity lithography reduces the mask damage and formation of mask defects. However, the resolution limit increases significantly [23]:
$$Resolution \sim \sqrt{g\lambda}, \tag{2.1}$$
where g is the mask-sample gap and λ is the exposure wavelength.

- **Projection lithography**. In projection optical lithography the pattern irradiated on the sample is smaller than the corresponding image in the mask, in contrast to contact and proximity lithography, where the image is the same size as mask pattern. The light passing through the transparent parts of the mask is converged onto the photoresist layer by dedicated optics. In this way it is possible to pattern much smaller features than contact optical lithography. At the same time,

having bigger masks brings down the mask production costs as lower resolution requirements must be met. It also eliminates the mask damage and contamination problems associated with contact lithography. This is the preferred technique for submicron patterning [24]. Lens imperfection, i.e. aberrations, can be generally considered negligible due to the high quality of lens production. Therefore, the limit of resolution in projection optical lithography is due to diffraction effects [23].

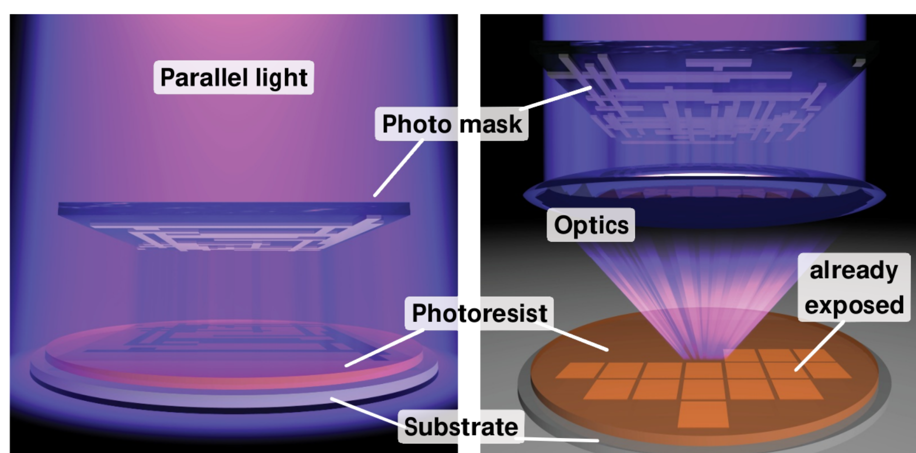


Figure 2.3: Schematics of the possible lithography methods [22]. Proximity lithography (left) and projection lithography (right) are shown. The schematics of contact lithography is the same as proximity lithography, but the mask and the photoresist layer are in close contact.

Direct laser writing

Direct laser writing is a maskless lithography technique. A UV laser scans through the sample and exposes the photoresist step-by-step (Fig. 2.4). This method eliminates the need of expensive photomasks. With a suitable software, the patterns can be immediately transferred to the laser writing machine, allowing great flexibility if the design has to be modified many times. The major drawback of this technique is the long writing time needed for each pattern. Writing times depend on the wanted resolution and can reach several hours. Direct laser writing is suitable when only few substrates must be patterned and it is the preferred method to produce photomasks.

The laser is optically focused onto the sample surface and the sample is placed on a $x - y$ stage. The laser beam scans the sample line-by-line in the x direction while translating in the y direction. Two types of writing are possible [17]: raster scan and vector scan. In raster scan every pixel is scanned, exposing only the desired pixels. On

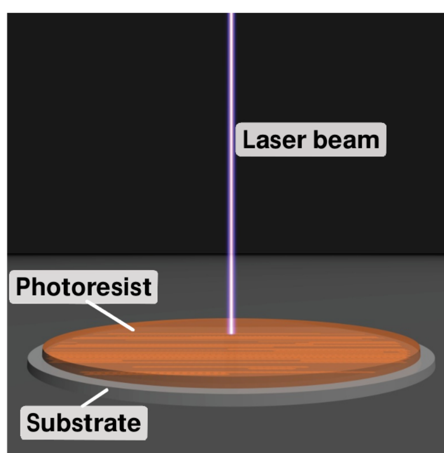


Figure 2.4: Direct laser writing working schematic [22].

the other hand, in vector scan, the empty pixels are skipped, which allows faster writing at the expense of accuracy and complexity.

2.2.4 Post-exposure bake

The post-exposure bake is a step required in order to complete the chemical reaction started by the exposure in some kinds of photoresists, called *chemically amplified resists* [17]. In this case the exposure only initiates the photopolymerization process, and the catalyst molecules generated by the UV light react during the bake.

In all resists, post exposure bake can be used to help the diffusion of photogenerated molecules, which smooths out the optical interference effects [23].

It is important to note that the effects of high temperatures on the degradation of photoresist properties discussed above for the pre-exposure bake, apply also here.

2.2.5 Development

During the development the soluble parts of the photoresist are etched away. For positive photoresist the exposed parts are removed. For negative photoresist the exposed parts become stable, while the unexposed parts remain soluble in the developer. The final outcome of photolithography is the combined effect of exposure and development optimization, and the two steps can compensate each other to a certain extent. Development is concluded by completely rinsing away the developer and drying the sample.

Sometimes after the development, an additional baking step at high temperatures is performed to harden the remaining resist, so that it will withstand the harsh conditions of the etching step [22].

2.3 Etching

Once the resist has the desired pattern, it protects the underlying material, while the exposed areas can be etched away. Etching can be distinguished into two categories: wet etching and dry etching, depending on whether the etchant is a liquid or a gas, respectively.

The basic steps are the same for both wet etching and dry etching: transport of etchant to the surface, surface process (including adsorption, reaction and desorption), and removal of product species. Etch rates are typically $10-1000$ nm/min, for both wet and dry processes [17].

Wet etching

Wet etching uses a liquid etchant able to dissolve the addressed material, resulting in soluble products. Wet etching mechanisms can be classified into two categories: metal etching by electron transfer and acid-base reaction etching [17].

Wet etching is usually performed in a heated quartz bath filled with the etchant solution. It is often desirable to be able to tune the temperature to control the rate of the reaction.

The reaction dynamic of wet etching can be either reaction-limited or transport-limited. In reaction-limited etching the etchant has great availability, while the chemical reaction at the surface is slow and determines the etching rate. The reaction rate increases by increasing the etchant concentration. Usual activation energies for reaction-limited etching are between $30-90$ kJ/mol. In transport-limited processes the reaction rate is limited by the availability of the etchant close to the surface. Therefore, the limiting mechanism is the transportation of the reactant to the surface by convection and diffusion. The etching rate can be increased by agitation or stirring. Typical activation energies are in the range $4-25$ kJ/mol [17].

Wet etching is generally isotropic, acting equally in all spatial directions. The isotropic etching front proceeds as a spherical wave from all points in contact with the etchant. This results in side etching below the photoresist layer (undercutting). Anisotropic wet etching can happen in case of crystalline materials, where the etching rate depends on the crystal plane orientation.

Dry etching

Dry etching involves the use of a gaseous etchant. Dry etching is usually performed in a vacuum chamber with an RF generator and a gas system, where plasma is generated.

Dry etching is a broad term which includes physical reaction, chemical reactions, or a combination of the two. Depending on the reaction involved, dry etching can be classified as follows [25]:

- **Ion-beam milling (IBE)**. Etching is performed only by a physical bombardment, which causes momentum transfer between energetic inert ions (usually Ar^+) and the substrate surface. It is usually accomplished at low pressures (10^{-4} Torr).
- **Chemical plasma etching (PE)**. Neutral etchant species diffuse on the surface and react with it, forming volatile products. In this case, the plasma is only needed to supply the gaseous etchant to the surface. Chemical etching dominates due to high pressures of about 1 Torr.
- **Reactive ion etching (RIE)**. The etching happens through physical and chemical etching. First, ions impact the surface perpendicularly damaging it; then, the plasma neutrals can react chemically with the surface. RIE happens at intermediate pressures ($10^{-3} - 10^{-2}$ Torr).

A desirable property of the etching process is good chemical selectivity, to be able to remove only the addressed material. Good chemical selectivity is important to avoid etching of the eventual underlying layers of materials, as well as also resist etching. To maximize selectivity, physical removal by bombardment of energetic ion should be decreased as much as possible. PE and RIE have good chemical selectivity thanks to the chemical component of the reaction.

In dry etching the degree of isotropicity can be controlled by the etching parameters. Good anisotropicty can be obtained as the particle bombardment is perpendicular to the horizontal surfaces, leading to vertical etching, while sidewalls do not experience ion bombardment, reducing the etch rate in the lateral direction. Therefore, low-pressure operation favors anisotropy because bombardment is more directional [17]. Anisotropic etching is obtained in IBE and RIE thanks to the physical etching reaction.

2.4 Conventional and lift-off photolithography

In conventional lithography the layout is designed onto the material which needs to be patterned. During the photolithography process, the photoresist is kept as a protection on the areas which need to be preserved. The uncovered areas are removed form the sample by the etching process.

However, in some cases lift-off photolithography is preferred. In lift-off photolithography, the photoresist is deposited and patterned before the material deposition. The pattern should be reversed with respect to conventional photolithography. Indeed, one should leave uncovered by the photoresist the areas in which the material should remain. Once the material is deposited, the photoresist is stripped away. In this way the material deposited over the photoresist is removed, while the material on the uncovered areas remains. This method is preferred in multi-layer structures to avoid etching of

the underlying layers. On the downside, lift-off patterning results in generally less defined structures and more residues [17]. It is not possible to use lift-off procedure when the deposited material covers the photoresist sidewalls, as the stripping medium can only dissolve the resist structures if it is able to reach it through the sidewalls. This makes lift-off unsuitable when combined with isotropic sputter processes and films of large thickness [22]. Moreover, it can not be used if the deposition is carried out using high temperatures, as the photoresist already present would be affected. Indeed, high temperatures can modify the photoresist chemical structure (cross-linking) or degrade it [22].

Figure 2.5 shows a comparison of the workflow of conventional photolithography and lift-off photolithography. It can be noted that the same pattern can be achieved changing a positive photoresist with a negative photoresist (or vice versa) when switching from conventional photolithography to lift-off photolithography. Equivalently the photomask can be inverted, achieving the same results.

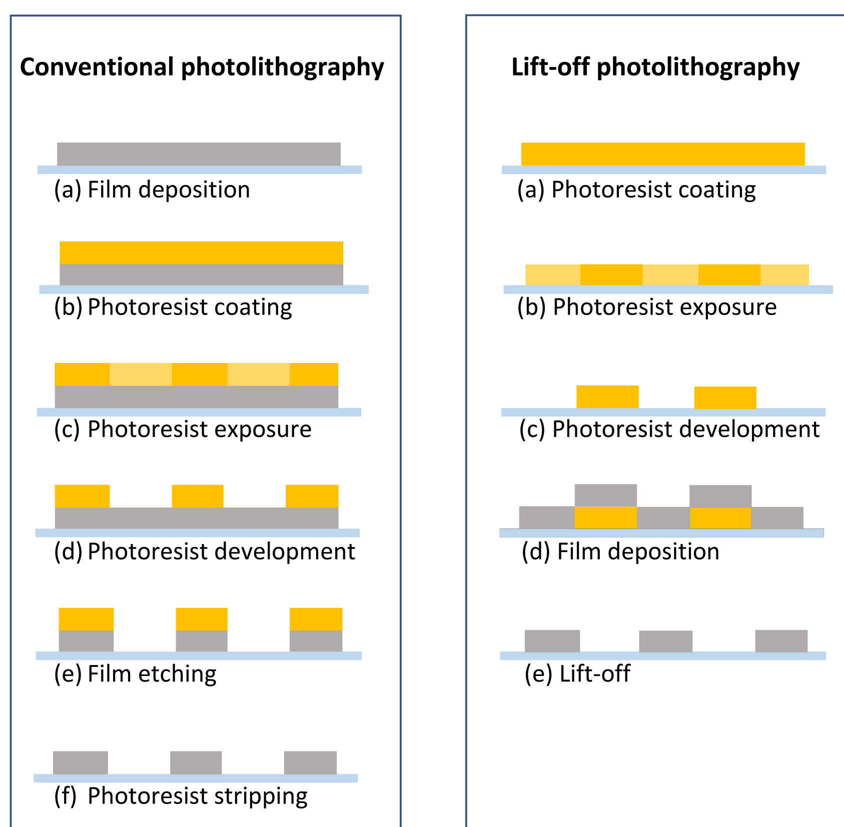


Figure 2.5: Comparison between conventional (left) and lift-off (right) photolithography workflows.

2.5 ROXFET fabrication procedure

The device fabrication was performed at CENIMAT clean-room facilities.

The produced devices are composed of four layers. For each layer the fabrication can be divided into two steps: deposition of the film material and patterning of the desired layout with optical lithography. Some additional processes, as surface treatment and thermal annealing, were performed at set steps to improve the device performances. The workflow of the fabrication procedure, which will be presented in the following sections, is summarized as follows:

1. **Preliminary step**: production of one photomask for each layer.
2. **Substrate cleaning**.
3. **Gate layer**:
   (a) Photolithography pattern with dedicated mask;
   (b) Mo sputter deposition;
   (c) IZO sputter deposition, needed as protective layer;
   (d) Lift-off.
4. **Gate dielectric layer**:
   (a) ALD deposition of Ta_2O_5 and Al_2O_3;
   (b) Photolithography pattern with dedicated mask;
   (c) Dry etching;
   (d) Resist stripping.
5. **Semiconducting layer**:
   (a) Photolithography pattern with dedicated mask;
   (b) O_2 plasma treatment;
   (c) IGZO sputter deposition;
   (d) Lift-off.
6. **Thermal annealing**: at 180°C or 300°C.
7. **Source and drain layer**:
   (a) Photolithography pattern with dedicated mask;
   (b) Mo sputter deposition *or* IZO sputter deposition;

(c) Lift-off.

8. **Thermal annealing** at 180°C.

Table 2.1 contains the details of the fabrication of each layer.

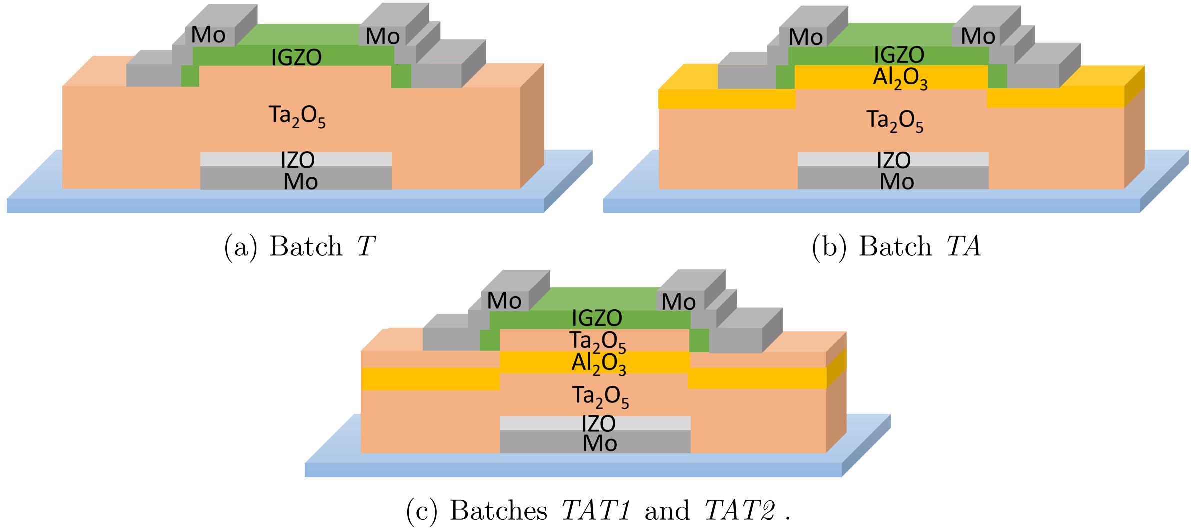
<table>
<tr><th>Layer</th><th>Deposition method</th><th>Material</th><th>Thickness</th><th>pattering method</th></tr>
<tr><td>Gate</td><td>sputtering</td><td>Mo</td><td>60 nm</td><td rowspan="2">lift-off</td></tr>
<tr><td>Protective layer</td><td>sputtering</td><td>IZO</td><td>30 nm</td></tr>
<tr><td>Dielectric</td><td>ALD</td><td>Ta_2O_5
Al_2O_3</td><td>100 nm total</td><td>dry etching (SF_6)
dry etching (CF_4/O_2)</td></tr>
<tr><td>Semiconductor</td><td>sputtering</td><td>IGZO</td><td>60 nm</td><td>lift-off</td></tr>
<tr><td>Source-drain</td><td>sputtering</td><td>Mo</td><td>60 nm</td><td>lift-off</td></tr>
</table>

Table 2.1: Outline of the layers composing the ROXFETs. The gate and its protective layer were patterned at the same time with the same structure. Batch T was replicated using 120 nm of sputtered IZO as source and drain material.

Four different batches were fabricated varying the gate dielectric composition. The total thickness of the gate dielectric layer was kept constant at 100 nm for all the samples. The dielectric layer of the fabricated batches was the following: **(i)** a batch with single gate dielectric layer made of Ta_2O_5, **(ii)** one with a bi-layer dielectric composed by 80 nm Ta_2O_5 and 20 nm Al_2O_3, and **(iii)** two batches with a tri-layer $Ta_2O_5-Al_2O_3-Ta_2O_5$ structure with different disposition (60 nm−20 nm−20 nm and 70 nm−20 nm−10 nm). For all the multi-layer structures the Ta_2O_5:Al_2O_3 ratio was kept constant (80%:20%).

All samples shared the same gate layer composed by molybdenum (Mo), with an indium-zinc oxide (IZO) protective layer on top. The semiconductor IGZO layer was common among all batches as well. Molybdenum was also used as the source and drain material in all the samples. Moreover, in batch T, the source and drain material effect was studied reproducing the same samples also with IZO top contacts. In this case the layer was sputtered, as for the other electrodes, and the thickness was 120 nm.

Figure 2.6 shows a schematic diagram of the layers composing the devices and highlights the differences among the batches.



(a) Batch *T*

(b) Batch *TA*

(c) Batches *TAT1* and *TAT2* .

Figure 2.6: Schematics of the layers composing the TFTs in the different batches. The layers are not to scale, therefore a single schematics was made for batches *TAT1* and *TAT2* since their only difference is the different relative thickness of the Ta_2O_5–Al_2O_3 layers. Batch *T* was replicated using IZO as top contact material (not shown).

For each batch with a certain gate dielectric layer, two different samples were fabricated comparing the effect of two different annealing temperatures (T = 180°C and T = 300°C) performed before the top-contact deposition.

Table 2.2 summarizes the distinctive features of each batch. Each batch is composed of two samples annealed at different temperatures. Each sample has a pattern containing 9 TFTs, which will be described in the following section.

Batch ID	dielectric composition	thickness (nm)	Sample ID	Annealing T (°C)
T	Ta_2O_5	100	*T (180)* *T (300)*	180 300
TA	Ta_2O_5–Al_2O_3	80–20	*TA (180)* *TA (300)*	180 300
TAT1	Ta_2O_5–Al_2O_3–Ta_2O_5	70–20–10	*TAT1 (180)* *TAT1 (300)*	180 300
TAT2	Ta_2O_5–Al_2O_3–Ta_2O_5	60–20–20	*TAT2 (180)* *TAT2 (300)*	180 300

Table 2.2: Overview of the distinctive features of the fabricated samples. One sample per type was fabricated with 9 TFT in each sample. The reported order of the layers composing the dielectric is the one followed during the deposition of the materials.

2.5.1 Sample's design

The design patterned (Fig. 2.7) on each sample is a 3 × 3 TFTs matrix. Each transistor has individual gate and drain contact pads, while the source is common. The TFT structure has channel dimensions $L = 20$ µm and $W = 320$ µm.

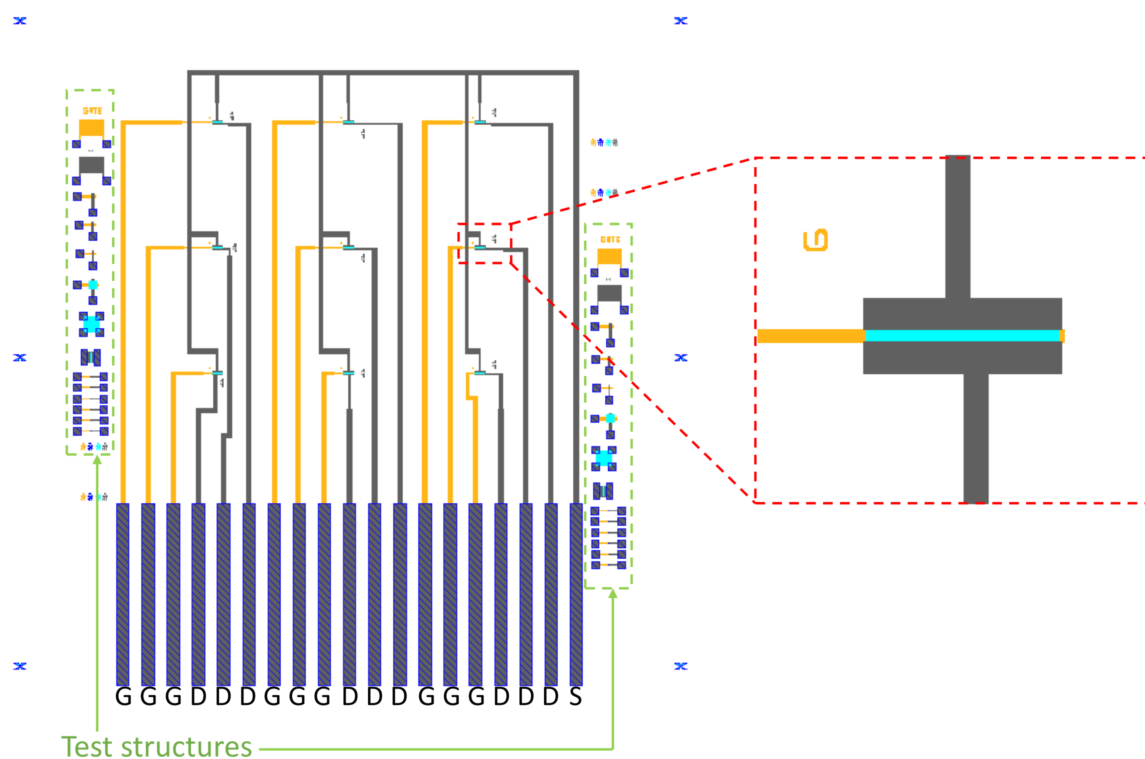


Figure 2.7: Layout used for the fabrication of the samples (left) and close-up of a single transistor (right). The different colors indicate different layers of materials: orange for the gate layer, light blue for the semiconductor layer, and gray for the source/drain layer. the dielectric layer covers all the sample except the areas dashed in blue, corresponding to the contact pads.

At the sides of each sample there are some test structures. Generally, the test structures have different patterns, which isolate the properties of each one of the layers composing the TFTs. They have three main purposes: (i) they can be used to measure the electrical parameters of each deposited layer, (ii) in case of malfunctioning devices, they can be used to determine the problematic step in the fabrication, and (ii) they are useful to assess the uniformity of the layers throughout the sample comparing the properties of corresponding structures at the opposite sides. For each side of the sample there is one resistive test structure for the gate, one for the source and drain, and one for the semiconductor. Moreover, there are four metal-insulator-metal (MIM) capacitive test

structures of size 20 µm × 20 µm, 50 µm ×, 50 µm, 100 µm × 100 µm and 200 µm × 200 µm; and two metal-insulator-semiconductor (MIS) ones of size 100 µm × 100 µm and 200 µm × 200 µm. Resolution test structures are also present to be analyzed by optical microscope, in order to asses the quality of the pattern. At each corner of the matrix and in the middle of the vertical sides there are patterns which help the alignment of subsequent layers.

2.5.2 Substrate preparation

The samples were produced on Corning Eagle glass cut in 2.5 cm × 2.5 cm squares. Each substrate was prepared performing the following standard cleaning process:

(i) 10 min acetone ultrasound bath;

(ii) 10 min isopropyl alcohol ultrasound bath;

(iii) rinse in ultra-pure deionized water;

(iv) dry with nitrogen flow;

(v) 10 min baking on a hot plate at 110°C.

The baths and the rinse were needed to remove contaminants from the surface. The acetone bath ensured the removal of organic particles, while isopropyl alcohol removed contaminated acetone [22]. The baking on the hot plate ensured the desorption of water molecules by evaporation.

2.5.3 Masks production

A mask was created for each layer of the ROXFETs. The mask was then used to pattern the design onto the substrate by photolithography, exposing the sample in a mask aligner.

The masks were prepared on 10 cm×10 cm Corning Eagle glass. The cleaning process was the same to the aforementioned for the substrates, but to ensure a higher cleanness degree, the substrates were initially also cleaned with soap. Then, a 200 nm thick layer of molybdenum was deposited by sputtering. The deposition was performed at room temperature, applying a RF power of 175 W, with a pressure of 1.7 mTorr, and 50 sccm flow of Ar.

The masks were patterned through direct laser writing, which is the most common patterning method for mask production. The machine used was a *Heidelberg Instruments µPG101 laser micro-writer* (Fig. 2.8).

The design was encoded in a GDS file, which was transferred to the machine to be written on the sample. The design was patterned on negative photoresist (*AZ nLOF 2020*) by laser writing, using a 20 mm writing head, 36 mW at 92%. Subsequently,

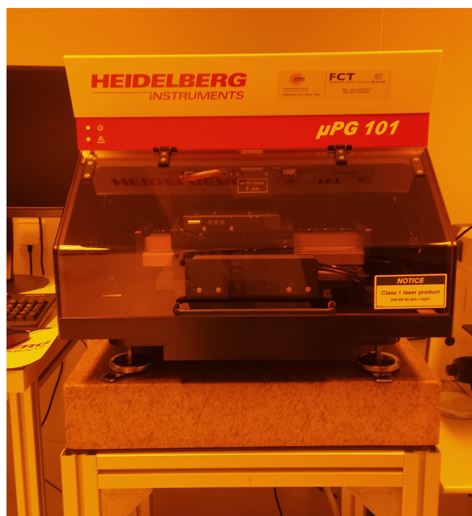


Figure 2.8: *Heidelberg Instruments µPG101 laser micro-writer* used to pattern the photomasks. The instrument has moving x-y stage and a changeable writing head.

the mask was dry etched by RIE with SF_6 gas. The etching was carried out at room temperature for 600 s, with a pressure of 50 mTorr, RF power of 60 W and SF_6 flow of 10 sccm.

2.5.4 Sputtering deposition

The sputtering deposition was performed in two *AJA ATC-1800* systems, one of which is shown in Figure 2.9. The sputtering parameters of the electrodes and the semiconductor layer are reported in Table 2.3. A pre-sputtering step preceded all the sputtering processes, which was needed to clean the target surface from eventual contamination. During this step the plasma was present, but the mechanical shutter between the target and the substrate was kept closed.

Electrode deposition

The gate layer was composed of 60 nm of Mo and 30 nm IZO, both deposited by sputtering at room temperature. The IZO layer was intended as an etching stopping layer as Mo and Ta_2O_5 are both etched by SF_6 gas.

The influence of the source and drain material was studied during this thesis. The properties of the source and drain composed by 60 nm Mo and 120 nm IZO were compared in batch *T*. Both materials were deposited by sputtering at room temperature.

Molybdenum is an optimal contact material because of its low work function (4.3–4.9 eV) and low reactivity to atmosphere [26]. IZO has a work function of 4.9–5.2 eV [27] and is suitable for transparent electronic applications. The work function of a-IGZO is

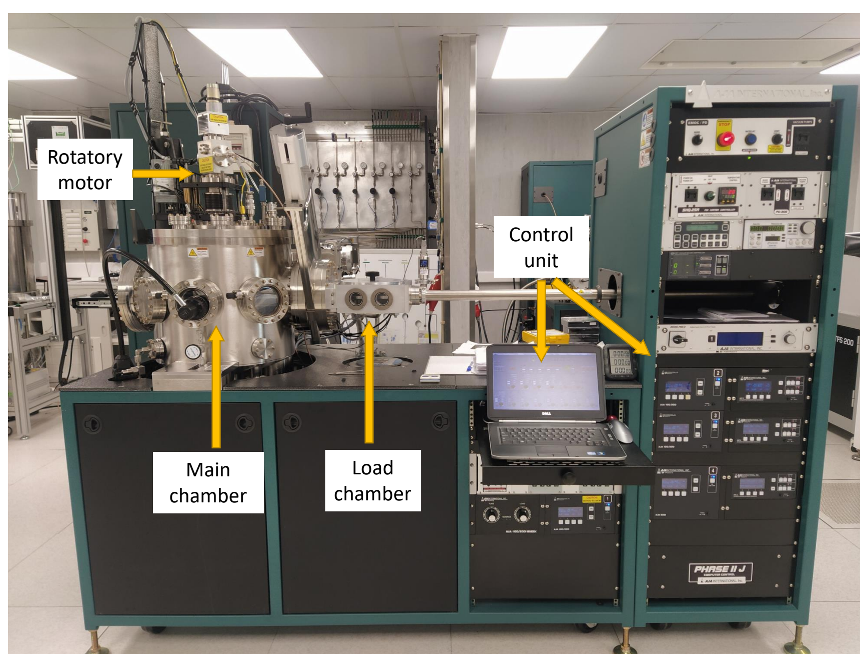


Figure 2.9: One *AJA ATC-1800* system used for the sputtering deposition. The Mo and the IGZO targets were in the same sputtering system (shown), while the IZO target was in another equivalent system (not shown). A rotatory motor rotates the sample holder, to guarantee high uniformity of the deposited film.

generally ~ 4.5 eV. Therefore, Mo is particularly suitable to obtain low contact resistance [28].

Semiconductor deposition

Sputtering is the most used deposition method of AOS. It allows low-temperature deposition (typically room-temperature) and guarantees good adhesion and dense structure of the deposited layers [13]. It is easy to modulate the film properties by adjusting the sputtering pressure and power. In addition, reactive sputtering involving different concentrations of Ar and O_2 can be used to adjust the oxygen content in the IGZO layer.

It is possible to perform the IGZO deposition both by a multi-component target sputtering and a co-sputtering of three targets (In_2O_3, Ga_2O_3 and ZnO). Co-sputtering allows to tune and optimize the components percentage in the film and it should be preferable. Although some early tests were carried out by co-sputtering IGZO deposition, the devices reported in this thesis were all fabricated with the multi-component target, due to contamination of the In_2O_3 target in the co-sputtering system.

The multi-component target resulted in a film with In:Ga:Zn atomic ratio of 2.5:1.2:1, measured by energy-dispersive x-ray spectroscopy. The atomic ratio is relevant, as the

Material	Temperature	RF power	Pressure	Gas	Gas flux
Mo	RT	175 W	1.7 mTorr	Ar	50 sccm
IZO	RT	100 W	2.3 mTorr	Ar	20 sccm
				O_2	0.3 sccm
				H_2	0.8 sccm
IGZO	RT	100 W	2.3 mTorr	Ar	20 sccm
				O_2	5 sccm

Table 2.3: Sputtering deposition parameters. Room temperature (RT) deposition means that no intentional substrate heating is performed. All the depositions are performed with an initial chamber pressure of $p \sim 10^{-7}$ mTorr.

different components give different properties to the IGZO. High indium content is generally linked to higher carrier concentration and higher mobility due to the In spherical 5s orbitals, which act as a carrier transport passage. [13].

2.5.5 Dielectric ALD deposition

The dielectric layer of the ROXFETs have been deposited with ALD using thermal activated processes. A *Beneq TFS 200* ALD system was employed, which is shown in Figure 2.10. The machine followed a highly automated procedure set by a recipe, a code-like language in which the operations to be performed are described in sequence.

The tantalum oxide precursor was tantalum(V) ethoxide, with chemical formula $Ta_2(OC_2H_5)_{10}$. It needed to be heated at 160°C to be used, due to its low vapor pressure. The deposition temperature of 225°C corresponded to a growth rate of 0.556 Å/cycle. The steps performed during each cycle were:

(i) 0.2 s precursor pre-chamber load;

(ii) 0.05 s wait;

(iii) 0.2 s precursor pulse (release form the pre-chamber);

(iv) 0.2 s line purge;

(v) 5 s N_2 purge;

(vi) 3 s H_2O pulse;

(vii) 5 s N_2 purge.

It should be noted that each cycle is extremely long (13.85 s), resulting in long deposition times (e.g. 7 hours and 11 minutes for 100 nm). The deposition is followed by 25 minutes of line purge.

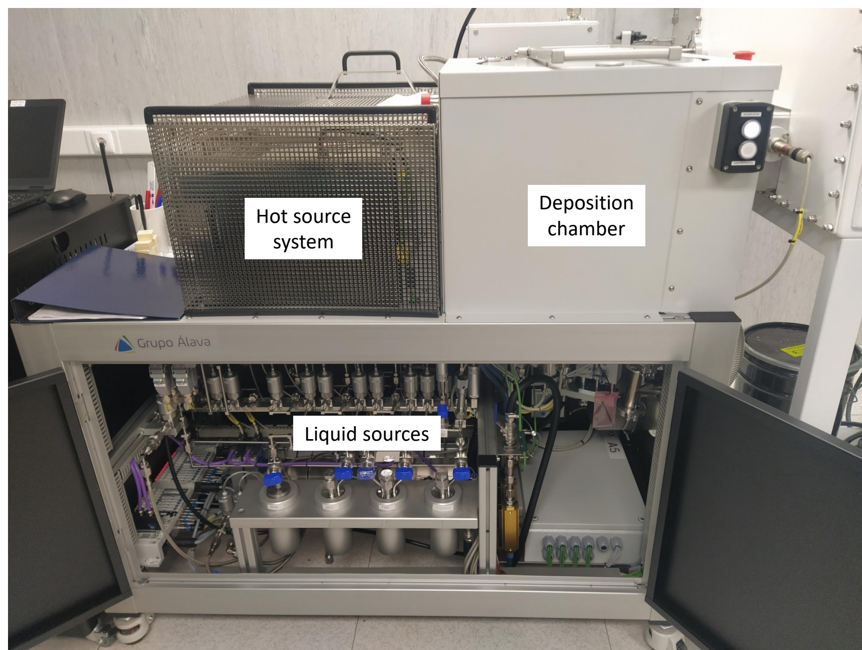


Figure 2.10: *Beneq TFS 200* ALD system used for ALD deposition of the gate dielectric. The system is controlled by a dedicated program run on a computer.

Aluminum oxide deposition used tri-methyl-aluminum (TMA) as a precursor, whose chemical formula is $(CH_3)_3Al$. The deposition was carried out at 225°C without precursor heating, and it had a deposition rate of 1.1654 Å/cycle. The steps performed during each cycle were:

(i) 0.15 s TMA pulse;

(ii) 0.65 s N_2 purge;

(iii) 0.15 s H_2O pulse;

(iv) 1 s N_2 purge.

The cycle here needed less steps, as precursor did not need to be heated. The deposition times of aluminum oxide were shorter thanks to shorter cycles (1.95 s each) and higher deposition rate per cycle. The deposition is followed by 4 minutes of line purge.

2.5.6 Photolithography

All the layers were patterned in a mask aligner, using a dedicated mask. The instrumentation used for the photolithography process is shown in Figure 2.11; to avoid undesired

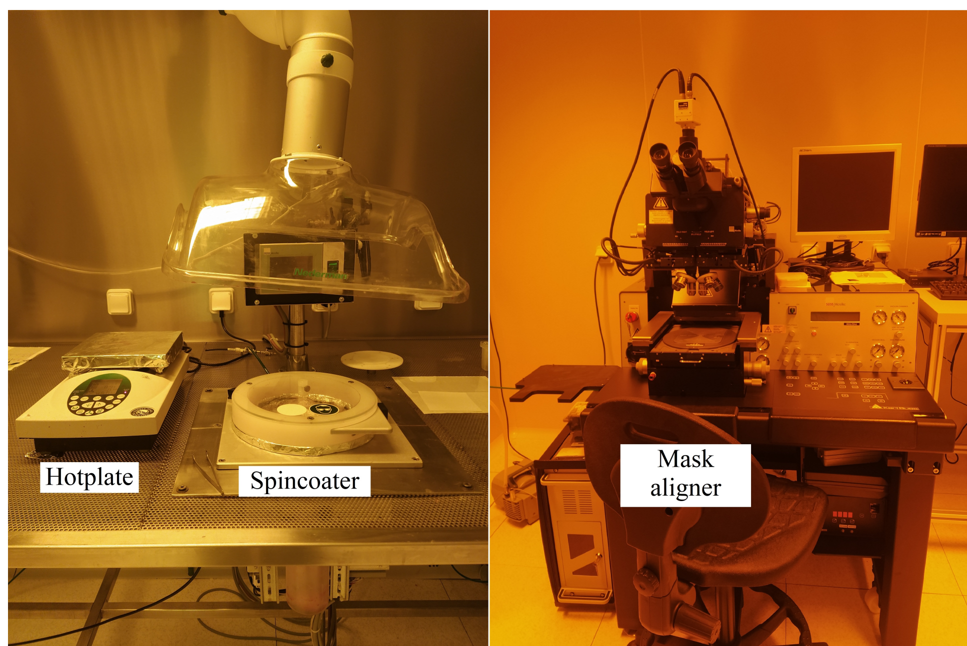


Figure 2.11: Photolithography setup. Hotplate used for pre- and post-exposure bake, spincoater used for the photoresist deposition and mask aligner used to perform the exposure.

reactions of the photoresist, all the process is carried out in a dedicated clean room with yellow light.

The photoresist was deposited by spincoating using a *Suss CT62* bench-mounted spincoater. Negative photoresist was used for all layers. Two photoresist of the *AZ nLOF* series [22] were used, the *AZ nLOF 2020* and the *AZ nLOF 2070*. They are both chemically amplified resists and they differ only by the layer thickness obtained under same spincoating conditions, 2 µm and 7 µm respectively. A thicker photoresist was used for the multi-layer dielectric, as the Al_2O_3 etching was very aggressive.

The exposure was performed in a *Suss MA6 UV* mask aligner, using an *OSRAM HBO* 350 W mercury lamp.

The irradiation dose was controlled changing the exposure time. The optimized exposure dose depends on the resist, the resist film thickness, and the emission spectrum of the light source [22]. Another factor that can influence the exposure time is the pattern size. Indeed, if the exposure dose is too high, light scattering in the resist film also exposes covered parts of the resist, preventing the realization of very small structures [22]. For the ROXFET devices, the exposure time was changed only when changing the photoresist, as thicker layer needed higher irradiation dose.

Post-exposure bake was needed to activate the chemically amplified resist. For layers patterned by lift-off a shorter time was used to ease the removal of the photoresist with

the deposited material on top. On the opposite side, for the etching process a longer time was needed to strengthen the photoresist so that it was not removed by the etchant.

The development was performed in *AZ 726* developer. The sample was placed in the developer for an appropriate amount of time, then it was rinsed in two subsequent baths in ultra-pure deionized water to remove residuals. Afterwards, the sample was blown dry with nitrogen flow.

To conclude, the samples were inspected with an optical microscope to check the quality of the pattern. In case of underdevelopment, the sample was placed again in the developer for a few seconds.

The parameters used for the photolithography are summarized in Table 2.4.

Process	Parameters
spincoating	4000 rpm for 30 s
soft baking	120 s at 110°C
UV exposure	1.5 s (*AZ nLOF 2020*) 3.9 s (*AZ nLOF 2070*)
post-exposure baking	120 s at 110°C for etching 90 s at 110°C for lift-off
development	50 s (*AZ nLOF 2020*) 90 s (*AZ nLOF 2070*)

Table 2.4: Parameters used for the photolithography process for the two photoresist. Note that regardless the photoresist used, the post-exposure baking times are different for conventional photolithography (etching) and lift-off photolithography.

2.5.7 Etching and lift-off

The dielectric layer was patterned by dry etching in *Trion PHANTOM III* reactive ion etching system (Fig. 2.12).

SF_6 etches Ta_2O_5 as well as Mo, therefore the presence of an IZO protective layer is necessary to avoid uncontrolled over-etching.

Aluminum oxide is often dry etched with Cl-based gases, which are not present at CENIMAT facilities. Therefore, during this thesis a dry etching process for Al_2O_3 based on CF_4 and O_2 was implemented. Aluminum oxide is etched by F radicals generated by the reaction between CF_4 and O_2 [29]. The parameters were optimized to maximize the etching rate while maintaining the lowest possible power, in order to minimize physical etching. According to the literature, the CF_4/O_2 relative percentage does not influence the etching rate, while the process pressure is a relevant parameter [29]. The etching rate was calculated using a mono-layer of 100 nm of Al_2O_3. The Al_2O_3 was deposited over a conducting material to be able to quickly probe the removal of the insulating layer

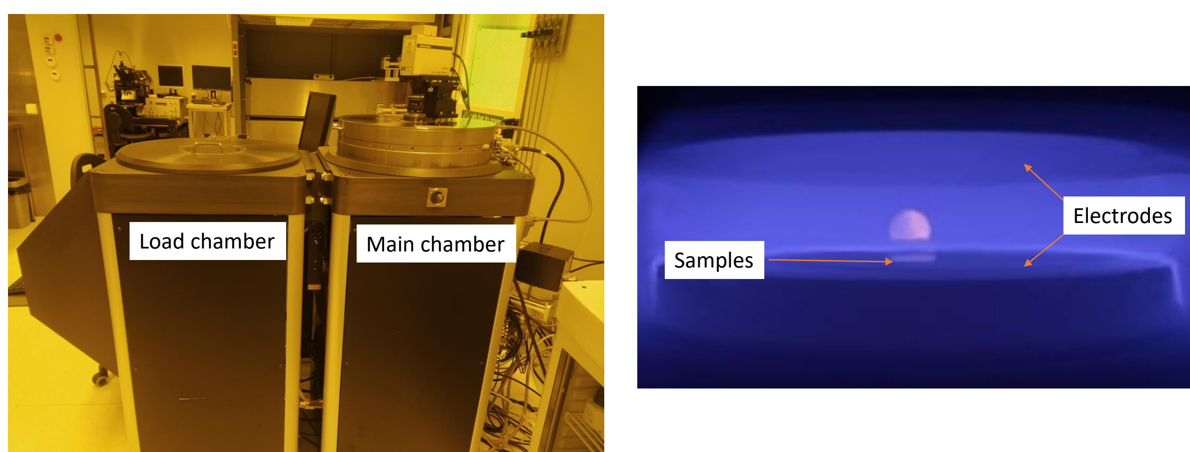


Figure 2.12: *Trion PHANTOM III* reactive ion etching system outside structure (left) and inside of the main chamber during plasma etching (right). The etching parameters are set by a control unit connected to the system.

by measuring the impedance of the surface with a multimeter. It would have been ideal to use an IZO layer to ensure that the ALD growth of Al_2O_3 was not affected by the starting surface, however IZO was etched by CF_4/O_2 RIE. Therefore, copper was chosen as underlying metal and the growth of 100 nm (875 cycles) Al_2O_3 ensured an accurate thickness control of the dielectric layer.

At first, small pieces of glass substrates were used to perform the etch tests. Once the etch rate was determined, a test was performed on a patterned sample, check the uniformity of the etching and to ensure that the photoresist was not removed during the process. A final test was performed on a sample with the same multi-layer of batch TA (80 nm of Ta_2O_5 and 20 nm of Al_2O_3). The time to completely etch the Al_2O_3 layer had to be increased compared to the previous tests performed, probably due to interface properties between Ta_2O_5 and Al_2O_3.

As fluoride etches also IZO and Mo, it is not recommendable to use this method in a device where the investigated structure has the Al_2O_3 layer in contact with the gate. Fluoride is very aggressive, thus significantly affecting also the photoresist layer. For this reason the thicker *AZ nLOF 2070* resist was used when Al_2O_3 was present in the gate dielectric layer.

Table 2.5 summarizes the etching parameters used for the gate dielectric layer.

After the patterning, the resist was stripped away with acetone. Although acetone is a commonly used stripper in laboratories, it tends to leave residues on the sample surface, making it unsuitable for industrial semiconductor processing [23]. To solve this problem, the sample was then placed in an isopropyl alcohol bath for 5 min to remove residues; finally it was rinsed with ultra pure water and dried with nitrogen flow.

Acetone was also used as a stripper for lift-off. To perform the lift-off, the sample was

Material to etch	Ta_2O_5	Al_2O_3
etching gas	SF_6	CF_4/O_2
gas flow (sccm)	10	12/3
chamber pressure (mTorr)	50	15
RF power (W)	60	60
etching rate (nm/min)	4.98	1.69

Table 2.5: Dry etching parameters used to etch Ta_2O_5 and Al_2O_3.

placed in an acetone bath for approximately 10 min. After that, the photoresist with the deposited material on top can be removed by gently brushing the surface. Brushing should be avoided if there are layers already present below. For this reason, for the last two layers, the container with acetone and the sample was placed in an ultrasound bath. The ultrasounds help the physical detachment of the photoresist from the surface. The majority of the photoresist was removed in this way and only small residuals needed to be brushed. In the ultrasound bath, the removed layer is broken into a lot of very small pieces which fluctuate in the acetone, thus extra care must be taken to ensure that the removed pieces do not redeposit on the sample surface.

Similarly to what was done for resist stripping after etching, afterwards the sample was placed in an isopropyl alcohol bath for 5 min to remove residues, then rinsed with ultra pure water and dried with nitrogen flow.

2.5.8 Surface plasma treatment

Before the semiconductor deposition an oxygen plasma treatment was performed.

A plasma treatment can be beneficial for different reasons. First, it removes possible contamination and photoresist residuals thanks to the so-called plasma cleaning. Moreover, it has been demonstrated that oxygen plasma treatment can tune the dielectric properties, both in tantalum oxide [30] and in aluminum oxide [31]. Oxygen plasma exposure can suppress oxygen vacancies present in the dielectric, leading to beneficial effects.

The oxygen treatment was performed in the sputtering machine just before the semiconductor sputtering itself. Since no material should be deposited during the surface treatment, the RF power supply was connected with the sample holder instead of the target. The treatment was performed for 10 minutes; the RF applied power was 10 W; the pressure was set to 2.3 mTorr, and the gas flow was 20 sccm of Ar and 20 sccm of O_2.

2.5.9 Thermal annealing

Two thermal annealings were performed on the samples: one after the semiconductor layer (pre-contact) and one at the end of the sample fabrication (post-contact).

Thermal annealing is a common practice in IGZO TFTs fabrication, to improve the stability and performances of the devices. Among the various effects of thermal annealing, it reduces the electron trap density in the bulk and at the interface, and reduces the sub-gap states, like oxygen vacancies [32]. It also releases the mechanical stress accumulated by the device. Sometimes annealing under controlled atmosphere is performed to favor the diffusion of different species in or out of the surface.

Smaller V_{th} instability has been demonstrated in IGZO TFTs thanks to annealing [33]. The annealing was shown to reduce the shallow trap states. However, smaller instabilities due to the deep charged defects remained.

Optimized two-step annealing has been shown to be beneficial to TFTs fabrication [34], improving the stability of the devices. Also, it is common practice to perform the annealing before the contact deposition when the chosen annealing atmosphere is oxygen, to avoid oxidation of the top contacts [4].

For each batch two identical devices were fabricated, varying only the temperature of the pre-contact annealing. Two different temperatures were considered: 180°C and 300°C. The temperature of the post-contact annealing was 180°C for all the samples. All the thermal annealings were performed in air on a hot plate for 1 hour with a temperature ramp of 450°C/hour, which was the maximum ramp available in the hot plate. After the annealing time was over, the samples were left to slowly cool down on the hotplate.

As two different temperatures were used only for the pre-contact annealing, form now only that one will be mentioned and it will be referred simply as "annealing".

Chapter 3

Devices characterization

3.1 Direct-current electrical measurements

The following sections describe the electrical characterization of ROXFET devices performed at CENIMAT facilities. It includes the standard electrical characterization for the extraction of the figures of merit from the transfer characteristics, and the stability measurements performed by Positive Gate Bias Stress (PGBS).

The device characterization was performed in the dark, as TFTs are sensitive to the light conditions [35]. Indeed, impinging light causes the photo-creation of oxygen vacancy states; then the subsequent photo-ionization of these states generates free electrons, which cause a negative shift in threshold voltage.

3.1.1 Electrical characterization

The current-voltage (I-V) characteristics were measured using *Cascade Microtech EPS 150* manual probe station connected to a *KEYSIGHT B1500A A* semiconductor device analyzer (Fig. 3.1) available at CENIMAT laboratories. The probe station is suitable for room temperature measurements performed with a dark box enclosure for light and RF shielding. It has three micro-manipulators, which are used to connect the measuring instrument to the sample contact pads.

The standard characterization to extract the transport parameters, performed on every sample was the following:

- **Stabilization**: Three transfer characteristics in saturation regime (V_D = 5V). A one-way curve was acquired going only from negative to positive gate voltages. It is known that ROXFETs tend to experience V_{th} shift during the first measurements, so this step was needed to stabilize the devices. The measurement was also needed to choose an appropriate V_G range for the following measurements. Moreover, the broken devices were identified and filtered out during this phase.

- **Transfer characteristic**: both in linear ($V_D = 0.1$ V) and in saturation ($V_D = 7$ V) regime. The curve was measured going from negative to positive V_G values and vice versa to evaluate the entity of the eventual hysteresis. The typical measurement ranges never exceeded ± 5 V.

- **Output characteristic**.

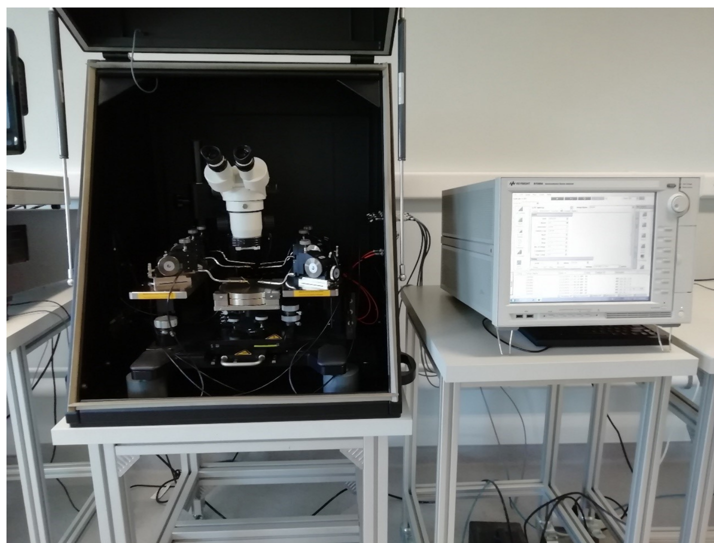


Figure 3.1: Probe station (left) and semiconductor parameter analyzer (right) used for the measurements performed at CENIMAT.

The transport parameters were extracted form the transfer characteristics according the relations reported in Section 1.1.1. It was chosen to calculate the threshold voltage form a linear regression of the $\sqrt{I}-V$ plot in saturation regime to be sure to minimize the contact resistance effect. Also the reported mobility is the one calculated in saturation regime for the same reason. The other parameters (S, I_{on}/I_{off} and the hysteresis) are calculated form the transfer characteristic obtained in linear regime.

3.1.2 Positive gate bias stress

Desirable properties for practical application of transistors are good stability and reliability upon the application of a current or voltage stress for a long time.

However, oxide transistors undergo a shift in the threshold voltage when a constant bias or current is applied to the device [6]. When a positive bias is applied to the gate electrode, the threshold voltage of the devices shifts towards more positive values. The shift can be caused either by negative charge trapping at the channel/dielectric interface or by negative charge injection into the gate dielectric bulk. The two processes can be

distinguished, as the latter requires a larger energy to recover, since the energy barrier is higher than in the charge trapping mechanism [32]. Moreover, the role of the interaction between the back-channel in the semiconductor layer and the atmosphere was shown to play a relevant role in the threshold shift [36]. Common practices to decrease these instabilities of oxide TFT are the addition of a passivation layer, or annealing at high temperatures [37].

Positive Gate Bias Stress (PGBS) test can be performed to assess the entity of the threshold shift. PGBS consists in the application of a constant positive bias to the gate electrode, while keeping the source and drain grounded. After defined intervals of time, the bias is interrupted to perform quick I-V transfer characteristics in linear regime. The transfers are needed to measure the threshold shift as a function of the stress time. It is important to note that the transfers alter the stress procedure, thus they should be performed as quickly as possible.

Generally, the threshold voltage shift is towards the value of the applied bias V_{bias}, and tends to recover to the original value, once the stress is removed. Typically, the threshold voltage shift (ΔV_{th}) as a function of time under PGBS can be described by a stretched exponential [37]:

$$\Delta V_{th}(t) = V_0 \left[1 - \exp\{-(t/\tau)^{\gamma}\}\right], \tag{3.1}$$

where τ is the characteristic time constant, γ is the dispersion parameter, and $V_0 = V_{th}(0) - V_{th}(\infty)$, with $V_{th}(0)$ corresponding to the threshold voltage at the start of the experiment and $V_{th}(\infty)$ the one at the end.

For practical applications, where stability of the devices during operation is essential, it would be ideal to have a large characteristic time constant during the stress time, and a small one during recovery.

The PGBS measurements were performed using the same apparatus employed for the standard electrical characterization described in the previous section. One transistor per sample was tested. A bias of $V_{bias} = 3$ V was applied for 1 h, and then the recovery was measured during an equal amount of time without stress with the probes disconnected from the device. Both for the stress and the recovery, the measurements were performed in the linear regime ($V_D = 0.1$ V) after 5 minutes from the start, 10 minutes, and then every 10 minutes.

3.2 Radiation characterization

The ROXFETs were tested under x-ray radiation at University of Bologna facilities, to asses their radiation response.

The aim of the measurements was to quantify the sensitivity of ROXFETs upon exposure to a specific radiation dose. The sensitivity is defined as the threshold voltage shift per unit dose received (dV/dGy). The doses considered in this thesis are referred to

Air Kerma, which is defined as the sum of the initial kinetic energies of all the charged particles liberated by uncharged ionizing radiation, per unit mass of air.

In addition to that, the cumulative dose degradation was estimated. The radiation sensitivity in solid state detectors decreases with increasing cumulative total dose. All the devices revert to their initial sensitivity after a sufficient period of time.

The radiation sensitivity was measured for all the samples with Mo top electrodes. In order to measure all the 9 transistors present in one sample sequentially, a customized sample holder was used. The structure was 3D printed previously for this project. During this thesis, all the wire connections were upgraded. At the same time, the structure was slightly modified to solve a previously present shading problem: a piece of the sample holder, which partially covered the structure from the x-ray source, was moved to assure higher control on the received dose. The sample holder was connected to a multiplexer, based on a *ADG333A chip*, which was directly interfaced with a *KEYSIGHT B2912A* source measure unit (SMU). The SMU drove the multiplexer to measure one transistor at a time sequentially. The SMU was controlled with a dedicated software on a computer. A *Hamamatsu microfocus L12161-07* was used as an x-ray source; it has a W-target, with variable accelerating voltage between 40 kVp and 150 kVp, and current in the range 10−500 µA. The apparatus is placed inside a shielded bunker for safety reasons, and it is shown in Figure 3.2.

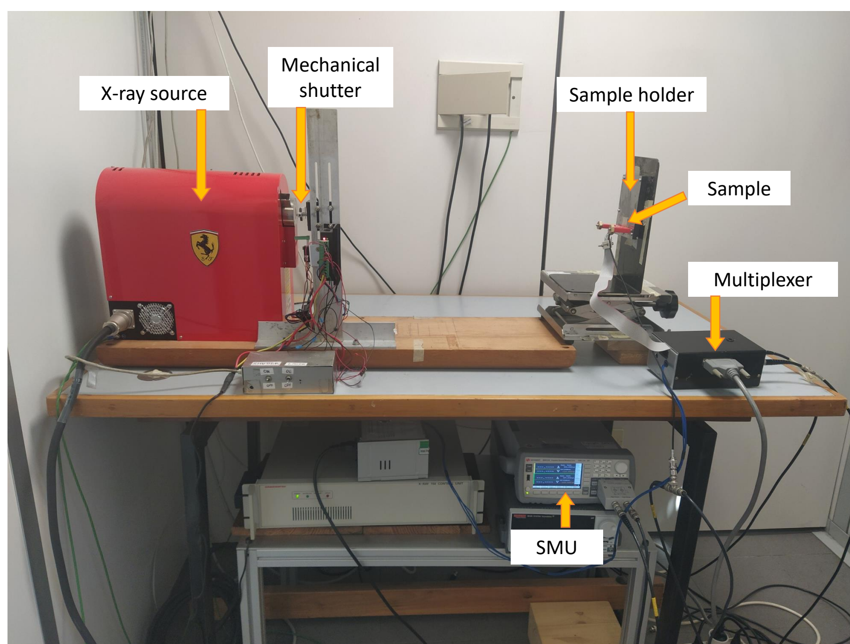


Figure 3.2: Apparatus used for the x-ray irradiations in the sensitivity measurements. The same x-ray source was used also for the *C*-*V* measurements. The apparatus is located inside a shielded bunker at University of Bologna facilities.

Prior to the x-ray irradiation, the devices were kept overnight in the dark with the electrodes connected to the ground. The aim is to stabilize the threshold voltage as much as possible, eliminating the unwanted accumulated or trapped charges. Indeed, all the devices had a positive V_{th} shift and during the initial hours of stabilization the entity of the shift was large enough to affect the sensitivity of the devices.

The irradiated dose was controlled, according to previous calibration, setting the current and accelerating voltage in the microfocus, and the distance between the source and the sample. For all the measurements the voltage was kept constant at 60 kVp and the source-sample distance was 50 cm. The current was changed between 169 µA and 411 µA, to obtain different dose rates. The exposure time was set thanks to a mechanical shutter controlled by a LabVIEW program.

The measurements were performed every minute throughout the duration of all the experiment. To ensure that the devices were stressed as little as possible, a specific section of the software controlling the SMU allowed "pulsed" measurements (Fig. 3.3). In these measurements the gate voltage was applied for a short time at specific values and the current was measured accordingly, instead of sweeping V_G continuously in a certain range. This method allowed extremely fast measurements with minimum stress to the devices.

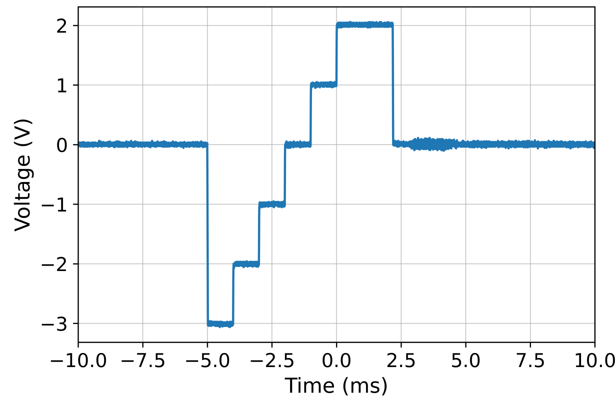


Figure 3.3: Example of the voltage applied by the SMU during a measurement in the range [-3, 2] V, in which the voltage was applied for 1 ms at steps of 1 V. The measurement was performed using an oscilloscope connected to the SMU.

The transfer curves were measured in saturation regime ($V_D = 5$ V), usually in the range $[-5, 5]$ V with steps of 1 V, resulting in a total measurement time of 11 ms. The range was adjusted as needed, as some samples showed large positive threshold voltage shift during the stabilization period. Then the irradiation was performed in the range form 1 mGy to 20 mGy. Multiple irradiations were performed for the smallest doses (1 mGy and 2 mGy) to be able to extract an average sensitivity. Afterwards the recovery

of devices was monitored for about two hours.

The recovery has been shown [10] to follow a stretched exponential curve:

$$\frac{V_{th}(t) - V_{th}(\infty)}{|V_{th}(0) - V_{th}(\infty)|} = \exp\{-(t/\tau)^{\gamma}\}, \tag{3.2}$$

where τ is the relaxation time constant and γ is the exponent. The normalization is needed to cancel the effect of different irradiated doses, indeed it was shown [10] that the recovery dynamics is independent on the dose.

3.3 Capacitance-voltage measurements for sub-bandgap density of states determination

A TFT can be considered as a parallel plates capacitor. When the source and drain electrodes are short circuited, the total capacitance of the metal-insulator-semiconductor structure can be probed.

Capacitance-voltage (C-V) measurements are widely used in TFT investigation to determine oxide thickness, oxide charges, interface trap density [38], flat-band voltage, and work function [39].

In this work, C-V measurements have been used to determine the sub-bandgap density of states (DOS) at the semiconductor-dielectric interface.

The capacitance can be related to the density of states [40, 41]. The proposed model is a physics-based model which takes into account the various parts of the transistor to build up the total measured capacitance C_{tot}. The model states that C_{tot} is composed of two contributions in series, the dielectric oxide capacitance C_{ox} and the capacitance of the density of states in the semiconductor layer C_{DOS}, i.e.

$$C_{tot} = \frac{C_{DOS} C_{ox}}{C_{DOS} + C_{ox}}. \tag{3.3}$$

The dielectric capacitance C_{ox} gives a fixed contribution. It depends only on the dielectric permittivity and its geometry, namely its thickness d and the channel area ($A = L \cdot W$). In series with this capacitance there is a variable contribution given by the accumulation of charges in the semiconducting layer, which is linked to the density of states, as the charges accumulate only when it is energetically possible. The quantum capacitance due to the density of states C_{DOS} is given by two parallel capacitance contributions: the capacitance of the localized charges in the sub-bandgap states (C_{loc}) and the capacitance due to the free electrons in the conduction band (C_{free}). At $V_G < V_{th}$, the contribution given by the sub-bandgap states is dominant because the conduction band is depleted from free electrons. When $V_G > V_{th}$ the channel becomes populated with electrons and C_{free} dominates.

As calculated in previous work [11], it is possible to link the measured capacitance with the semiconductor DOS. The DOS (g) is related to the quantum capacitance with the following relation:

$$g(E) = \frac{C_{DOS}}{q_0 A d}, \tag{3.4}$$

where q_0 is the elementary charge and the g is a function of the energy E. The energy in a TFT can be related to the applied gate voltage potential by

$$E = \int \left(1 - \frac{C_{tot}}{C_{ox}}\right) dV_G \tag{3.5}$$

with a constant offset that can be determined if the flat-band potential is known.

The C-V measurements were performed before and after the irradiation of a dose of 400 mGy. The aim was to extract the change in the sub-bandgap DOS due to the ionizing radiation. To perform the irradiation the *Hamamatsu microfocus* described in the previous section used. The microfocus was placed inside a shielded bunker for safety reasons, and it was operated by a remote control system on a computer. The total dose of 400 mGy was obtained applying an accelerating voltage of 60 kVp and a current of 411 µA, and by placing the sample at 25 cm distance for 100 s.

The setup for the C-V measurements is schematized in Figure 3.4.

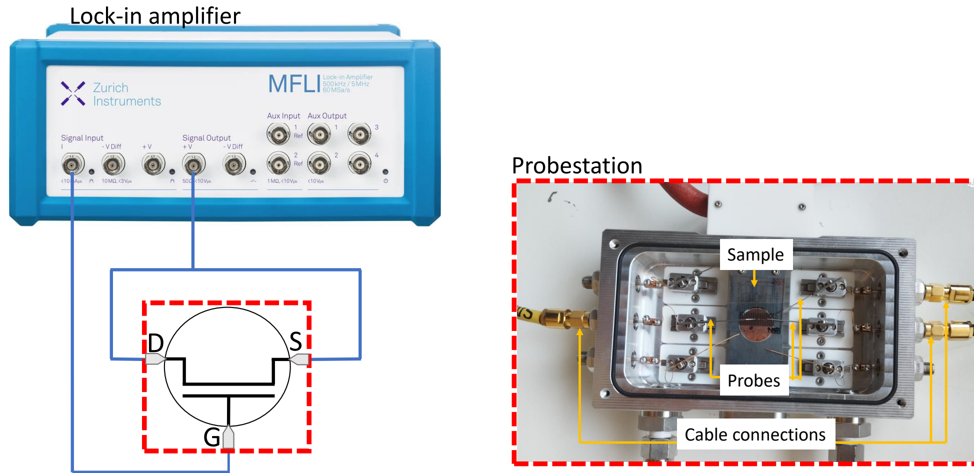


Figure 3.4: Schematic representation of the setup used for C-V measurement. The source and the gate of the measured transistor were short circuited and connected to the output signal of the lock-in, while the gate was connected to the input signal.

A multi-frequency analysis was performed using a *Zurich Instruments MFLI* Lock-in Amplifier, controlled by a dedicated software. The device is able to provide AC

signals of known frequency (ν) and root-mean-square amplitude (V_{RMS}), up to 5 MHz with a maximum DC offset of ± 10 V. The characterization was performed over different frequencies below the cutoff frequency of the TFT. The lock-in was connected to one TFT in the sample by a *NEXTRON* micro-probe station, using three spring-fixed probes. The micro-probe station allowed to place the setup inside the shielded bunker with the sample under radiation and to perform the C-V measurements right before and after x-ray exposure. For every fixed frequency, the offset voltage applied to the gate was swept in the range $V_G \in [-5, +5]$V, where the switch on/off of the transistor occurs. To obtain the actual offset applied to the gate it was necessary to reverse the sign of the applied voltage, as the signal was erroneously applied to the source-drain electrodes instead of the gate. The measured parameter was the root-mean-square of the output current (I_{RMS}). The frequency range was limited for low frequency by the added noise to the measurement, while for high frequency the measurements are less noisy but the capacitive contribution to the impedance decreases. To verify that the measured impedance is due to a capacitance, it was sufficient to check if the phase of the response to the AC signal was close to 90°. Multiple measurements were performed changing at the frequencies $\nu = 7$ kHz, 10 kHz, 30 kHz, 70 kHz, 100 kHz, 300 kHz and 700 kHz. The measured capacitance is not sensitive to the frequency if the aforementioned constraints are followed, therefore in the analysis only $\nu = 300$ kHz will be shown for a better visual comparison between the measurements taken before and after irradiation.

From the measured values, the modulus of the impedance Z can be extracted as

$$Z(V_G) = \frac{V_{RMS}}{I_{RMS}(V_G)}. \tag{3.6}$$

At high enough frequencies the parasitic resistance of the setup can be ignored, leaving the TFT capacitance as the only contribution to impedance $Z = (2\pi\nu C)^{-1}$

$$C(V_G) = \frac{1}{2\pi\nu Z(V_G)} = \frac{I_{RMS}(V_G)}{2\pi\nu V_{RMS}}. \tag{3.7}$$

Chapter 4

Results and discussion

The devices were inspected with an optical microscope and by atomic force microscopy to assess the fabrication procedure.

The direct current electrical characterization of the devices was performed at CENIMAT facilities after the fabrication of each batch. The transport properties were assessed by measuring the transfer characteristics of the devices; moreover, the electrical stability was assessed with positive gate bias stress test. From the transfer characteristic measurements, it was also possible to assess the number of working TFTs inside each sample. The gate dielectric composition of the batches was chosen looking at the results obtained from the previously fabricated ones. The first fabricated batch was the mono-layer dielectric *T*, then the bi-layer *TA*, and finally the two tri-layers *TAT1* and *TAT2*.

The measurements under x-ray irradiation were performed at University of Bologna facilities, after the fabrication of all the samples.

4.1 Optical and AFM inspection

The transistors were inspected with an optical microscope. The inspection was performed for every layer to check the success of the deposition and pattering processes. Then, the physical dimensions of the channel were checked using a dedicated software. Figure 4.1 shows the picture of one TFT obtained with a 50x magnifying lens.

Further analysis was preformed using Atomic Force Microscopy (AFM). The instrument used was a *Park NX10* AFM available at University of Bologna and the scan was performed in non-contact mode. Figure 4.2 shows a scan of the channel area of one of the TFTs in the ROXFET sample.

Both from the optical inspection and from the AFM scan, the channel dimensions were measured to be $W = 320$ µm and $L = 18$ µm. The discrepancy between the mask channel length and the real TFT one was attributed to the optical lithography process. As all samples resulted having the same channel length, no additional concern was paid

to it, and in the analysis the measured L was used instead of the mask one.

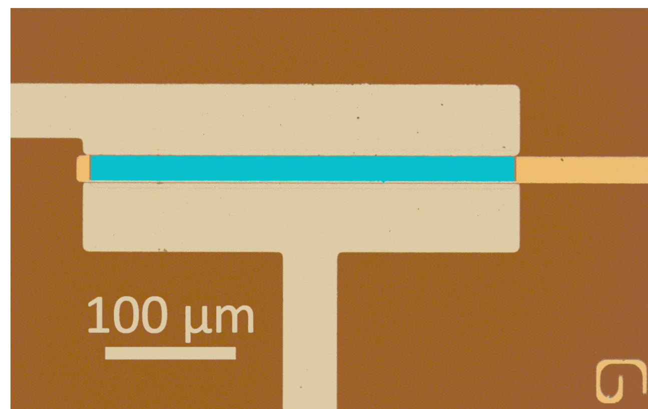


Figure 4.1: Optical picture of one TFT.

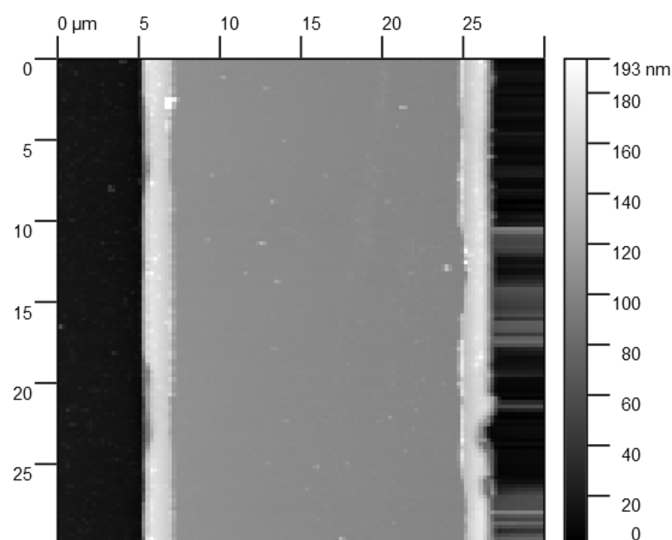


Figure 4.2: Scan of the x-y plane using the AFM in non-contact mode. The gray scale corresponds to the height. The central area corresponds to the channel of the TFT. Some artifacts in the horizontal direction are present on the right hand side of the picture, linked to the scanning direction of the AFM tip.

4.2 Electrical characterization

The I-V transfer characteristic was measured for all the transistors in every sample. From the transfer characteristics it was possible to distinguish the TFTs which exhibited

a transistor-like behavior. The fabrication procedure was considered successful, as the majority of the 9 TFTs present on each sample showed a transistor-like behavior, except for sample *TAT1 (300)* with only 4 working transistors (Table 4.1). On average, excluding the outlier *TAT1 (300)*, 87.3% of TFTs present in each sample worked correctly. This yield is much higher than the one obtained for previous samples fabricated with ALD gate dielectrics [11]. It was therefore demonstrated that it is possible to obtain a reproducible fabrication procedure for ROXFETs made with ALD gate dielectric layer.

Sample ID	n° working TFTs	Sample ID	n° working TFTs
T (180)	8	*TAT1 (180)*	8
T (300)	9	*TAT1 (300)*	4
TA (180)	6	*TAT2 (180)*	8
TA (300)	9	*TAT2 (300)*	7

Table 4.1: Number of working transistors in each sample containing a total of 9 TFTs.

During the stabilization procedure, it was observed that not all the samples had transistors able to stabilize. Regarding the samples annealed at 180°C, only *T (180)* had a stable behavior during the initial three transfers, while for all the other ones the threshold voltage shifted towards positive values and did not stabilize. On the other hand, all the samples annealed at 300°C were stable during the stabilization procedure, except for sample *TA (300)*. Figure 4.3 shows the stabilization procedure performed on batch *TAT2*, as a representative example of a non-stable device (*TAT2 (180)*) and a stable one (*TAT2 (300)*).

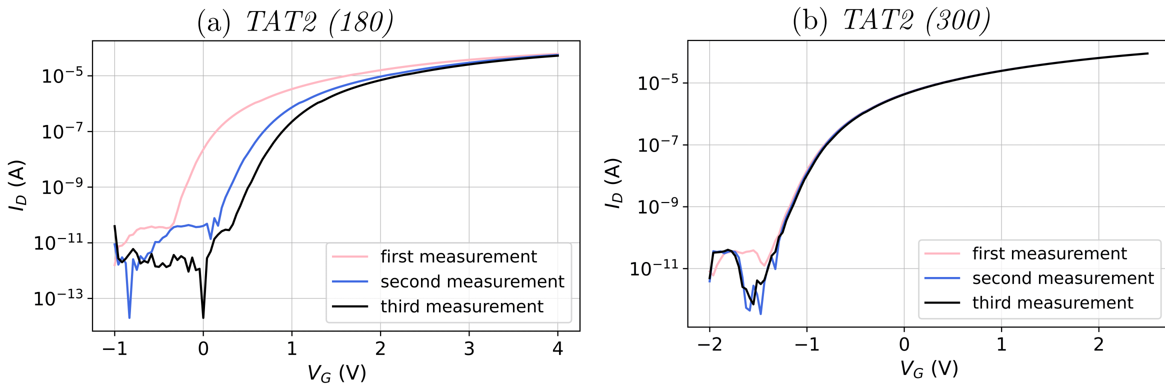


Figure 4.3: The three consecutive measurements performed during the stabilization procedure on one TFT in batch *TAT2* annealed at (a) 180°C and (b) 300°C.

Figure 4.4 shows the transfer characteristics of linear regime in logarithmic scale, while Figure 4.5 shows the $\sqrt{I_D} - V_G$ plot in saturation regime of all the samples with molybdenum top contacts.

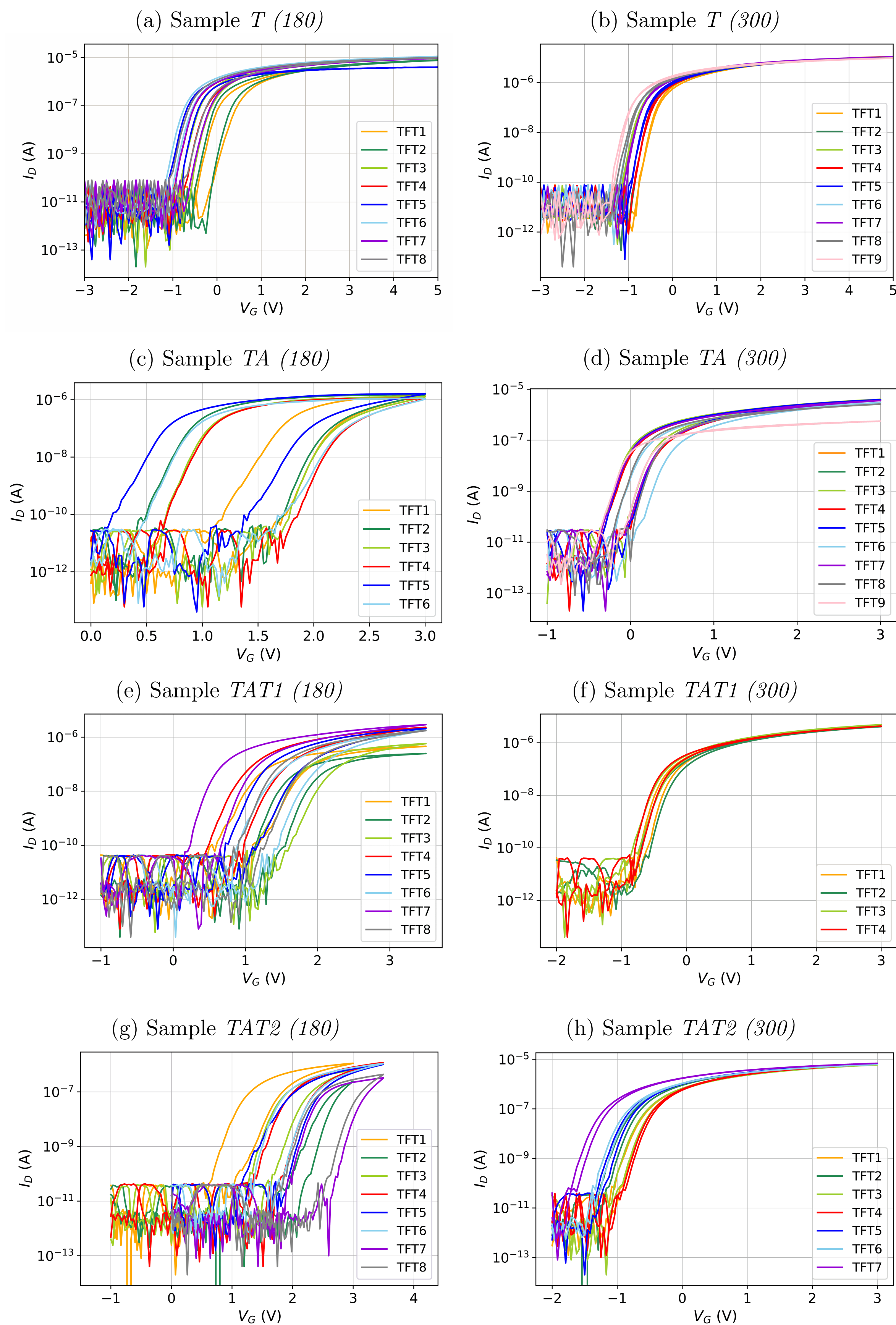


Figure 4.4: Transfer characteristics of linear regime ($V_D = 0.1$ V) in logarithmic scale.

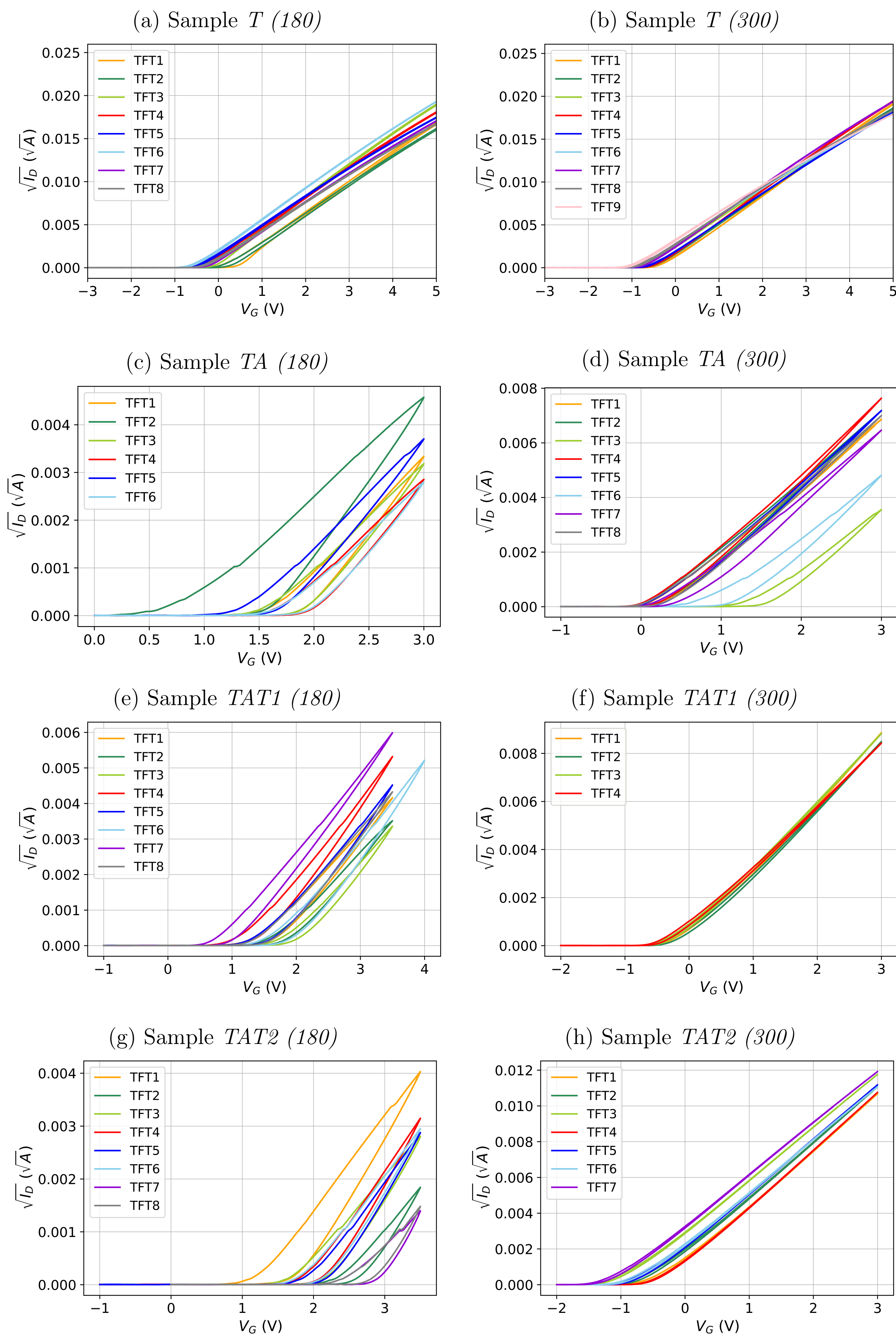


Figure 4.5: $\sqrt{I_D} - V_G$ plot in saturation regime ($V_D = 7$ V).

In batch *TA*, it was observed that the devices hysteresis depended strongly on the applied gate voltage range. Indeed, the hysteresis value doubled if the maximum applied gate voltage was increased from $V_G = 3$ V to $V_G = 5$ V. This could be linked to stress-related degradation of the Al_2O_3−IGZO interface. As a comparison, in batch *T* the maximum applied gate voltage could be extended up to $V_G = 8$ V, without any significant increase in hysteresis. To avoid unwanted stress effects during the measurement procedure, the measurement range was kept as small as possible.

For the samples with Mo source and drain contacts, the transport parameters extracted from the transfer characteristics are reported in Table 4.2 for the samples annealed at 180°C, and in Table 4.3 for the ones annealed at 300°C. The errors connected to the average values account for the dispersion of values of all the working transistors of each sample.

The dielectric capacitance per unit area necessary to calculate the mobility was obtained through the measurement of the eight MIM test structures present on each batch. For batch *T* the measured capacitance of the dielectric layer was $c = (203 \pm 12)$ nF/cm^2, coherent with the value expected for Ta_2O_5. For the multi-layer dielectrics, batch *TA* had $c = (162 \pm 17)$ nF/cm^2, while for *TAT1*, and *TAT2* the average capacitance per unit area was measured to be $c = (154 \pm 10)$ nF/cm^2.

Sample ID	μ_{sat} (cm^2/Vs)	V_{th} (V)	S (V/decades)	I_{on}/I_{off} (decades)	Hysteresis (V)
T (180)	7.8±1.9	-0.68±0.12	0.12±0.03	4.4±0.5	0.35±0.14
TA (180)	7.2±1.4	1.3±0.5	0.099±0.014	4.5±1.6	1.0±0.3
TAT1 (180)	6.3±1.2	1.1±0.3	0.14±0.06	4.6±1.4	0.43±0.14
TAT2 (180)	7.2±0.8	1.7±0.4	0.11±0.05	4.4±1.9	0.51±0.19

Table 4.2: Average parameters calculated over all the working transistors for the samples annealed at 180°C

Sample ID	μ_{sat} (cm^2/Vs)	V_{th} (V)	S (mV/decades)	I_{on}/I_{off} (decades)	Hysteresis (V)
T (300)	7.1±0.8	-0.72±0.16	0.10±0.02	4.6±0.5	0.01±0.04
TA (300)	6.8±1.3	0.2±0.5	0.088±0.012	4.9±1.7	0.23±0.06
TAT1 (300)	6.6±0.8	-0.70±0.04	0.11±0.02	5.2±1.2	0.08±0.07
TAT2 (300)	7.8±0.9	-1.3±0.2	0.11±0.03	5.1±1.3	0.08±0.06

Table 4.3: Average parameters calculated over all the working transistors for the samples annealed at 300°C

The samples show good mobility for amorphous structures, only slightly lower than typical values obtained for high-mobility AOS (~ 10 cm^2/Vs). The saturation mobility

is similar for all the samples and does not show a clear pattern between the samples annealed at 180°C and the ones annealed at 300°C.

The threshold voltage value is small enough to allow low voltage operations of the transistors. For the higher annealing temperature, the threshold voltage shifts towards more negative values, resulting in an absolute value decrease for all the batches except of batch *T*.

The subthreshold value is very small, as expected for AOS TFTs, and it decreases with increasing annealing temperature. The values of the interfacial trap density calculated with Eq. 1.4 are reported in Table 4.4. Batch *TA* is the only batch in which the dielectric-semiconductor interface is between Al_2O_3-IGZO instead of Ta_2O_5-IGZO, and it is the configuration with lowest N_t.

Batch ID	N_t (traps/cm^2)	Batch ID	N_t (traps/cm^2)
T (180)	$(1.3 \pm 0.4) \times 10^{12}$	*T (300)*	$(9 \pm 1) \times 10^{11}$
TA (180)	$(6.7 \pm 0.9) \times 10^{11}$	*TA (300)*	$(4.8 \pm 0.8) \times 10^{11}$
TAT1 (180)	$(1.30 \pm 0.6) \times 10^{12}$	*TAT1 (300)*	$(8.2 \pm 0.9) \times 10^{11}$
TAT2 (180)	$(8 \pm 1) \times 10^{11}$	*TAT2 (300)*	$(8.2 \pm 0.9) \times 10^{11}$

Table 4.4: Trap density at the dielectric-semiconductor interface in each sample extracted from the subthreshold swing value.

The samples annealed at 300°C have also higher on/off ratio. Therefore, it was demonstrated that the transport properties of the samples annealed at 300°C are superior with respect to the samples annealed at 180°C.

Moreover, the annealing at 300°C significantly reduced the hysteresis of the transfer characteristics with respect to the lower annealing temperature. At the same time, also the dispersion of the curves is improved, showing that higher temperature annealing not only improves the transport properties, but it also helps the homogeneity of TFT characteristics inside the same sample.

It is noticeable that batch *TA* has much higher hysteresis values compared to the samples form the other batches with same annealing temperature. Batch *TA* is the only structure with Al_2O_3, instead of the Ta_2O_5, in contact with the semiconductor layer. This result suggests that the Al_2O_3-IGZO interface could play a role in increasing the electrical instability of the transistors when a bias is applied to the gate.

The leakage current is the current flowing across the dielectric layer to the gate I_G. During the measurement of the transfer characteristics, I_G was acquired too. As expected, batch *T*, whose dielectric is made of a single layer of Ta_2O_5, has an extremely high leakage current for negative V_G. Figure 4.6 shows the transfer characteristic in saturation regime of one device in sample *T (300)*, plotted in logarithmic scale to show the leakage current, which is almost of the order of $I_G = 10^{-8}$ A for $V_G \sim -7.5$ V. On the other hand, in all the batches with Al_2O_3 in the gate dielectric, the leakage current

never exceeds 10^{-10} A.

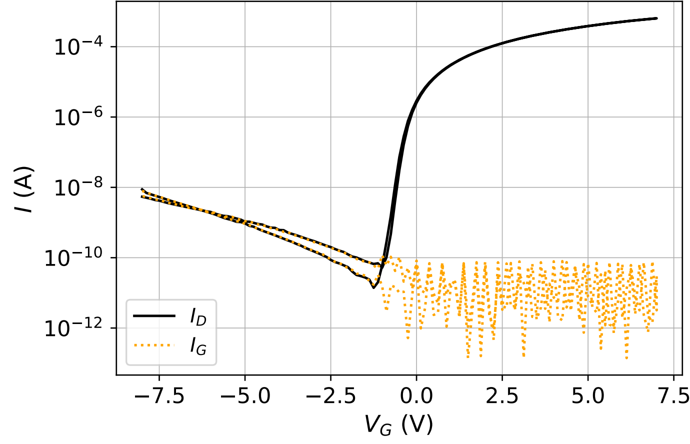
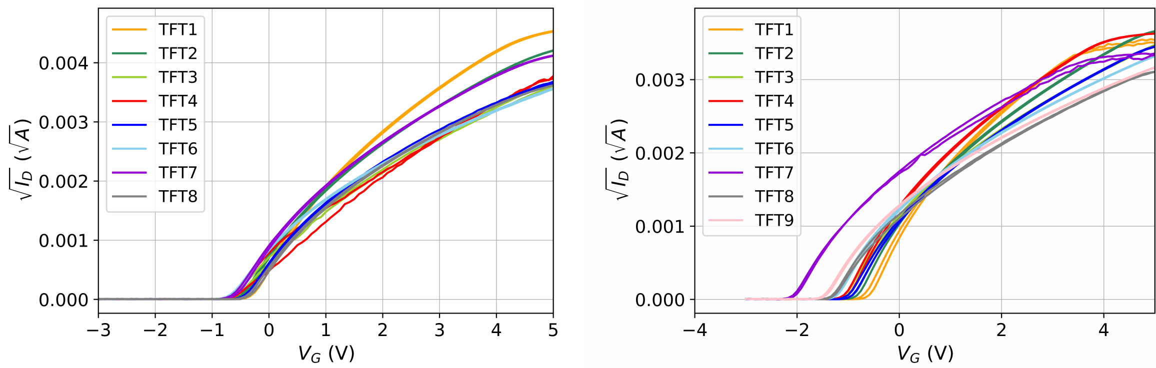


Figure 4.6: Transfer characteristic in linear regime of one device in sample *T (300)*, showing the drain current I_D and the gate leakage current I_G.

The samples with IZO source and drain contacts had strongly non-linear *I-V* characteristics in the linear regime for high V_G, which was attributed to high source-drain contact resistance. In saturation regime the contribution of contact resistance should decrease, however the $\sqrt{I_D} - V_G$ plot maintained a non-linear behavior as shown in Figure 4.7.



(a) Sample having the same structure as sample *T (180)*, but with IZO top contacts.

(b) Sample having the same structure as sample *T (300)*, but with IZO top contacts.

Figure 4.7: $\sqrt{I_D} - V_G$ plot in saturation regime ($V_D = 7$ V) of the samples having the same structure as batch *T* but with IZO top contacts.

From the linear regression in the linear part of the $\sqrt{I_D} - V_G$ curve, the extracted

transport parameters are compatible with the samples with molybdenum top contacts, except for the saturation mobility, which is lower, e.g. for sample *T (180)* $\mu_{sat} = (1.1 \pm 0.4)\text{cm}^2/\text{Vs}$, and for *T (300)* $\mu_{sat} = (1.2 \pm 0.3)\text{cm}^2/\text{Vs}$. The resistivity ($\rho$) of the source and drain layer was measured with the dedicated test structures, giving as a result $\rho_{IZO} = (2.4 \pm 0.4)\text{m}\Omega\text{-cm}$ for the IZO contacts, compared to $\rho_{Mo} = (78 \pm 2)\mu\Omega\text{-cm}$ for the Mo contacts. It was concluded that the devices with IZO top contacts had very high contact resistance and no significant benefit in the transport properties. Therefore, all the subsequent analysis was performed only on the samples with Mo source and drain.

4.3 Stability properties

Positive gate bias stress

The PGBS test was performed on all the samples annealed at 300°C, as they proved to be the most stable ones during the stabilization procedure and with smallest hysteresis. Figure 4.8 shows the normalized threshold voltage shift ΔV_{th} of all the samples annealed at 300°C.

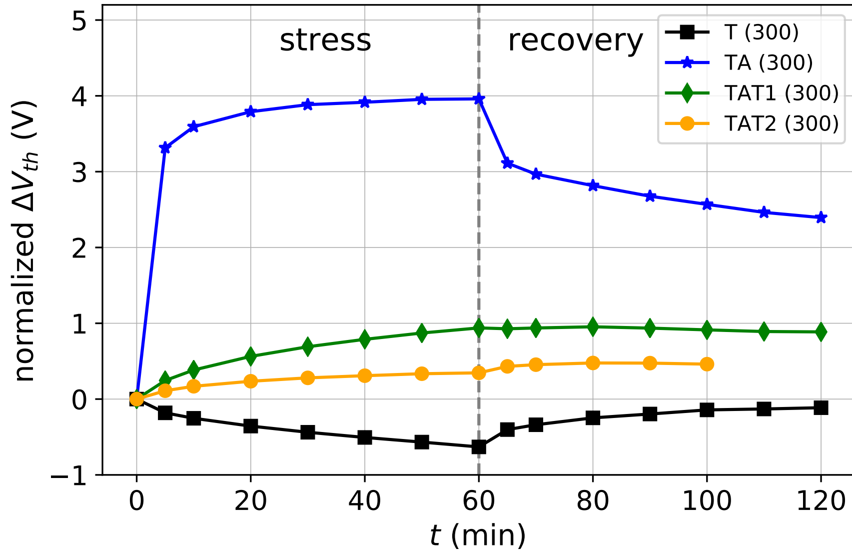


Figure 4.8: Normalized threshold voltage shift as a function of time during the stress and recovery periods.

All the tested devices show a relatively big threshold voltage shift. The instability due to bias stress was observed in literature, and it was attributed to the charge trapping in high-k dielectrics in IGZO-based TFTs [42].

Sample *T (300)* has an anomalous threshold voltage shift. The physical reason behind it is not clear and it would require further analysis. In sample *TA (300)*, the threshold voltage rapidly approaches the value of the applied bias V_{bias}, which is an asymptote for V_{th}. This measurement is in agreement with the large hysteresis of batch *TA*, which confirms the electrical instability of the Al_2O_3-IGZO interface. The two samples with the tri-layer gate dielectric (*TAT1 (300)* and *TAT2 (300)*) show a normal ΔV_{th} towards positive values. The entity of the shift is smaller in the sample with a thicker Ta_2O_5 between Al_2O_3 and IGZO (*TAT2 (300)*). This can be linked again to the role of Ta_2O_5 in stabilizing the electric properties of the dielectric-semiconductor interface. In samples *T (300)* and *TA (300)* the fast recovery at room temperature indicates that the threshold voltage shift should be attributed to charge trapping at the semiconductor/dielectric interface rather than charge injection in the dielectric bulk [32]. Samples *TAT1 (300)* and *TAT2 (300)* have anomalous recovery, indicating possible complex mechanisms happening among the three dielectric layers.

Afterwards, the PGBS was performed also on the samples annealed at 180°C of batches *T*, *TAT1* and *TAT2* as they proved to be the ones more stable electrically. Table 4.5 summarizes the results obtained by fitting ΔV_{th} over time during the stress period with Eq. 3.1.

Sample ID	τ (min)	γ
T (180)	11.8±1.3	0.82±0.09
TAT1 (180)	0.47±0.08	0.34±0.02
TAT2 (180)	0.75±0.15	0.35±0.03

Sample ID	τ (min)	γ
T (300)	17.6±0.5	0.9±0.04
TA (300)	1.26±0.11	0.431±0.019
TAT1 (300)	17.5±0.9	0.98±0.08
TAT2 (300)	14.8±0.7	0.91±0.06

Table 4.5: Parameters extracted from the fit of the threshold voltage shift over time during one hour of stress with $V_{bias} = 3$V.

Time stability

Before the radiation sensitivity measurements, the samples were stabilized overnight in the dark, with the electrodes connected to ground. All the devices exhibited a threshold voltage shift towards positive values. The entity of the shift can be evaluated as $\Delta V_{th}/\Delta t$ in the hour before the first irradiation, and the values are summarized in Table 4.6.

For batches *T* and *TA* the smaller threshold voltage shift is present in devices with lower temperature annealing, while for batches *TATA* and *TAT2* the opposite happens. However, it is important to compare the threshold voltage drift with the sensitivity of the device, which is given by the negative V_{th} shift for a given dose. Indeed, devices with large sensitivity will be less affected by a certain positive V_{th} drift than devices with a low sensitivity, because the V_{th} shift due to the drift is proportionally smaller.

Sample ID	$\Delta V_{th}/\Delta t$ (mV/min)	Sample ID	$\Delta V_{th}/\Delta t$ (mV/min)
T (180)	0.10±0.07	*T (300)*	0.58±0.11
TA (180)	0.30±0.02	*TA (300)*	0.70±0.06
TAT1 (180)	3.4±0.3	*TAT1 (300)*	0.15±0.03
TAT2 (180)	4.09±0.2	*TAT2 (300)*	0.15±0.02

Table 4.6: Threshold voltage shift per minute during the hour preceding the first irradiation.

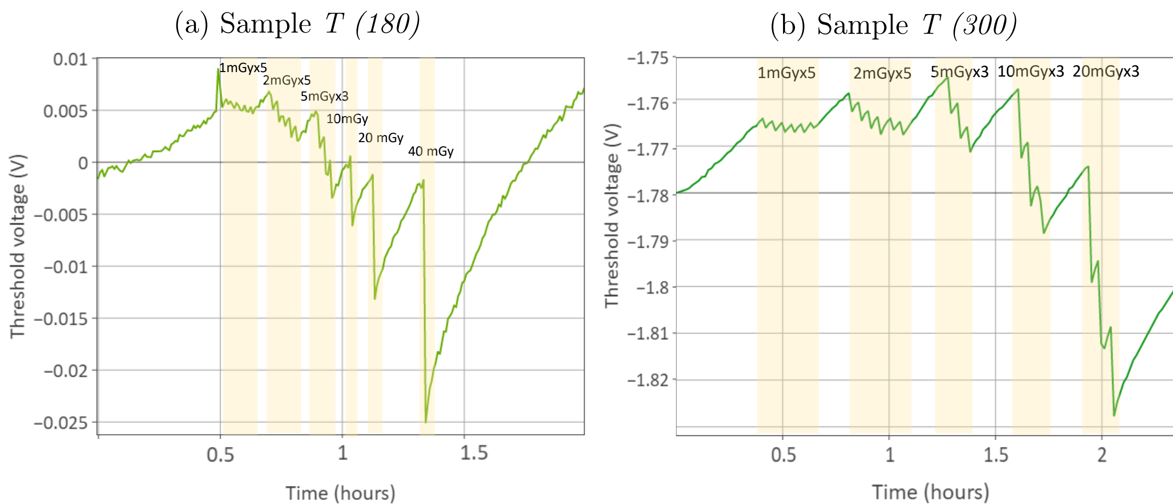
At least 13 hours were needed to approach a stable value, and not even one of the sample was completely stable when the irradiation started. Unfortunately, it was possible to calculate the threshold voltage over time only after the complete acquisition had finished, therefore it was difficult to assess if the device was stable while performing the measurement.

The positive threshold voltage shift could have affected the sensitivity measurements, where the voltage shifts in the opposite direction. However, due to the fast response of the ROXFET devices and their comparatively slow recovery, it is reasonable to assume that the results were not compromised by this.

4.4 X-ray sensitivity

The shift in threshold voltage due to radiation exposure was measured. For the lower tested doses, multiple irradiations were performed in order to have a significant statistic.

The graphs showing the threshold voltage as a function of time are shown in Figure 4.9. For the sake of clarity, only one representative device per sample is shown. However, all the following analysis is performed on the average of all the working transistors.



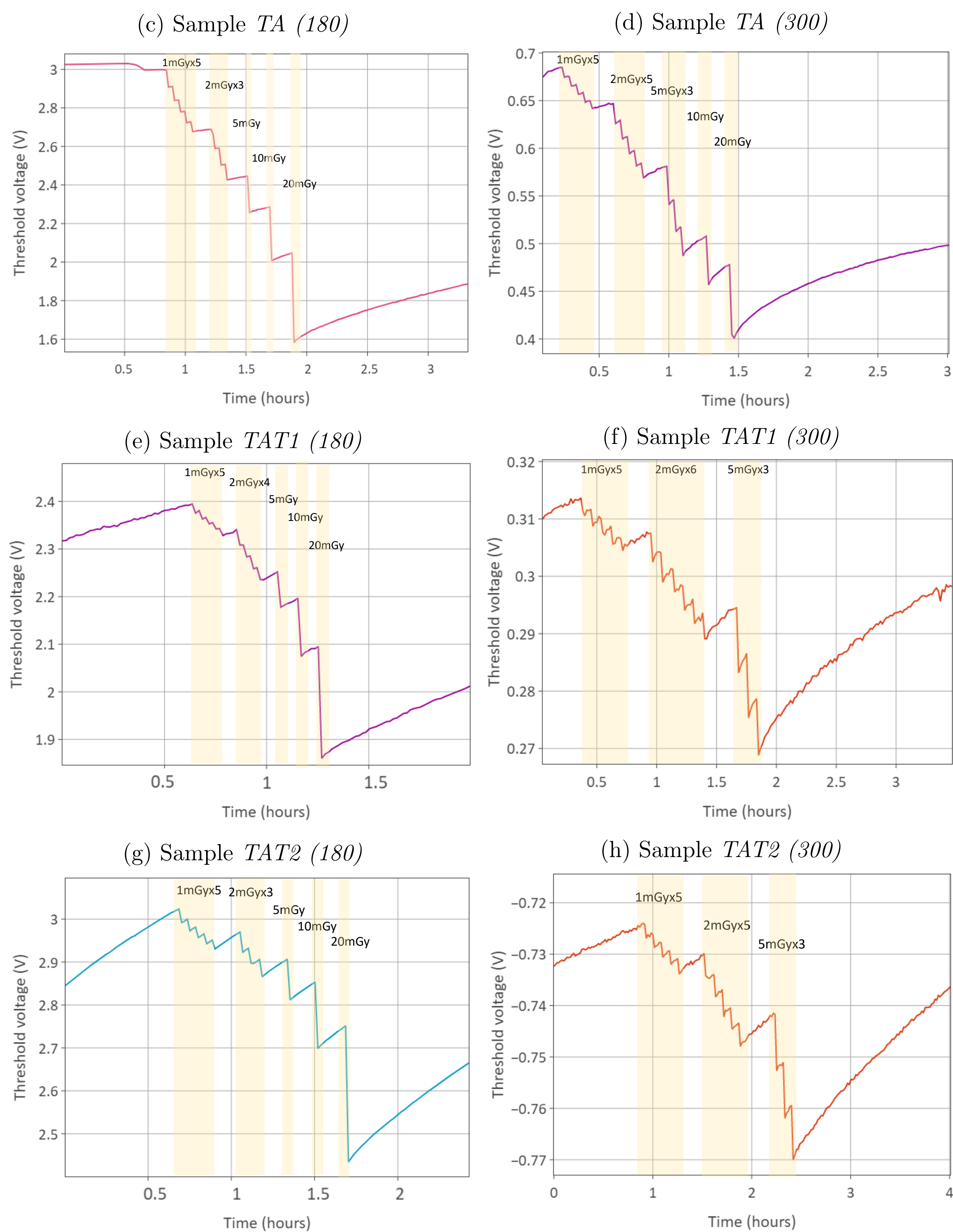


Figure 4.9: Plots of the threshold voltage during irradiation as a function of time. The areas shaded in light yellow represent groups of different number of irradiation of the same dose, separated from each other by 3 minutes recovery.

The average sensitivity is reported in Table 4.7. The reported value is given by the average of all irradiations performed at the smallest detected dose (1 mGy or 2 mGy). This was done in order to compare the devices response at their best conditions, avoiding effects such as the lowering of sensitivity with increasing cumulative dose, due to saturation of the detectors at high doses. This phenomenon will be described in the following section in detail.

Sample ID	Sensitivity (V/Gy)	Sample ID	Sensitivity (V/Gy)
T (180)	0.66±0.17	*T (300)*	1.54±0.4
TA (180)	65±3	*TA (300)*	10±2
TAT1 (180)	16±2	*TAT1 (300)*	2.6±0.3
TAT2 (180)	22±5	*TAT2 (300)*	2.7±0.3

Table 4.7: Average sensitivity at the minimum measured dose. The average is performed for each transistor over all the 5 irradiations at the minimum dose, and then over all the working transistors (variable number) in each sample. For all the samples the minimum detected dose was 1 mGy, except for Batch *T (180)*, where only one transistor was sensitive to 1 mGy, thus the average was performed on the 2 mGy irradiations.

When comparing samples from the same batch (i.e. with the same dielectric structure), the samples annealed at 180°C are always more sensitive than the samples annealed at 300°C. Looking at samples with the same annealing, the sensitivity increases significantly in the structures with the Al_2O_3−IGZO interface (batch *TA*), compared to the Ta_2O_5−IGZO interface (batches *T*, *TAT1* and *TAT2*). This can be explained looking at the physical properties of the two dielectrics. Ta_2O_5 has a high radiation stopping power, which results in a high electron-hole pair generation. However, the holes which accumulate at the dielectric close to the semiconductor interface are rapidly passivated by the electrons present in the semiconductor channel due to the low bandgap of Ta_2O_5. On the other hand, when the Ta_2O_5 is separated from the semiconductor by a Al_2O_3 layer, the positive charges accumulated in the dielectric are not neutralized by the channel electrons, as the Al_2O_3 has a larger bandgap, which blocks the passage of electrons. This assumption is demonstrated in batches *TAT1* and *TAT2*. Indeed, when the Al_2O_3 is below the Ta_2O_5 layer, the sensitivity decreases with respect to batch *TA* as the electrons are able to enter the 10 nm or 20 nm of Ta_2O_5. This result also supports the model which states that the positive charge accumulation in the dielectric happens close to the semiconductor interface.

Sensitivity saturation

An ideal detector would present a linear response over the full range of interest, it is thus important to evaluate the effect of the total cumulative dose received. The sensitivity of the devices decreases with increasing irradiated dose, as the cumulative

threshold voltage shift does not follow a linear trend. To reduce this effect, the different irradiations were separated by a few minutes (3 minutes between irradiations with the same dose and approximately 10 minutes for irradiations with different doses), to favor the independence of consecutive readings. The small recovery was not sufficient to grant sensitivity independent from the cumulative dose. Figure 4.10 shows the behavior of the cumulative threshold voltage shift as a function of the cumulative irradiated dose of all the previous irradiations. It is possible to see that the behavior deviates from the ideal linear trend.

Both samples in batch *TA* have trends which deviate completely from linearity. On the other hand, in the other batches the cumulative ΔV_{th} deflects, but remains compatible with a linear trend.

The tests are performed reaching different total cumulative doses, as the values are taken from the sensitivity measurements, and the irradiation performed varied according to the sample needs in terms of detection. Indeed, in the less sensible samples higher doses were used to assure a readable signal.

Recovery

The recovery of the samples after irradiation was monitored for approximately 2 hours. Table 4.8 reports the recovery parameters obtained by fitting the data with 3.2.

Sample ID	τ (min)	γ	Sample ID	τ (min)	γ
T (180)	39±2	1.31±0.07	*T (300)*	11.5±0.4	1.77±0.06
TA (180)	42±9	1.29±0.19	*TA (300)*	152±12	0.77±0.07
TAT1 (180)	27.9±0.6	1.9±0.8	*TAT1 (300)*	64±4	1.15±0.05
TAT2 (180)	40.2±1.3	1.8±0.6	*TAT2 (300)*	92.3±1.2	1.5±0.6

Table 4.8: Recovery parameters extracted after the irradiations, where τ is the recovery time constant and γ is the exponential factor.

The recovery time constant is not clearly linked neither with the sensitivity nor with the device structure. Its value is generally of the same order of magnitude of the one previously reported for ROXFETs [10], except for sample *TA (300)* which shows one order of magnitude increase.

It is interesting to compare recovery time constant of with the time constant calculated for the PGBS. Sample *TA (300)*, which is the most unstable among the samples annealed at 300°C in the PGBS, is the one showing the largest recovery time constant. Similarly, sample *TA (180)* is the sample with the highest recovery time constant among the samples annealed at 180°C. The observation highlights that the *TA* structure is unstable under electrical stress, but not when when the stress is minimal as during the fast pulsed *I-V* measurements performed to extract the x-ray sensitivity.

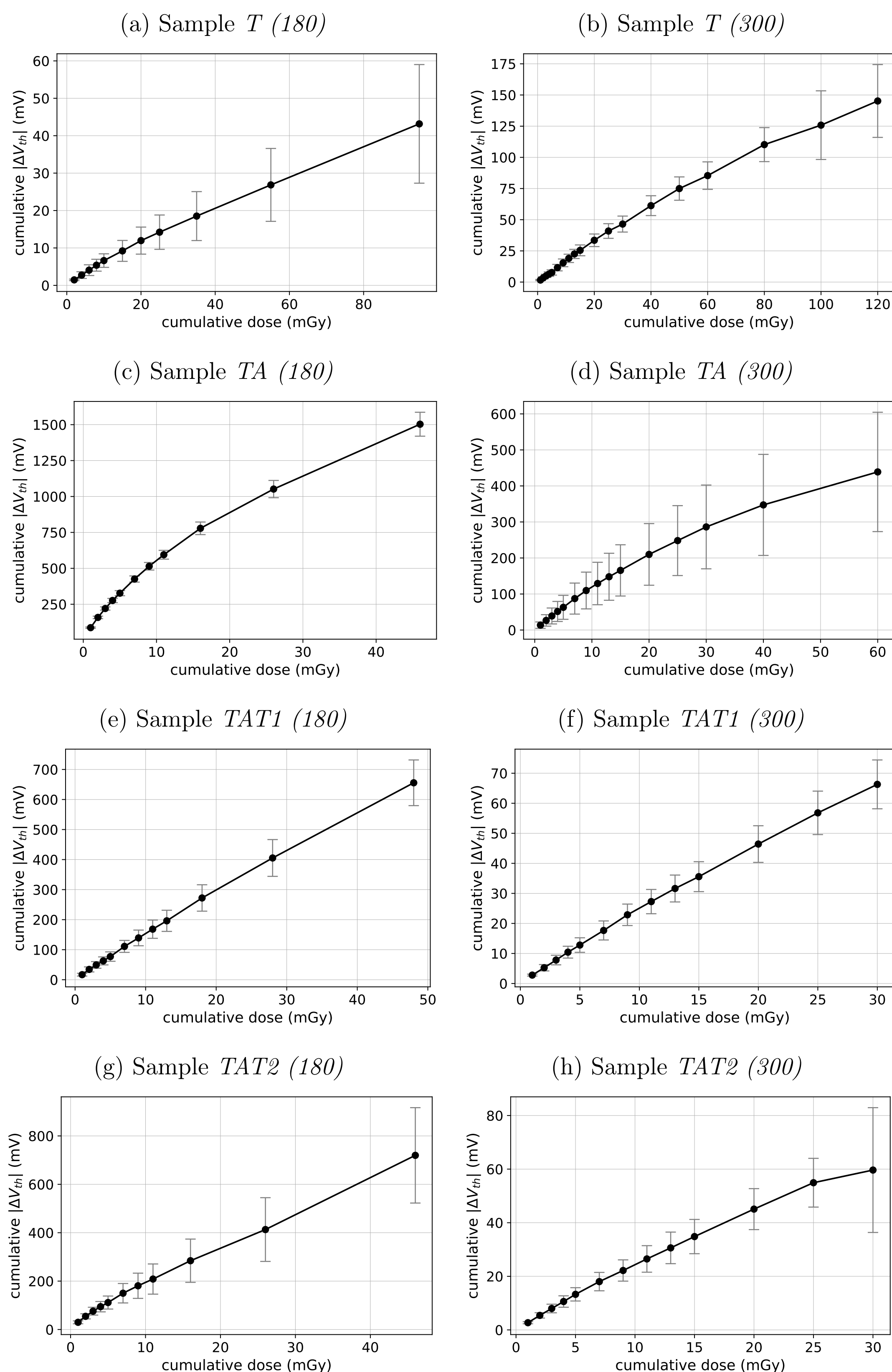


Figure 4.10: Cumulative absolute value of the threshold shift due to irradiation as a function of the cumulative dose received. The values are the average calculated among all the working transistors in each sample and the error bars indicate the dispersion of values of the transistors.

4.5 C-V measurements for sub-bandgap DOS extraction

Capacitance-voltage measurements were performed before and after the irradiation of 400 mGy at 60 kVp on all the samples. Figure 4.11 shows the measured capacitance as a function of applied gate voltage acquired at $\nu = 300$ kHz.

The results observed by the *C-V* plots are coherent with the sensitivity previously measured. A shift of the channel onset towards lower gate voltages is expected in accordance with the negative shift of the threshold voltage observed upon irradiation. In batch *T*, the capacitance of neither batch is affected by the irradiation. Sample *T (300)* has an anomalous decrease of capacitance for higher V_G, which does not seem to be affected by radiation exposure. In batch *TA* both samples show a shift towards lower gate voltages, and the appearance of humps after irradiation. For the tri-layer dielectric batches *TAT1* and *TAT2*, the negative shift is observed for the samples annealed at 180°C and not for the ones annealed at 300°C. This is coherent with the remarkably higher sensitivities of the batches with annealing at lower temperatures.

The semiconductor DOS was calculated for the acquired *C-V* measurements according to Eq. 3.4 and 3.5. Figure 4.12 shows the density of states before and after irradiation acquired at $\nu = 300$ kHz.

Batch *T* does not show any relevant change in the DOS upon irradiation. The result is not surprising, as the sensitivity of this structure is extremely low. In batch *TA*, it is noticeable that the DOS shifts towards lower energies after irradiation, which is coherent with the expected behavior. In sample *T (300)* the DOS at higher energies has an anomalous shape as the model does not account for the decrease of capacitance for higher V_G. The two tri-layer structures, batches *TAT1* and *TAT2*, have a similar behaviors. In the samples annealed at lower temperature (180°C), after the irradiation the DOS at high energies is slightly lower than before irradiation. On the other hand, the two samples annealed at 300°C do not have any significant change in the DOS when irradiated.

The irradiation does not cause any significant change in the shape of the density of states in any sample.

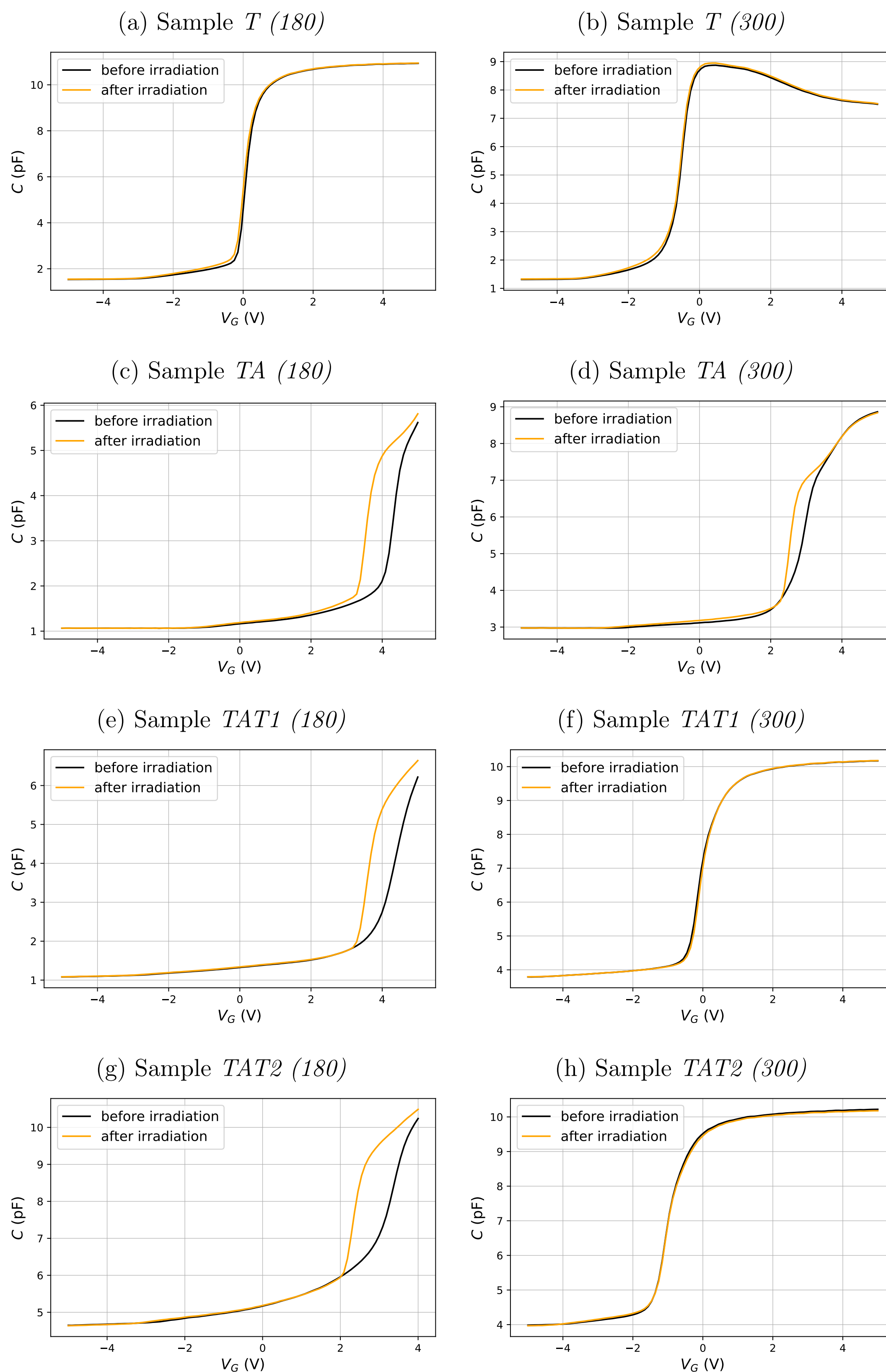


Figure 4.11: C-V measurement performed at 300 kHz before and after an irradiation of 400 mGy for the tested transistor in each sample.

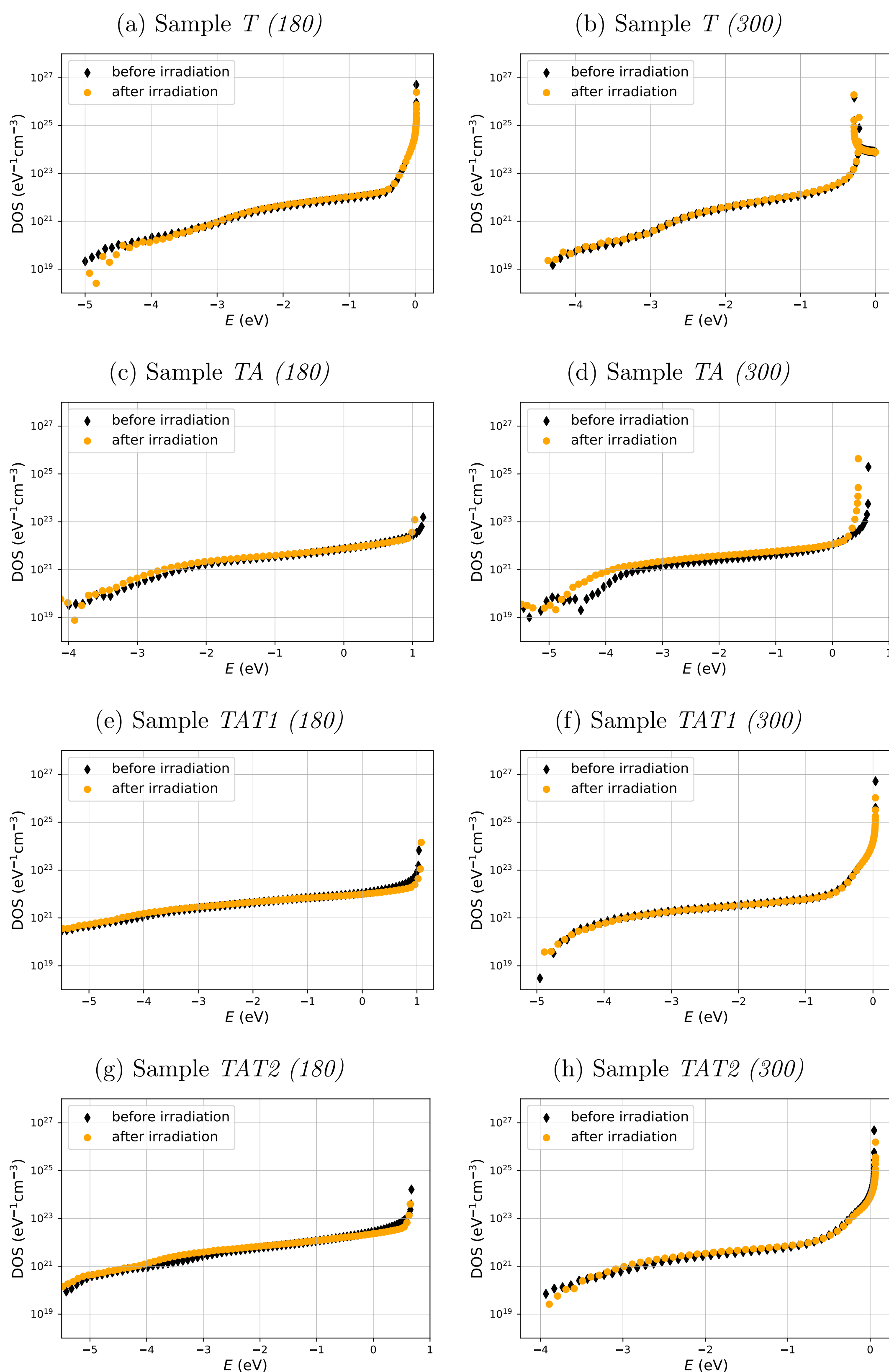


Figure 4.12: Semiconductor DOS as a function of energy extracted from the C-V measurement at 300 kHz before and after 400 mGy irradiation.

4.6 Future perspectives

Thanks to the promising results obtained in this thesis, it is worthy to further investigate ROXFET devices fabricated with ALD gate dielectric. In particular, due to its outstanding sensitivity compared to the other samples, the bi-layer dielectric structure of batch *TA* should be considered. From the electrical measurements it was seen that the Al_2O_3 interface with IGZO creates instability when the device is stressed electrically. A possible explanation lies in the hydroxyl (-OH) groups present on the Al_2O_3 terminating layer, as a result of the ALD deposition cycle. It would be suggestible to implement a surface treatment to reduce the hydroxyl groups concentration, to see if there is an improvement in the electrical stability. The ideal surface treatment will decrease the source of the electrical instability but will leave the sensitivity properties unaltered.

It is recommendable to investigate the effect of the deposition of a suitable passivation layer, which has been demonstrated to improve the stability by reducing the absorption and desorption of O_2 and H_2O molecules [36]. In addition to the passivation layer, a light-blocking layer is necessary to avoid light-induced threshold shift. The stability of the threshold voltage of devices with a suitable passivation and light-blocking layer should be assessed.

It was seen that the samples annealed at 180°C showed to be impressively more sensitive to ionizing radiation compared to the same structures annealed at 300°C. The low temperature annealing is compatible with fabrication on plastic substrates, which allows to go towards flexible detectors. Sample *TA (180)* should be replicated on a plastic substrate to determine how the properties of the device are affected by the substrate. Also, it will be important to perform an electrical comparison of the properties of the devices after a mechanical bending stress test.

Conclusions

In this thesis, ROXFET devices were fabricated and subsequently characterized. The fabrication was carried out changing different parameters in order to determine the best performing configuration. The main focus of the work was the impact of ALD gate dielectrics: four batches were fabricated with different stacks made of Ta_2O_5 and Al_2O_3 layers. For each batch with a given gate dielectric structure, two samples were compared to analyze the impact of two different annealing temperatures, 180°C and 300°C. The device performances were assessed through electrical and radiation response measurements.

It was possible to establish a standard fabrication procedure, which guarantees good reproducibility of the devices and a high ratio of working transistors inside each sample. Indeed, excluding an outlier sample, on average the 87.3% of the 9 TFTs present in each sample worked.

All the devices showed high mobility (in the range 6.3−7.8 cm^2/Vs) and low sub-threshold swing (<0.14 V/decades) compatible with typical values of AOS-based TFTs. The threshold voltage is small ($<|1.7|$ V), thus allowing low voltage operations.

It was shown that higher annealing temperature improves the sub-threshold swing, the on-off ratio, and significantly reduces the hysteresis in the transfer characteristics.

Higher annealing temperature increases the electrical stability of the devices. Indeed, the devices annealed at 300°C had bigger time constant under PGBS, compared to the respective structures annealed at 180°C. Furthermore, it was found that the dielectric stack in which the Al_2O_3 is in contact with the semiconducting IGZO has the largest instability when stressed electrically. Specifically, when comparing samples with the same thermal annealing at 300°C, batch *TA* was the one with the largest hysteresis in the transfer characteristics and smallest time constant in the PGBS tests.

Regarding x-ray sensitivity, it was seen that, for the same dielectric structure, the sensitivity increases when the annealing temperature is lower. Comparing the different dielectric structures with the same annealing temperature, it is clear that batch *TA* stands out for its higher sensitivity. It is possible to assume that when the Ta_2O_5 is in contact with the semiconductor, the channel electrons are able to easily neutralize the positive charges accumulated in the dielectric due to the low bandgap of Ta_2O_5. On the other hand, an Al_2O_3 layer effectively reduces the recombination of accumulated

free charges. The best performing sample, *TA (180)*, has the impressive sensitivity of (65 ± 3)V/Gy, increasing the previously reported value, (3.4 ± 0.2)V/Gy [10], of an order of magnitude.

Concerning the change in the semiconductor sub-bandgap DOS upon ionizing radiation, it was observed a shift of the DOS towards lower energies caused by irradiation in both samples of batch *TA*. In the other batches, the DOS energy does not shift. This is related to the higher sensitivity of the bi-layer structure of batch *TA*.

Thanks to the promising results obtained in this thesis, it is worthy to further investigate ROXFET devices fabricated with ALD gate dielectric. Future work should focus on improving the stability of the devices, using a passivation and light-blocking layer as well as suitable surface treatments to improve the dielectric-semiconductor interface properties.

To conclude, this thesis was successful in the establishment of a stable and reliable fabrication procedure for ROXFETs based on high-quality ALD gate dielectrics. The effect of gate dielectric composition and annealing temperature was studied by electrical measurements and irradiation tests.

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