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Progettazione e diagnostica dei sistemi isolanti elettrici

Assessment of partial discharge activity and conductivity in IGBT modules as a reliability index

Scariche parziali e conducibilità come indici di affidabilità per moduli IGBT

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Abstract

Al giorno d'oggi l'elettronica di potenza deve essere in grado di operare in ambienti ostili e in condizioni di lavoro difficili. Il tema dell'affidabilità è diventato fondamentale quanto quello dell'efficienza.
Questa tesi si focalizza sull'IGBT, in particolare sul suo sistema d'isolamento. Il primo passo è stato studiare in dettaglio i meccanismi di guasto possibili e più frequenti. Dal momento che le scariche parziali risultano essere un problema per l'affidabilità dei dielettrici solidi, in questo studio si esamina l'attività di PD su moduli IGBT nuovi ed invecchiati, in diverse configurazioni, con forme d'onda di tensione e temperature differenti. Si sono effettuate anche misure di corrente di dispersione su moduli nuovi ed invecchiati alla temperatura di lavoro. I risultati sono stati post-processati statisticamente tentando di ottenere indici di affidabilità per quei moduli. Quasi tutti i moduli invecchiati sono interessati da PD e i risultati mostrano che il PDIV, assieme ad altri fattori, è sicuramente influenzato dall'ageing. I risultati del monitoraggio della corrente di dispersione mostrano una tendenza all'aumento con l'invecchiamento. Si sono svolte anche simulazioni con software agli elementi finiti e rilevazioni ottiche di PD ed entrambe supportano i risultati ottenuti. È necessario effettuare ulteriori indagini su un data set più ampio al fine di migliorare un algoritmo di diagnostica predittiva basato sui valori di PDIV e conducibilità.

Abstract

Power electronic systems nowadays have to be able to operate in harsh environment and field conditions. The issue of reliability has become as fundamental as efficiency. This thesis focused on IGBT module, in particular on its insulation system. The first step was to study possible and most frequent failure modes. Since Partial Discharges are known to be a reliability issue for solid dielectrics, this study investigates PD activity under different waveforms and temperatures on new and aged IGBT modules in different configurations. Measurements of leakage current at working temperature were also carried-out in new and aged modules. Results were statistically postprocessed attempting to obtain reliability indexes for those modules.

Almost all of the aged modules were affected by PDs, and results show that PDIV is certainly affected by aging, together with other factors. Results from leakage current monitoring shows an increased trend with aging. FEM Software Simulation and optical PD measurements are also carried out and both support obtained results. Further investigations on a larger dataset have to be conducted in order to improve a life prediction algorithm based on PDIV and conductivity values.

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Introduction

Power semiconductor devices are the main components of power electronic systems, as well as one of their most critical parts in terms of reliability. IGBT modules are one of the most used semiconductor devices and nowadays they are replacing MOSFETs or BJTs in many applications.

Considering the increasing role of power electronic converters in critical applications, such as automotive, aerospace, transportation, and energy, significant safety requirements, features such as reliability, lifetime, health monitoring, and predictive maintenance become increasingly important. In addition, in this application context, they are required to work under harsh operational and environmental conditions for extended target lifetime that may reach 30 to 40 years in some applications.

According to field experience, power electronic converters are considered a weak link that has significant influence on overall electrical system reliability. In an industry-based survey ([1],[2]), semiconductor switches and capacitors are the most vulnerable components of the power converters. Unexpected overloads and system transients are main reasons for random failures, while thermal stresses followed by mechanical vibrations and humidity are the main causes for failures caused by long-term wear-out. The failure of these switches reduces the efficiency of the whole system and can lead to system failure.

Although IGBT and power converters manufacturers test their IGBT modules (according to IEC 60747-9 and IEC 60749 series of standards), when a converter arrives to the customer site for commissioning and operation, it might have much lower reliability than expected, because of mechanical or temperature shock events occurring during storage and transportation stage,

or incorrect handling and assembly of IGBT modules before site commissioning.

Moreover, another aspect to consider is that qualification tests carried out on IGBT modules at the manufacturer site may not be adherent and representative of the life and performance of the converter since the working environment of IGBTs, often harsh and hostile, is *a priori* unknown to the manufacturers. Overstress and wear-out may cause IGBT modules to reach end-of-life early before the product target lifetime. For safety-critical and mission-critical applications, redundancy may not be the best option; so there is a strong demand for further improvement of the reliability of IGBT modules, which represents a serious challenge to both power converter and IGBT modules manufacturers. That has led them to adopt a so-called design-for-reliability approach. This approach is meant to consider the knowledge of the field failures, failure mechanisms, and the expected operational conditions into design stage. Addressing long-term reliability and life predictions are key elements in the design-for-reliability approach. Accelerated life tests are typically used to study long-term reliability issues. In these tests, IGBT modules are subjected to stresses higher than typical field conditions to accelerate wear-out failure modes ([3], [4], [5], [6]).

Today the most difficult target for electronic devices manufacturers and users is to predict as accurately as possible the end of the useful life of a component, in order to act in advance by replacing or repairing it. The aim of this work is to do tests on IGBT modules, in particular on their electrical insulation, to find out measurable quantities to be taken as diagnostic markers. Therefore, they will be used to create new models or to refine existing ones in order to predict and prevent the failure of the single component, which could cause the machine to stop working or, even worse, the failure of other parts of the system.

In this case the measurements carried out are tests of electrical conductivity and resistance to partial discharges. The results were then statistically processed to find any correlations between values of a given quantity and ageing of the devices. Another activity, undertaken in parallel with measurements, was to carry out computer FEM simulations to corroborate obtained results and verify their trustworthiness.

IGBT

IGBT: working principles

Power IGBT is a semiconductor electronic component developed in the second half of the 1980s to combine the advantages of BJTs with those of MOSFETs. It is a mixed conduction device since it has the output characteristics of a BJT, i.e., low conduction losses (limited ON state resistance), and the input characteristics like those of power MOSFETs, with quite fast switching and a simple driver with low power dissipation. The equivalent circuit of an IGBT consists in fact of a Darlington connection with pnp BJT as output transistor, and a MOSFET as input transistor (Figure 1).

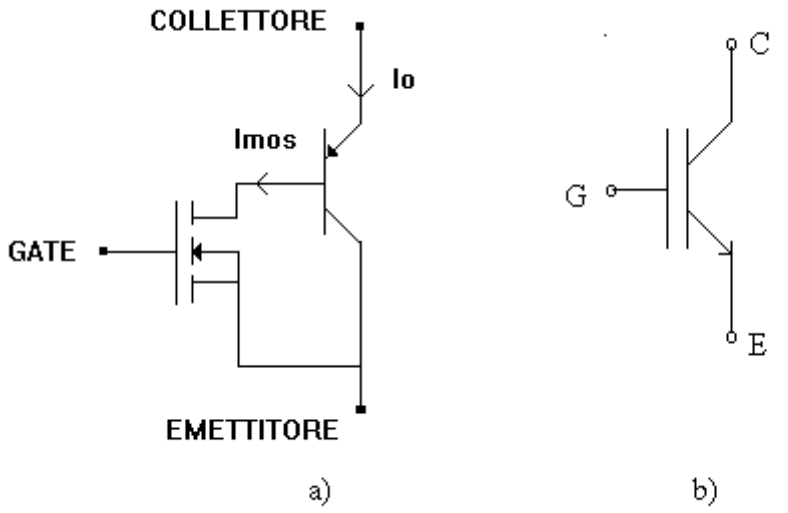


Figure 1. a) Equivalent circuit. b) Graphic symbol in circuit.

The structure of an IGBT is similar to that of a vertical diffusion power MOSFET (VDMOS), except for an additional p+ layer above the collector as seen in figure 2. The main characteristic of the vertical configuration is that the collector (drain) forms the bottom of the device while the emitter (source) region remains the same as a traditional MOSFET.

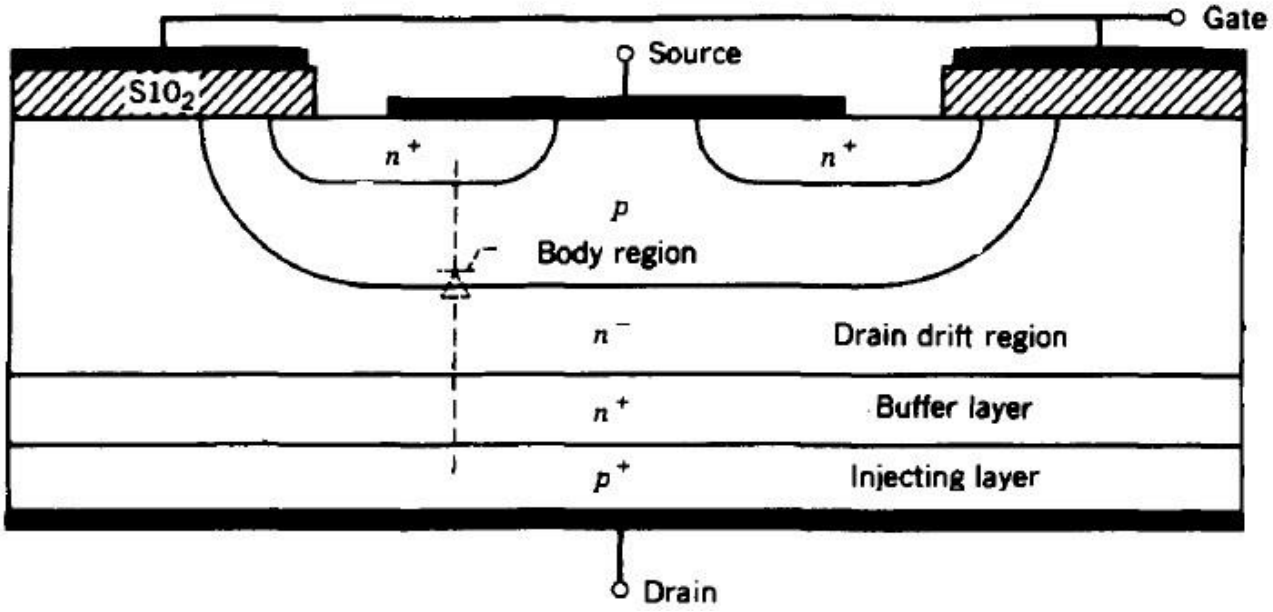


Figure 2. Typical internal cross-section of IGBT

The majority of carriers in this device are electrons. The additional p+ layer in the IGBT acts as a source of holes that are injected into the body (n- region) during operation. These holes enable quick tum-off by recombination with excess electrons that remain in the body of the IGBT after switch-off. Applying a positive voltage to the gate switches on the device when an inversion layer (i.e., a conductive channel) is created in the p- region just below the gate oxide allows for electron flow to take place. Electrons flow from the emitter through the conductive channel to the collector terminal. A positive voltage applied to the collector with the emitter at ground causes the injection of positive carriers from the p+ layer, which contacts the collector, into the body. This allows for conductivity modulation of the device, leading to a lower on-resistance compared to the power MOSFET. Since an IGBT is switched on by voltage rather than current, it results in faster switching speeds in comparison to BJT. [7]

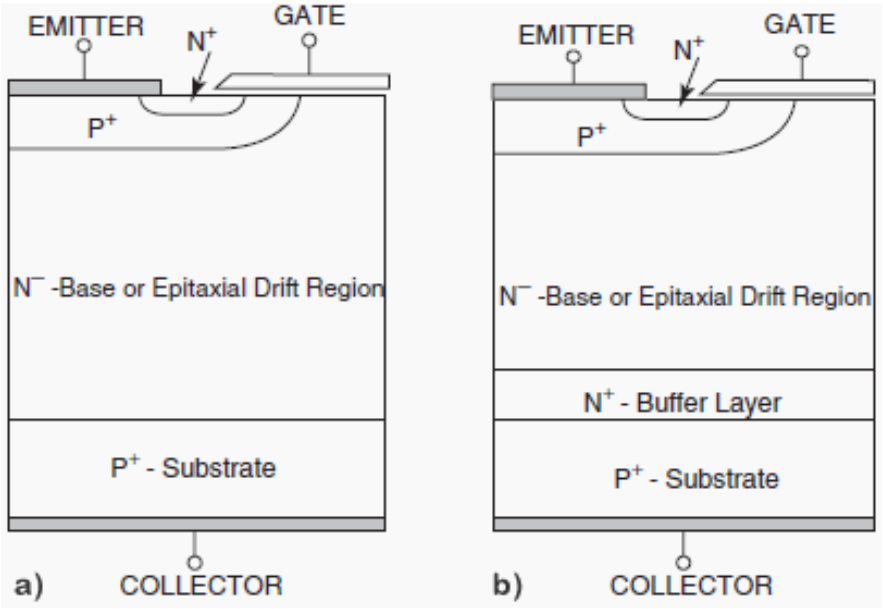


Figure 3. (a) Non-punch-through IGBT (b) punch-through IGBT

The punch-through IGBT (fig. 3b) has an additional n+ layer, called the buffer layer, above the p+ layer that contacts the collector terminal. These IGBTs have asymmetric voltage blocking capabilities. The additional n+ layer leads to faster evacuation of the stored charges in the base of the IGBT. This reduces the current fall time and turn-off time for the IGBT and for this reason punch-through IGBTs are used for inverter and chopper circuits. IGBTs without n+ buffer layers are called non-punch through IGBTs. They have symmetric voltage blocking capability and they are usually used for rectifier type applications.

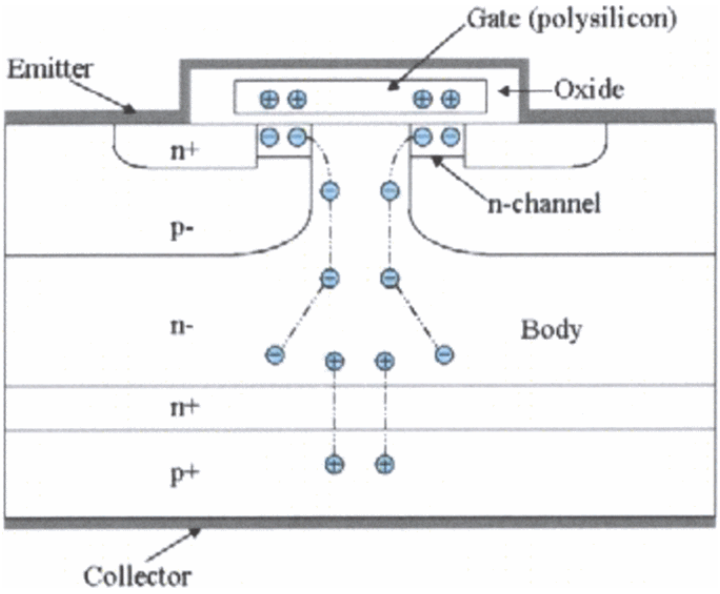


Figure 4. Charge carriers flow in punch-through IGBT

IGBT module structure

The overview of IGBT modules is categorized with two levels: die and package. This classification is based on the role of dies and packages in IGBT modules. Dies provide the essential function of power semiconductor devices, i.e. control of electrical power, whereas packages provide electrical interconnection, heat dissipation path, and environmental and handling protection.

IGBT dies

Typically, an IGBT chip or die is composed of several cells per chip area spaced by cell pitch. The cell pitch and the number of cells per chip area determine the current density of the IGBT chip. Gate-connection layout determines how multiple IGBT cells per unit area are connected together in parallel. Factors such as current density, cell technology, cell performance, and manufacturing affect the choice of gate. The interconnection of IGBT cells forms the active area of the device as shown in figure 5.c. [8]. The polysilicon gate connections running across the chip underneath the emitter gate bonding pads are required to connect the gate terminal to external gate driver circuit. The gate pad layout is determined based on the bond wire scheme used in the IGBT module design and it has an impact on the switching performance of the IGBT chip.

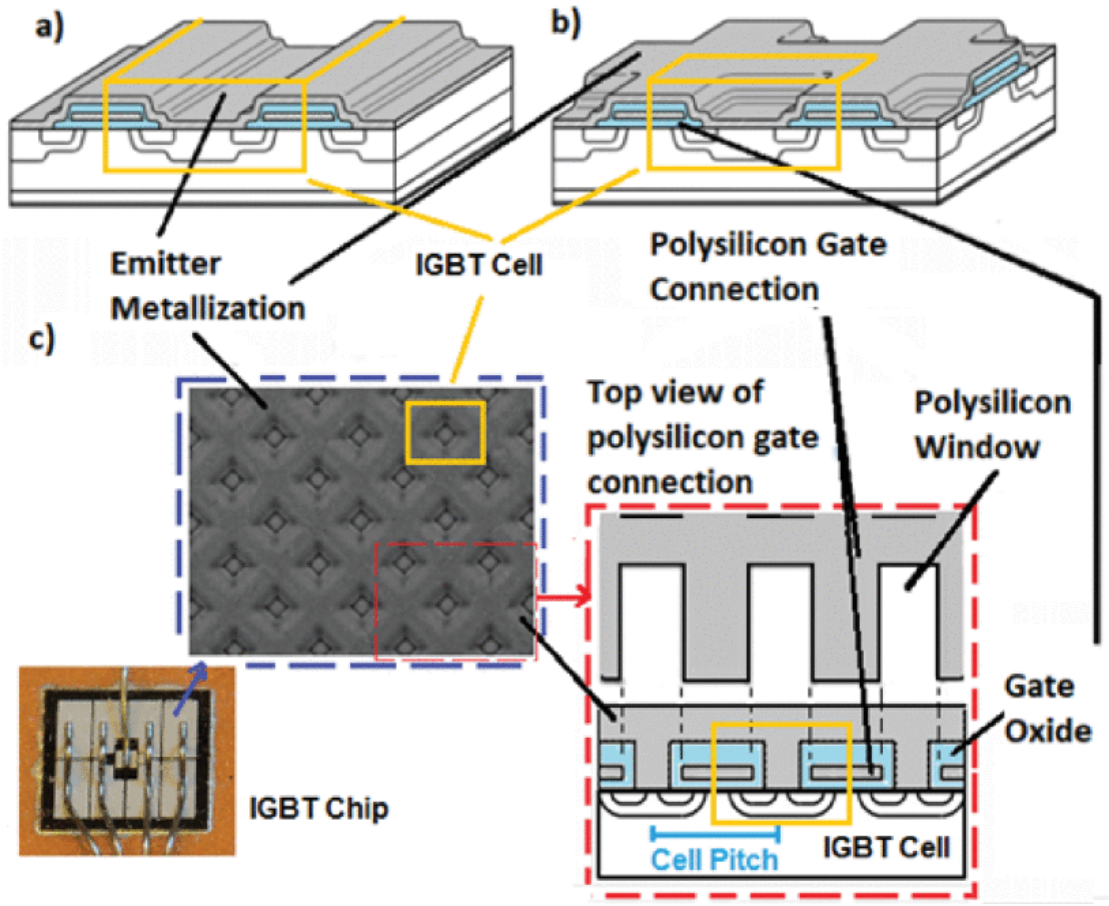


Figure 5. IGBT die layout and cells interconnection

The emitter metallization is made from aluminum alloy for aluminum wire bonding to form an electric connection between emitter and an external terminal. Most of the emitter metallization designs consider multiple bonding pads ordered in a matrix formation. The main reason behind having several emitter bonding designs is to ensure uniform current distribution on the emitter metallization and the bond wires, thereby, preventing the formation of hotspots [9].

On the other side of the chip, the collector metallization has three roles. First, it works as electrical connection between the collector and the package. Second, it acts as thermal interface between the die and the package. Third, it functions as an adhesion layer between chip and the solder layer which is used to attach the chip to the package. Extra layers are added to the backside metallization to protect the die from contamination either by diffusion of particles coming from the solder or oxidation [10].

The adoption of improved and innovative IGBT technologies, for example wide band-gap semiconductor materials such as SiC and GaN different form more traditional Si or new technologies based on superjunctions, potentially introduces new failure modes and mechanisms, which can complicate the tasks of failure analysis and prediction of RUL (remaining useful life) of IGBTs.

IGBT package

In IGBT modules, several IGBT chips and free-wheeling diode (FWD) chips are packaged together. Freewheeling diodes can fail under various loading conditions, in particular during the turn-on transition of IGBTs with a high switching frequency. The failure eventually slows down the switching speed of power converters. [11]

The reasons of the packaging are:

- to form new power electronic building blocks such as chopper, half-bridge (like in figure 6), six-pack, etc.
- to achieve higher current carrying capability through optimal paralleling IGBT cells and FWD cells of lower current carrying capability inside the module.
- to provide electrical conduction paths between the IGBT/FWD chips and the external circuitry.
- to transfer heat generated at the chips to a heat sink.
- to provide a means for mechanical mounting and protection against environment.

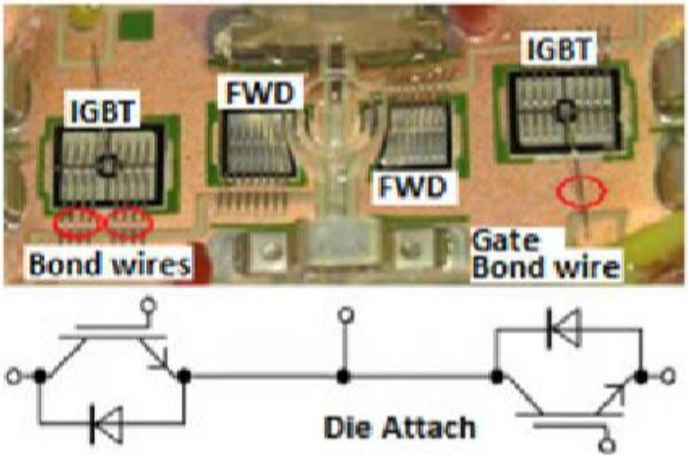


Figure 6. Example of module internal circuit configurations

Two packaging techniques have been used traditionally: wire bond modules and press-pack modules [12]. Cross-sectional views of the two modules are illustrated in fig. 7. As the most widely used technology for IGBT packaging, wire-bond modules adopt well-established and low-cost aluminium wire bonding technologies to provide electrical connections between the pads on the top of the die and the output terminals.

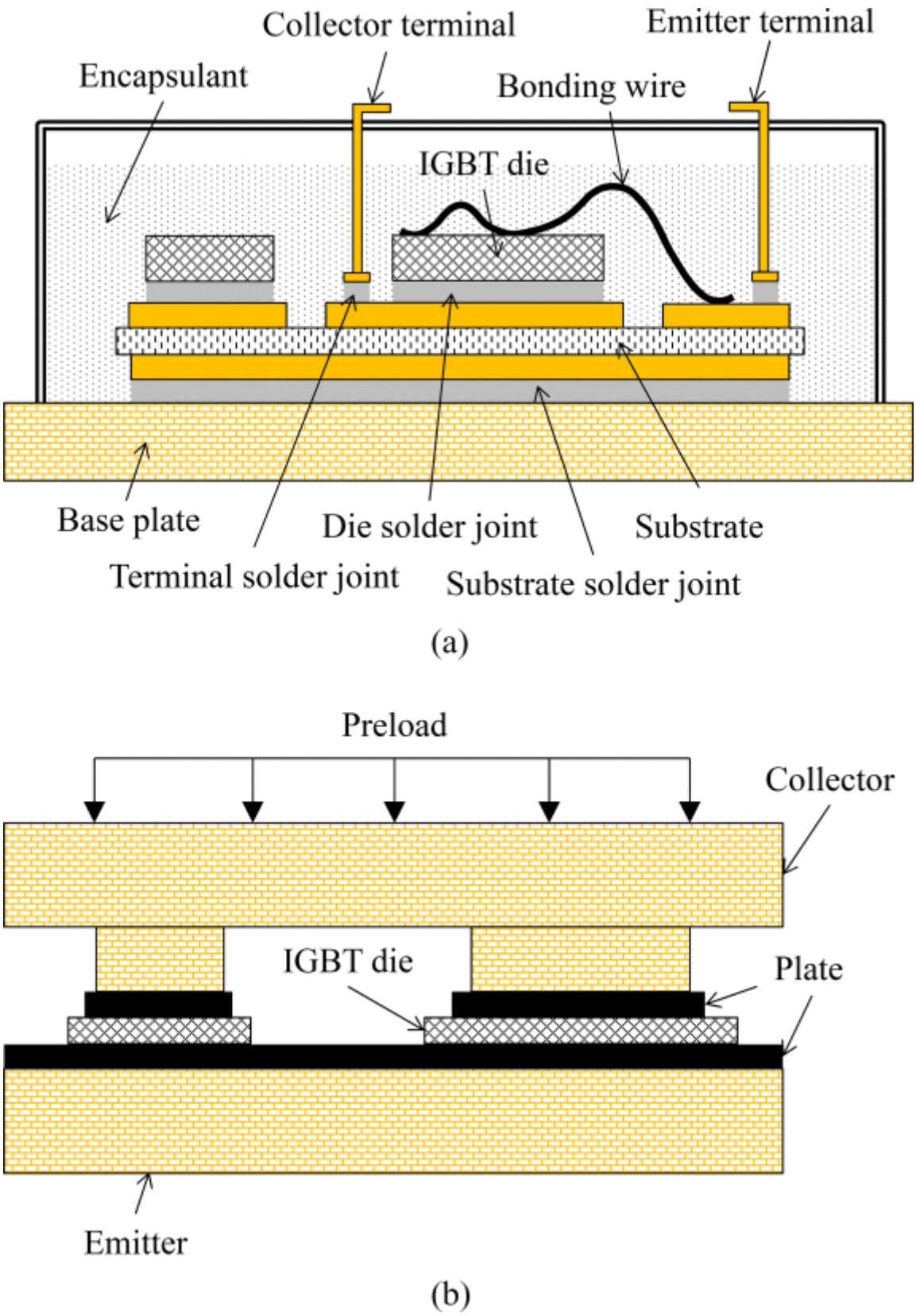


Figure 7. (a) wire bond module (b) press-pack module [13]

The advantages and disadvantages of wire-bond modules and press-pack modules are compared in table 1. Several studies ([14] ÷ [16]) claimed that the implementation of IGBT dies in press-pack modules should guarantee higher reliability.

Table 1. Comparison between wire-bond and press-pack module [13]

Feature	Wire-bond module	Press-pack module
Power and thermal cycling reliability	Mismatch in CTE can lead to fatigue failure	The possibility of fatigue failure is reduced since wire bond and solder interconnect are substituted with bondless pressure contact [31].
Single die failure susceptibility	The state (open- or short-circuit) after a single die failure is not defined. It can lead to catastrophic failure of the whole module.	With a redundant design, the module can continuously operate with a single die failure. A failed die can be replaced during planned system services.
Explosion safety	An explosion was observed when short-circuit conditions were met [92], [93].	The plasma formed by a short circuit can be confined inside the module through proper designing.
Cooling system	Simple; for example, a heat sink with a cooling fan is used.	Complicated; for example, deionized water is used.
Heat dissipation	Large temperature differences between individual dies can occur due to inherent variability in thermal resistance of their solder interconnects and substrates.	Uneven heat dissipation is reduced by sharing common heat sink blocks; for example, the temperature difference between the hottest and the coldest dies were 6 °C during the heating phase of a power cycle [29].
Current distribution	Current flow in individual dies can be uneven due to their temperature differences.	Current flow in individual dies is "quite homogenous" between individual dies [29].
Die mounting	Conventional (inexpensive)	Unique (expensive)
Electrical insulation	A ceramic layer itself in the DBC substrate provides the internal insulation.	A die carrier subassembly requires housing for the insulation.
Transient voltage at high switching frequency	Transient voltage of individual dies varies unless their electrical circuits are perfectly identical.	Differences in transient voltage of individual dies are reduced since a common inductive path is shared.

The packaging techniques for IGBTs have been evolving continuously for further improvements. It should be noted that the adoption of a new technology to mitigate one failure mechanism often leads to the exposure of another.

The metallization layers on the top side of IGBT/FWD chips (dies) are connected to the top copper layer of DBC (direct bonded copper layer) through aluminum bond wires. This copper layer serves as power track to connect devices to each other and to module terminals. The metallization layers on the bottom side of the chips are soldered to the top copper layer of DBC. These solder layers are called die attach or chip attach which serves three functions:

1. to conduct current from the chips to top copper layer of DBC.
2. to transfer heat from the chips to DBC.
3. to fix the chips into the DBC.

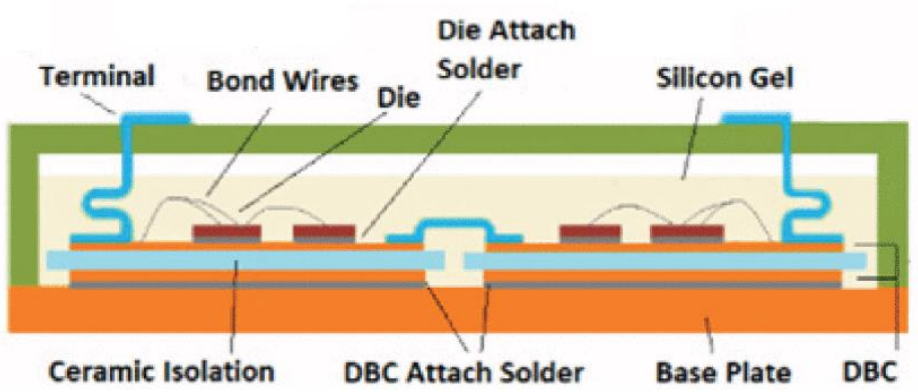


Figure 8. Cross-sectional sketch of IGBT module

DBC consists of two copper layers sandwiching a ceramic layer to provide electrical isolation between the chips and the base plate. DBC is soldered to a copper base plate. This solder layer is called DBC attach which serves two functions:

1. it transfers heat from DBCs to the base plate.
2. it fixes DBCs to the base plate that is mounted on a heat sink.

On mounting the module on the heat sink, thermal interface layer (TIM) is used to improve the thermal conductivity of the base plate to heat sink interface.

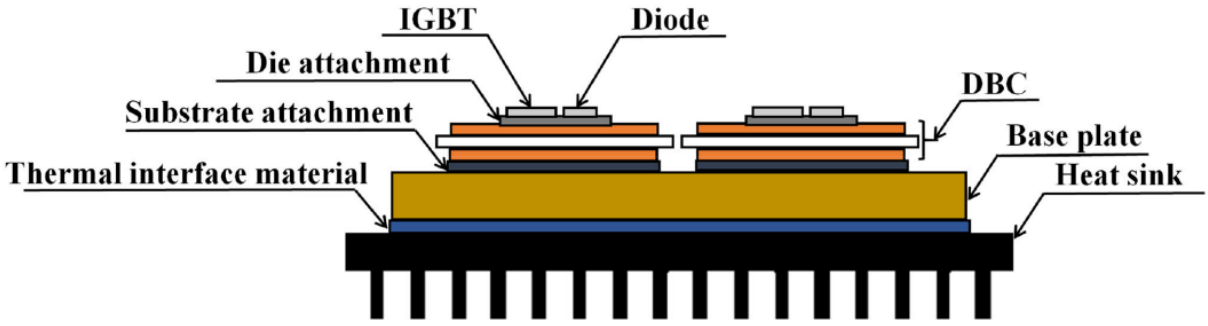


Figure 9. Cross-sectional sketch of the IGBT module with heat sink

IGBT module failure analysis

Before starting the analysis, an observation needs to be done. The term “ageing mode” defines a degradation process that leaves the device functional. Metallurgic degradation of metallization or wire bonds is typical of this type. The term “failure mode” is associated with a destructive process that renders the device non-functional, as a thermal runaway of the chip (short circuit) or as a completely broken connection (open circuit). Ageing modes inevitably lead to failure modes if device operation is not interrupted in time, so we consider ageing modes as a particular type of failure modes.

IGBT modules are complex structures of different material layers, which are brought together to form the chip and the package. IGBT modules’ field failures can be linked to manufacturing defects including chip defects, and module defects such as bond wire, solder, metallization, and insulation defects. Use and environmental conditions accelerate the latent defects into the failures. Therefore, the failure of IGBT module is linked to many possible failure modes. However, there are dominant failure modes to which most of the failures are related. These failure modes can be categorized into two main groups:

- **failure modes associated to chips**
- **failure modes related to the package**.

Another classification depending on the type of stress IGBT is subjected in field can be made. There are:

- **overstress failure modes**; the failure is due to random and sudden overstress events, such as overvoltage or overcurrent.
- **wear-out failure modes**; modules may fail under sustained loading conditions due to long-term degradation

Table 2. IGBT failure mode classification from [8]

Chip-related Failure Modes	Overstress [18, 19, 20, 21, 23, 35]	Gate overvoltage (Voltage breakdown)	System Effects: - Open circuit faults - Short circuit faults (Majority of the cases)
		Overvoltage (Voltage breakdown)	
		Overcurrent	
		Cosmic rays burnout	
	Wear-out [23, 33, 36-40]	Time dependent dielectric breakdown (TDDB)	System Effects: - Mal-operation of gate drivers & switches. - Loss of chip’s voltage blocking capability
		Hot carrier injection (HCI)	
		Electro-chemical migration	
Package-related Failure Modes	Overstress [23, 24, 34]	Mechanical shock and stresses	System Effects: - Open, or short circuit faults - Accelerate wear-out - Melting & Burnouts (More common in harsh environments)
		Thermal shock	
		Thermal runaway & Flashovers	
	Wear-out [23, 24, 34,36-40]	Thermo-mechanical fatigue	System Effects: - Thermal issues (Majority of the cases). - Stray (leakage) current issues. - Loss of module’s voltage blocking capability.
		Thermo-mechanical creep	
		Electro & electro-chemical migration	
		Insulation degradation	

Chip related, overstress failure modes

Overstress failure modes are mainly due to events such as:

- **gate overvoltage**, it may happen due to external surge, gate driver anomalies, and gate oscillation especially during short circuits.
- **collector-emitter overvoltage**, it may take place due to surges, control signal and measurement signal anomalies, and unexpected load condition.
- **overcurrent**, that may occur due to internal or external faults, improper control actions, and unexpected load events.
- **incidence of cosmic rays**

IGBT catastrophic failure behaviours can be further classified as **open-circuit failure** and **short-circuit failure**. Normally, open-circuit failure is not fatal to the converter immediately, since the converter can operate with lower quality of output but may result in secondary failure in other devices and the converter. Short-circuit failure is almost fatal to converters, as the uncontrolled short-circuit current may destroy the failed IGBT and/or other components in the circuit.

The mechanisms of open circuit are:

- **Bond wire lift-off or rupture**

Multichip IGBT modules for high-power applications typically include up to 800 wedge bonds. Since about half of them are bonded onto the active area of semiconductor devices (IGBT and freewheeling diodes), they are exposed to almost the full temperature swing imposed both by the power dissipation in the silicon and by the ohmic self-heating of the wire itself.

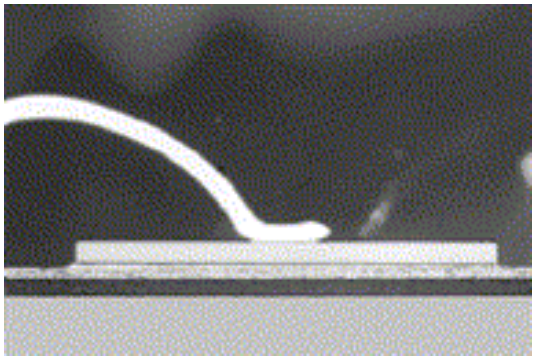


Figure 10. Example of wedge bond. Cross-section through the gate bond wire of an IGBT module (optical image 3x) [17]

Emitter bond wires are usually 300–500 µm in diameter. The chemical composition of the wire can be different from manufacturer to manufacturer, however in all cases, the pure aluminum is hardened by adding some few thousand parts per million of alloying elements, such as silicon and magnesium, or nickel for corrosion control. The current capability of a bond wire decreases as well-known over-proportionally with the length and just slightly depends on the substrate temperature. The maximum DC current capability of a bond wire

is limited by melting due to ohmic self-heating. In a 1 cm long wire loop in air, it is of 25 A for 300 µm (35 kA/cm^2) and of 60 A for 500 µm (30 kA/cm^2) aluminum wires.

During switching operation, the current density distribution across the section of a bond wire is strongly inhomogeneous due to the skin effect. The wires are connected by ultrasonic wedge bonding either onto the aluminum metallization (with a thickness ranging from 3 to 5 µm), or onto the strain buffer.

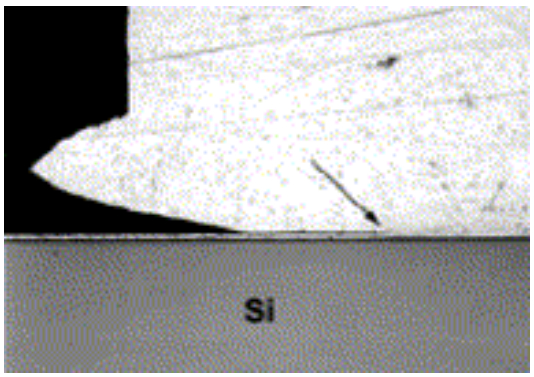


Figure 11. Cross-section through a wedge bond, before thermo-mechanical stress. The arrow indicates the transition from the non-bonded to the welded region, where the bond wire material cannot be distinguished from the aluminum metallization. [17]

Failure of a wire bond occurs predominantly as a result of fatigue caused either by shear stresses generated between the bond pad and the wire, or by repeated flexure of the wire. The failure of a single or of multiple bond wires causes a change either in the contact resistance or in the internal distribution of the current, such that it can be traced by monitoring V_{CEsat} [7]. The observed failure mode can be different depending on the stress the devices are submitted. If the test is not interrupted after exceeding a pre-defined threshold, the end-of-life failure mode observed during power cycles is melting of the survivor bond wires. On the contrary, during high-voltage test or field operation, a frequently observed secondary failure mechanism is the triggering of parasitic BJTs and latch-up.

- **Bond wire lift-off**

Bond wire lift off has been observed to affect both IGBT and freewheeling diodes. No bond wire lift off occurs at the wire terminations bonded onto copper lines. This is mainly due to the fact that copper lines do not experience large temperature swings. Additionally, the CTE (Coefficient of Thermal Expansion) mismatch between aluminum and copper is less severe than with silicon. There is experimental evidence that the crack leading to the failure is initiated at the tail of the bond wire (Fig. 11) and propagates within the wire material until the bond wire completely lifts off.

Each metal exhibits its own yield strength. If stress exceed this value, detachment of the wire from chip is immediate. If it is lower, dislocations of atoms occur, which will lead to lift-off with an atomic scale process speed depending on intensity and duration of the applied force. [17]

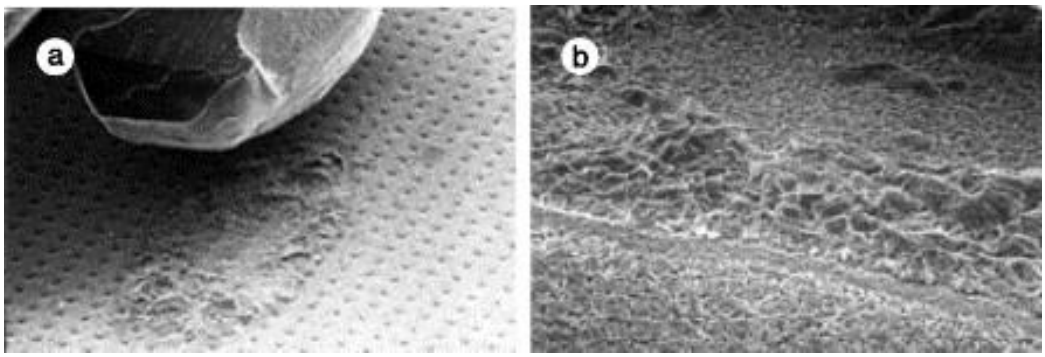


Figure 12. (a) shows a bond wire after lift off. Due to the spring action exerted by the aluminum wire loop, the wire loses the electrical continuity with the IGBT chip. (b) Close view of the footprint of an aluminum bond wire after lift off (SEM image, 100). [17]

At present, two main technological countermeasures are common for facing the bond wire lift off failure mechanism. The first one makes use molybdenum–aluminum strain buffers [18], which are mounted on the top of the IGBT and of the diode chips, with the scope to eliminate thermo-mechanical fatigue by distributing the CTE mismatch of aluminum and silicon across a thick layer. The second solution is gluing the bond wires with a coating layer. The coating consists of one or of multiple polymeric layers with graded hardness, which are painted onto the wires immediately after ultrasonic bonding.

- **Bond wire heel cracking**

Bond wire heel cracking rarely occurs in advanced IGBT multichip modules. However, it can be observed mainly after long endurance tests and especially in cases where the ultrasonic bonding process was not optimized. The failure mechanism is due again to a thermo-mechanical effect. In fact, when the wire is subjected to temperature cycles it expands and it contracts undergoing flexure fatigue. In the case of a typical bond wire length of 1 cm and of a temperature swing of 50°C, the displacement at the top of the loop can be in the 10 μm range, producing a change in the bending angle at the heel of about 0.05°. An additional stress is introduced by the fast displacement of the bond wire (e.g. at the turn on) within the silicone gel, which can be considered as a very viscous fluid. In those cases, where the temperature change within the bond wire is dominated by the ohmic self-heating, heel cracking can also be observed at the wire terminations welded on the copper lines of both IGBT chips and freewheeling diodes.

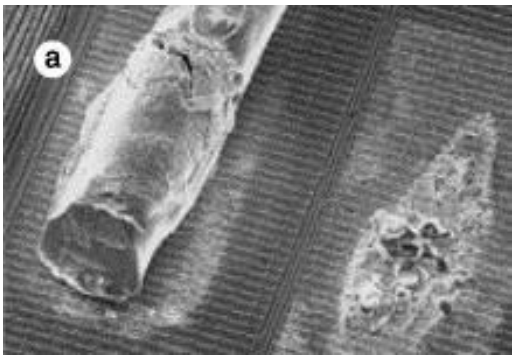


Figure 13. Bond wire heel cracking due to low-cycle fatigue stressing (SEM image, 25).

In the first case heel cracking and bond wire lift-off occur at the same time (fig. 13). However, while the adjacent bond has been completely removed by lift-off, the cracked wire still presents some electrical continuity with the chip. This is a clear indication of fact that even if the bonding parameters are not too close to the optimum, heel cracking is slower than the lift-off mechanism.

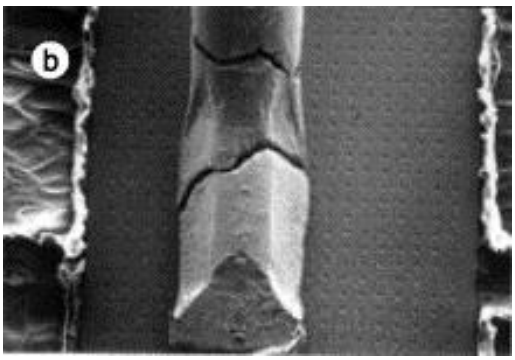


Figure 14. Bond wire cracking due to improper bond wire coating (SEM image, 25).

The failure imaged in figure 14 could lead to a wrong identification of the failure mechanism. In fact, in this case, the wire rupture has not been caused by heel cracking, but by the shear stress arising due to the use of a too rigid bond wire coating layer.

Double bonding wire is a bonding wire interconnection technique adopted to control the value of wire bond inductance and overcome frequency limitation. An example is showed in figure 15.

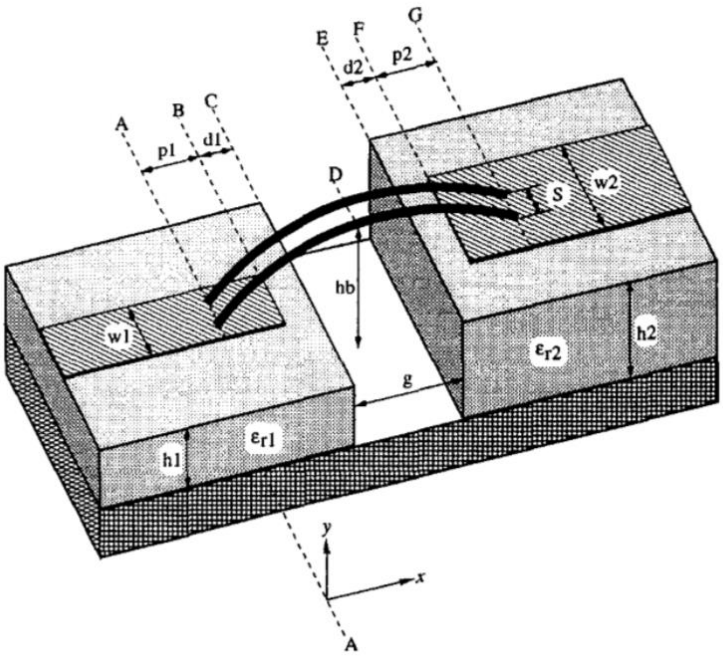


Figure 15. Double bonding wire interconnection [19]

The couple of wires in fig. 16 indicates that heel cracking preferably occurs at those locations where the aluminum wire has been previously damaged by the bonding tool. In fact, the bond wire at the left in fig 16 presents a thin crack at the same location where the crack fully developed in the wire at the right side. Additionally, it has to be mentioned that the temperature distribution in double bonds due ohmic self-heating and indirect heating through the chip is much more asymmetric than for single bonds.

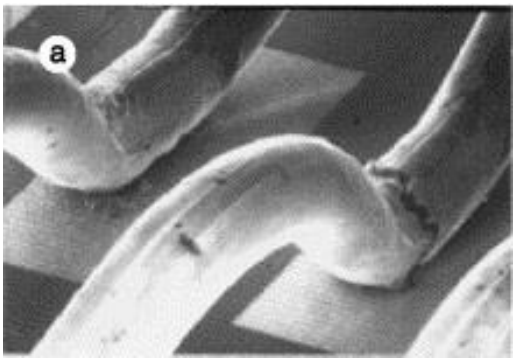


Figure 16 Heel cracking in a double wire bond. Crack initiation can also be observed in the double bond in the back (SEM image, 25).

- **Gate driver failure**

There are various causes of gate driver failure, such as power stage devices (e.g. BJTs or MOSFETs) damaged, wires between drive board and IGBT disconnected. The driver failure may result in IGBT intermittent misfiring, degraded output voltage, and overstress of other IGBTs and capacitors. Abnormal work conditions in power terminals of IGBT can also lead to driver failure. Continued narrow overvoltage spikes between collector and emitter may open the gate-emitter resistance, while overcurrent of IGBT's collector may lead to gate-emitter resistance degradation. Gate open-circuit failure can result in thermal runaway, or high power dissipation.

Among the short-circuit failure modes we can include:

- **High voltage breakdown**

High voltage spikes induced by high falling rate of collector current I_C and stray inductance can destroy IGBTs during turn-off, especially under repetitive spikes. Due to the high turn-off voltage spikes, electric fields can reach critical values and breakdown of a few IGBT cells first, and lead to high leakage current as well as high local temperature. Subsequently, the heat-flux radially diffuses from the overheated region to the neighbouring cells. Collector-emitter voltage (V_{CE}) collapses after the voltage spike instead of stabilizing at the steady state value, and then I_C rises again. Also, the gate terminal may also fail, which results in a rising gate voltage (V_{GE}). High value of V_{CE} and V_{GE} can also lead to short-circuit during turn-on. An abrupt destruction and peak current happen after several microseconds during turn-on. The hole current caused by avalanche generation concentrates on a certain point (usually high-doped p+ region). The destruction point is always located at the edge of the active area close to the device's peripheral region. Therefore, it is critical to clamp V_{GE} and V_{CE} during switching transients. [20]

- **Loss of blocking capability**

IGBTs are designed to withstand and block a voltage between collector and emitter. Once the IGBT is turned off, the load current I_L diverts from the transistor to a free-wheel diode FWD. The parasitic effects due to the interconnections are also taken into account in the following schematic through the resistor R_σ and the inductor L_σ (figure 17).

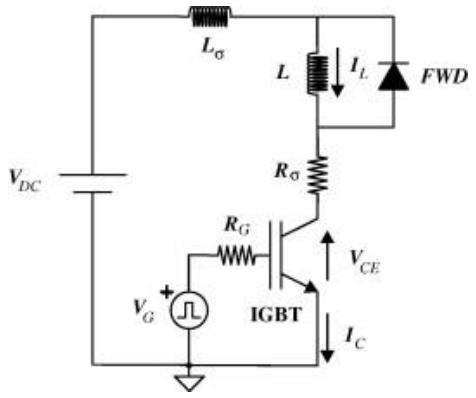


Figure 17. Equivalent circuit of IGBT, including power supply and parasitic parameters

A typical safe turn-off process is depicted in fig. 18a. When the turn-off signal is applied to the IGBT gate (V_G), at time t_0, the gate–emitter voltage V_{GE} first falls down to a plateau and remains constant until the completion of the well-known Miller-effect [21]. Then, at time t_1, the collector–emitter voltage, V_{CE}, starts rising up and V_{GE} decreases further. At time t_2, the diode FWD is forward-biased and starts conducting, and therefore, I_C starts decreasing. V_{GE} falls rapidly to zero and below. The observed voltage overshoot on V_{CE} is due to the electrical parasitic effects of the external interconnection (bus bar, cables, etc.), also shown in real applications.

Figure 18b shows a turn-off where the device fails. In this figure, the experimental current and voltage waveforms show that after removing V_{GE}, V_{CE} increases with the corresponding decrease of I_C close to zero (see circled area in fig. 18b). However, some microseconds after the turn-off, I_C increases first slowly, and then, V_{CE} collapses with a sharp current peak. This fact indicates that the device has lost its high voltage blocking capability determined by the high resistive IGBT base.

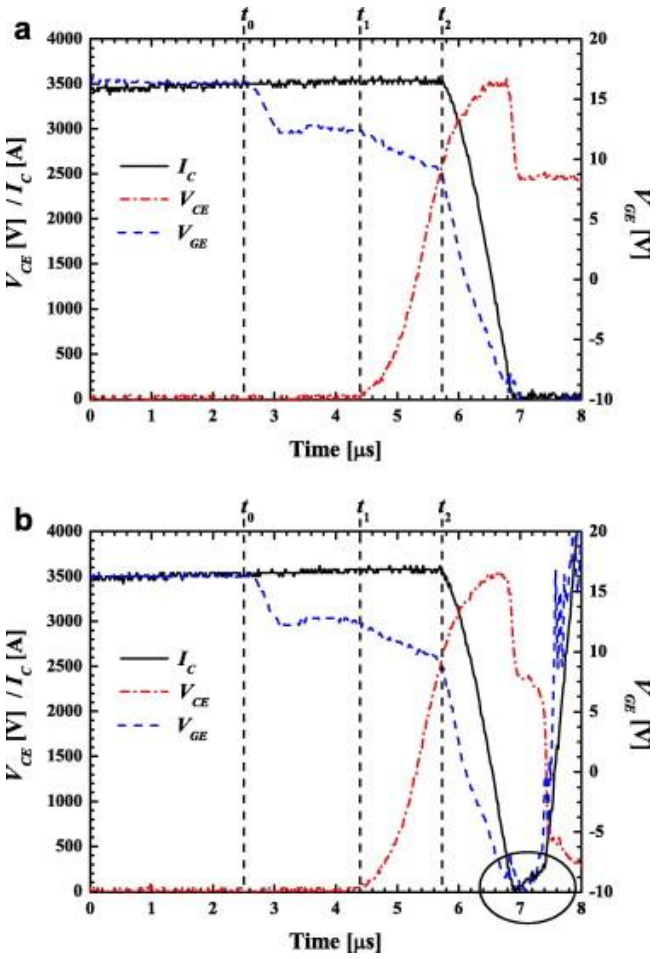


Figure 18. Experimental current and voltage waveforms for a safe (a) and for a failure-affected (b) turn-off transition performed during robustness tests. [22]

In this situation, the failure is characterised by the fact that the IGBT cannot sustain the voltage during its off-state and the causes are substantially two: secondary breakdown or latch-up.

- **secondary breakdown** in the inherent BJT structure of the IGBT

Secondary breakdown is a kind of local thermal breakdown for transistors due to high current stresses, which can also happen to IGBTs during on-state and turn-off switching. With a given collector-emitter voltage V_{CE} the failure mechanism of secondary breakdown occurs when the collector current exceeds a certain value. This means a current density of 100/1000 A/cm^2 inside the device. The critical current density is matched, when the number of travelling charge carriers almost equals the number of the locally doped charge. As a result, the electric field across this region will be influenced to critical values of more than 10^4 V/mm. If current still rises, second breakdown of collector-emitter voltage and a fast increase of collector current will only be limited by the load inductance of the circuit. With the increase of current, in fact, the collector-base junction space charge density increases, and the breakdown voltage decreases, resulting in a further increase in the current density. This process continues until the area of the high current density region reduces down to the minimum area of a stable current filament. Then, the filament temperature increases rapidly due to self-heating and a rapid collapse in voltage across IGBT occurs. However, since second breakdown is basically related to avalanche carrier multiplication at high electron current regimes, it mainly affects p-channel IGBT devices. [23]

The maximum dissipated power takes place when high current I_C and high V_{CEmax} voltage levels simultaneously coexist across the device. During all this process, T_{max} presents an overshoot near the end of the turn-off process, then decreasing to an almost constant level. This fact is related to the heat diffusion along the upper part of the device. This peak in T_{max} corresponds to the current constriction due to the high voltage being applied. This current constriction gives rise to an increase of the local temperature which is subsequently extended to the rest of the drift layer. When all of the current is freewheeling through the diode and the excess charge in the bipolar base is extracted, the residual temperature level can be enough to locally generate electrons to overcome the doping concentration. This creates an instable current filament that locally increases the temperature in the drift region. This fact originates a positive feedback effect that finally gives rise to the V_{CE} collapse. The location of the failure event should be in the drift region at a depth close to that of the local maximum peak temperature.

As previously stated, it can be observed in fig. 18b that the device is almost turned-off after the turn-off process, but suddenly a slight increment in I_C appears. This low current level can be due to several instable current filaments. They are originated by local hot-spots which thermally generate free-carriers (the material locally becomes an intrinsic semiconductor), exceeding the background doping level concentration. Subsequently, a thermoelectrical positive feedback occurs, i.e. the local temperature increase feedbacks the current density rise, and vice versa.

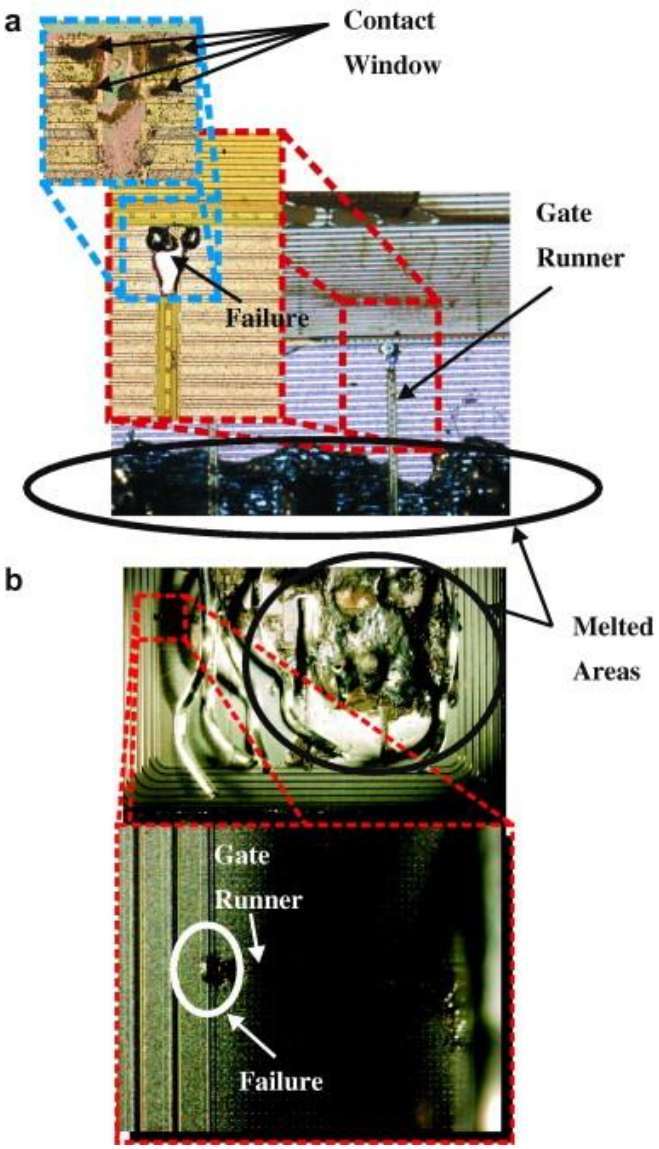


Figure 19. Signature in failed IGBT devices coming from the field (railway application) (a) and from performed robustness tests (b). [22]

Inspection of the surface of device failed by secondary breakdown shows the existence of burn-out spots in silicon layers of individual IGBT cells at the end of the gate runners, in the vicinity of the device edge termination (figure 19). This signature has also been observed in equivalent multichip modules with IGBTs from different fabrication technologies and layouts. The shape of the burn-out spot in particular suggests that the IGBT failure is due to a current filamentation produced by the temperature increase inside the IGBT substrate. [22]

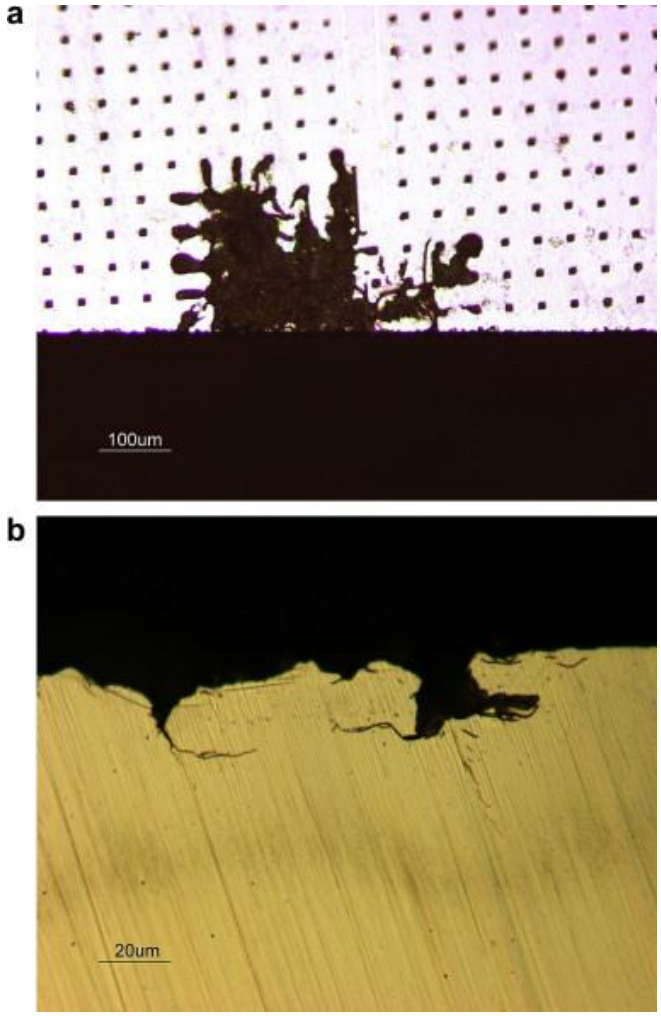


Figure 20 (a) Top view of the failure at the end of the gate runner, (b) device vertical cross-section showing melted and burned areas, arriving up to 50 µm inside the device.

In figure 20, it can be seen as the failure event is occurred in the device bulk (located at 50 µm depth), which is in accordance with the performed simulations in [22]. This failure takes place at the edge of the gate runners close to the edge termination region where the number of IGBT cells is lower than in the rest of the device and the carrier excess is more rapidly removed in comparison to the rest of the device centre. This failure signature is true for IGBT devices from different technologies and IGBT basic cell design.

This behaviour could be understood in terms of the less existing carrier excess, which in turns, makes feasible to be the region where the excess charge is firstly removed and then the highest probability to turn into an intrinsic material. According to the simulation results, the hot-spot produced by the current constriction during the turn-off is not in agreement with a latch-up destruction mechanism, since the signature related to secondary breakdown takes place inside the drift region. [22]

- **latch-up**

The latch up is a failure mechanism inherent to IGBT devices. The latch up mechanism manifest itself through a sudden collapse of the collector to emitter voltage, and once this failure mechanism is activated the device cannot be longer controlled through the gate. The failure mode associated with latch up is always a generalized low-ohmic short circuit of collector, emitter, and base. With respect to fig. 21, latch-up happens when the parasitic NPN transistor is turned on and works together with the main PNP transistor as thyristor, and then the gate loses control of I_C.

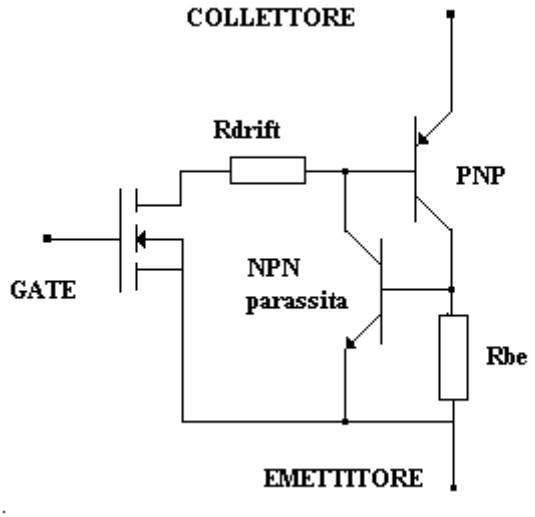


Figure 21. Simplified equivalent circuit of an IGBT, which takes into account just quasi-static effects.

IGBT latch-up can be divided into two types, static and dynamic latch-up. Static latch-up happens at high collector currents, which turn on the parasitic NPN transistor by increasing the voltage drop across the parasitic resistance R_{be}. Dynamic latch-up happens during switching transients, usually during turn-off, when the parasitic NPN transistor biased by the displacement current through junction capacitance between the deep p+ region and the n-base region.

Under normal forward operating conditions the voltage drop caused by the collector current over the permitter diffusion (represented by the resistor R_{be}) is almost negligible. Therefore, the parasitic BJT is in the non-conducting state and the IGBT device is controlled by the electron flow injected into the base of PNP BJT through the MOS transistor.

On the contrary, if the collector current reaches the critical value for which the voltage across R_{be} exceeds 0.6 V, parasitic NPN BJT enters in conduction and provides the base current to the PNP BJT. Since the additional base injection turns into an increase of the collector current, this effect is regenerative and leads to the thermal destruction of the device, which is not controlled by the gate voltage anymore. This simple quasi-static

model illustrates how latch up may arise in n-channel IGBTs, while forcing the collector current to increase. This situation can occur in an IGBT module, if the number of operating cells within a module is reduced with time, due to a degradation mechanism, as for example bond wire lift-off. When latch-up happens, IGBT will be almost inevitably damaged due to the loss of gate control.

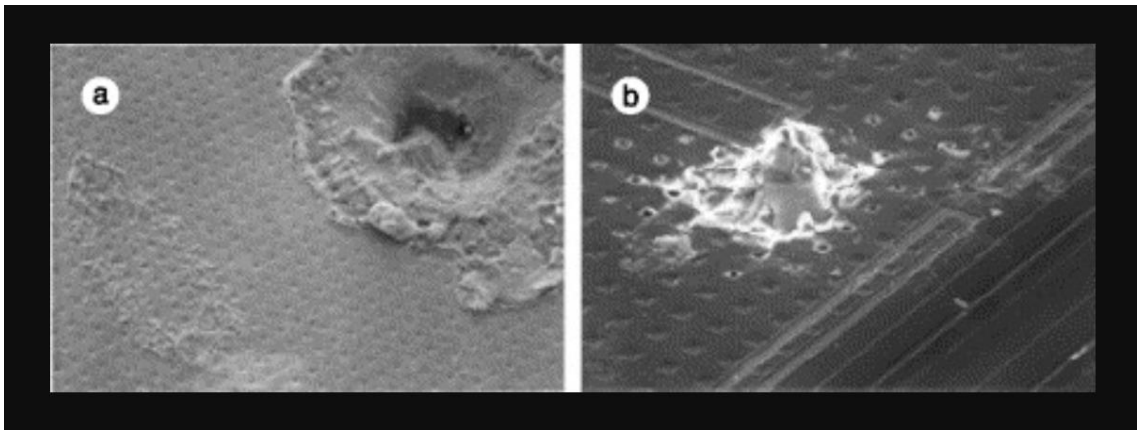


Figure 22. (a) Melted pit in an IGBT due to a latch up event, which occurred in conjunction with bond wire lift off (SEM image, 50x). (b) Same effects than in the previous image but localized to some few cells (SEM image, 90x). [17]

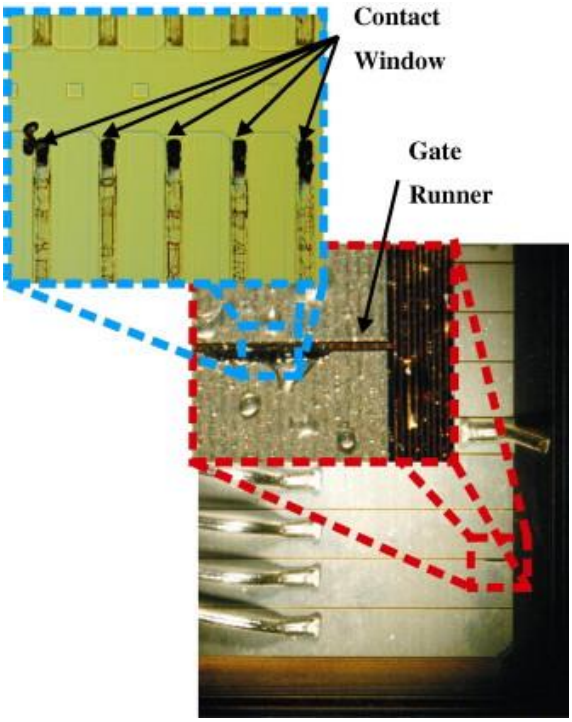


Figure 23. destroyed regions located close to the gate runner fingers, possibly due to a latch-up mechanism. [22]

Moreover, a latch-up failure would be observed from voltage waveforms at the initial stages of the turn-off. One may expect that this phenomenon will be predominantly located to the IGBT surface and will be detected by burned emitter contacts.

This phenomenon is of special relevance, because most of the root causes mentioned above activate this mechanism. It has to be noted that the latch-up is mainly a problem related to the ability of a certain device design to survive stresses out-of-specification. That latest-generation IGBTs with trench-gate structure and heavily doped p-base region under n-emitter, have been proved to have good latch up immunity, and latch-up is not a common failure in the latest devices anymore. When working in unrestrictive temperature environments, the dynamic latch-up failure is more prone to happen, whereas the secondary breakdown is expected in high temperature scenarios.

- rapid rise in junction temperature (**thermal runaway**) due to **energy shocks** (high-energy dissipation)

Failure may happen also due to high power dissipation within a short time e.g. short circuit at the on-state, defined as energy shock. The high short-circuit current will result in energy shock and high temperature. However, IGBTs will not immediately fail when the junction temperature exceeds the rated temperature. Since the cooling system isn't designed to remove heat in a short time, temperature continues rising and the dissipated power energy increases until the melting of parts of IGBT.

Thermal runaway happens only if a critical threshold of energy or a critical temperature, which depends on the structure of the device, is exceeded. Short-circuit currents inevitably introduce high energy and temperature to IGBT chips, therefore it is important to design an efficient thermal management to improve the ability of withstanding short circuits in order to have time to detect failure and protect IGBTs.

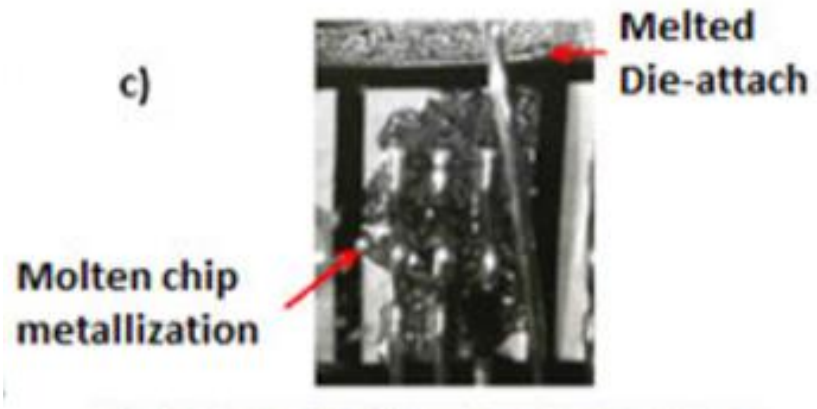


Figure 24. Large scale melting of chip metallization and die-attach solder due to thermal runaway caused by high-energy dissipation during the fault. [8]

- **burnout due to cosmic rays**

Device burnout is a failure mode, which is very frequently observed either as the final act of wear-out, or as consequence of a failure cause occurring randomly. Burnout is often associated with a short circuit condition, where a large current flows through the device (or through a portion of it), while it is supporting the full line voltage. Sustaining a short circuit over a long-time interval inevitably leads to thermal runaway and finally to a fast destruction of the device. In fact, since IGBTs do not require any di/dt snubbering, the device itself limits the current increase rate. Therefore, after the failure the current may increase at a rate up to 10 kA/μs. In this case, the main part of the stored capacitive energy is released in few hundreds of nanoseconds reaching a peak power up to 100 MW. The capacitive energy is dissipated by the ohmic components of the circuit, i.e. mainly by the bond wires and by the silicon chip. As consequence of the adiabatic heating process, the bond wires evaporate, by producing a preferential conductive path for arching through the module. The resulting shock wave rapidly propagates through the silicon gel by leading to the catastrophic destruction of the device.

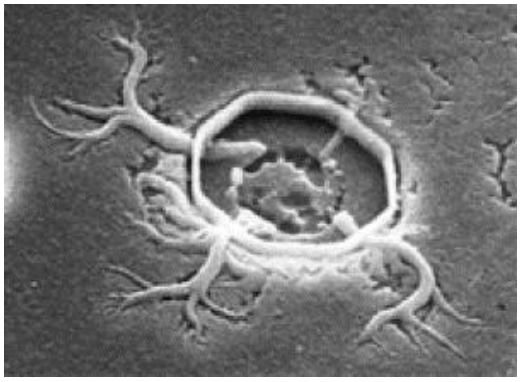


Figure 25. Polysilicon filamentation in an IGBT as a consequence of a short circuit between gate and emitter, due to pre-damaged insulation during wire bonding (SEM image, 2000×). [17]

Cosmic-ray neutrons can trigger a single-event burnout (SEB). Recoil ions produced by nuclear spallation reactions between incident neutrons (cosmic rays) and silicon nuclei form highly localized electron-hole plasma. The first current peak indicates that the initially generated charge carriers along the ion track are accelerated by the electric field in the depletion region at time (2) (figure 26).

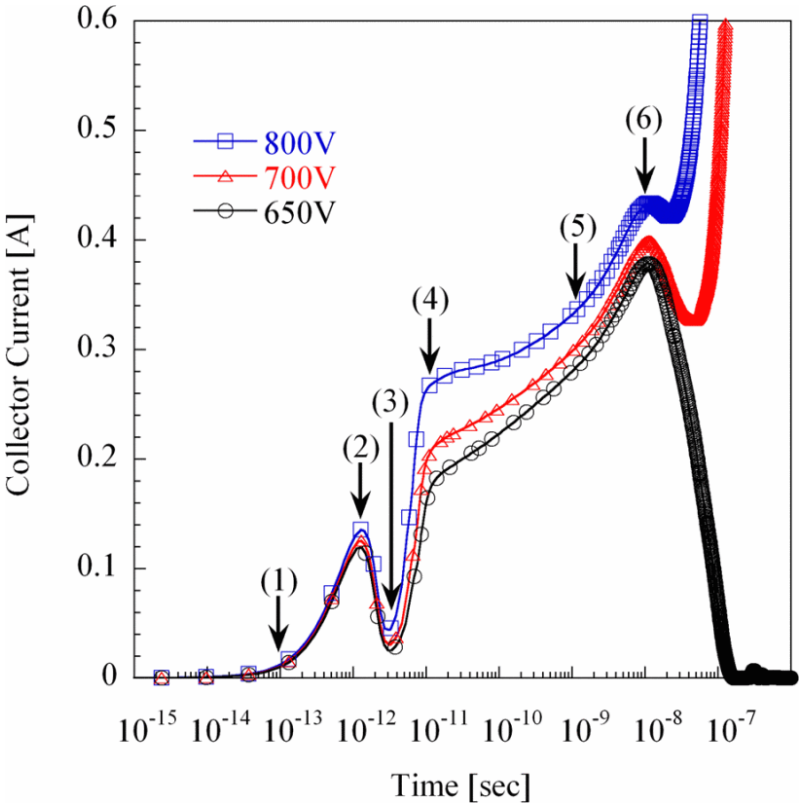


Figure 26. Applied voltage dependency of the collector current. [24]

The peak electric field strength shifts from the n- drift/p- body junction to the n drift/n+ buffer junction (n/n+ junction). This is the base push-out effect due to the highly localized current in the reverse biased IGBT. Therefore, the electric potential distribution is changed to a funnel-like shape and consequently carriers are generated at the n-/n+ junction due to the impact ionization. (Figure 27a and 27b).

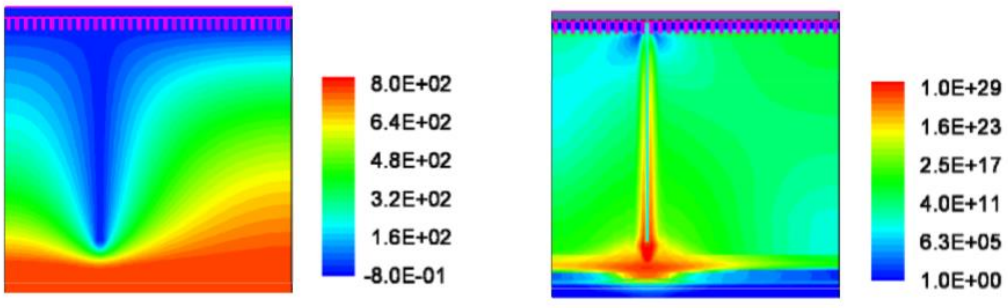


Figure 27. Cross-sectional view of IGBT simulated. (a) Electrostatic potential [V] at time (3). (b) Impact ionization rate [$s^{-1}cm^{-3}$] at time (3), equal to $3*10^{-12}$ s

Injection of the generated carriers into the base neutral region triggers the turning-on of the inherent parasitic PNP transistor (p- body/n- drift/p+ collector). Consequently, the hole carriers are injected into the n- drift region from the backside of the device (fig. 28a and 28b).

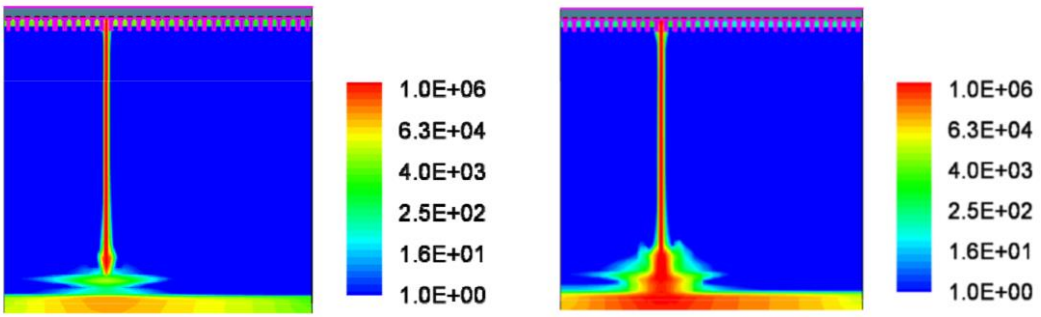


Figure 28. (a) Hole current density [Acm^{-2}] at time (3). (b) Hole current density [Acm^{-2}] at time (4)

At the second current peak at time (6) in fig. 26 ($1.06 * 10^{-8}$ s), the inherent parasitic NPN transistor (n+ emitter/p body/n- drift) turns on, and electrons are subsequently injected into the n- drift region (fig. 29).

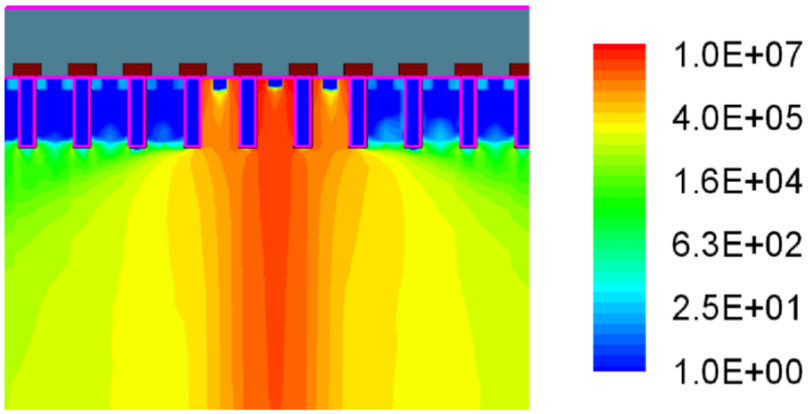


Figure 29. Electron current density [Acm^{-2}] at time (6).

Therefore, the electric field strength at the n-/n+ junction decreases due to the electron injection at this time. The lowering of the electrical potential between p- body and n+ emitter junction due to the electron injection leads to a temporary decrease in the collector current. Ultimately, the latch up of the parasitic thyristor action results in positive feedback of the collector current and, consequently, device destruction. (Figures 27 ÷ 29 are transient simulation results for triggering mechanism of single-event burnout from [24].

Chip related, wear-out failure modes

The most common IGBT chip wear-out failure modes are:

- **Time Dependent Dielectric Breakdown (TDDB)**

TDDB is the result of gate oxide degradation caused by high gate voltage bias stress with time. Gate oxide degradation is caused by accumulation of defect charge in the gate oxide layer. A large number of research results show that there are various forms of charges in the system of Si-SiO_2, which can be generally classified into the following four types: fixed oxide charge Q_f, mobile ion charge Q_m, interface-trapped charge Q_{it} and oxide-trapped charge Q_{ot}. Q_f and Q_m are mainly produced in the manufacturing process of devices, which are controlled in quantity and their influence on equipment can be ignored with the improvement of manufacturing technology. For Q_{it} and Q_{ot}, these traps are randomly generated under gate stress. The nearest neighbor traps form conductive groups, and excessive low-level current flows through these conductive groups, as shown in the figure 30. The higher the trap density is, the higher the current flows. When the trap density in the local area reaches a critical value, the conductive groups make the gate and substrate conduct, forming a percolation path and causing local dielectric breakdown. [25]

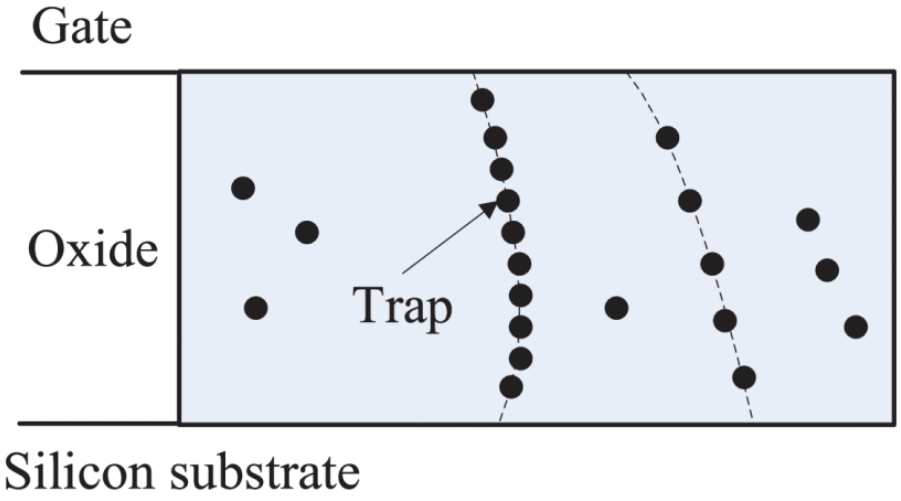


Figure 30. Physical model of breakdown due to trap accumulation in the oxide [25]

- **Hot Carrier Injection (HCI)**

Hot carrier injection (HCI) is a phenomenon in solid-state electronic devices where an electron or a hole gains sufficient kinetic energy to overcome a potential barrier necessary to break an interface state. These energetic carriers can lead to impact ionization within the substrate and the generated electrons or holes inside the channel or the heated carriers themselves can be injected into the gate oxide and generate interface or bulk oxide defects. Hot electrons have sufficient energy to tunnel through the thin oxide gate to show up as gate current, or as substrate leakage current. Since the charge carriers can become trapped in the gate dielectric, numerous physical damage processes that can drastically and permanently change the device characteristics over prolonged periods,

such as threshold voltage or the switching characteristics, and eventually cause the circuit to fail. The accumulation of damage resulting degradation in device behaviour due to hot carrier injection is called “hot carrier degradation”.

- **Electrochemical migration (ECM)**

In humid environments, under high voltage and temperature, electro-chemical migration at chip passivation layer and terminal structure causes an increase in leakage currents and gradual loss of blocking capability. Devices are used often in harsh conditions, especially for the automotive industry, where the components are exposed to higher humidity, rapid changes in temperatures and condensation cannot always be fully avoided. All the above raises the amount of ECM related issues like dendrites or whiskers. The condition of two oppositely biased and closely spaced electrodes across a non-metallic medium (electrolyte) can lead to an electrochemical reaction of metals and an inadvertent conducting path creation. The phenomenon of electrochemical migration (ECM), sometimes referred to as electrolytic migration, is known as a form of corrosion.
The term electrochemical migration refers to a three-step process: corrosion of one electrode, metal migration, and metal redeposition on the other electrode.
For an IGBT chip the most critical region is the junction termination with the metallization of the active area (cathode) and of the channel stopper (anode) being the adjacent conductors at different potentials. The process starts with the decomposition of water (see figure 31a) and the movement of the resulting ions according to their respective charge and the applied electric field. Depending on the solution properties, cathodic reactions may involve oxygen reduction and/or hydrogen production (figure 31a), while corrosion and formation of metal complexes, salts, or oxides is possible at the anode [26,27].

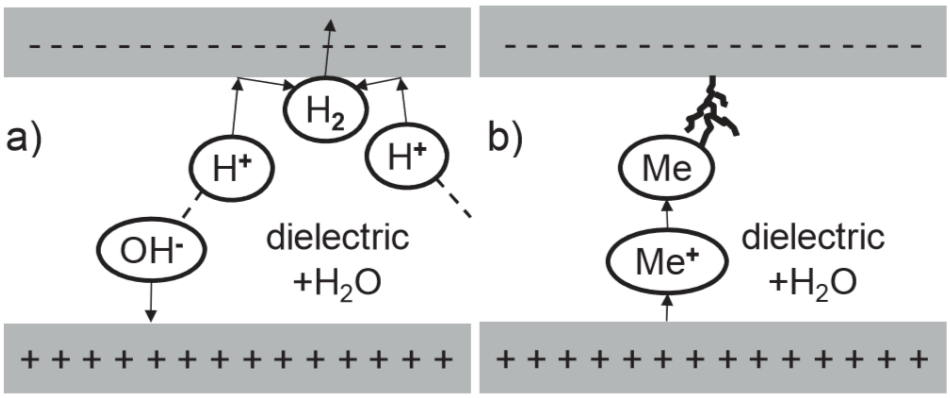


Figure 31. ECM between metallisation stripes. a) decomposition of water and metal corrosion. b) metal migration and formation of a dendrite [26]

Many factors influence electrochemical migration, including relative humidity, temperature, voltage bias, conductor material and spacing. Type and amount of contamination may also have an important influence on corrosion.

Due to the importance of TDDB and electro-chemical migration, since the dawn of IGBT, standard reliability demonstration tests have been designed to address them [10], [28].
The high temperature reverse bias test (HTRB), sometimes also referred to as hot reverse test, verifies the long-term stability of the chip leakage currents. During the HTRB test, the semiconductor chips are stressed with a reverse voltage at or slightly below the blocking capability of the device at an ambient temperature close to the operational limit. No degradation can be expected in the bulk silicon of the devices at these temperatures, but the test is able to reveal weaknesses or degradation effects in the field depletion structures at the device edges and in the passivation.
The high temperature gate stress test or high temperature gate bias test (HTGB) confirms the stability of the gate leakage current. Even though the maximum allowed gate voltage is limited to ± 20 V, this voltage is applied to not more than 100 nm thick gate oxide layer in state-of-the-art IGBTs and MOSFETs. This results in an electrical field of 2 MV/cm across the gate oxide. For a stable leakage current, the gate oxide must be free of defects and only a low density of surface charges is tolerable.
The temperature humidity bias test, also known as high humidity high temperature reverse bias test (H3TRB), is focusing on the impact of humidity on the long-term performance of a power component. Capsules are – when defect-free assembled – hermetically sealed against the environment. This is not the case for the majority of power module packages. Although bond wires and chips are completely embedded in silicone soft mold, this material is highly permeable for humidity. Therefore, humidity can intrude the package and can reach the chip surface and junction passivation. This test aims to detect weaknesses in the chip passivation and to initiate humidity-related degradation processes in the packaging materials.
Temperature swings are an essential stress condition for every power electronic component in application. The temperature cycling test and the temperature shock test are two test methods to simulate ambient temperature swings during the field lifetime. The test conditions are discriminated by the change rate of the externally imprinted temperature. If the rate of temperature change is slow in the range of 10–40°C/min, the test is called temperature cycling test. In a temperature shock test, the ambient temperature is changed typically in less than 1 min. [29]

Table 3. Some of most important international reliability standard. [28]

Test	Standard / Test Method	
HTRB	JESD22-A108D: T_j=150°C, V_{GS}= 0V; V_{DS}= 90% V_{rated}; test duration: 1,000h	IEC 60747-9:2007 and IEC 60747-8:2010: $T_{vj,max} - T_{(Pv)}$; $V_{CE} \geq 0.8\ V_{CE,max}$ (IGBT), $V_{DS} \geq 0.8\ V_{DS,max}$ (MOSFET); V_{GE} = 0 V (IGBT), V_{GS} = 0 V (MOSFET); test duration ≥ 1,000h
HTGB	JESD22-A108D: T_j= 150°C; V_{GS}= ±25V; V_{DS}= 0V; test duration: 1,000h	IEC 60747-9:2007 and IEC 60747-8:2010: $T_a = T_{vj,max}$; V_{CE} = 0 V (IGBT), V_{DS} = 0 V (MOSFET); $V_{GE} = V_{GE,max}$ (IGBT), DUT switched off; $V_{GS} = V_{GS,max}$ (MOSFET), DUT switched off; test duration ≥ 500h (100% DUTs) or ≥1,000h (50% DUTs)
H3TRB	EIAJ ED-4701/100-102: T_a= 90°C; RH= 90%; V_{GS}= 0V; V_{DS}= 65% V_{rated}; test duration: 1,000h	IEC 60749-5:2003: RH=85%, T_a=85°C (constant); V_{GE} = 0 V (IGBT), V_{GS} = 0 V (MOSFET); $V_{CE} = 0.8 \cdot V_{CE,max}$ (IGBT), max. 80 V; $V_{DS} = 0.8 \cdot V_{DS,max}$ (MOSFET), max. 80 V; test duration ≥ 1,000h (switched off)
TC	EIAJ ED-4701/100-105: $T_{stg,min}$ = -50°C (10min); $T_{stg,max}$ = +150°C (10min); V_{DS}= 0V, V_{GS}= 0V, N_c = 1,000	IEC 60749-25:2003: $T_{stg,min}$ = -40°C; $T_{stg,max}$ = +125°C; T_{change} < 30s; t_{dwell} > 15min; N_c > 1,000

Package related, overstress failure modes

The main causes of package-related overstress failures are:

- **Mechanical shocks and stresses**

Vibration accelerates the bonding lift off or solders cracks phenomena combining with other constraints. If the terminals or pins are subjected to stress from a large external force or vibration, the internal electrical wiring of the product could be destroyed. Figure 32 shows an example of mounting a gate drive printed circuit board (PCB) on top of the IGBT module. As shown in 32a, if the gate drive printed circuit board is mounted without clamping, any vibration could cause flexing, stressing the module pins and causing or internal electrical wiring damage.

Mechanical shock can cause degradation of package's internals, in particular brittle cracking and fatigue crack propagation. Voids or cracks in the dielectric layers compromise voltage blocking capability resulting in voltage breakdown. [17, 30].

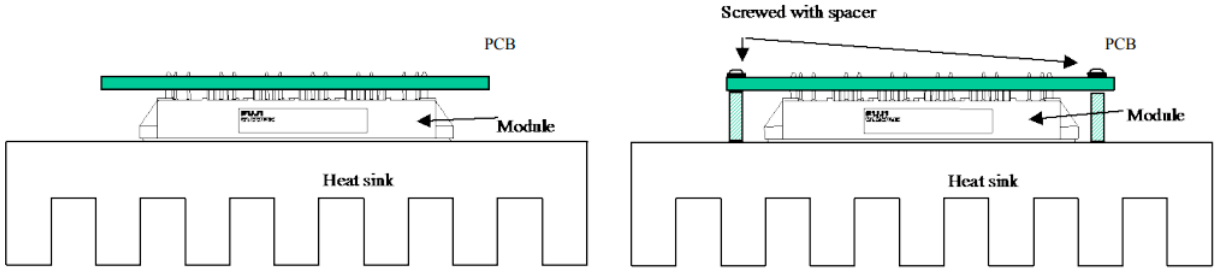


Figure 32. a) Mounting that exposes module terminal to stress. b) Mounting that exposes module terminal to stress-free. [31]

This is particularly important in applications like avionics, where the IGBT modules are subjected to strong combined stresses, and a shock/frequency profile for stress testing is indeed well established [31].

- **Brittle cracking and fatigue crack propagation**

The brittle materials used in advanced IGBT multichip modules are the single crystal silicon, the thin insulating layers on it, and the ceramic substrate. One among the main assumptions in fracture mechanics of brittle materials is that the sharp stress concentration at pre-existing damages leads to the rupture under the influence of external mechanical stresses. Ultimate brittle fracture can occur suddenly without any plastic deformation, when an initial crack is present, whose length exceeds a critical size, which is a characteristic of every brittle material. Failures due to brittle cracking are usually observed immediately after mounting or powering the device. However, even if the initial crack does not reach the critical length, it can develop by fatigue crack propagation under the influence of the applied stresses, until the threshold for brittle fracture is exceeded.

Mechanical stresses can amplify pre-existing defects, originated for example by processing problems (e.g. during dicing), by assembly problems (e.g. hard wire bonding), or by soldering (e.g. voids in solder alloys). Figure 33a shows a notch on the bottom side of an IGBT chip, which has been caused during diamond sawing of the silicon wafer. Different sources of stress are present, which can lead to brittle failures. One among these is the bending stress, which arises while mounting modules with a bowed base plate onto a flat heat sink. Fig. 33b shows an unusual horizontal crack in the sub-surface region of an IGBT chip, which developed very likely as consequence of the peeling stress arising when mounting a module with an excessively convex base plate.

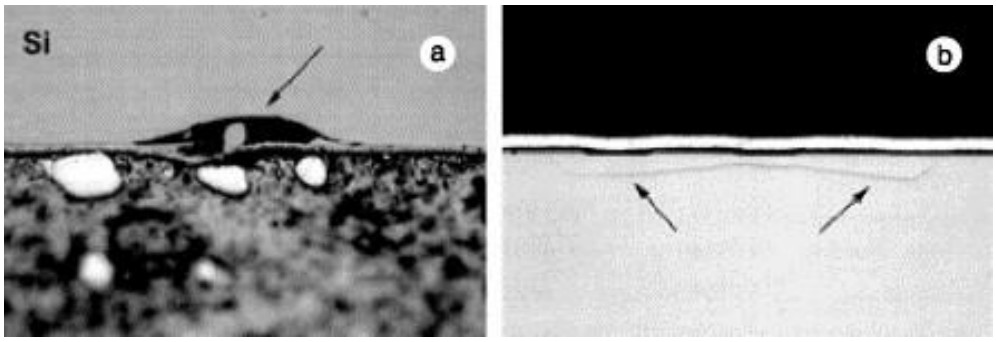


Figure 33. (a) Notch in the silicon chip (micro-section, optical image, 250×). (b) Crack in the silicon chip due to bending stresses in the base plate (micro-section, optical image, 300×).

Fig. 34a shows the vertical cracks caused across an Al_2O_3 ceramic substrate by the horizontal tensile stress produced by the same failure cause as in previous case. In fig. 34b a similar crack propagating from the border of a large void within the solder layer between the ceramic substrate and the base plate is represented. Cracks across the ceramic substrate are particularly insidious because they can transform with time into insulation failures, which can dramatically impair the partial discharge withstanding properties of a multichip module.

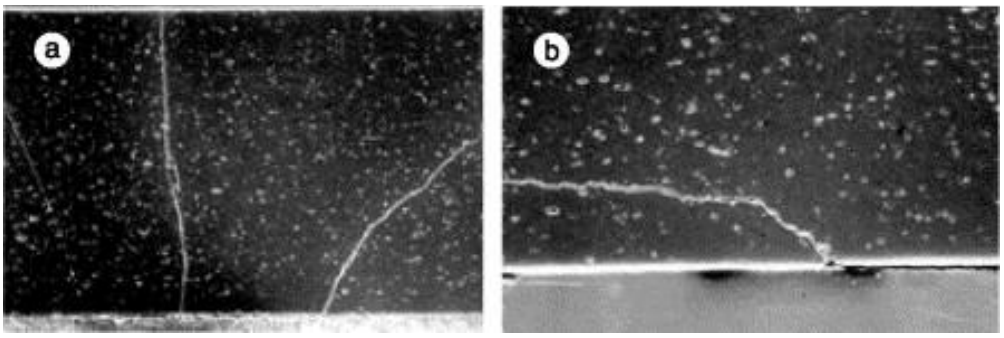


Figure 34. (a) Vertical crack within an Al_2O_3 ceramic substrate, due bending stresses (micro-section, SEM image, 400×). (b) Crack within an Al_2O_3 ceramic substrate initiated from an inhomogeneity in the solder layer (micro-section, SEM image, 600×).

Due to the conservative design of the compliant layers, brittle cracking of the silicon chip and of the ceramic substrate due to thermo-mechanical mismatch only is unusual in advanced IGBT multichip modules.

- **Thermal shocks**

Extreme thermal shocks, where the thermal transient can be so fast that it cannot be followed by the stress relaxation through the plastic deformation of the compliant layers could initiate and propagate a fracture.

This kind of pre-damage is usually introduced during the bonding phase of the emitter bond wires, due to uncalibrated bonding tools. Pre-damaged modules often pass the final production tests, since the device does not exhibit any anomalous characteristic. Due to the thermal and thermo-mechanical stresses, which arise during operation, the microcrack in the polyoxide propagates, leading to a current leakage between the gate and the emitter, and thus to an early failure. A glaring example of this type of situation is shown in figure 35, in which a defect, which may exist even before starting operation, is visible only through specific inspections and when fault is already occurred. Fig. 35 illustrates one among the most insidious cases of fatigue crack propagation leading to a latent short circuit between gate and emitter. When the liquid crystal microthermography has been performed before removing the bond wires, no hot spot could be detected, even at high levels of power dissipation. After careful removal of the emitter bond wires (but one) the failure mode was unaffected, but a hot spot has been found within the footprint of a bond wire (Fig. 35a). Selective etching of the metallization (Fig. 35b) revealed a damaged polyoxide with traces of interdiffusion between aluminum and polysilicon.

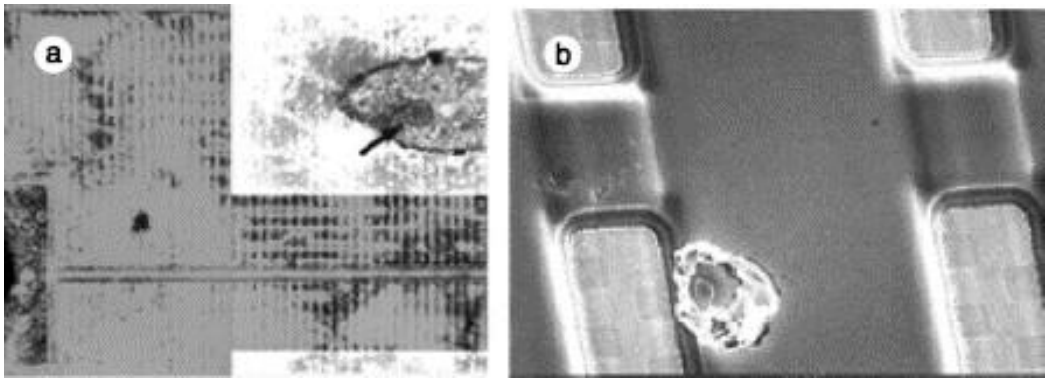


Figure 35 (a) Localization of a leakage path between emitter and gate by liquid crystal microthermography (80×). (b) The hot spot is located below an emitter bond wire, and it is due to a mechanical damage of the polyoxide (SEM image 500×).

- **Burnouts due to flashovers**

The phenomenon of burnout is the same as the one previously described too. It may be due to different causes. One of these is flashover, which refers to electrical discharges in the insulation of the IGBT. They are more common in humid and contaminated environments [14], [15].

Package related, wear-out failure modes

The main causes of wear-out package-related failure modes are:

- **Thermo-mechanical fatigue**

In normal operation, IGBTs keep switching between on and off states. Conduction and switching power losses associated with IGBT operation generate pulsating heat flux at the chip (junction). The repetitive heating and cooling of the junction results in temperature cycling. This temperature cycling caused by actively heating and cooling of the junction is called power cycling, while temperature cycling due to passive heating and cooling is called thermal cycling. The heat flux produced at the junction flows through the thermal path across the different layers of the IGBT module towards the case (or heat sink).

The IGBT consists of multiple layers of different materials, and since each layer has a different thermal conductivity and capacitance, a temperature gradient along the thermal path takes place. At the junction, average and the peak-to-peak temperature fluctuations are higher than that at the case. The thermal capacitance along the thermal path has a filtering effect on high frequency temperature fluctuations. Temperature fluctuations along the thermal path cause repetitive expansion and contraction of the layers forming the path. The difference in the coefficient of thermal expansion (CTE) between adjacent layers in the package cause them to expand differently. Shear stresses are exerted on interfaces between different material layers, causing deformation at the intersection of the two different materials, that includes cracks, empty holes, etc. These stresses result in thermo-mechanical fatigue of material layers of the package.

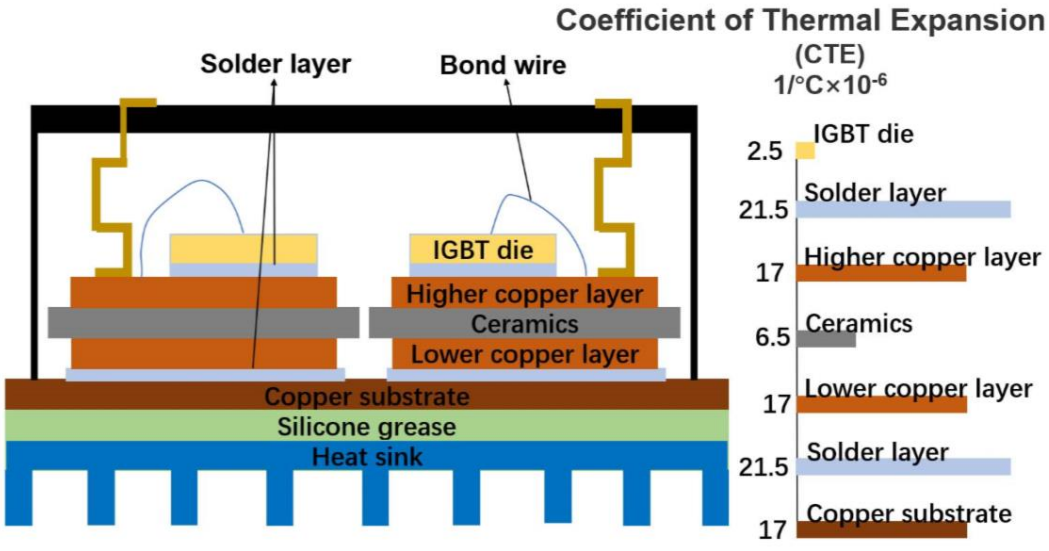


Figure 36. IGBT structure and coefficients of thermal expansion of each layer with different materials. [32]

As shown in fig. 36, the package structure of the IGBT and the thermal expansion coefficient of each layer, wherein the differences between the thermal expansion

coefficients of each two adjacent materials of the IGBT and the thermal expansion coefficient of solder layer is the largest, and theoretically, the deformation caused by the heat is most likely to occur. This in turn affects the life of the device. According to [33], even a package with identical CTE values in each layer would not be stress-free in the presence of a temperature gradient. It is impossible theoretically to design a stress-less package for the whole range of operation conditions. However, it is possible to optimize the selection of the materials properties of the adjacent layers to reduce stresses according to application requirements. New interconnection and soldering technologies have been proposed by IGBT module manufacturers to improve long-term reliability of the module, not producing stress-free modules but with the aim of postponing the onset of degradation caused by thermo-mechanical fatigue beyond application lifetime requirement, given the operating conditions.

- **Thermomechanical creep**

In mechanics of materials, the term creep indicates the inelastic deformation process in presence of a constant stress over time. Creep is a phenomenon that requires a high temperature and a stress, which provides the directionality of deformation process. Creep is thermally activated, i.e. it occurs in a material only if a specific value of the homologous temperature is exceeded. Homologous temperature is defined as the ratio between the temperature of material and its melting temperature. There are three creep mechanisms, which are referred to as diffusion, gain boundary sliding, and dislocation creep in action. Each of these mechanisms is activated depends on certain factors including temperature. Thermo-mechanical creep, caused by high operating temperature, leads to weakening of the mechanical strength of different package layers. This accelerates the process of cracks and voids formation [17],[34].

Creep and thermomechanical fatigue result in bond-wire cracks and lift-off, delamination and cracking of solder layers, and degradation of chip metallization, that cause failures of IGBT modules in the long run.

- **Metallization reconstruction**

During thermal cycling of IGBT devices and of freewheeling diodes, periodical compressive and tensile stresses are introduced in the thin metallization film by the different CTEs of the aluminum and of the silicon chip. Due to the large thermo-mechanical mismatch between both materials and due to the stiffness of the silicon substrate, the stresses, which arise within the aluminum thin film during pulsed operation of the device can be far beyond the elastic limit. Under these circumstances, the stress relaxation can occur by diffusion creep, grain boundary sliding, or by plastic deformation through dislocation glide, depending on temperature and stress conditions.

In the case of IGBT devices, the strain rate of the metallization is controlled by the rate of temperature change. Because the typical time constants for thermal transients in IGBT

are in the range of the hundreds of milliseconds, if the devices are operated cyclically at maximum junction temperatures above 110 °C, the stress relaxation occurs mainly by plastic deformation at the grain boundaries. Depending on the texture of the metallization, this leads either to the extrusion of the aluminum grains or to cavitation effects at the grain boundaries.

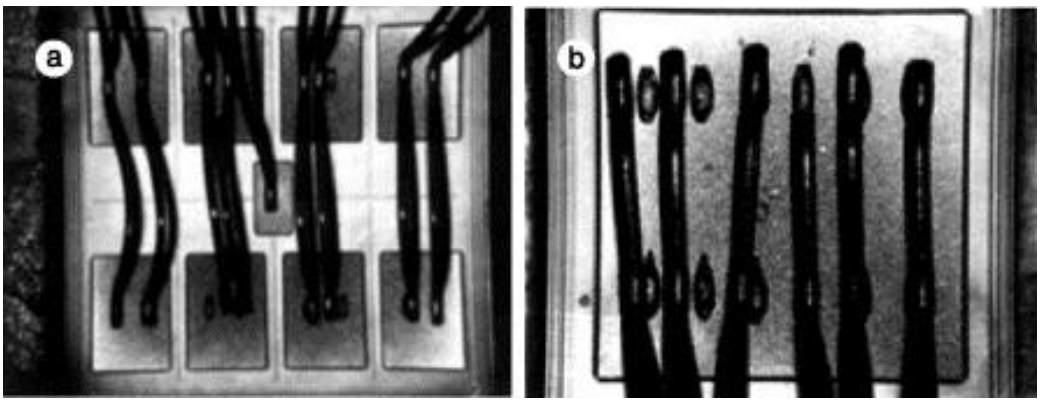


Figure 37. a) and b) metallization of an IGBT and of a freewheeling diode after reconstruction. In optical images reconstructed regions look dark, because of the light scattering due to the surface roughness.

Reconstruction is more evident at the center of the chip, where the junction temperature reaches its maximum, while surface reconstruction is negligible in those peripheral regions of the chip, where the maximum junction temperature does not exceed 110 °C. Fig. 1.37b shows that surface reconstruction sometimes occurs as a secondary mechanism in conjunction with bond wire lift-off. In fact, after release of the bond wires on the left side of the diode, the (pulsed) current has been carried by the bond wire on the right side only, by leading to an increase of the local temperature with consequent reconstruction of the metallization.

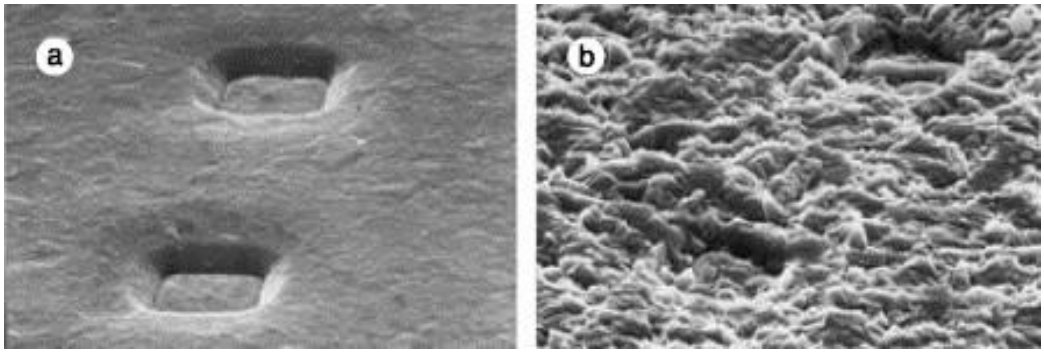


Figure 38. The emitter metallization of a virgin IGBT chip (a) is compared with that of a similar device, which survived 3.2 million of cycles between 85 and 125 °C (b).

After stress, it can be seen that non-columnar aluminum grains are extruded from the thin film surface, while voids are present at the boundaries of larger grains. In field failures turning into a destructive burn out of the device, aluminum reconstruction may be less evident, due to remelting of the metallization as consequence of the high-temperature levels that can be reached. In any case, aluminum reconstruction reduces the effective cross-section of the metallization and results into an increase of the sheet resistance of the aluminum layer with time.

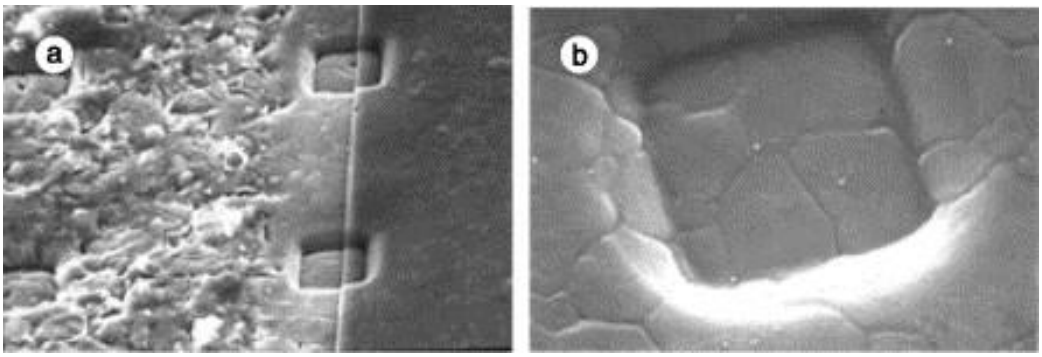


Figure 39 (a) and (b) effects of compressive layer on aluminum reconstruction.

Figure 39a shows the role of a compressive layer in suppressing reconstruction phenomena in aluminum layers. In fact, after selective removal of the polyimide passivation, it can be clearly seen that this overlayer has almost inhibited the extrusion of metal grains in the center of the image. Therefore, the use of compressive overlayers can be considered an effective countermeasure for controlling the increase of the sheet resistance of metallization layers submitted to large temperature swings.

Figure 39b shows a close view of the aluminum metalization at an emitter contact that has been coated with a compressive layer and then power cycled with a maximum temperature of 125 °C. As expected, no reconstruction occurs. However, one can clearly see that the grain boundaries have been depleted as a consequence of cavitation effects.

- **Solder degradation**

In the IGBT module structure, there are a chip solder layer and a substrate solder layer. The solder layer of the chip connects the chip and the copper layer on the DBC and is more susceptible to failure due to a greater temperature shock. At the interface constituted by solder between the ceramic substrate and the baseplate, especially in the case of copper baseplates, we find the worst mismatch in the CTEs, the maximum temperature swing combined with the largest lateral dimensions, therefore it is a critical interface too. In a general way, failure of the solders in IGBTs is co-determined by three factors or micro-defects: voids, cracks and delaminations.

- **Solder voids**

Both solder layers are affected by voids, which usually appear as unwanted defects during solder formation process. Voids can interact with the thermal flow and with the crack initiation within the solder layer.

From the study on effects of solder voids [35], it is assumed that in a healthy layer the heat is diffused downward from the center to the periphery and the temperature is gradually reduced. In the case of voids in the solder layer, the maximum junction temperature of the chip increases significantly, the highest junction temperature appears above the void, and the temperature gradient increases at the void. Furthermore, since the heat flow within an IGBT module is almost one-dimensional, when a relatively large void is present in a solder layer, the heat must flow around it by creating a large local temperature gradient such that the heat dissipation performances of the assembly are degraded. On the contrary, if the large void is broken up into many smaller voids, the perturbation to the heat flow is less evident and has a much smaller impact on the overall thermal resistance of the multilayer.

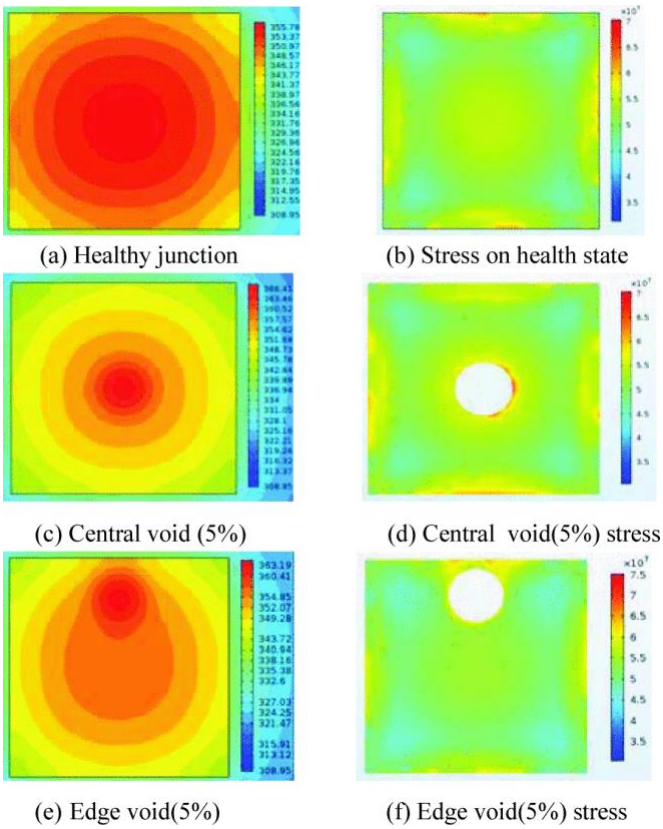


Figure 40. Heat flow and stress simulations with different size of voids. [35]

In the void free layer, the edge stress is significantly higher than the inside of the solder layer and the voids cause an increase in the stress at the edge of the void, which is close to the maximum stress, (limit stress based on Von Mises criterion). The higher the

temperature, the more easily the void expands to the periphery. Due to the solder layer process, randomly distributed small voids were inevitable when the solder layer was formed. As the solder layer ages, the small voids gradually expand, and the voids in adjacent locations become fused, causing the void to grow faster. Many small voids tend to merge, reducing their number but forming a bigger void.

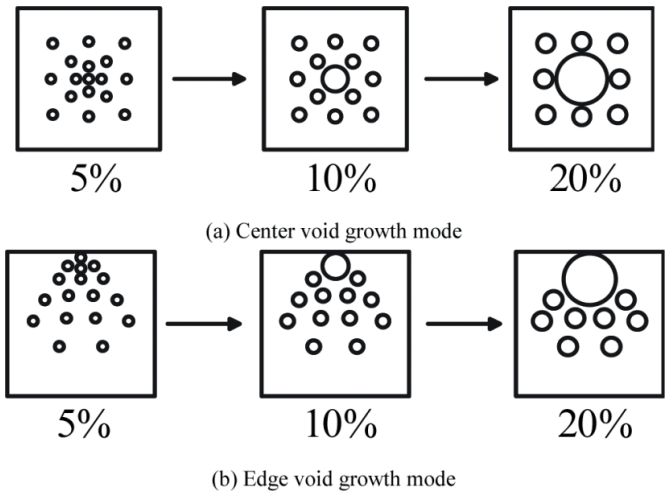


Figure 41. Effect of ageing on solder voids

Besides the size of the voids, another important aspect is their location inside the solder layer. In the IGBT chip, the heat at the center of the chip is the highest, and the heat transferred downward is also the most. Therefore, the voids appearing in the center of the solder layer have the greatest hindrance to heat transfer and have the highest influence on the junction temperature. This is true at the initial stage of void growth, in fact no considerable differences between voids in different positions are observed at the end of the void fusion process.

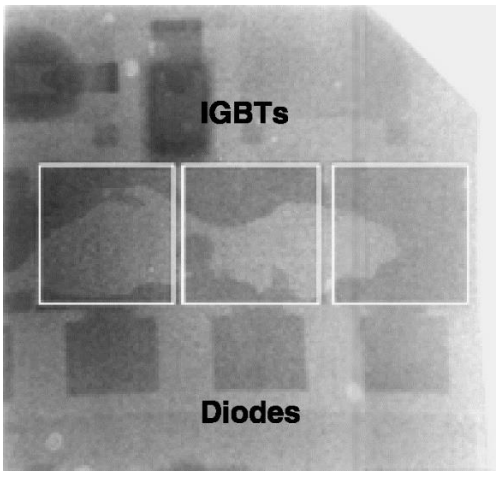


Figure 42. X-ray microscopy image of an IGBT module, which shows a large void immediately below three IGBT chips (0.8×). The void is located in the die attach layer. [17]

Since IGBT are vertical devices the die attach has to provide at the same time an efficient thermal and electrical conduction path. Therefore, the most insidious voids within the die attach are those, which hinder the thermal flux to the heat sink without inducing any noticeable reduction of the current distribution within the semiconductor. They are for instance edge cracks or shallow voids and delaminations at the interface with the ceramic substrate.

Both gross voids and extended fatigue-induced cracks can have detrimental effects on dissipating devices. In fact, they can significantly increase the peak junction temperature of an IGBT or of a diode and therefore accelerate the evolution of several failure mechanisms including bond wire lift off and solder fatigue. Although steps are made to avoid the formation of gaseous inclusions and the growth of voids, the quality of solder joints is a critical point of the assembly and packaging processes.

- **Solder fatigue**

Solder degradation either takes the form of solder cracks or solder delamination. A recent analysis on evolution of micro-defects in lead-free solder alloys [36] states that voids, cracks of Sn-Ag-Cu (SAC) alloys and detachment of Si/SAC interfaces are three major micro-defects in the die-attach solder.

Solders were often modelled ad a single homogeneous phase, but they are constituted of more phases. Fig 43b shows the cross section of IGBT modules by scanning electron microscope (SEM). It demonstrates that the die-attach solder is mainly composed of ß-Sn phases. A large number of voids, whose size range from a few microns to hundreds of microns, and intermetallic particles (second particles) are also found. Voids mainly result from the reflowing process and can be classified as the birth defects. Intermetallic particles (red dotted circles in Fig. 43b), such as Cu_3Sn, Cu_6Sn_5 and Ag_3Sn, are dispersed inside the ß-Sn matrix. There is also an intermetallic compounds (IMCs) layer with the thickness of about 5 μm between the die-attach solder and Si-chip.

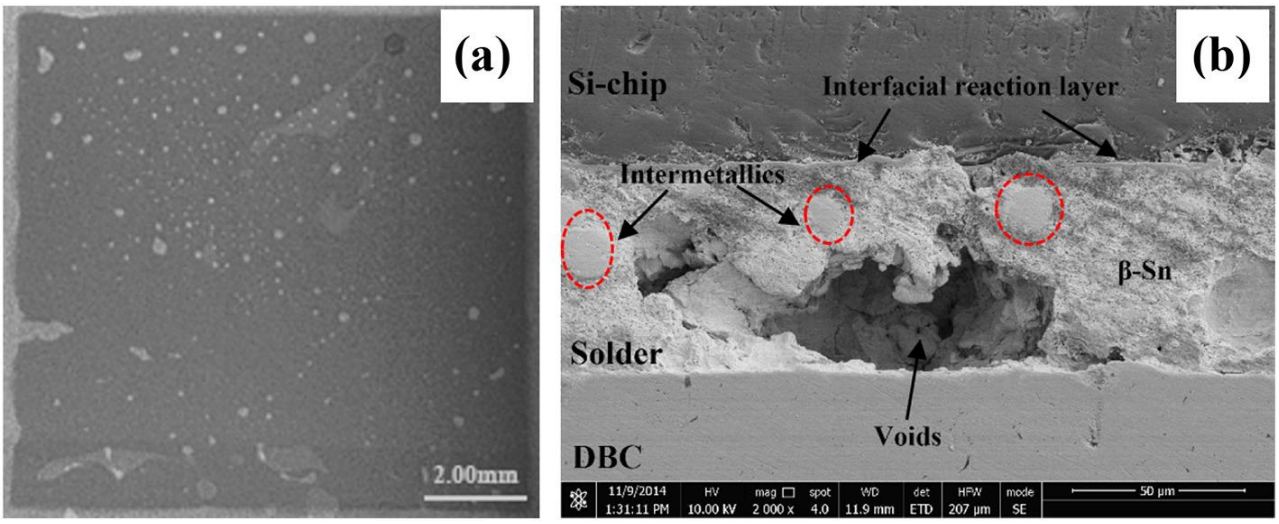


Figure 43. Microstructure in the die-attach solder of IGBT modules before power cycling: (a) X-ray image, (b) SEM image of cross section.

After a power cycling stress test conducted in [36] the void basically remains unchanged, but two micro cracks have initiated from the void edges and propagated along the horizontal direction. Moreover, the Si/SAC interface near the void was peeled-off (as showed in figure 44). Voids in the die-attach solder usually cause a local increase of stress (stress concentration) where the viscoplastic deformation of SAC alloys is far higher than other regions. Fatigue cracks are vulnerable to initiate and propagate near these high stress regions. This result demonstrates that voids in the solder may act as one kind of sources for fatigue cracks.

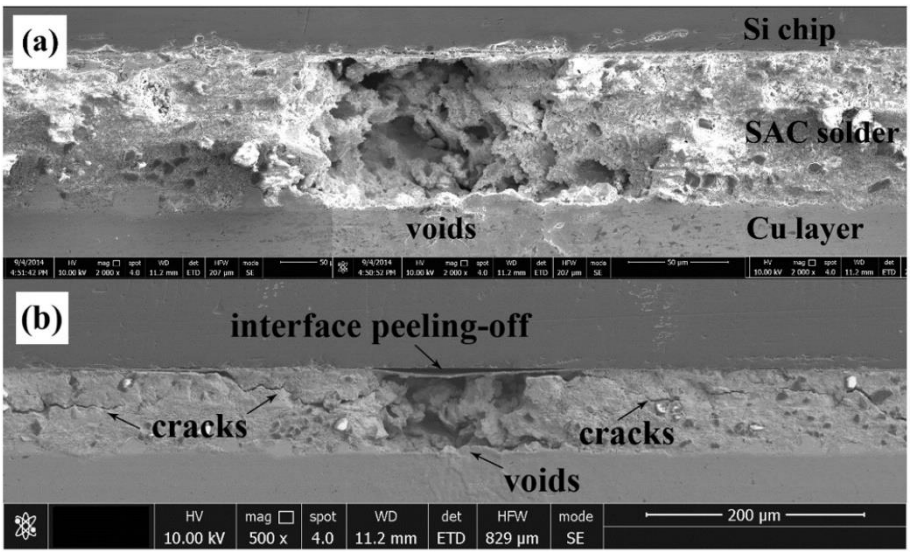


Figure 44. Morphology of the cross section of IGBT modules before and after power cycling: ΔT_j = 100 °C, t_{on}/t_{off} = 1.00 s/1.00 s, $T_{j\_average}$ = 100 °C, (a) 0 cycles, (b) 10000 cycles.

Cracking of SAC alloys and detachment of Si/SAC interfaces are dominant failure mechanism of die-attach solder under different conditions. The reason is attributed to difference in thermal/mechanical properties of materials (SAC alloys and Si/SAC interfaces). SAC alloys are one kind of metal materials with low melting point, low yield strength, high ductility, while intermetallic particles (second phase of material) have opposite characteristics.

Due to the lower recrystallization temperature (in a range from −100 °C to −30 °C), the viscoplastic deformation of SAC alloys happens under normal service temperature of IGBTs. Therefore, under ordinary thermal stress SAC solder alloys accumulate a large amount of viscoplastic strain energy. When it exceeds the critical value, microcracks would initiate from SAC alloys, in particular in the weakest zones, i.e. near the void and intermetallic particles. These micro-cracks keep propagating with the increase of power cycles and would converge into a large crack until failure of materials.

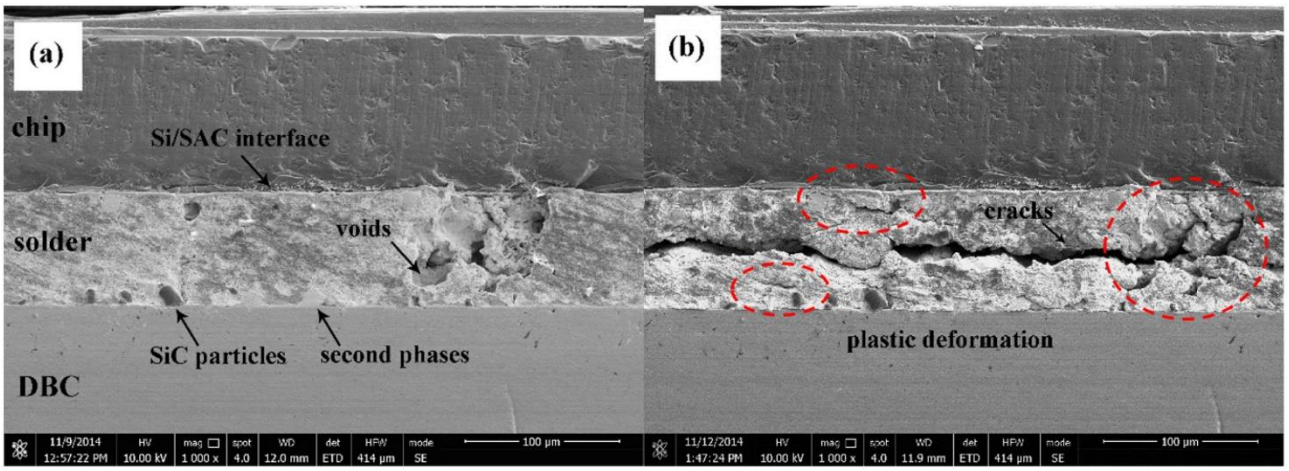


Figure 45. Morphologies of die-attach solder before and after power cycling: ΔT_j = 40 °C, t_{on}/t_{off} = 2.00 s/2.00 s, T_j = 50 °C – 90 °C. (a) 0 cycles, (b) 750000 cycles.

After 750000 power cycles, a large size crack has initiated from the edge of void and propagated horizontally inside the die-attach solder (Fig. 45b). SAC alloys near the void and intermetallic particles are also severely plastically deformed (red dash cycles). Some micro-cracks have initiated near these severe plastic deformation regions. This result indicates that cracking of SAC alloys is the root cause for fatigue of the die-attach solder under conventional power cycling.

As mentioned above, thermal/mechanical properties of Cu-Sn intermetallic compounds are quite different from ß-Sn phases. When the cyclic thermal stress is lower than the bonding strength of Si/SAC interfaces, it throws a rather limited adverse effect on the microstructure and mechanical properties of Si/SAC interfaces, because the IMCs layer gives Si/SAC interfaces high fracture strength and low ductility, so they aren't affected by plastic deformation, to which ductile materials are prone.

When the thermal stress is between the yield strength of SAC alloys and the bonding strength of Si/SAC interfaces, the viscoplastic deformation of SAC alloys is the unique

mechanical process to the die-attach solder and fatigue cracking of SAC alloys is the dominant failure mode for die-attach solder. However, once the thermal stress exceeds the bonding strength of Si/SAC interfaces, their detachment becomes the dominant failure mode because fracture cracks would propagate along the Si/SAC interfaces at a very fast rate, much faster than fatigue cracking of ductile materials.

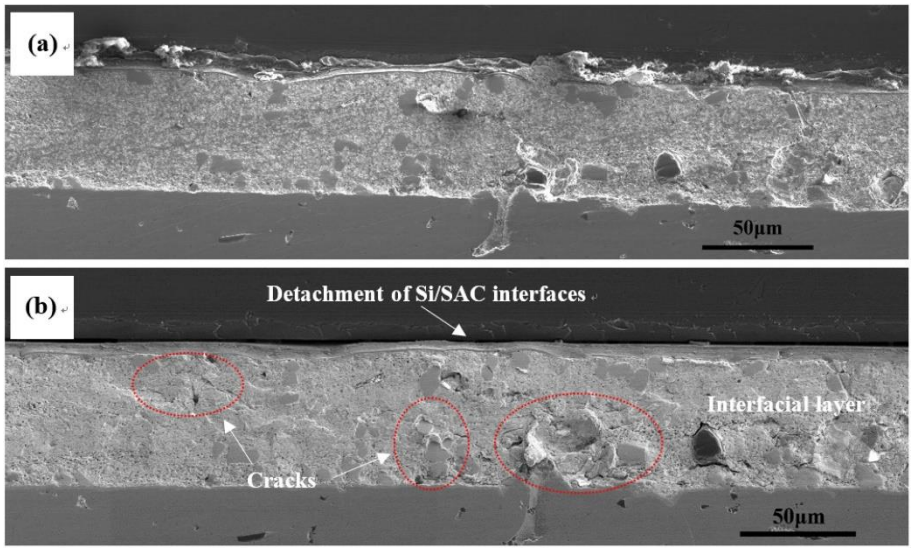


Figure 46. Morphologies of the cross-sectioned IGBT module before and after pulse high current cycling: ΔT_j = 120°C, T_{jm} ~ 110°C, t_{on}/t_{off} = 0.02 s / 2.98 s, (a) 0 cycle, (b) 3000 cycles.

To conclude the analysis on solder layer fatigue, in can be stated that voids are one kind of birth defects and could accelerate the evolution of cracks and interface detachment, which belong to the acquired defects under periodic thermal stress. Cracking of SAC alloys is the dominant failure mode under conventional power cycling and delamination of Si/SAC interfaces turns to be the dominant failure mode under pulsed high currents cycling, for example electrical transients or thermal shocks.

Transverse cracks or interface detachment deflect the heat transferring path and remarkably increase the junction-to-case thermal resistance. Some simple design rules for minimizing the fatigue of solder joints, derived from simulations and models of this failure mode, are reducing the size of the solder joint, matching the CTE of the materials, reducing the edge voids, and increasing the thickness of the solder (compatibly with the requirements imposed by the thermal resistance).

Other common causes of wear-out package-related failure modes are:

- **Electro-migration**

Electro-migration is the process of transportation of metal ions at a certain temperature due to electrical current and can cause failure in interconnect lines and metallization layers of integrated circuits through the formation of voids and hillocks. [37]

- **Corrosion**

Corrosion of aluminum is a well-known failure mechanism since the early times of microelectronics. When pure aluminum (e.g. bond wires) is exposed to an oxygen containing atmosphere, a thin native Al_2O_3 surface layer is grown that passivates the metal. Aluminum is self-passivating also in pure water, where the aluminum oxide is converted into a hardly soluble layer of aluminum hydroxide $Al(OH)_3$.

Galvanic corrosion of those passivation layers has been observed on the metallic components of a module. The identification of the exact mechanisms promoting corrosion in IGBT multichip modules is a quite complex issue, since several causes may concur to the failure. In fact, IGBT packages might face multiple contamination sources, with different metals and alloys, temperature gradients, as well with static and periodic mechanical stresses. Furthermore, the active devices and the bond wires are embedded in gel or resins, whose influence on the corrosion is not completely understood.

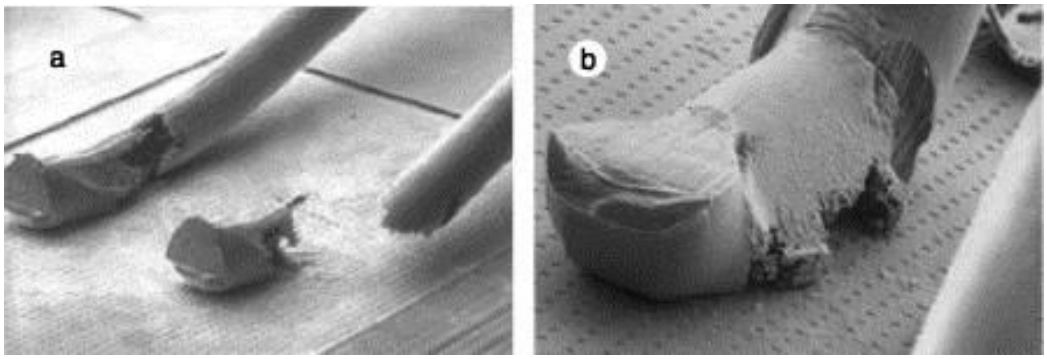


Figure 47 shows aluminum bond wires with no strain buffer that have been corroded at different grades during power cycle tests, which lasted over one million of cycles. [17]

In this example, the corroded areas were mainly located at those sites of the bond where the wire suffered the most severe deformation: at the heel of the bond wire, and at the top of the wire loop. These corrosion events have been observed to occur in conjunction with the local formation of gaseous inclusions within the silicone gel (Fig. 48b) that can

be sometimes noticed during high-temperature operation of the devices. These gaseous inclusions are dangerous because they might give rise to partial discharges.

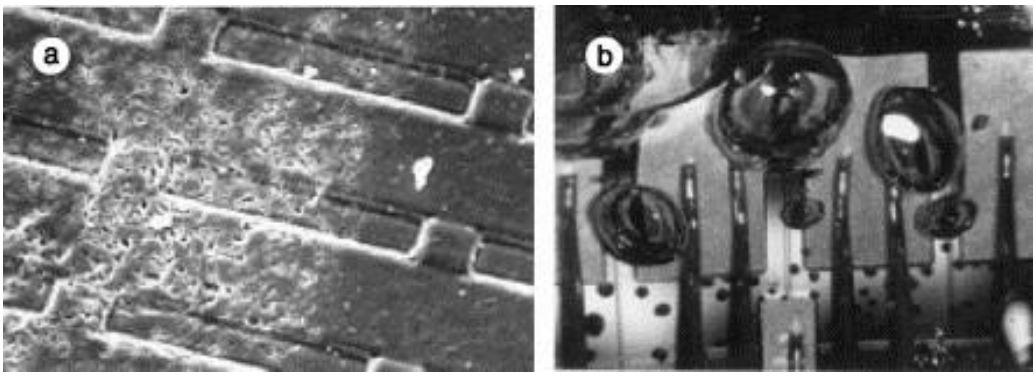


Figure 48. (a) Corroded emitter bond pad close to an emitter bond wire (SEM image, 160 x). (b) Formation of gaseous inclusions into the silicone gel during power cycling (optical image, 8 x). [17]

The absence of reaction by-products and the corrugated surface of the corroded bond wires leads to the conclusion that the observed bond wire corrosion is strongly correlated with the mechanical stresses, which arise either due the thermo-mechanical cycling, or due to residual deformation stresses in the bond and may indicate that the corrosion occurs at the grain boundaries of the aluminum. In summary, these indications are compatible with the stress corrosion failure mechanism.

Recently, the incidence of this failure mechanism has been mitigated by more effective cleaning processes after assembly, by the control of the water content in the silicone gel, and by the use of corrosion-hardened bond wires [17]. Nevertheless, it is very difficult -if not impossible- to prevent or avoid factors like high levels of humidity and corrosive chemicals existing in many industrial applications, e.g. mining, cement, oil and gas, and marine, that may result in corrosion of bond wires accelerating their mechanical degradation, and eventually leading to their rupture.

Partial discharges in IGBT

The only norm concerning partial discharges in IGBT modules is the IEC 61287. The procedure to be performed is as follows. The object under test is pre-stressed with an A.C. voltage ramped up to $1.5 \cdot \frac{U_m}{\sqrt{2}}$ in 10 s, where U_m is the maximum blocking voltage of the module (in r.m.s), and maintained for 1 minute. During this time (t_1) some partial discharges might be observed. The voltage is decreased to $1.1 \cdot \frac{U_m}{\sqrt{2}}$ for a window of 30 s (t_2) and, after 25 s, PDs are recorded. The complete representation of test procedure is displayed in figure 49, in which the time windows of PD measurement is sketched with a red band. Acceptance is based on the measured level of PD as specified by the manufactures. A typical value to pass the test for a component and a subassembly is 10 and 50 pC, respectively. Additional recommendations, related to waveform used, are not listed in the standard.

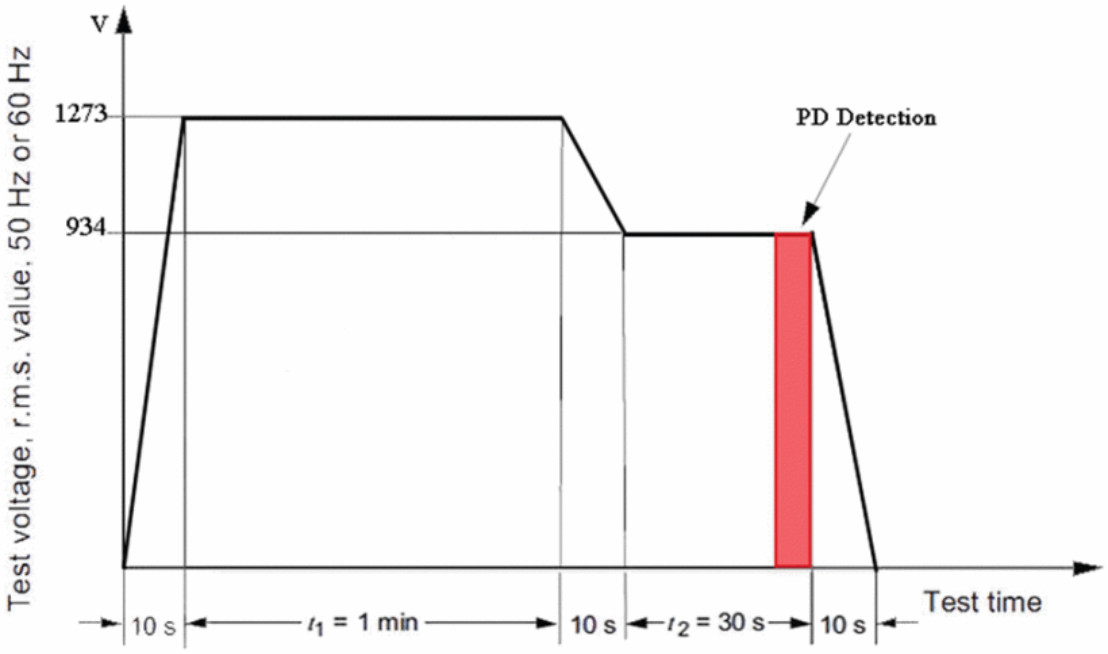


Figure 49. IEC 61287-1 for PD test. Example for sample having U_m equal to 1.2 kV

In [38], it is stated that aforementioned test mainly stresses the ceramic material (the substrate) and not the other types of materials, in particular the bulk of the gel is not adequately tested. This material may present gas filled cavities in its bulk (which may be considered as bubbles in liquid insulation). Moreover, the softness of this type of materials, as regards the impact of PD on it, makes it a key point for the module reliability.

Other methodologies were proposed in addition to this IEC standard. Their aim is to stress all insulation parts and to simulate a more realistic stress condition. The test voltage suggested in [38] is an AC voltage superimposed on a DC one that is directly applied to the

component turned off using a negative gate polarisation. The usage of an inverse DC offset with magnitude greater than the AC peak used as test voltage avoids diode conduction.

[39] performed measurements with PWM power supply and [40] proposes two types of tests with a DC voltage.

They indicate that PD may be observed in power modules for voltage magnitudes lower than the ones obtained during the normalized test. For example, a module might be able to pass the tests suggested by the standard, but not when subjected to PWM stresses, which is a typical IGBT operating condition.

An advantage of AC testing are the so-called Phase Resolved PD (PRPD) patterns. Those are able to reveal a lot of information about the type of defect where discharges occur.

When the pattern is purely symmetric (from a statistical point of view) the discharge is occurring in a cavity whose bounds have the same nature (homogeneous dielectric, for example the gel or the ceramic). Such PD patterns (figure 50) are in general considered to be due to internal discharges occurring in cavity (or cavities) of "the dielectric-bounded" type.

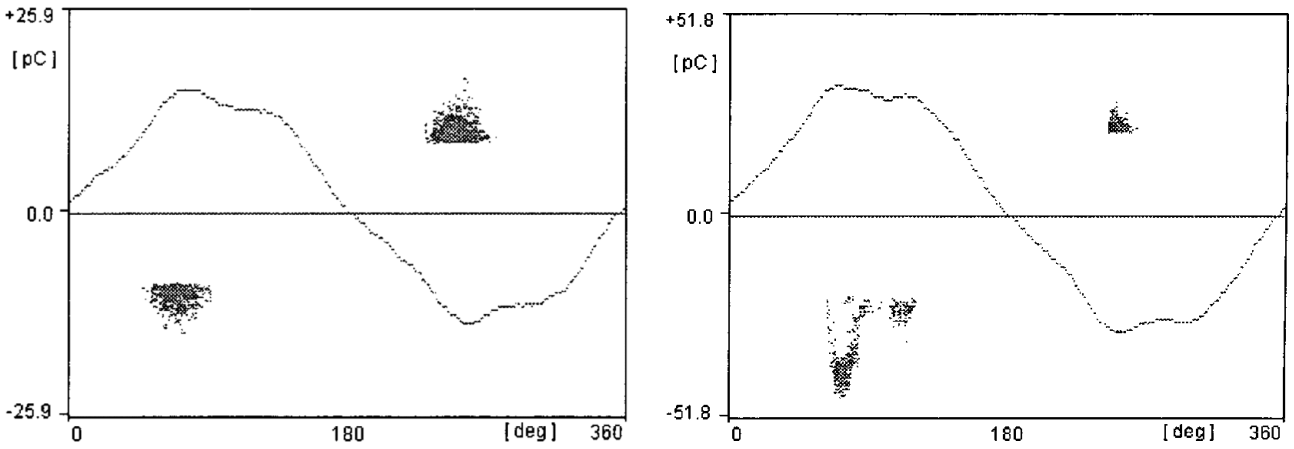


Figure 50. PRPD pattern from [38]

On the contrary, when a difference exists between the number of discharges during the two half cycles, the discharges occur in a cavity whose bounds are not of the same nature (for example gel and ceramic). The extreme case is an asymmetric PD pattern occurring in a cavity of the "electrode-bounded" type. In that case, discharges occur in a cavity whose bounds are not of the same nature (for example a metal and a dielectric, when considering an internal discharge, or to a surface discharge starting from one electrode). In the last two cases the asymmetric behaviour is, from a physical point of view associated to the difference of secondary emission coefficients between the metal and the dielectric, which do not allow to the same quantity of electrons and ions to be injected in the plasma, leading to the difference observed during the two half cycle of the applied voltage.

A classification between different types of PDs in IGBT module was made. The following possible partial discharges can be listed:

- internal discharge in the surface passivation layer (die level)
- surface discharge at the IGBT die and gel interface (die-packaging interface)
- corona discharge at the interface between the bonding wire and gel (packaging level)
- surface discharge at the interface between the DBC and gel (packaging level)
- internal discharge in the gel (packaging level)

For [38] the most probable case is the existence of PD at the interface of the two dielectrics. It is claimed that the interface between the ceramic and the dielectric gel is the main source of discharges, but the interface between the copper of the DBC and the ceramic may also be considered as a second PD source.

It was reported in [41] that the PD of a metallised ceramic in an isolating liquid occurs at the maximum voltages at 90° and 270° and the amount of PD does not rise sharply with increasing voltage. However, for the same metallised ceramic embedded in silicone gel, PD was found at a phase between zero and maximum voltage between 0 – 90° and 180 - 270° and as the number and magnitudes of the PDs strongly increases with rising voltage, it was argued that the origin of this discharge phenomenon is due to discharges at the interface between the silicone gel and the substrate and not due to locally restricted cavities in silicone gel.

When the applied voltage is a PWM type, patterns always show a concentration of the discharge activity on the rising and falling voltage flanks, and no clear information can be obtained from the PRPD pattern.

Finally, in [41] possible solutions to control partial discharges phenomenon were listed. They are:

- Geometrical electric field control. A reduction of maximum electric field values through a modification of module geometry parameters such as sharpness of edges.
- Linear resistive electric field control. Electric field is modified applying functional materials with a specific conductivity on the highly stressed region.
- Non-linear resistive electric field control. Same method as the previous one but with a layer made of a FDC (field-dependent conductivity) material.
- FDP (field-dependent permittivity) stress relieving control. The FDP stress relieving dielectric material is realized through the inclusion of a ferroelectric filler, barium titanate, in the base silicone gel. The ferroelectric filler particles enhance polarisation mechanisms leading to reduce high electrical stresses.
- The use of substrates, which have a better behaviour against PDs.

Since PD activity is clearly able to undermine the reliability of modules, and their inception is strictly linked to the dielectric properties of the insulation system of IGBTs, this work will also attempt to identify a diagnostic marker linked to the aging level of modules, based on PD activity and patterns, when present.

Description of devices under investigation

IGBT modules used in this work are models from the same manufacturer, here named “KE4” and “KT4”. Those modules are rated for a 1.2 kV collector to emitter voltage, and a packaging insulation rated for 4 kV RMS, 50 Hz AC for 1min. The only difference between models is that the “KT4" has shorter response times, therefore slightly better performance in terms of switching speed and switching losses. Each module is composed of two subsystems, in turn consisting of one IGBT and its freewheeling diode in antiparallel. These subsystems are connected in series to create an inverter branch, as shown in the scheme of figure 51.

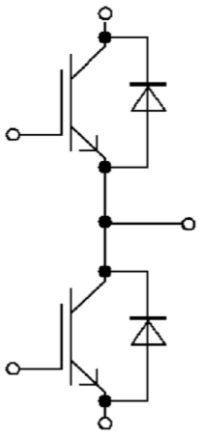


Figure 51. Internal configuration of IGBT modules

Figure 52. External view of incapsulated module with numerated terminals

The IGBT module has 7 terminals, 3 of these are contacts in the central part of the structure while other 4 are lateral pins. Circuit diagram headline of IGBT module is represented in figure 53, taken from component datasheet.

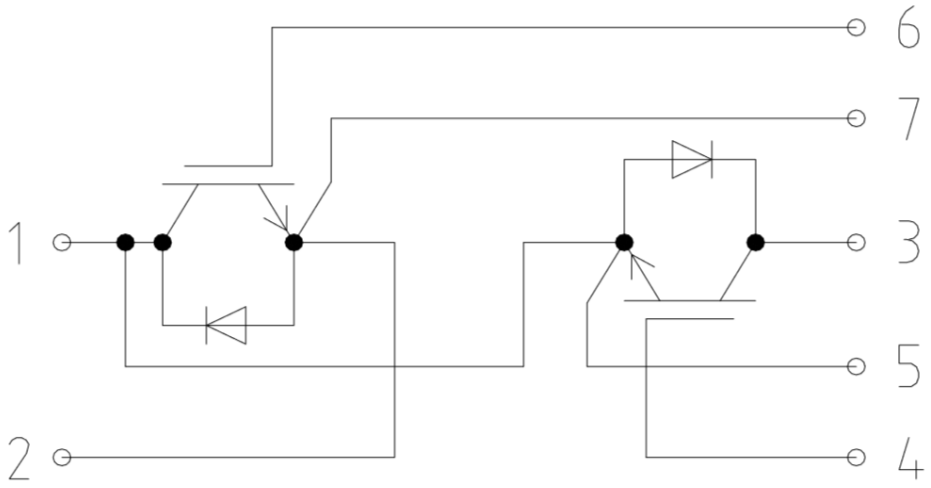


Figure 53. Circuit diagram headline of IGBT module

Terminals of both types of modules are:

Number	Description
1	contact of emitter of upper IGBT and of collector of lower IGBT. It's the output door of the inverter branch
2	emitter contact of lower IGBT. It's the ground voltage input of inverter branch
3	collector contact of upper IGBT. It's the high voltage input of inverter branch
4-5	gate-emitter pins of upper IGBT. They are input pins of driver circuit
6-7	gate-emitter pins of lower IGBT. They are input pins of driver circuit

As can be seen from the circuit diagram (figure 53), terminals 1 and 5 are equipotential, like terminals 2 and 7 too.

54 specimens were tested. They have different characteristics: model, aging period, working conditions, the application in which they were used, etc, that allow to make different classifications to analyse results of the carried-out tests.

Nomenclature and all features of tested IGBTs are summarized in table 15 in the appendix.

Measurements

To investigate behaviour of IGBT modules' insulation with the aim to utilize electrical parameters as diagnostic markers of degradation of IGBT module system, two different types of measurement were carried out, that are:

- measurement of PDIV and PD activity, under different waveforms and temperatures
- measurement of leakage current and conductivity at working temperature

Partial discharges tests

PDIV measurements were performed using different circuits, to test different parts of modules and with different temperatures and voltage waveforms.

Two different strategies were followed in those tests. A first investigation was conducted connecting collector, gate and emitter connectors in parallel to a high voltage source, while the baseplate was grounded (Figure 54), as specified by the IEC norm 61287.

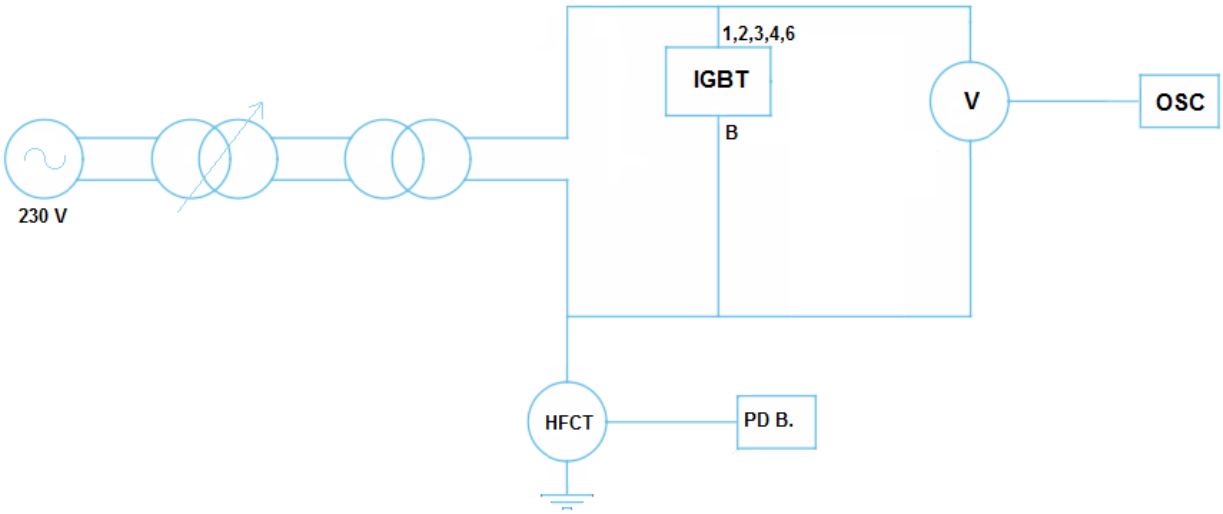


Figure 54 – Testing circuit stressing the DBC plate, following the IEC norm 61287

For each specimen, the tests were performed at ramping peak voltage, up to either the detection of PD activity or the application of a voltage corresponding to 2 kV_{pk}.

Results were fitted to a two parameter Weibull distribution, that is:

$$F(x) = 1 - \exp\left[-\left(\frac{x}{\alpha}\right)^{\beta}\right] \quad (1)$$

where x can consist of PDIV values, α is the scale parameter (corresponding to breakdown voltage probability 63.2%) and β is the shape parameter.

This methodology was followed to address the degradation of the insulation system separating the grounded baseplate from copper regions in the module (DBC plate).

On the other hand, a second option was also investigated, performing the same kind of measurements and postprocessing of raw data on the IGBT chip insulation system and diodes.

This was done stressing the module while connecting the collector to a high voltage source consisting of a DC bias superimposed to and AC voltage, so that a unipolar sinusoidal supply was produced (Figure 55). A bias voltage of -15V was applied to the gate pin to avoid that voltage gate became floating and the IGBT turns on, while the emitter connector was grounded.

Each module features a total of four IGBTs, and this kind of test allowed to test them separately in pairs, distinguishing results for the “Top” and “Bottom” pair being tested (Figures 56 and 57).

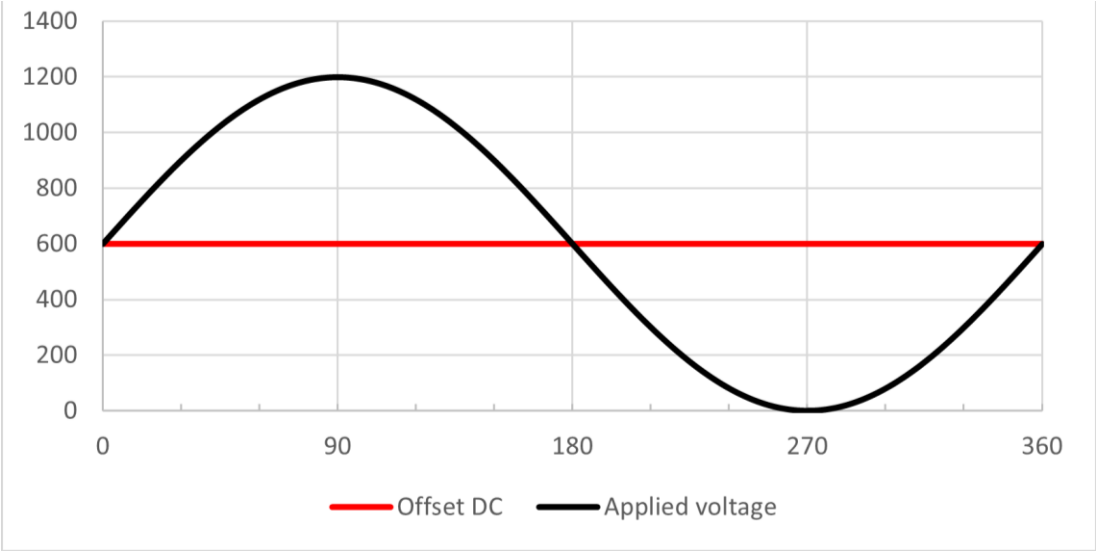


Figure 55 – Unipolar sinusoid applied to single IGBT chip pairs.

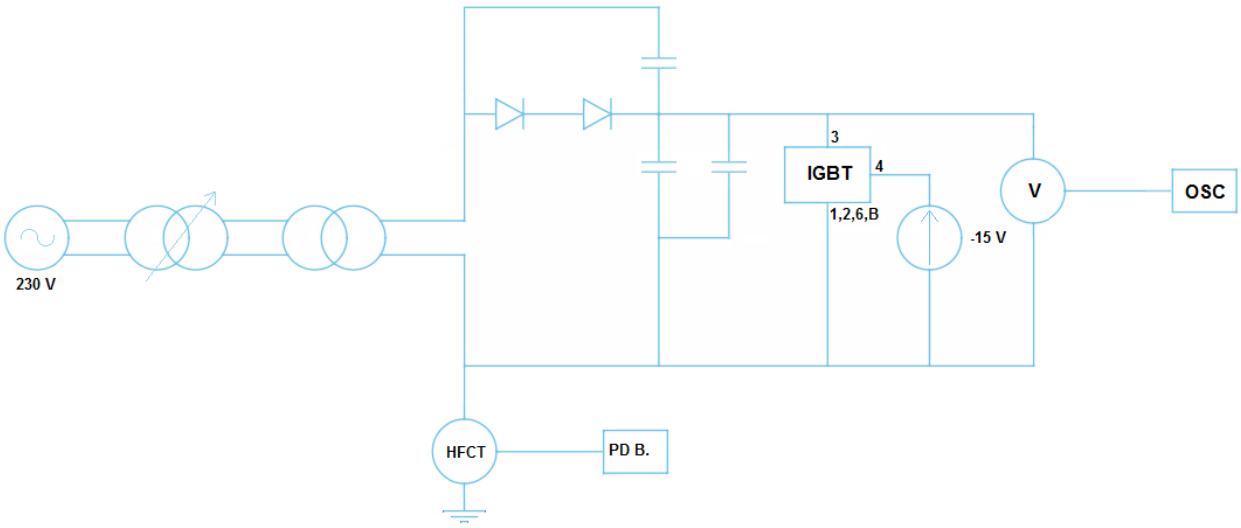


Figure 56. Testing circuit stressing single pairs of IGBT chips: “Top” IGBTs test configuration

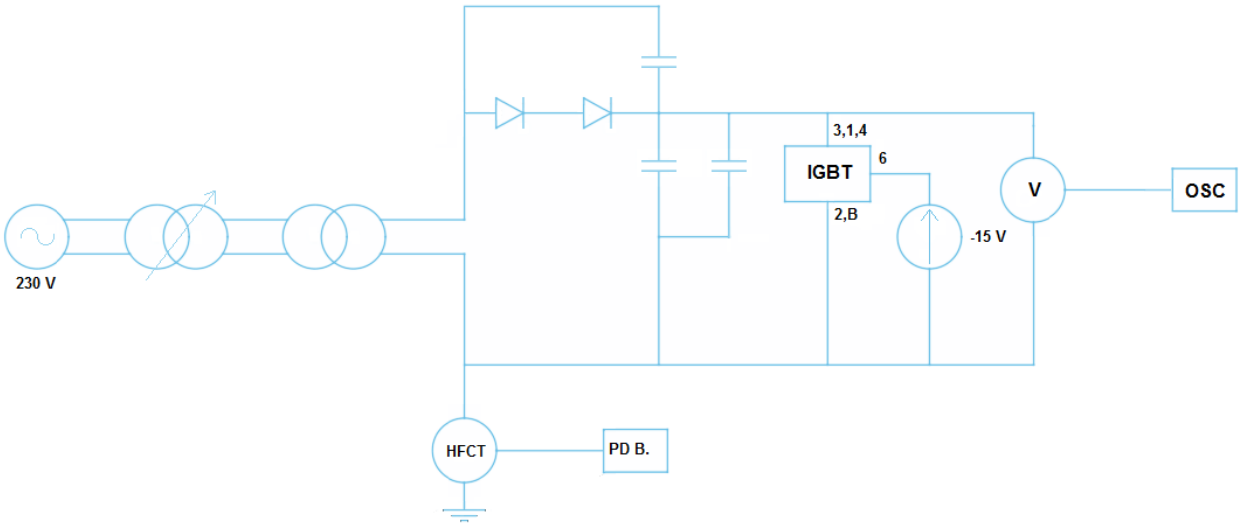


Figure 57 - Testing circuit stressing single pairs of IGBT chips. “Bottom” IGBTs test configuration

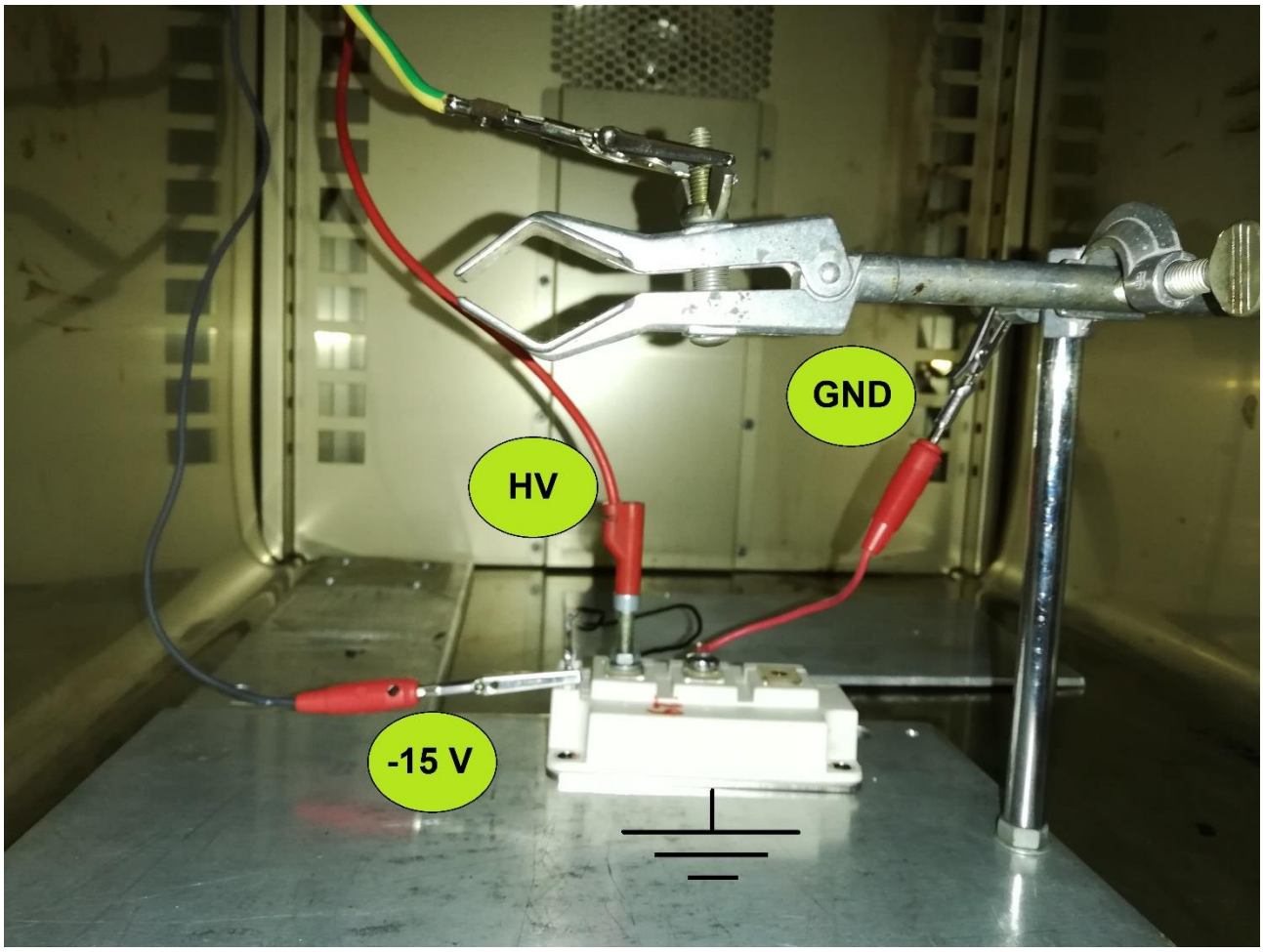


Figure 58 Imagine of a module inside the oven before conductivity test

For each type of set-up 3 PDIV measurements in different conditions are carried out as summarized in diagram of figure 59.

Test 1	Test 2	Test 3
• sinusoidal voltage • room temperature	• sinusoidal voltage • working temperature	• square voltage • working temperature

Figure 59. Conditions of the 3 types of PD test.

Insulation module PD tests

Tests on each module were repeated at least 3 times, and mean values were considered as representative values for the tested specimen. PDIV levels for different sets of modules were fitted to a Weibull distribution, estimating the relevant scale and shape factors for each set of data. The 1% percentile was also extrapolated, in order to highlight potentialities of low-probability inception levels. A better quality of fit might come from fitting data to 3-parameter Weibull distributions, but results would eventually have the same interpretations here observed.

PDIV measurements on DBC plates detected the inception of PD in almost all of the modules, with voltages starting from 1.06 kV_{pk}.

Results are classified in different ways to better investigate data with the aim to find out the existence of possible correlations, which are in the case model, ageing and application.

The following Figures 60, 61, 64 and Table 4 ÷ 7 report the scale and shape parameters of the 2-parameter Weibull distribution fitting measured PDIV values, together with the extrapolation of the 1% percentile, highlighting low (but still significant) probability inception voltages for each set of data.

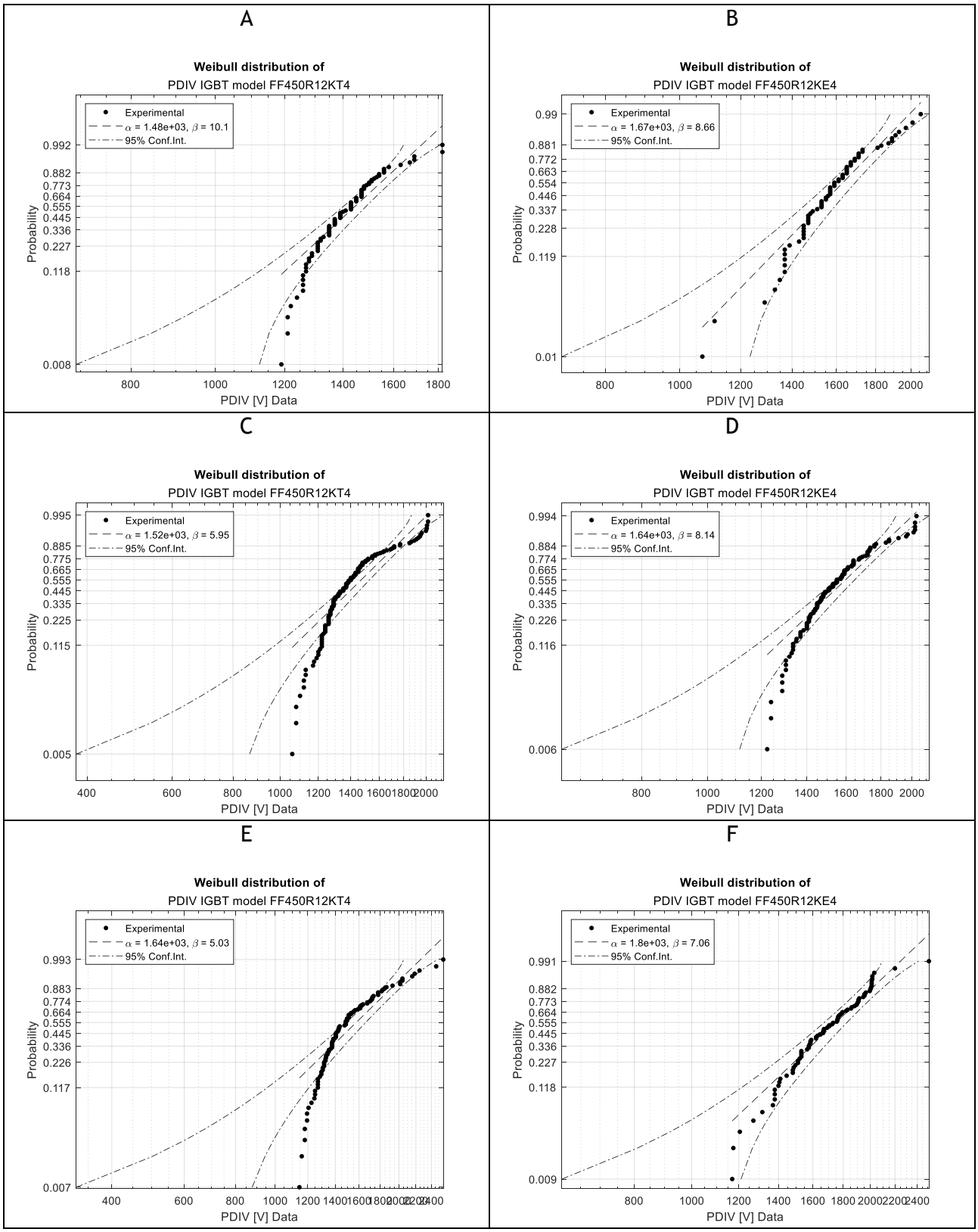


Figure 60. – Weibull plots of results obtained on different models, under different conditions. Model “KT4” (A) TEST 1, (C) TEST 2, (E) TEST 3; Model “KE4”: (B) TEST 1, (D) TEST 2, (F) TEST 3.

Table 4. – Scale and shape parameters and 1% percentile extrapolation of different models tested.

Estimation of the parameters of the Weibull distribution function					
IGBT model	**Voltage**	**Temperature**	**α [V]**	**β**	**PDIV 1% [V]**
KT4	Sinusoidal	Room (20°C)	1476	10.11	936
	Sinusoidal	Working (80°C)	1524	5.95	703
	Square	Working (80°C)	1642	5.03	658
KE4	Sinusoidal	Room (20°C)	1670	8.66	981
	Sinusoidal	Working (80°C)	1638	8.14	931
	Square	Working (80°C)	1803	7.06	939

All the scale factors characterizing both of the modules are above the voltage rating of the samples, and well above the voltage rating of their applications (900 V). However, it must be highlighted that the parameter α is the 63.2% percentile of the failure distribution function (or a reliability of 36.8%). Once a different reliability level is considered (e.g. 99%), the extrapolated 1% percentile of PDIV is much closer to the voltage ratings of the applications those modules are employed in. In particular this value is below 900 V, for "KT4" model at working temperature. This fact implies that, although with a low probability, also in ordinary working PDs may be triggered in a weak point of the insulation. Indeed, this model appears to be the most sensitive to a temperature increase, for which the shape factor β is halfed, going from 10 at 20°C to about 5/6 at 80°C. Results on conductivity also suggest a higher dispersion of data on those models, which might be characterized by a generally increased variability of properties.

On the other hand, the "KE4" model features less dispersed results, and temperature appears to have an overall lower influence on results. It might be possible that this is not an intrinsic property of the manufacturing process, but rather the different working conditions those different models have been operated at during their life, for example with reduced stresses for the "KE4" models.

In general, with the increase of temperature, PDIV tends to increase slightly. This fact may be due to a change in permittivity of the gel. [42] discovered that permittivity of potting materials significantly influences PDIV. If ε of gel enhances electric field difference between gel and ceramic substrate reduces, and consequently the needed voltage to trigger PD increase. For most commercial gels, increase of temperature causes an increase of permittivity, but this enhancement is quite small from 20°C to 80°C, and this relationship isn't valid for all gels. Furthermore, there might also be an influence of the humidity in the gel, which should decrease rising temperature, and therefore also

decrease the gel permittivity, mitigating the predominant beneficial effect of temperature.

Another observation to report is that PDIVs are higher for a square voltage supply than a sinusoidal one. A reason might be in the circuit itself with which the measurement is made. A square wave voltage is supplied by a waveform generator and a high voltage amplifier (Trek 20/20-HS). The latter also generates a lot of noise; therefore the trigger value of the PD detector must be increased with respect of “test 1” and “2” and if first partial discharges had a small amplitude, they wouldn’t be detected. Another difficulty encountered in this type of measure is that the frequency of part of the Trek’s noise was in the same range of the typical spectrum of discharges, so the filtering action had limited effectiveness.

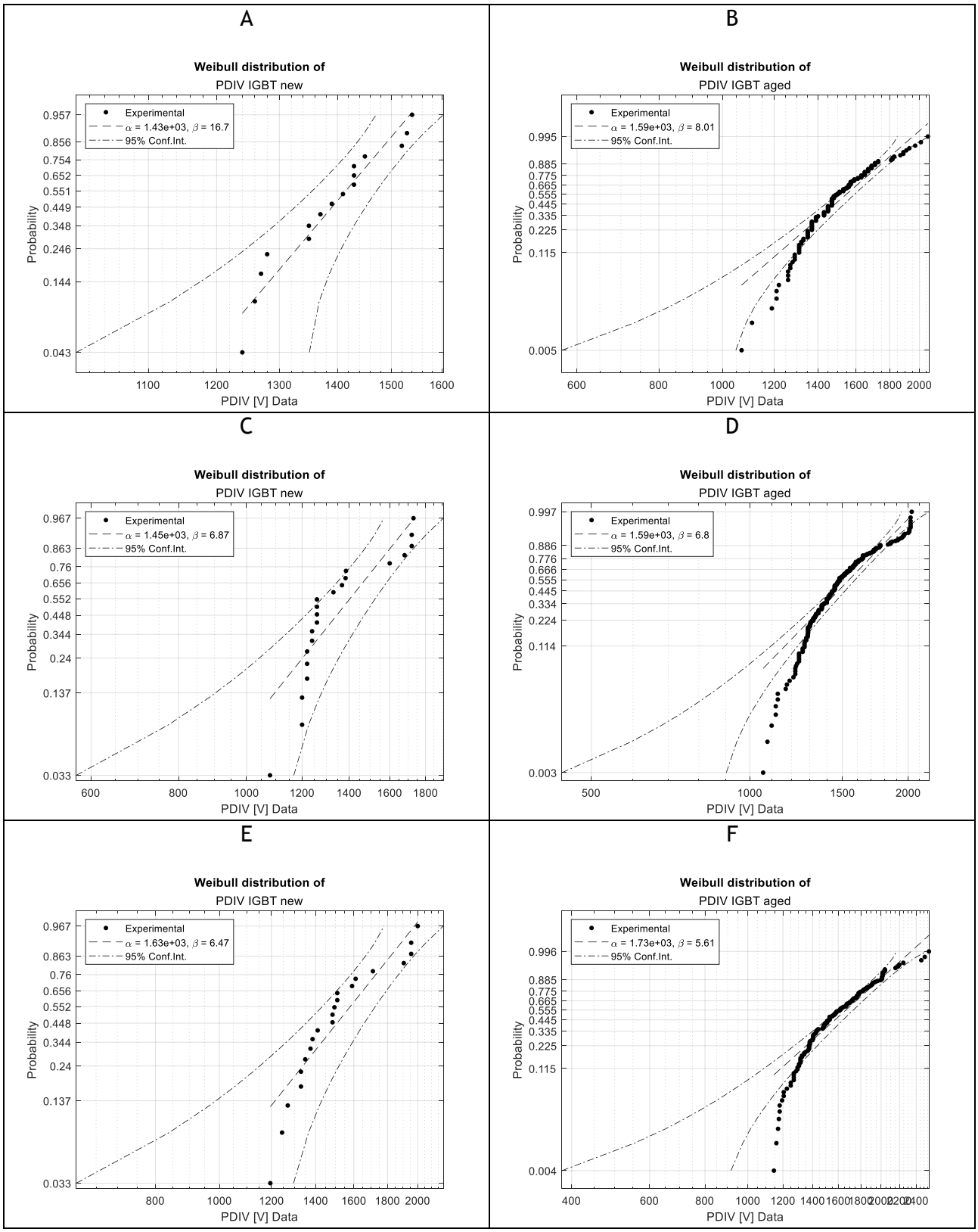


Figure 61. – Weibull plots of results obtained on different ageing modules, under different conditions. New module (A) TEST 1, (C) TEST 2, (E) TEST 3; Aged module (B) TEST 1, (D) TEST 2, (F) TEST 3.

Table 5. – Scale and shape parameters and 1% percentile extrapolation of different ageing tested modules.

Estimation of the parameters of the Weibull distribution function					
IGBT ageing	**Voltage**	**Temperature**	**α [V]**	**β**	**PDIV 1% [V]**
New	Sinusoidal	Room (20°C)	1434	16.73	1089
	Sinusoidal	Working (80°C)	1450	6.87	742
	Square	Working (80°C)	1635	6.47	803
Aged	Sinusoidal	Room (20°C)	1588	8.01	894
	Sinusoidal	Working (80°C)	1592	6.80	809
	Square	Working (80°C)	1729	5.61	761

For a correct interpretation of results of this kind of data classification it's important to point out two things. First of all, the number of new IGBT modules tested is much smaller than the aged ones. Moreover, about half of new IGBTs weren't affected by discharges, until the maximum voltage was reached. The absence of a PDIV value made it so that those weren't counted in this statistical elaboration.

To better understand the obtained results, a further partition of data intersecting model and ageing was made. The same statistical parameters were calculated and shown in table 6.

Table 6. Scale and shape parameters and 1% percentile extrapolation of different ageing and model tested modules.

Estimation of the parameters of the Weibull distribution function					
IGBT	**Voltage**	**Temperature**	**α [V]**	**β**	**PDIV 1% [V]**
KT4 -New	Sinusoidal	Room (20°C)	1434	16.73	1089
	Sinusoidal	Working (80°C)	1294	17.63	997
	Square	Working (80°C)	1491	11.20	988
KE4 - New	Sinusoidal	Room (20°C)	\	\	\
	Sinusoidal	Working (80°C)	1710	55.31	1574
	Square	Working (80°C)	1970	65.35	1836
KT4 - Aged	Sinusoidal	Room (20°C)	1484	9.78	927
	Sinusoidal	Working (80°C)	1548	6.04	722
	Square	Working (80°C)	1667	4.91	653
KE4 - Aged	Sinusoidal	Room (20°C)	1670	8.66	981
	Sinusoidal	Working (80°C)	1632	7.95	915
	Square	Working (80°C)	1789	6.89	918

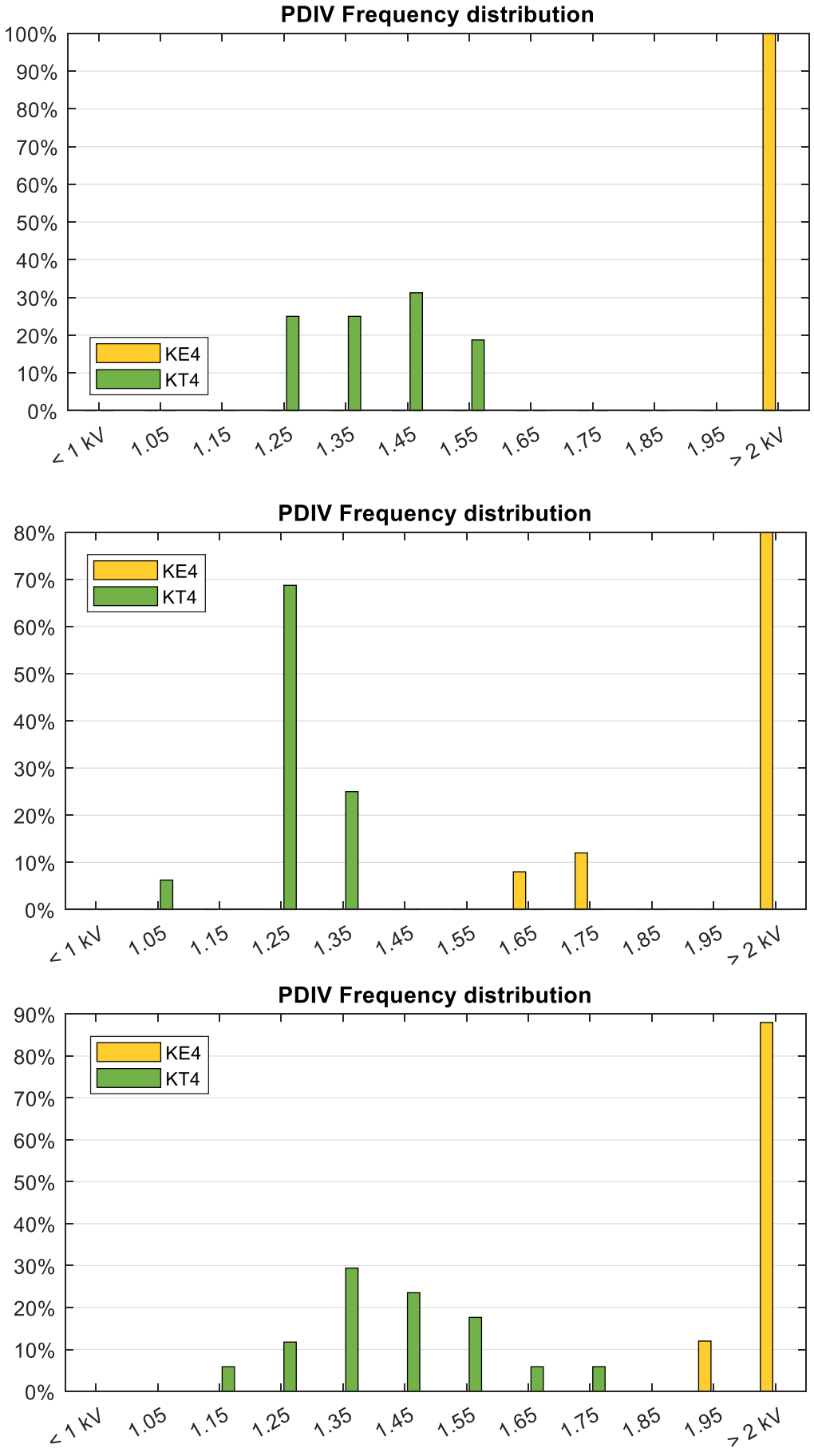


Figure 62. New modules PDIV divided by model distribution probability histograms (test 1; 2; 3)

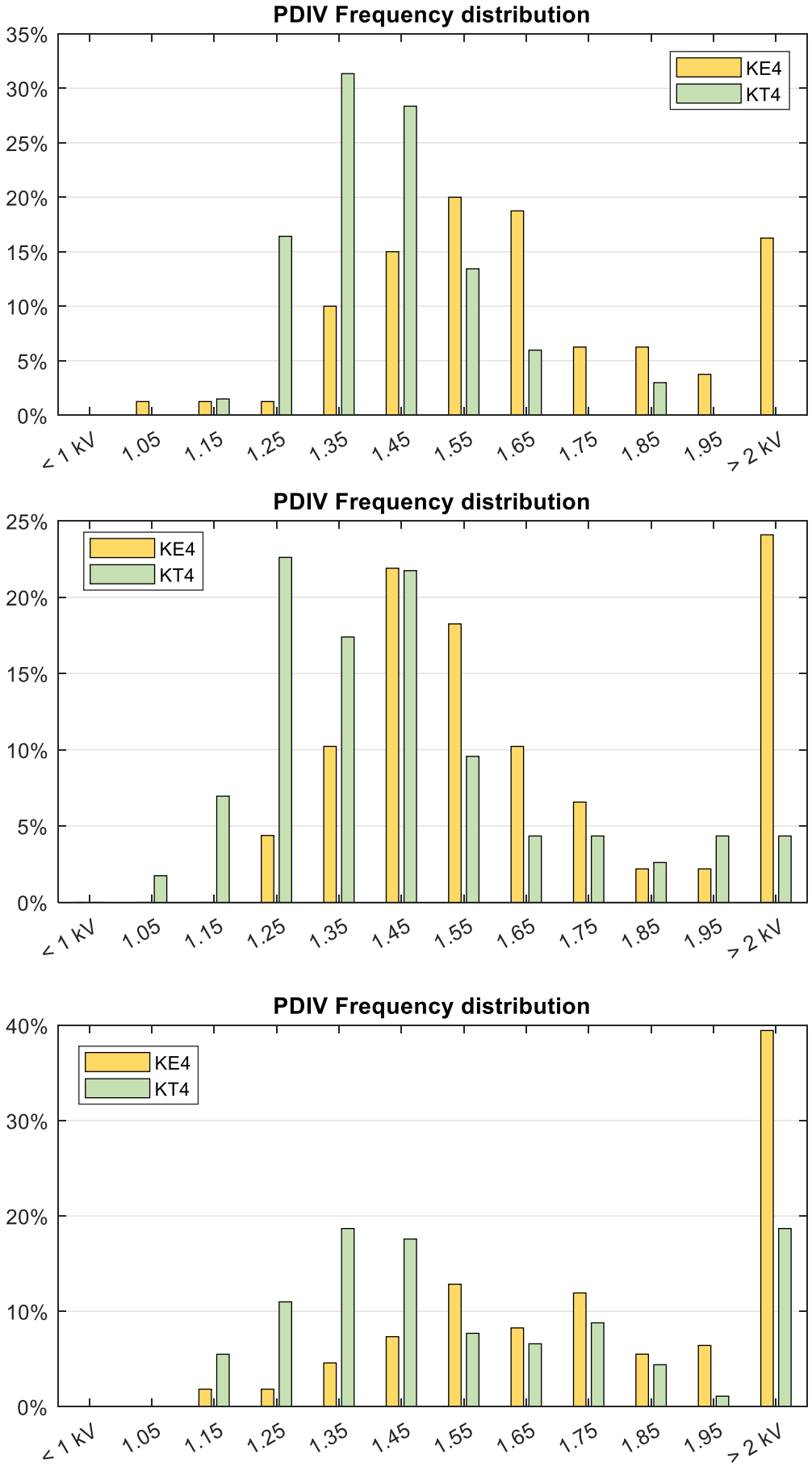


Figure 63. Aged modules PDIV divided by model distribution probability histograms (test 1; 2; 3)

There is a huge diversity between different new IGBT modules. From histograms of figure 62, it's interesting to note that almost all new "KE4" modules (in the case 5 out of 6) have a PDIV greater than 2 kV_{pk}. Trend of PDIV average values as a function of age seems to be opposite for different models, in particular mildly increasing with ageing for "KT4" model and decreasing for "KE4" model.

Focusing on the scale parameter, the increase of PDIV of KT4 modules goes from a PDIV increase of 50 V for test 1 to 250 V for test 2, while the decrease of PDIV for the "KE4" modules goes from about 80 V for test 2 and to at least 300 V for test 1. But combining these results with trend of β, it can be noticed that dispersion of PDIV is always higher for aged modules and 1% percentiles PDIV decrease with ageing for both models.

Stating that great difference of new modules in resistance to partial discharges is due to the difference between models could be a mistake if storage and transportation conditions weren't taken into account. In fact, they are the only factors that may have influenced the health state of new specimens and only if they were the same for each module, a correct comparison might be done.

Remembering the purpose of the thesis, thus, to assess if PDIV could be a reliability index, only a much more numerous data set and the knowledge of life conditions before test, like temperature, humidity or mechanical shock events allow to use PDIV as rough reliability evaluation criterion.

Despite that, dispersion of data is such that on average ageing seems to not significantly affect PDIV because differences in α are on average about 100/150 V. For this data classification same considerations previously made about α and 1% percentile PDIV values are valid. α values are widely above rated voltage but considering low failure probabilities PDIV is below rated voltage. The trigger of partial discharges in ordinary working and above all the persistence of them for a long time is a harmful phenomenon for insulation because it accelerates its aging process.

Further analysis was carried out by dividing data according to application which aged IGBTs were implemented in. They were components of buck-boosters, inverters or rectifiers within an UPS machine. Model of modules used in buck-boosters is “KT4” and for inverters and rectifiers is the other model.

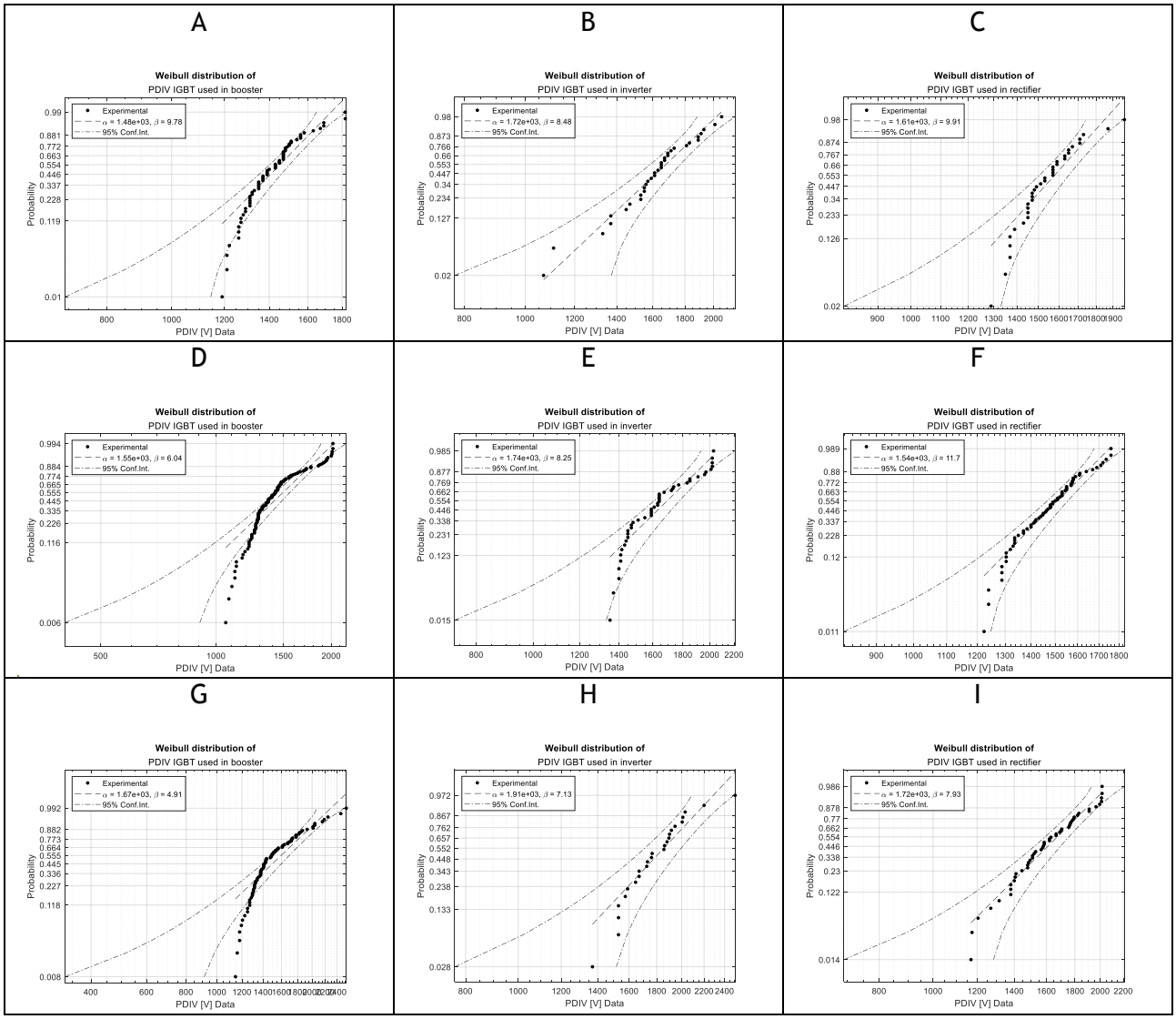


Figure 64 – Weibull plots of results obtained on different application of aged modules, under different conditions. modules used in buck/booster converters (A) TEST 1, (D) TEST 2, (G) TEST 3; used in inverters (B) TEST 1, (E) TEST 2, (H) TEST 3; used in rectifier (C) TEST 1, (F) TEST 2, (I) TEST 3.

Table 7. – Scale and shape parameters and 1% percentile extrapolation of tested modules from different application.

Estimation of the parameters of the Weibull distribution function					
IGBT application	**Voltage**	**Temperature**	**α [V]**	**β**	**PDIV 1% [V]**
Buck-booster	Sinusoidal	Room (20°C)	1484	9.78	927
	Sinusoidal	Working (80°C)	1548	6.04	722
	Square	Working (80°C)	1667	4.91	653
Inverter	Sinusoidal	Room (20°C)	1721	8.48	1001
	Sinusoidal	Working (80°C)	1738	8.25	995
	Square	Working (80°C)	1912	7.13	1003
Rectifier	Sinusoidal	Room (20°C)	1611	9.91	1013
	Sinusoidal	Working (80°C)	1539	11.70	1039
	Square	Working (80°C)	1720	7.93	963

PDIV of modules from inverters are the highest for all tests and those from buck-boosters are in general the lowest. As anticipated before, also considering cases in which PDIV is higher than 2 kV, differences would be amplified since almost all of the modules for which partial discharges weren't detected came from inverters.

From graphs of figure 64 it could be noticed that booster application modules PDIV trend doesn't match perfectly with Weibull distribution, in particular it deviates at low probabilities. Statistical dispersion of PDIV for these modules is the highest, and the conclusion may be that sets of modules used in buck-booster converters underwent electrical or thermal stresses of varying intensity, although belonging to the same machine. Conductivity data (see figures 85, 86) show the same dispersion features.

From the point of view of a possible correlation between average value of PDIV and electric stress of the module, it might be stated that buck-booster is the most stressing application for IGBTs.

Comparing inverter and rectifier-used modules, which belong to the same model family, modules constituting inverter branches are likely less stressed, since PDIV is on average higher, but focusing on the shape parameter, ß of the rectifiers is higher for all three tests than inverters. This means that PDIV values are less dispersed, hence the stress level to which modules of rectifiers are submitted might be more uniform and similar for each component. A possible reason is that rectifiers generally work for more time but unceasingly, because they have to charge or to maintain charged batteries, while inverters

come into operation only if there are voltage sags or interruption or if it is necessary power loads with a stable voltage to protect them from grid disturbances.

PRPD pattern analysis

Phase Resolved Partial Discharge (PRPD) patterns were also analysed in the attempt to identify the typology of discharge (hence defect) originating PD activity.

They immediately highlight extreme variability of the PD phenomenon and defects randomness.

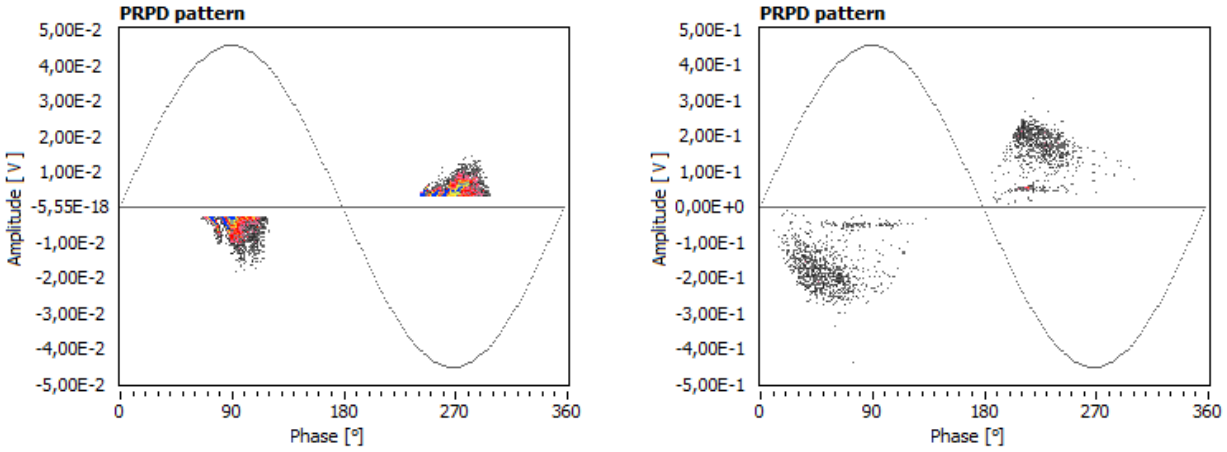


Figure 65. PRPD patterns. IGBT N1 (left) and IGBT N3 (right) under 1450 V (peak voltage), test 2.

In fact, as pattern of figure 65 shows, two IGBT, same model, both news and at the same voltage and temperature, present two different defects. First module pattern is attributable to superficial discharges while internal PDs are distinguishable in the second.

Each defect inside insulation is characterized by its own PDIV, so if at a certain voltage only one PD cluster is identified, increasing voltage a second PD event might trigger. An example of this fact is given by figure 66. PRPD pattern are both referred to the same sample, but on the left voltage applied corresponds to PDIV (about 1.69 kV_{pk}) and on the right voltage is higher, equal to 2 kV_{pk}. It's evident that another PD event is triggered at the highest voltage.

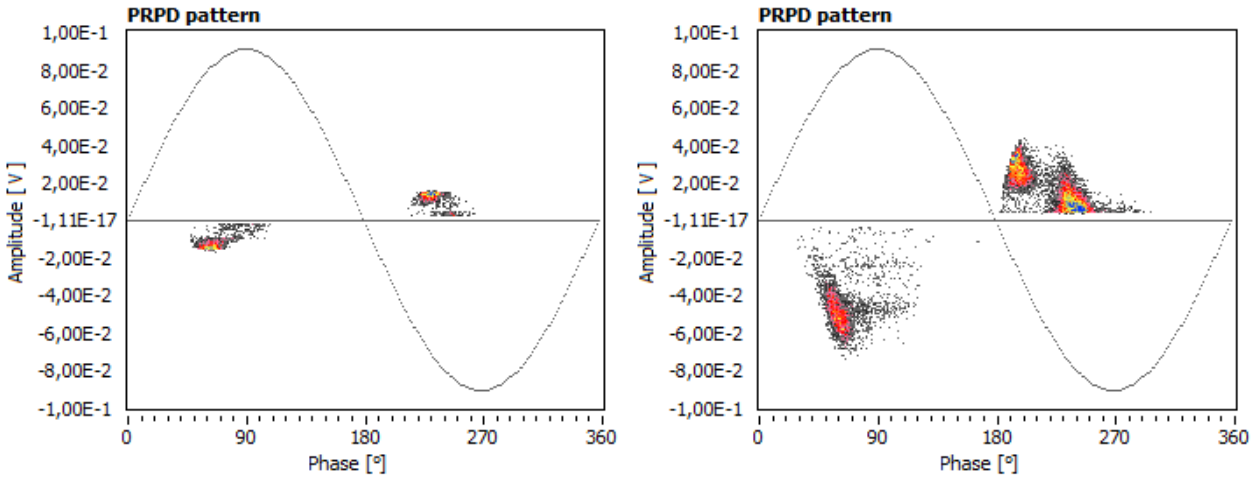


Figure 66. PRPD pattern of same IGBT (number 37) at 1.69 kV (left) and at 2kV (right)

Taken note of the intrinsic variability of phenomenon, a comparison between PRPD pattern, as objective as possible, has been tried to make. Patterns on selected modules (7,14,36, respectively used for Rectifier, Inverter and Buck-Booster applications) were obtained under an applied voltage of 1.8 kVpk and two temperatures (20°C and 80°C). The selected modules had similar PDIV levels, in the range 1.50-1.53 kVpk at room temperature, and 1.39-1.48 kVpk at working temperature. This could mean that defects of similar dimensions should be present in those modules, but this should be confirmed since also the location of the defect is crucial for the determination of PDIV levels.

PRPD patterns can be found in Figures 67 and 68 respectively at room and working temperatures, while PD average amplitudes, their repetition rate, scale and shape factors of the Weibull fitting of PD amplitudes acquired are also reported in Tables 8 and 9. A “damage rate” was obtained multiplying the PD amplitude with repetition rate.

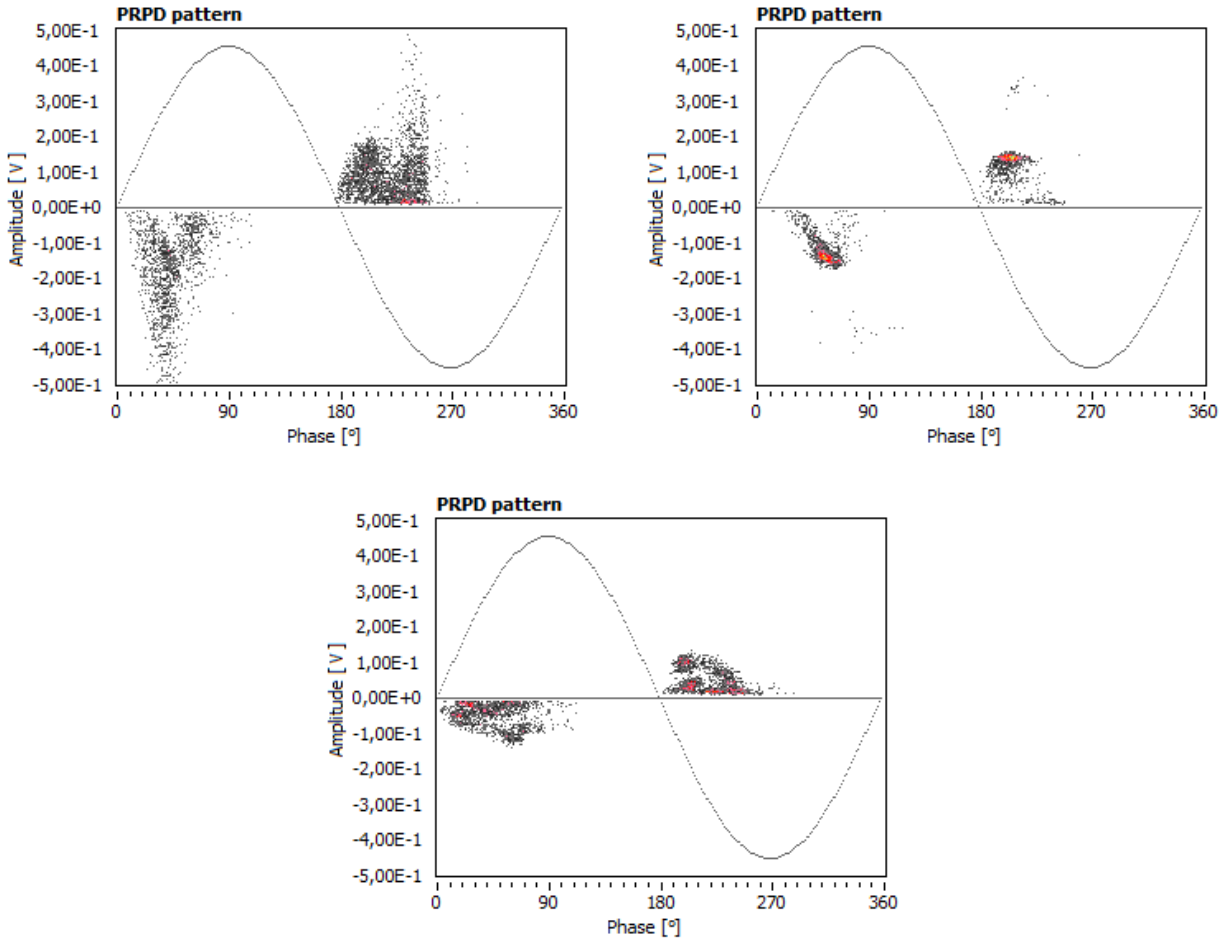


Figure 67. PRPD patterns obtained for IGBT 7 (rectifier, top left), IGBT 14 (inverter, top right), IGBT 36 (buck-boost converter, bottom) at 1.8 kVpk and room temperature (test 1).

Table 8. PD amplitudes, repetition and damage rates for IGBT 7 (rectifier), IGBT 14 (inverter), IGBT 36 (buck-boost converter) at 1.8 kVpk and room temperature (test 1).

	Rectifier (7)	Inverter (14)	Buck-Boost (36)
Scale factor [V]	0.132	0.134	0.054
Shape factor	1.50	2.61	1.56
Mean Amplitude [V]	0.120	0.124	0.050
Rep. rate [1/s]	206.9	108.8	170.5
Damage rate	24.9	13.4	8.5

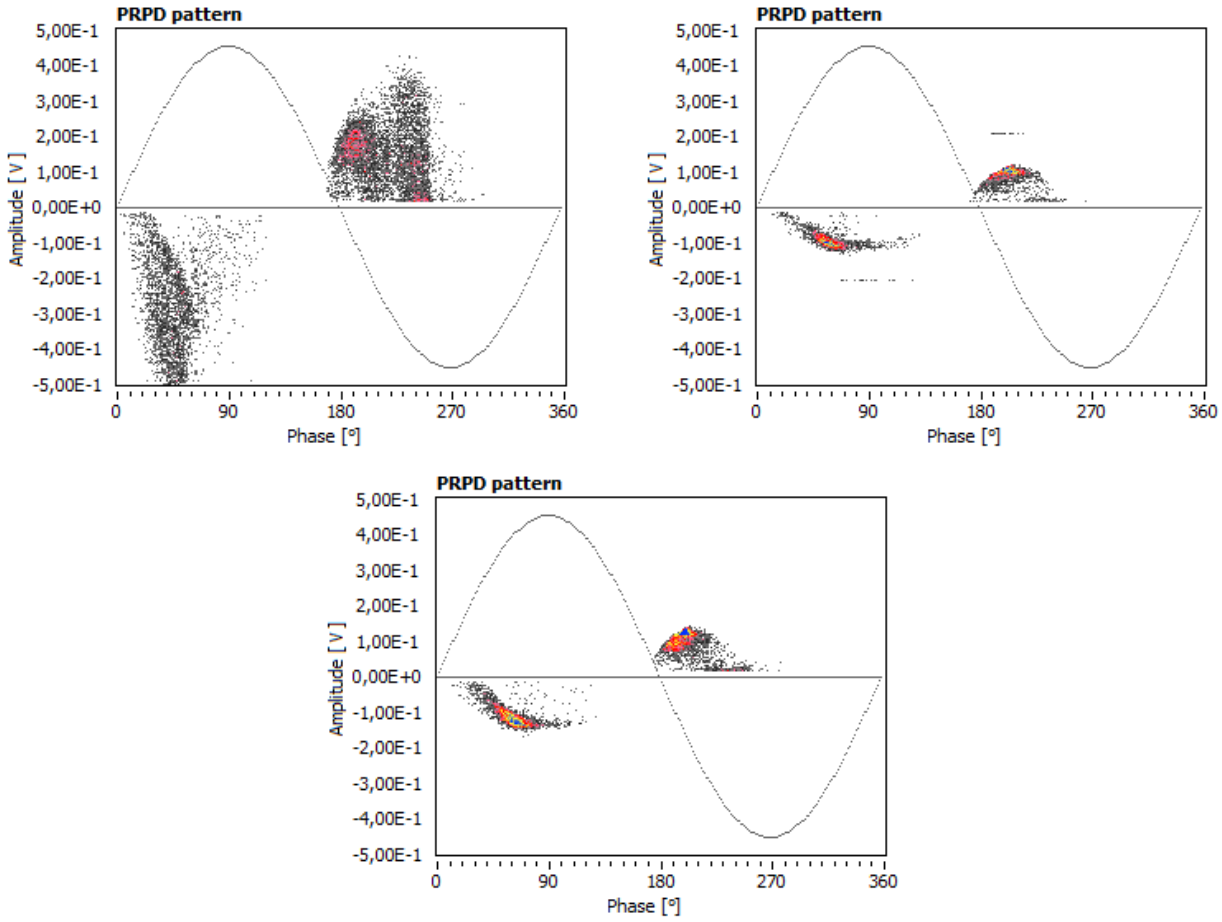


Figure 68. PRPD patterns obtained for IGBT #7 (rectifier, top left), IGBT #14 (inverter, top right), IGBT #36 (buck-boost converter, bottom) at 1.8 kVpk and working temperature (test 2).

Table 9. PD amplitudes, repetition and damage rates for IGBT #7 (rectifier), IGBT #14 (inverter), IGBT #36 (buck-boost converter) at 1.8 kVpk and working temperature (test 2).

	Rectifier (7)	Inverter (14)	Buck-Boost (36)
Scale factor [V]	0.216	0.097	0.111
Shape factor	2.10	3.77	4.42
Mean Amplitude [V]	0.195	0.091	0.104
Rep. rate [1/s]	156.3	99.6	104.9
Damage rate	30.5	9.1	10.9

Results show that while KE4 modules, belonging to an inverter or a rectifier, are characterized by the activation of 1 or 2 defective locations (generally one “main” defect, and a superimposed minor activity from a second one), for KT4 (used in buck-boost converters), the amount of defective locations is much higher (4-6), each with similar activity levels. Regarding the typology of defects, the PRPD structure suggests the presence of “internal” cavities (meaning they are in the bulk of the dielectric layers) in IGBTs from buck-boost and inverters, while defects on the surface should be present in

the IGBT from the rectifier. The asymmetry of phase and amplitude on the first and second patterns should also be due to the exposure of metal, ground side. The last pattern, referring to the buck-boost IGBT, apparently has cavities facing bare metal in both sides (some facing high voltage, some ground). The same result is observed at both testing temperatures.

Regarding the destructive potential of those discharges, at room temperature, it is clear that the IGBT used in the rectifier features the highest PD amplitude among the three. Calculating the damage rate also shows that this IGBT also has the highest aging rate. Since, as mentioned, the dimension of those defective regions could be on the same order of magnitude, the interpretation of this result is relatively simple. If on the one hand, the aging rate of the IGBT #7 (from the rectifier) is the highest, on the other hand it should also be, among the three, the one with lower aging of the three, meaning lower average stresses and a higher residual life. On the other hand, IGBT #36 (from the buck-boost converter) should be the one with higher aging, and lower residual life. This is due to the fact that when PD activity is induced in a defect, the dielectric quality of inner surfaces allows for relatively high charge accumulation, which is directly related to the amplitude of the discharge. With time and ageing, the quality of those surfaces will be degraded, and much lower accumulation will be present, due to the increase of local conductivity of surfaces and increased recombination rate. PD amplitude will be gradually decreased over time. In other words, the fact that despite similar PDIV levels the PD amplitude and overall activity in one IGBT is higher than others might be a sign of a lower overall aging of the dielectric. It must be also said that this also depends on the location of those defects and should be confirmed by further testing.

For square wave voltage test pattern analysis is more complicated. In test 3, PRPD patterns look like these:

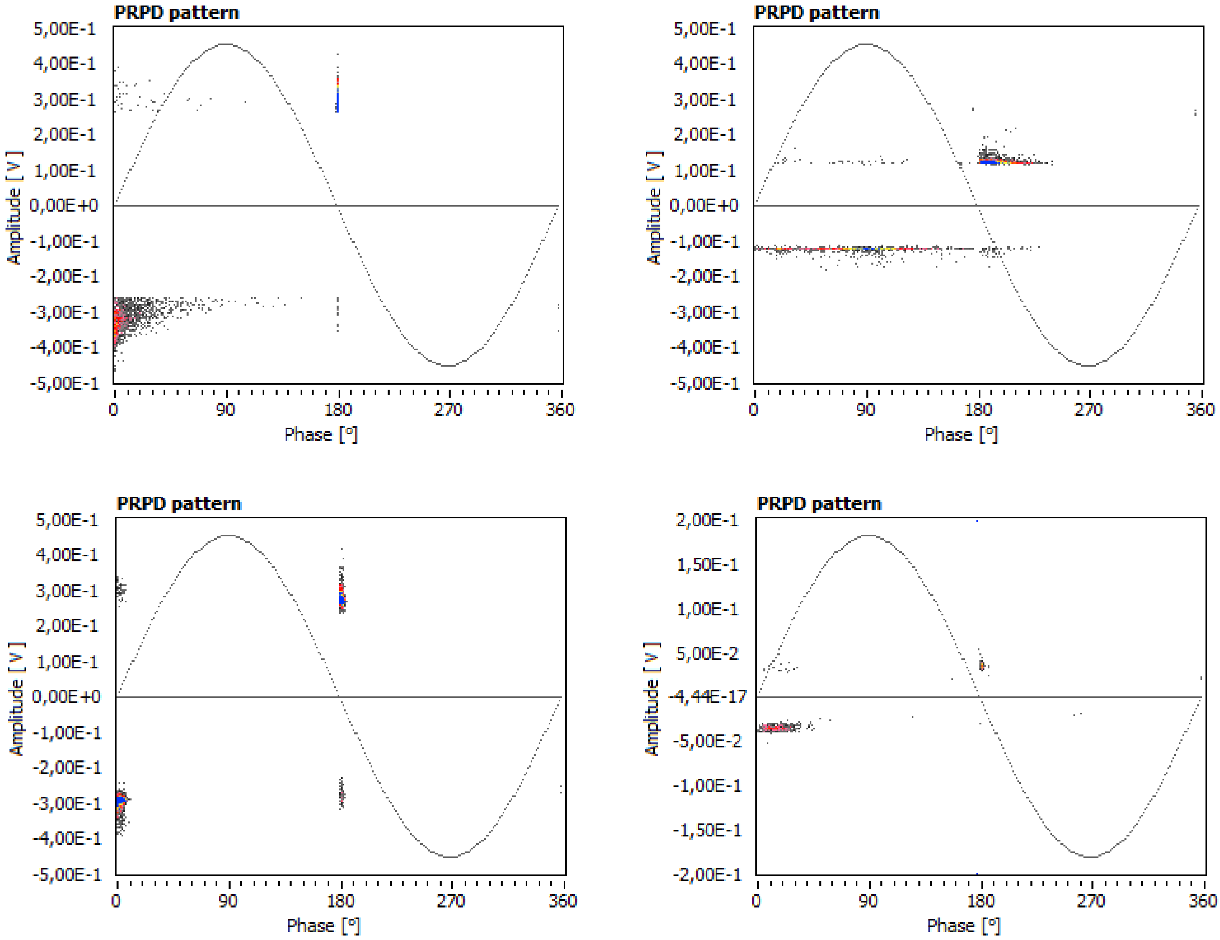


Figure 69. PRPD pattern from test 3. Igbt 5, at 2.97 kV (peak to peak square wave voltage) (top left) – igbt 15, 4.02 kV_{pkpk} (top right) – igbt A4, 2.63 kV_{pkpk} (bottom left) – IGBT N10, 3.81 kV (bottom right)

The most common pattern is like that top-left of figure 69. Looking at these patterns, it's clear that they are very different from patterns obtained under a sinusoidal waveform, which have a well-known shape. PD under a square wave voltage predominantly occur at 0° and 180°, thus phases in which voltage changes polarity and insulation is subjected to a rapid voltage variation in time. In addition to this aspect, first PD which have obviously a small amplitude, are borderline with trigger value and they could be easily confused with noise, that is always present (figure 70).

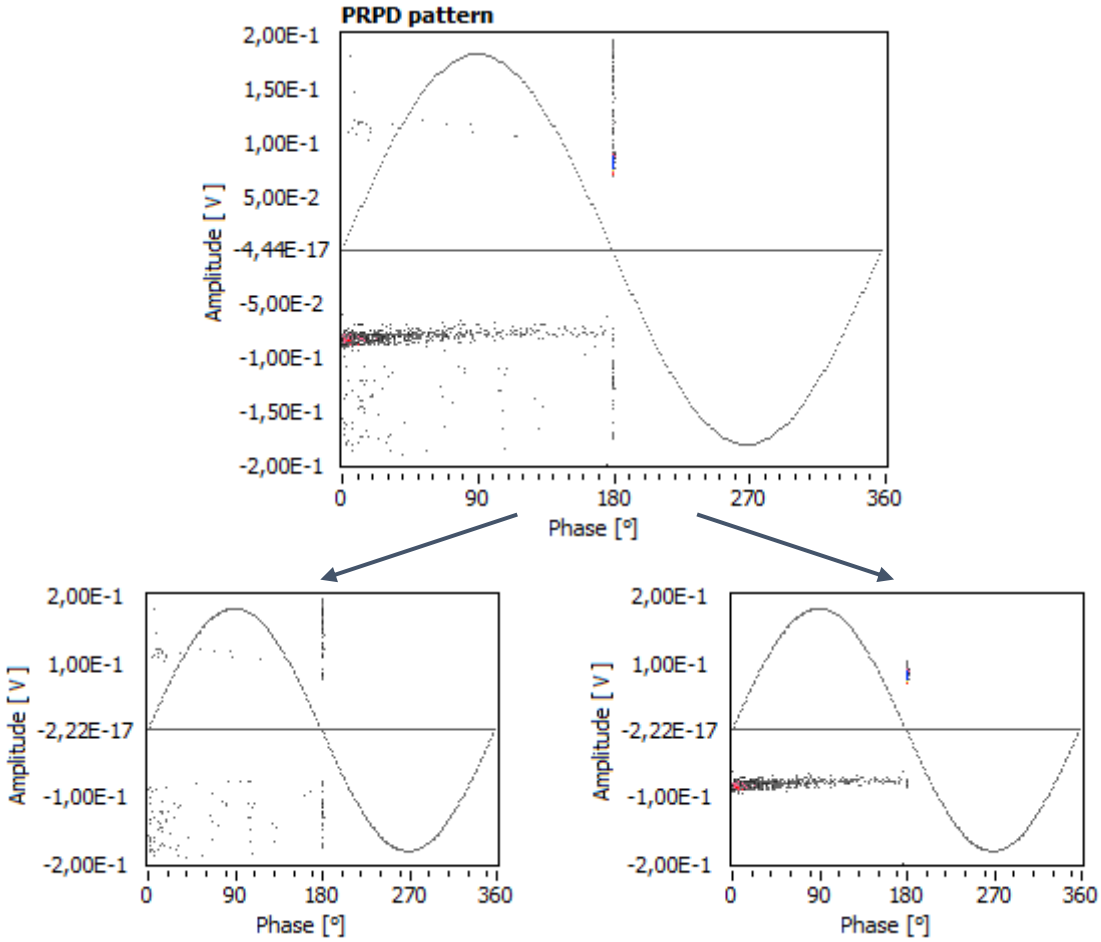


Figure 70. An example of PRPD pattern obtained with waveform acquisition (top). Although having a filtering action only after a post-processing elaboration, noise signal (left) could be separated from PD signal (right).

Therefore, to be sure to have detected a PD during the detection, the only possible way is increasing trigger up to high levels to check if waveform corresponds to one of partial discharge, as shown in figure 71.

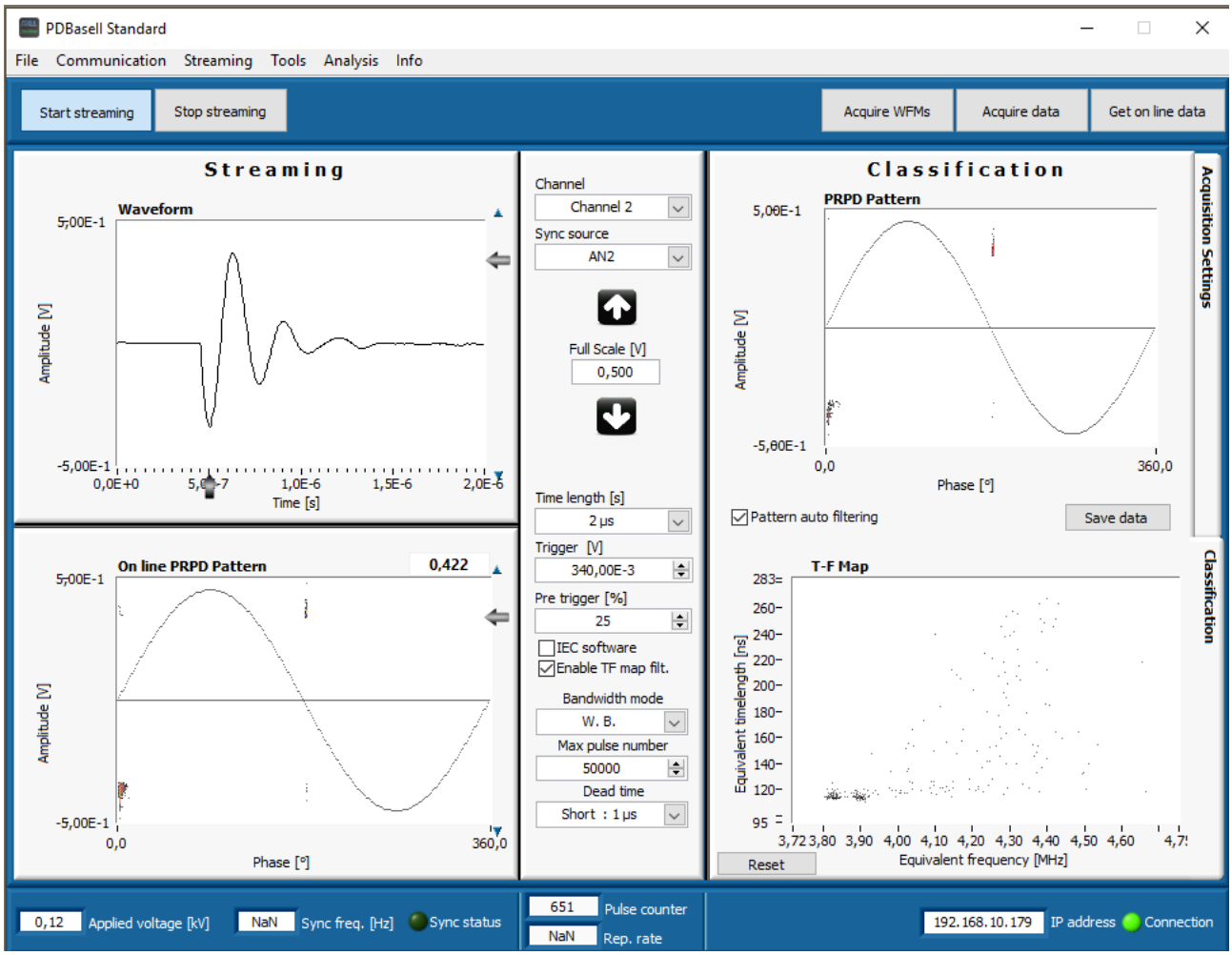
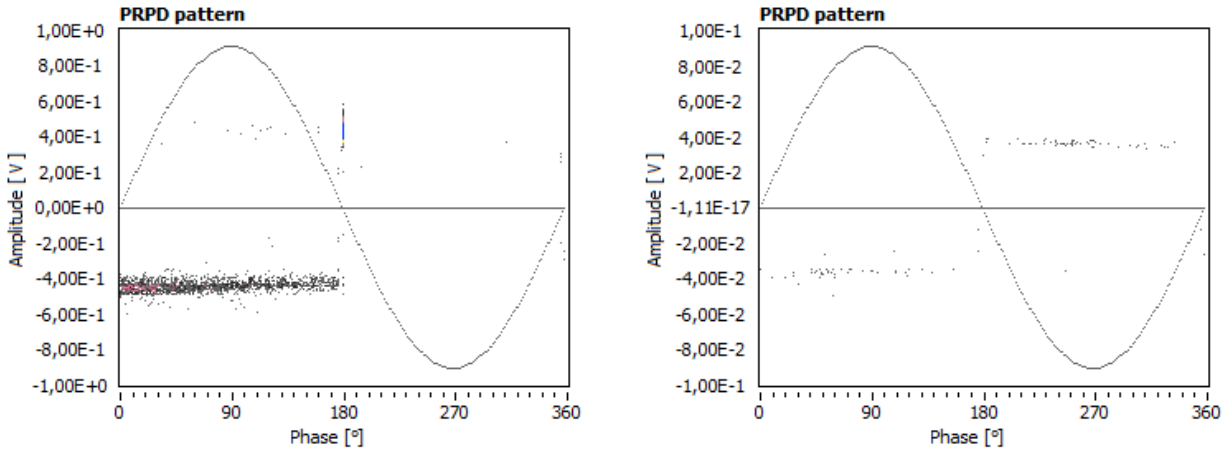


Figure 71. Screenshot of PD-base software display.

For the sake of completeness same comparison for test 3 patterns is reported. It has to be noticed that IGBT 14 wasn't affected by PD at 1.8 kVpk, so pattern is referred to a 2 kVpk voltage.



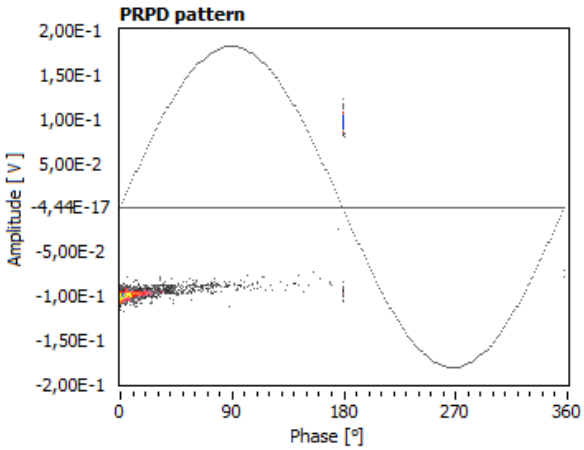


Figure 72. PRPD patterns obtained for IGBT #7 (rectifier, top left) at 1.8 kVpk, IGBT #14 (inverter, top right) at 2 kVpk, IGBT #36 (buck-boost converter, bottom) at 1.8 kVpk in test 3.

Table 10. PD amplitudes, repetition and damage rates for IGBT #7 (rectifier), IGBT #36 (buck-boost converter) at 1.8 kVpk and IGBT #14 (inverter) at 2 kVpk in test 3.

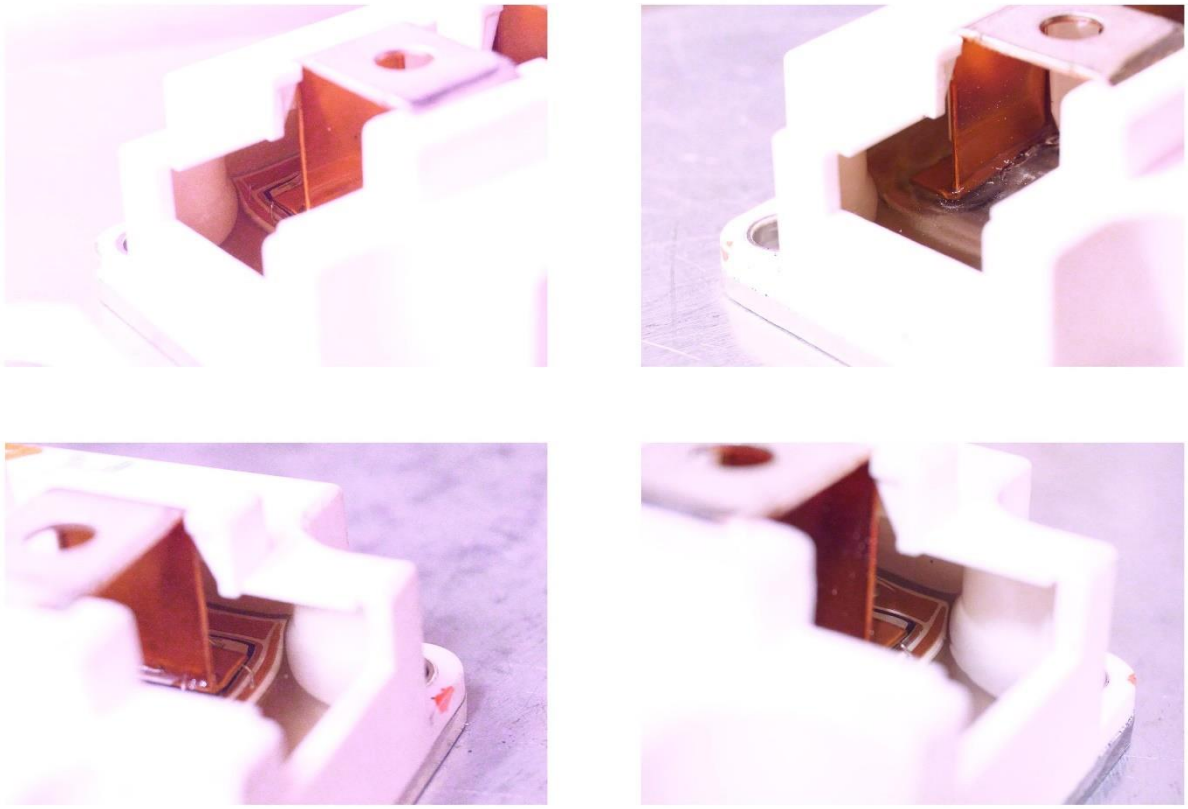
	Rectifier (7)	Inverter (14)	Buck-Boost (36)
Scale factor [V]	0.444	0.037	0.098
Shape factor	13.83	17.83	19.81
Mean Amplitude [V]	0.435	0.035	0.097
Rep. rate [1/s]	31.3	0.9	29.2
Damage rate	13.6	0.0321	2.83

PD optical measurement

One of aims of PD tests is not only find the type of defect but also locate where it is inside insulation system. In this regard, knowing that light radiation is emitted when a discharge happens, an attempt was made to immortalize a discharge with a camera. There were two main difficulties. First, only a part of the inside of module is visible removing central contacts because of the plastic case encapsulation. Second, radiation emitted is not necessarily in the visible spectrum.

Applying a constant voltage amplitude of $2\ kV_{pk}$ to the partially disassembled module, while capturing a 30 seconds exposure with a digital camera (Sony alpha-6000, 50mm f/11, ISO 3600) and postprocessing images highlighting light emitting regions, no discharges were captured although they are detected by the PD-Base. As stated above, either discharges were in a lateral area of insulation, impossible to catch with camera or radiation emitted was mostly in the non-visible range.

Increasing voltage to values greater than $3\ kV_{pk}$ a discharge spot was found out near the terminal block (figures 74 and 75).



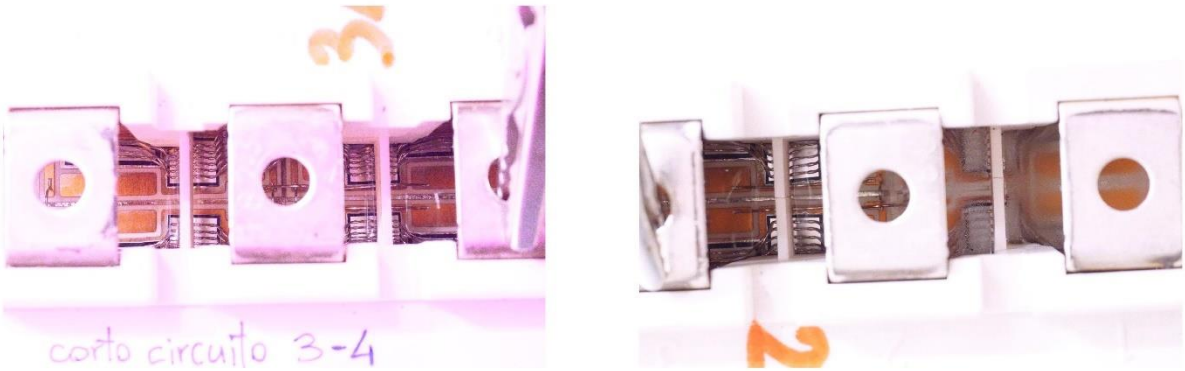


Figure 73. Right corner, left corner, top view of a “KT4” model (left side) and “KE4” module (right side). From all these positions, PD weren’t detected by camera.

Photos are correlated with PRPD patterns. Looking scales of graphs, it can be noticed that the discharge amplitude is much larger than those measured at the PDIV, therefore the intensity of emission is such that the emitted glow becomes visible.

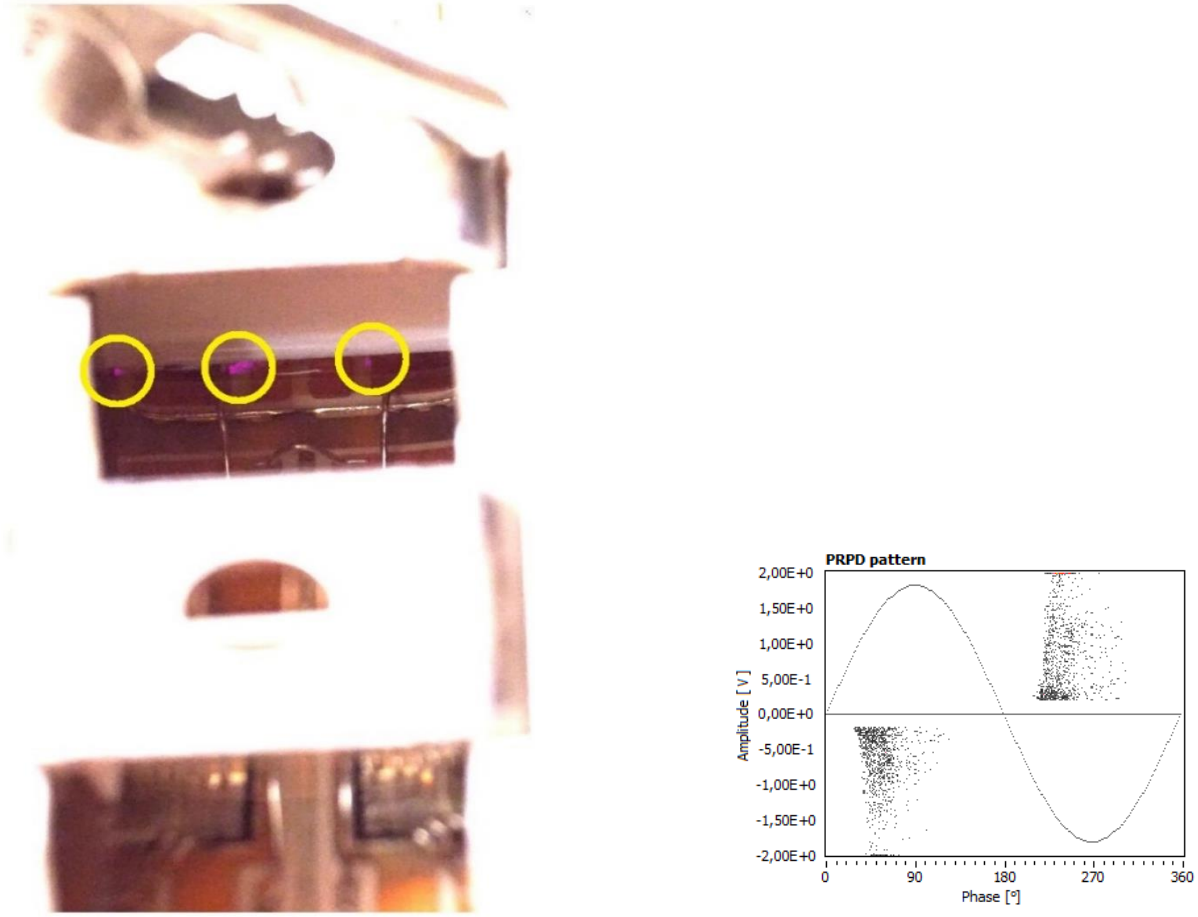


Figure 74. Igbt number 34. Lighting discharges are highlighted by yellow circles. They are all close to gate pads. Relative pattern on the right.

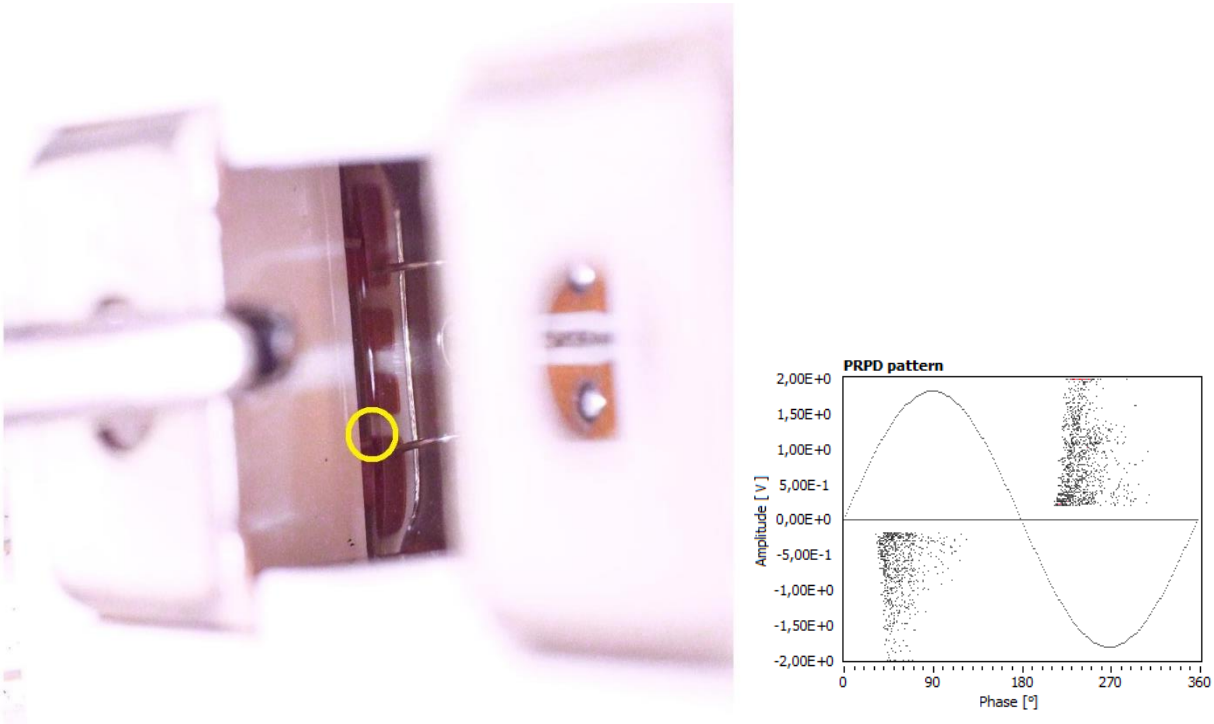


Figure 75. Igbt number 29. Only one spot but in a similar position. Relative pattern on the right.

Single pairs IGBT PD tests

Practically no PD activity was detected during those tests, up to an applied voltage of 1.2 kVpk, for all of the 3 types of tests.

In this type of measurement test 3 is a bit different from 1 and 2, because in sinusoidal test configuration (see figures 56-57) the circuit composed of diodes and capacitive divider makes possible to output a unipolar sinusoid with a DC offset proportional to the amplitude of the sinusoid itself. While in test 3 the function generator isn't able to do the same thing, so the offset DC is pre-set to its maximum value, that is 600 V, and the only variable parameter is the amplitude of the square wave. This discrepancy, however, didn't reveal any observations on test results.

An interesting result obtained with those tests is the fact that more than often, IGBTs would tend to enter their conductive state with maximum applied voltages between 1.15 kV_{pk} and 1.2 kV_{pk}, which is close to the voltage rating of the module (1.2 kV), sometimes with destructive effects, resulting in permanent short circuit between collector and gate pins. Generally speaking, "KT4" modules are more prone to suffer breakdowns.

All breakdowns occurred at room temperature, being the modules tested first in this condition. It is possible that the reduced humidity content at increased temperature is able to increase the performance of the dielectric. But it is also probable that the increased conductivity level of the silicone gel will induce a different field distribution in the insulation system, possibly reducing its level in the potting, when a DC component is present on the applied voltage, since in this condition field distributes not only depending on the permittivity (which is the case when purely in AC), but also on conductivity. Second hypothesis is supported by the fact that some of IGBTs gone in breakdown in the working temperature test for exceeding maximum rated voltage, present a short circuit between gate and emitter contacts instead of between gate and collector. An appropriate evaluation would require an entirely different simulative approach to validate it, with proper determination of constants based on temperature, which is out of the scope of this work.

The subsystem, which superimposes a direct voltage on a sinusoidal alternating one, inevitably distorts the latter. Scope distinguishes 2 different measures: peak-to-peak voltage, which is obtained simply as the difference between maximum and minimum detected voltage and amplitude, determined as the amplitude of the ideal sinusoid and the former is greater than the latter.

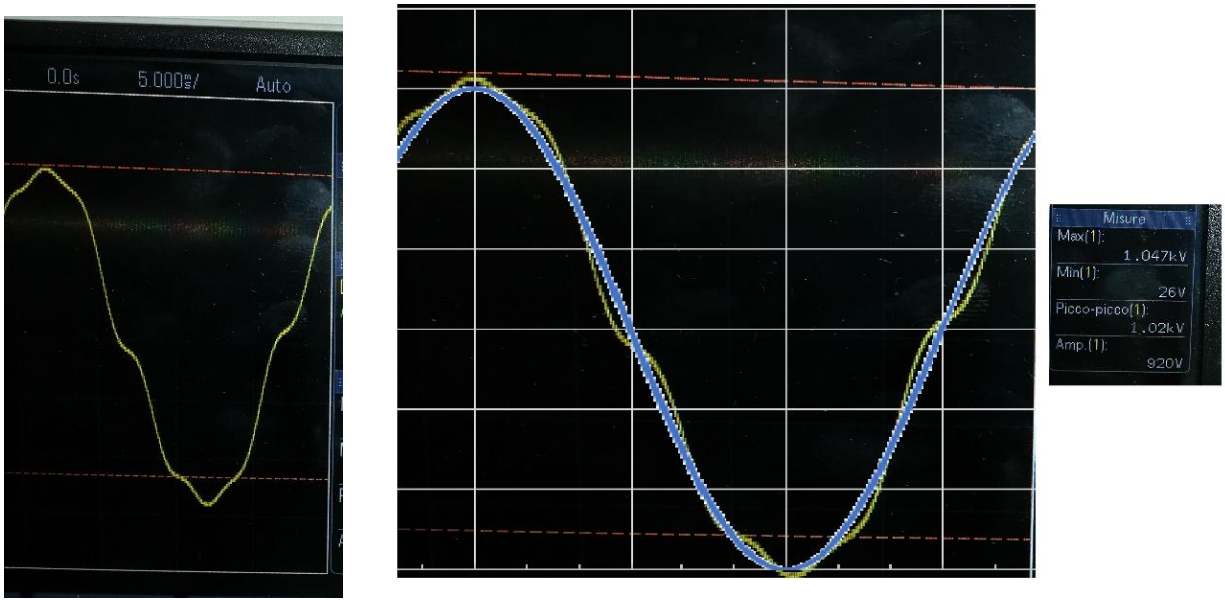


Figure 76. Real waveform applied in test 1 and 2. Ideal sinusoid waveform (blue line).

Single pairs IGBT PD tests were made reaching 1.2 kV as absolute maximum voltage, but value of amplitude was about 100 V less. In some cases, a 1.2 kV of amplitude was reached, with a maximum voltage that exceeded 1300 V. When the applied voltage exceeds rated voltage, that is the maximum tolerable voltage for IGBTs and free-wheeling diodes, a strange signal is detected by instrument. From PRPD pattern it might seem a corona discharges because points that represent discharges are located at 90° and the pattern is unipolar. (as shown in figure 77).

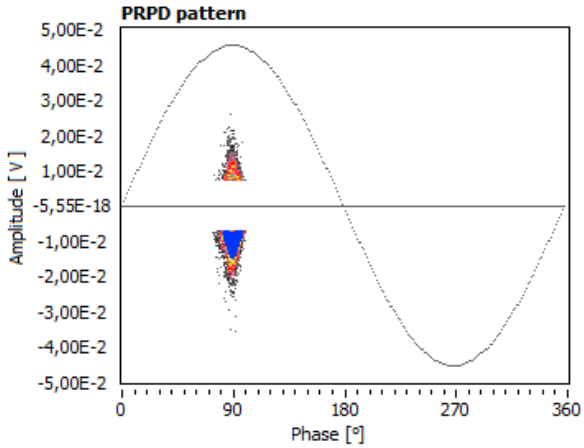


Figure 77. PRPD pattern of top IGBT, in which a current signal was detected.

Analysing also waveform of these signals (some examples are reported in figure 78), it has concluded that they aren't partial discharges but the leakage current from the diode, which is in parallel to the IGBT during those tests. This might lead to breakdown if this condition persists for a long time.

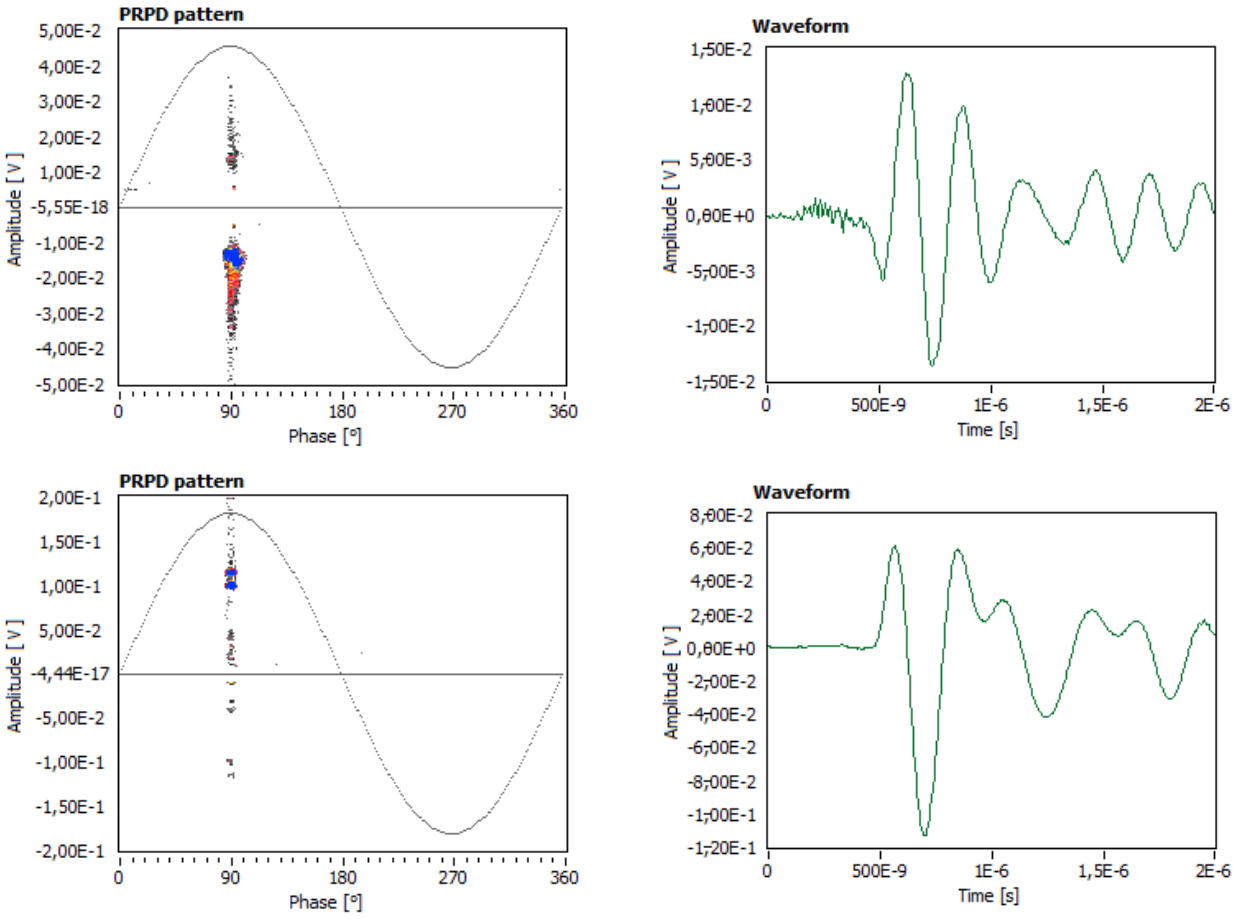


Figure 78. PRPD Pattern and relative waveform of 2 of IGBTs, in which is more evident this phenomenon.

This current signal was also recorded in one specimen in test 2 at a voltage lower than rated voltage, hence there is a small probability that diodes do have a higher leakage in ordinary working conditions. Regarding power supply voltage, under-dimensioning the system is advisable as a precaution.

Conductivity tests

Conductivity measurements need to quantify the conductivity of ceramic insulation of the modules. They are made at 80°C, which is working temperature of IGBTs.

The measurement circuit is very simple: every pin of module is connected to the high voltage clamp, while the baseplate is grounded. A pico-ammeter, inserted in series to IGBT baseplate, measures the leakage current flowing to ground.

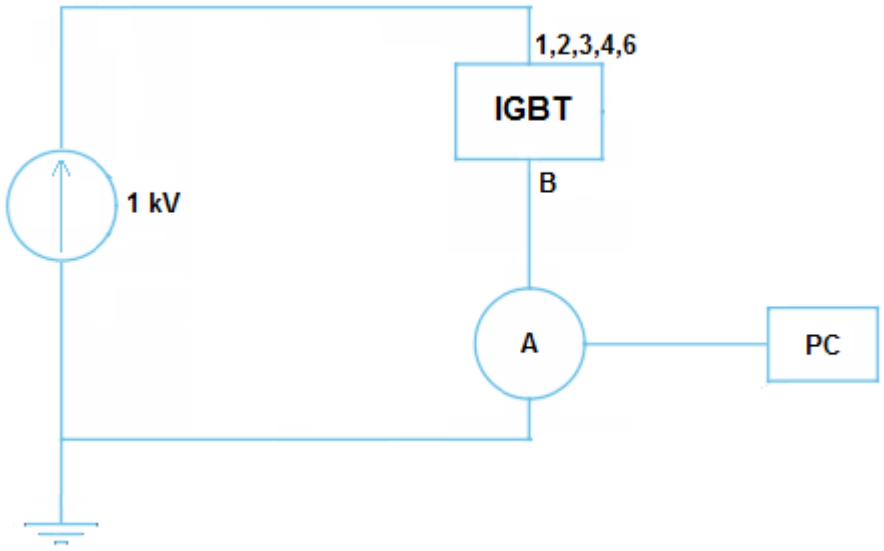


Figure 79. Circuit diagram of the conductivity test

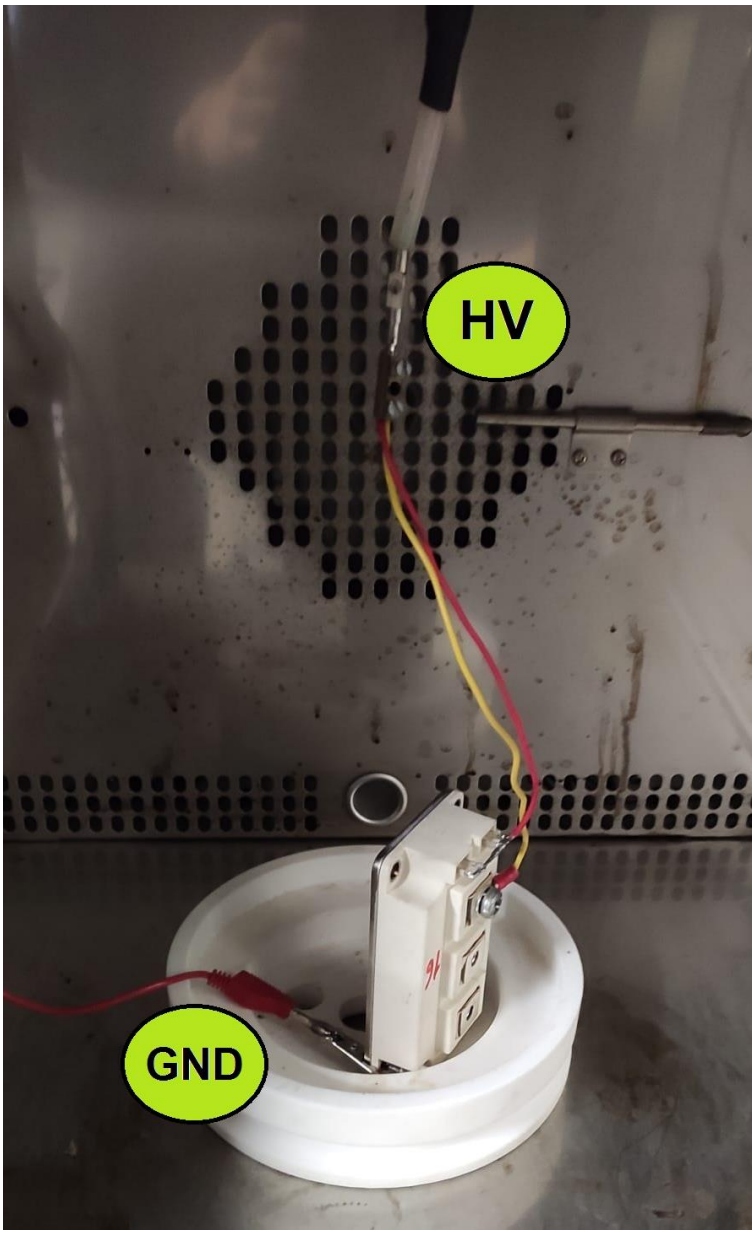


Figure 80. Imagine of a module inside the oven before conductivity test

The specimens are placed inside an oven at 80°C for at least 1 hour prior to the beginning of the test to ensure that they will always internally reach the desired temperature (as shown in figure 80). After that, a DC voltage generator, set to output 1 kV, is turned on and monitoring of the polarization current begins. A computer is connected to record and plot the overall trend of current. The test lasts at least 24 hours to allow current to stabilize at the steady state value. Starting from current value and the knowledge of insulation sample geometric dimensions, such as thickness and area, conductivity σ is estimated as:

$$\sigma = \frac{J}{E} \tag{2}$$

where J is the current density and E is the electric field.

An example of conductivity plot obtained from this measurement is shown in figure 81.

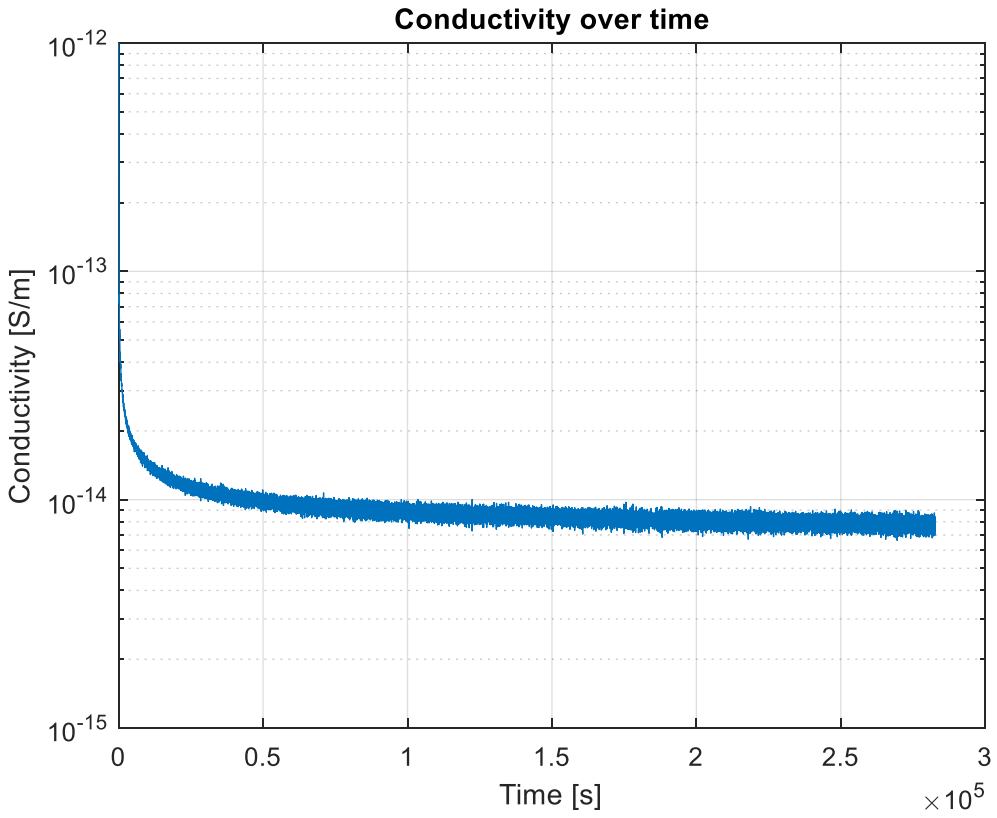


Figure 81. Conductivity trend over time graph of a tested IGBT

Conductivity results

Conductivity values are calculated as mean of the last 100 read values. Conductivity of each sample is reported in table 15 in Appendix.

The following Figure 82 ÷ 88 and Table 11 ÷ 14 report boxplot graph, mean value and standard deviation of conductivity data sample based on type of classification. Adopted data classifications are the same as those used for PDIV study.

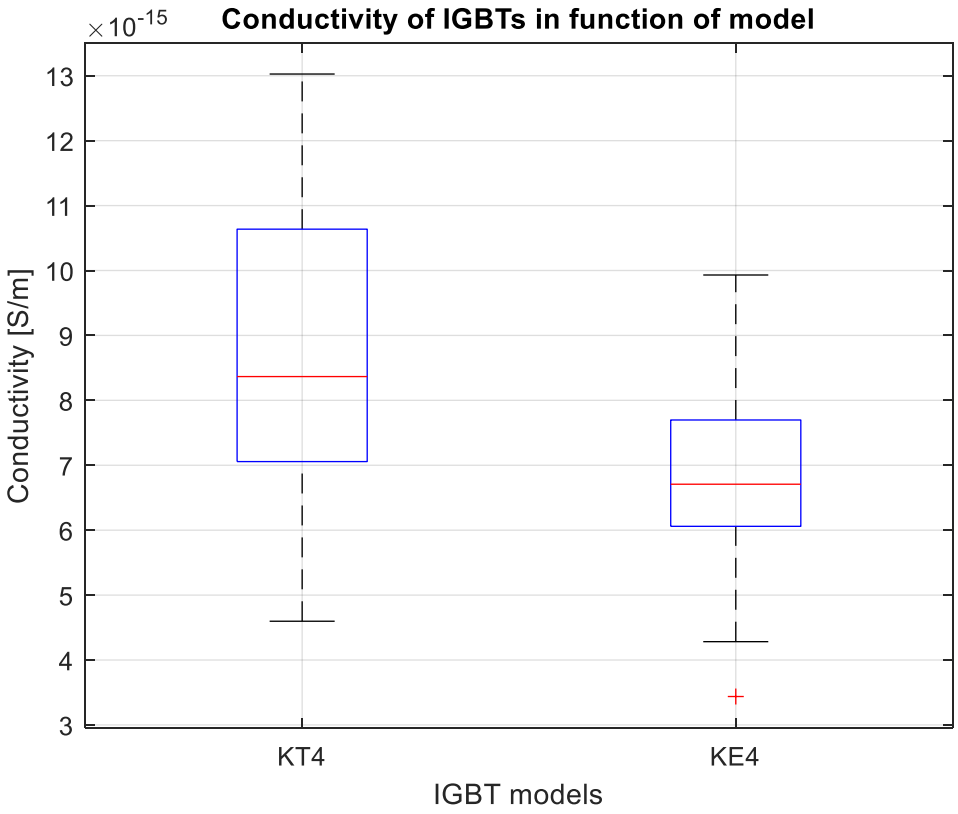


Figure 82. Boxplot of IGBT modules conductivity in function of model.

Table 11. Mean and standard deviation of tested modules in function of model.

Estimation of conductivity parameters		
IGBT model	**μ mean [S/m]**	**σ standard deviation**
KT4	8.65E-15	2.56E-15
KE4	6.77E-15	1.46E-15

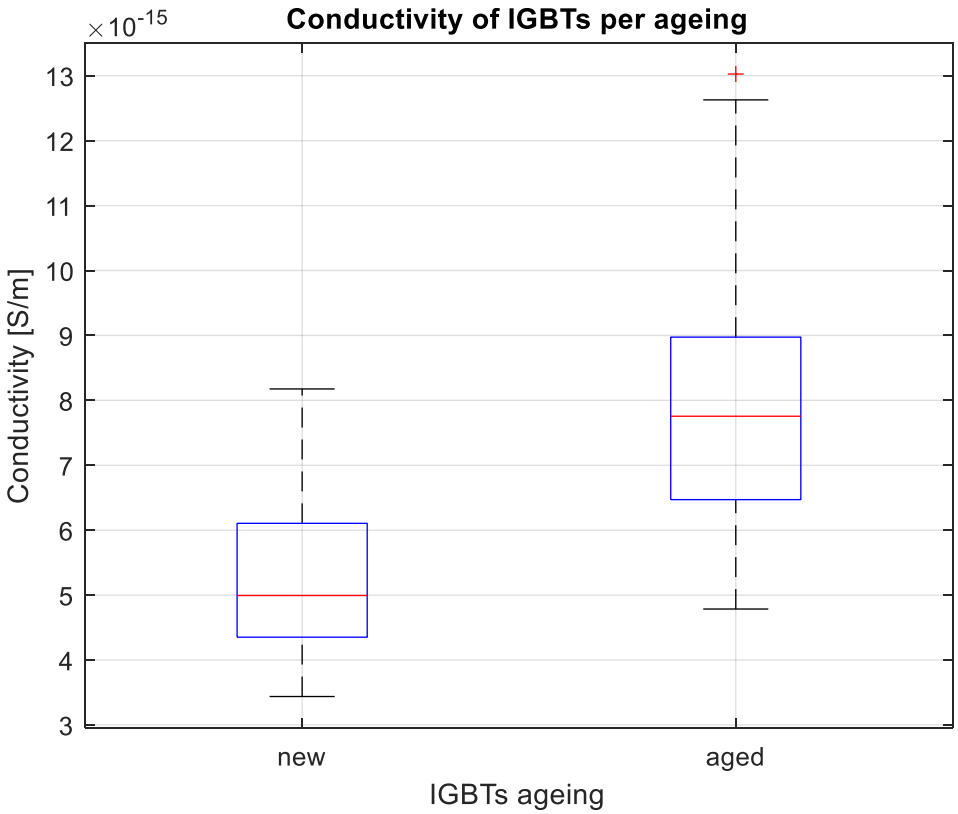


Figure 83. Boxplot of IGBT modules conductivity in function of ageing.

Table 12. Mean and standard deviation of tested modules in function of ageing.

Estimation of conductivity parameters		
IGBT ageing	**μ mean [S/m]**	**σ standard deviation**
New	5.36E-15	1.39E-15
Aged	8.11E-15	2.05E-15

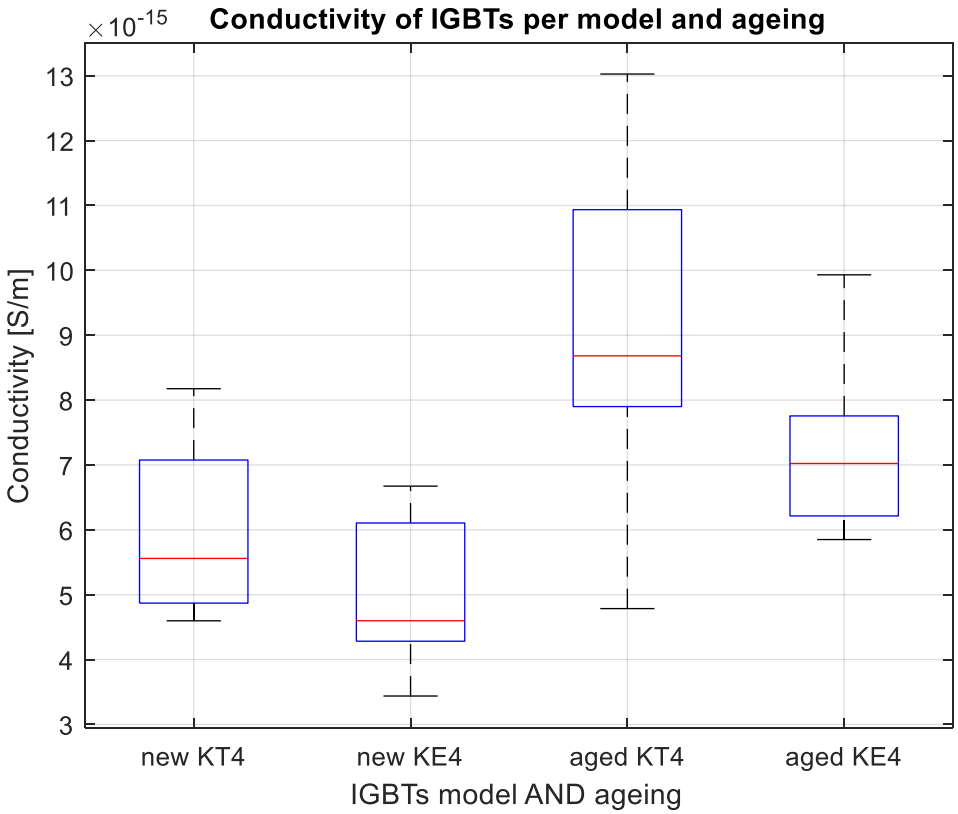


Figure 84. Boxplot of IGBT modules conductivity in function of ageing and model.

Table 13. Mean and standard deviation of tested modules in function of ageing.

Estimation of conductivity parameters		
IGBT	**μ mean [S/m]**	**σ standard deviation**
KT4 - New	5.97E-15	1.57E-15
KE4 - New	4.95E-15	1.22E-15
KT4 - Aged	9.19E-15	2.40E-15
KE4 - Aged	7.22E-15	1.13E-15

In interpreting results a complication arises. Alumina, which is the ceramic dielectric, is not the only part of insulation tested because silica-gel encapsulation can contribute to conductivity, in fact the leakage current can pass not only through DBC but also superficially through the gel, which wraps all the solid component.

It's difficult to understand if any differences or anomalies in conductivity values are attributable to the degradation of one or the other component of insulation. Nevertheless, a conclusion can be drawn. In fact, as figures 83 and 84 show, conductivity of new modules

is generally lower than that of aged ones. Gap between average values isn't huge. It's about 2.5-3 * 10^{-15} S/m in absolute value but focusing on relative value, increase of conductivity is between 46 % and 54 %.

Considering the promising results, a starting point is to measure the conductivity of specimens with the same identical characteristics but with a different ageing in order to discover an empirical-mathematical formula that links degradation of the insulation with the life of the component.

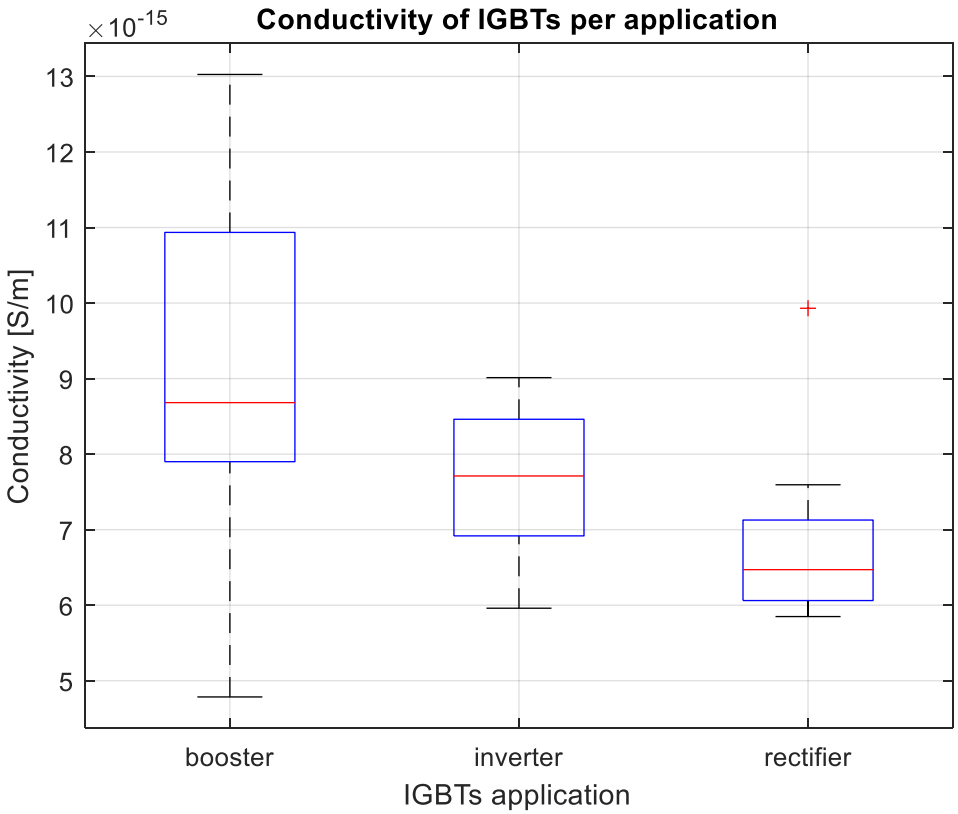


Figure 85. Boxplot of IGBT modules conductivity in function of application.

Table 14. Mean and standard deviation of tested modules in function of application.

Estimation of conductivity parameters		
IGBT application	**μ mean [S/m]**	**σ standard deviation**
Buck-booster	9.19E-15	2.40E-15
Inverter	7.64E-15	1.01E-15
Rectifier	6.80E-15	1.12E-15

The most interesting aspect is that IGBT used in buck-boosters have a large dispersion in conductivity, so there might be differences in stress to which they are subjected for this application. While inverter and rectifier results are closer, that might indicate that stress is uniform between modules. That is in agreement with considerations made for PDIV analysis.

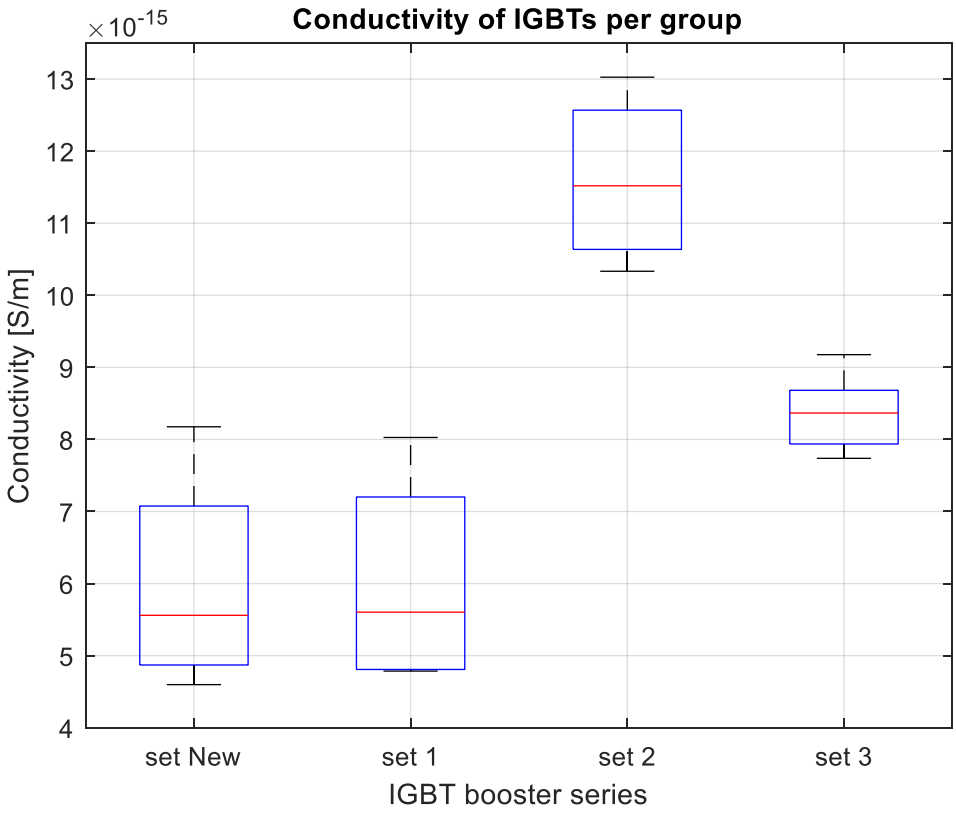


Figure 86. Boxplot of buck-booster IGBT modules conductivity divided by set provenance

A more in-depth analysis was conducted on modules from buck-boosters. Graphs of figure 86 emphasizes the big variability on buck-booster module results. New "KT4" model modules were compared with different series of aged IGBT. Set 1 (composed of aged IGBT A1 ÷ A4) has a very similar behaviour of new ones while set 2 (IGBT 19 ÷ 26) and set 3 (IGBT 33 ÷ 40), which comes from the same UPS machine, have conductivity values higher than new modules but also different from each other. This fact might be explained hypothesizing that they were subjected to different stresses, electric or thermal, maybe they were placed in different locations one much farther away from the cooling system.

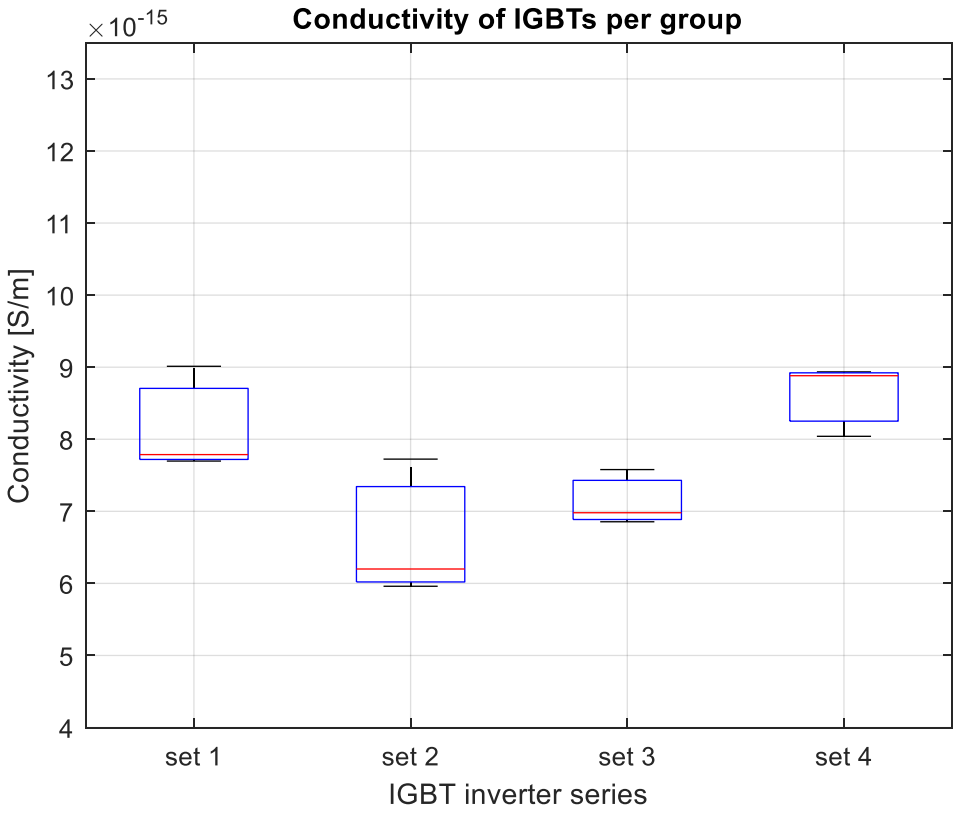


Figure 87. Boxplot of inverter IGBT modules conductivity divided by set provenance

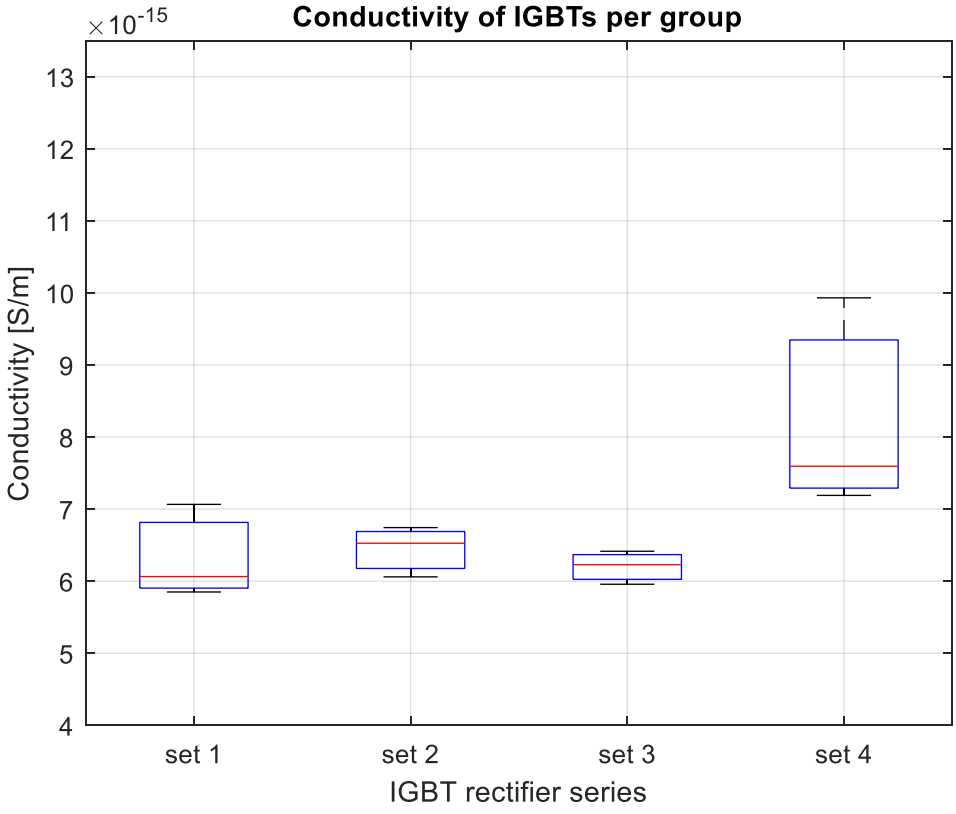


Figure 88. Boxplot of rectifier IGBT modules conductivity divided by set provenance

From boxplot of figures 87 and 88 (in which the same y axis scale of figure 86 was specially taken) it's evident that deviation in conductivity values between different sets of aged modules (all from the same UPS machine) is much less marked, practically nothing for almost all cases.

Polarization trend

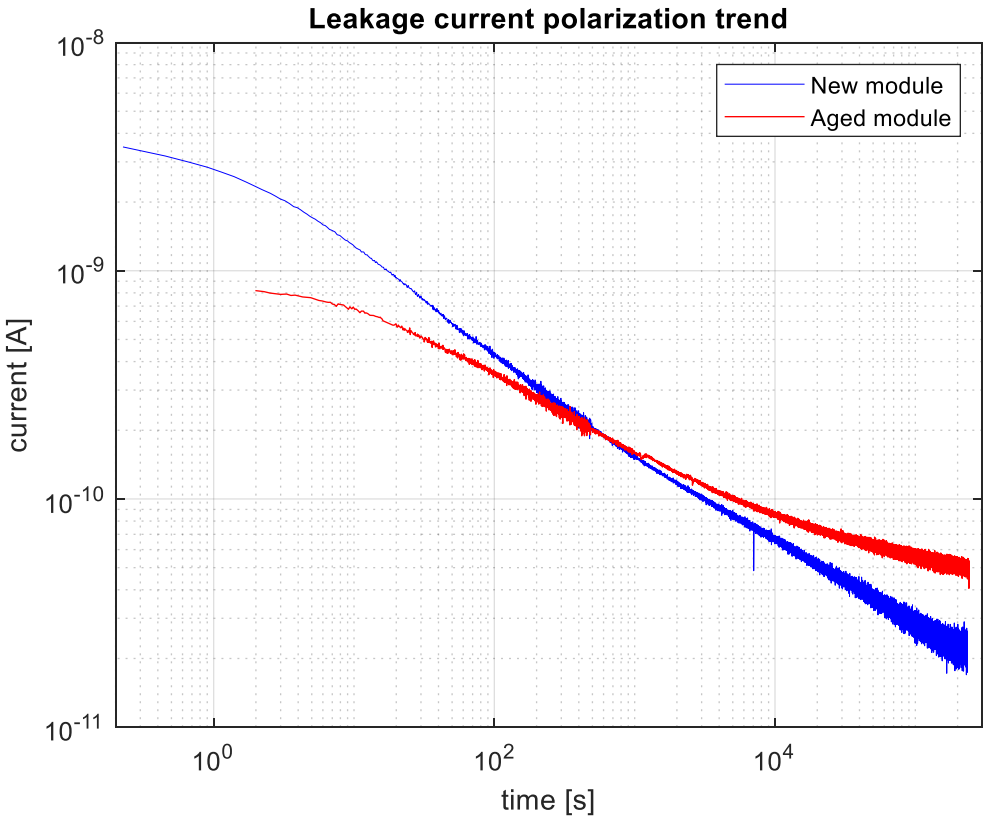


Figure 89. Comparison of two polarization curves of a new module (blue) and an aged one (red).

The slope characterizing the polarization current of aged modules is lower than with new ones. Indeed, fitting leakage current trends with a common empirical power law:

$$J = J_0\, t^{\gamma} \tag{3}$$

and observing the value of the exponent γ, new specimens are characterized by values always above -0.3, while aged modules feature higher values, up to -0.13.

Model and simulations

The outcome of PDIV measurements were also correlated with modelling of the electric field distribution in the module, providing insights on possible locations of the defects highlighted by PDIV measurements. A 2D electrostatic model was built and run in COMSOL Multiphysics, reproducing the same testing conditions used to stress those modules for PD measurements, highlighting those locations that are most possibly able to incept PD activity, when a defect is present.

Model creation

Through an exploded module and photos of sectioned faulted IGBTs (like that in figure 90), it was possible to trace the internal connections of the system.

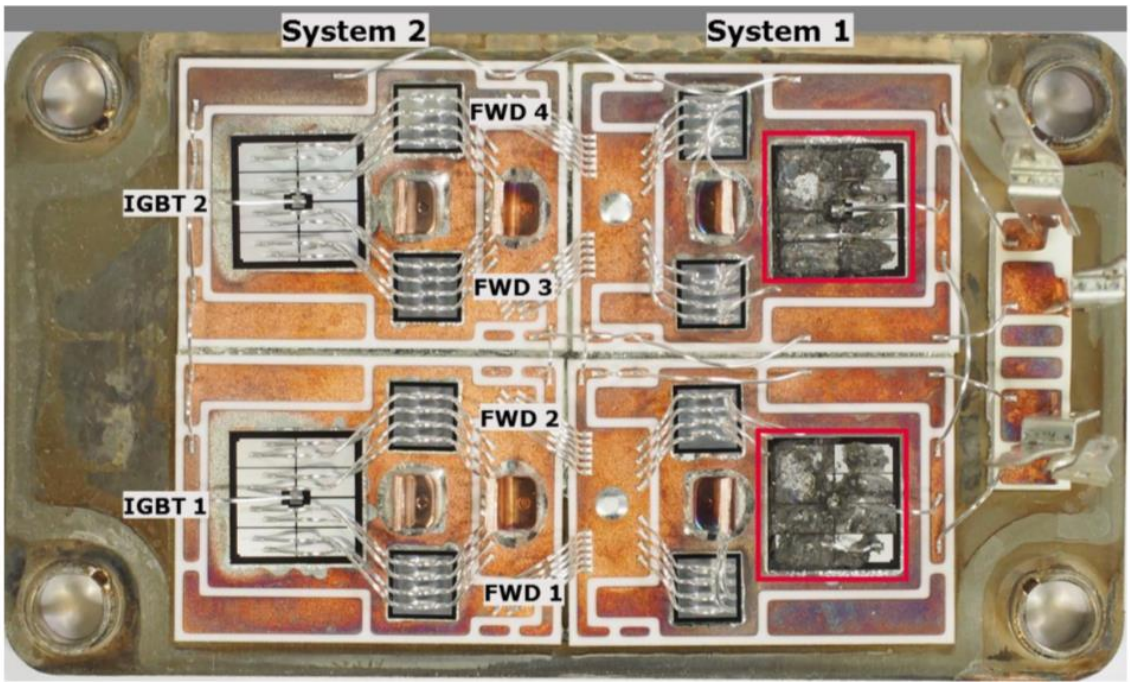


Figure 90. Overview image of module P03 after removal of housing and gel. The destroyed IGBTs are marked in red.

Internal horizontal section of IGBT is drawn with software “Fusion 360”, then a coloured map of internal structure of contacts is realized and shown in figure 91. It constitutes a simple bidimensional model of IGBT, which is object of electric field simulations.

Figure 91. Cross section of internal structure of IGBT module surface.

Simulations results

The aim of simulations, made with “COMSOL Multiphysics 5.6”, a cross-platform finite element analysis, solver and simulation software, is to calculate electric field applied to the insulation of module for all the tests carried out and to find critical points, where the field reach its maximum value.

The electric potential and electric field distribution obtained from simulations, for an applied voltage of 1.2 kVpk under testing conditions of circuit of figure 54 (partial discharges in DBC) and no defective regions, are shown in Figure 92 ÷ 94 below.

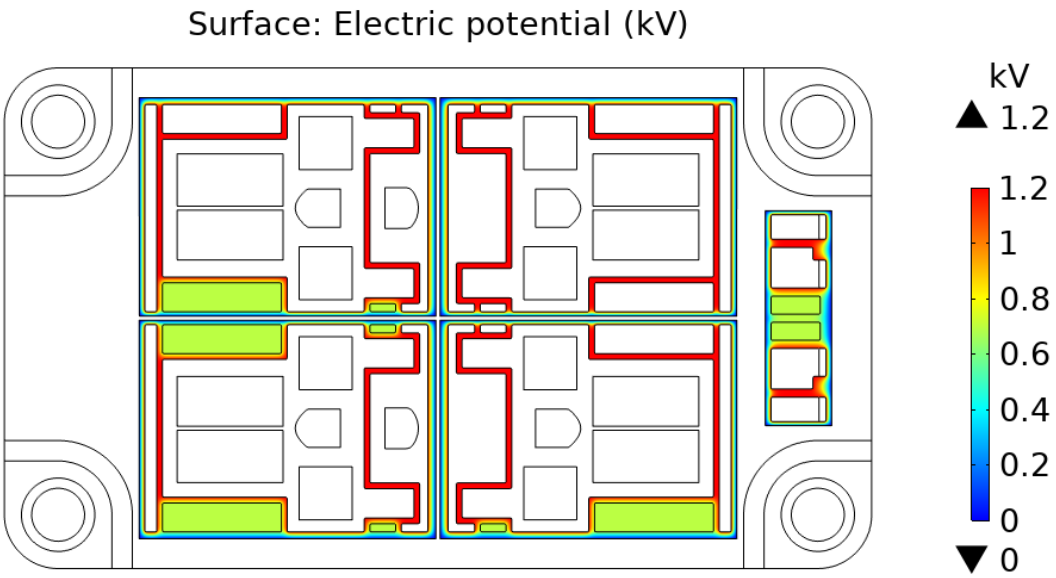


Figure 92. Potential distribution in module PD test simulation

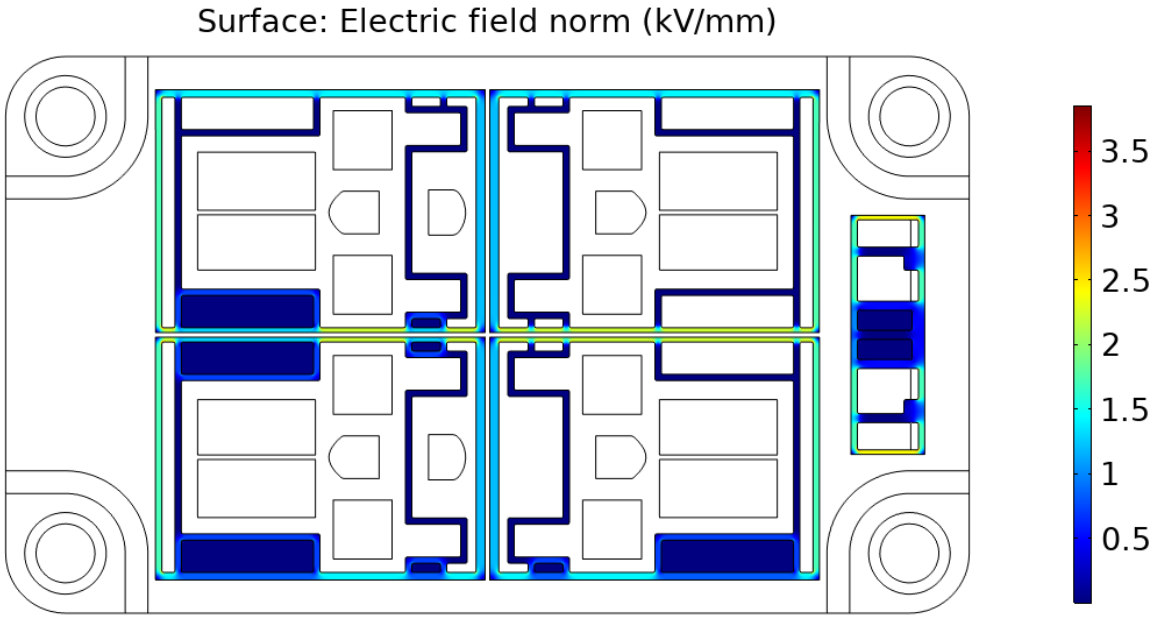


Figure 93. Electric field distribution in module PD test simulation

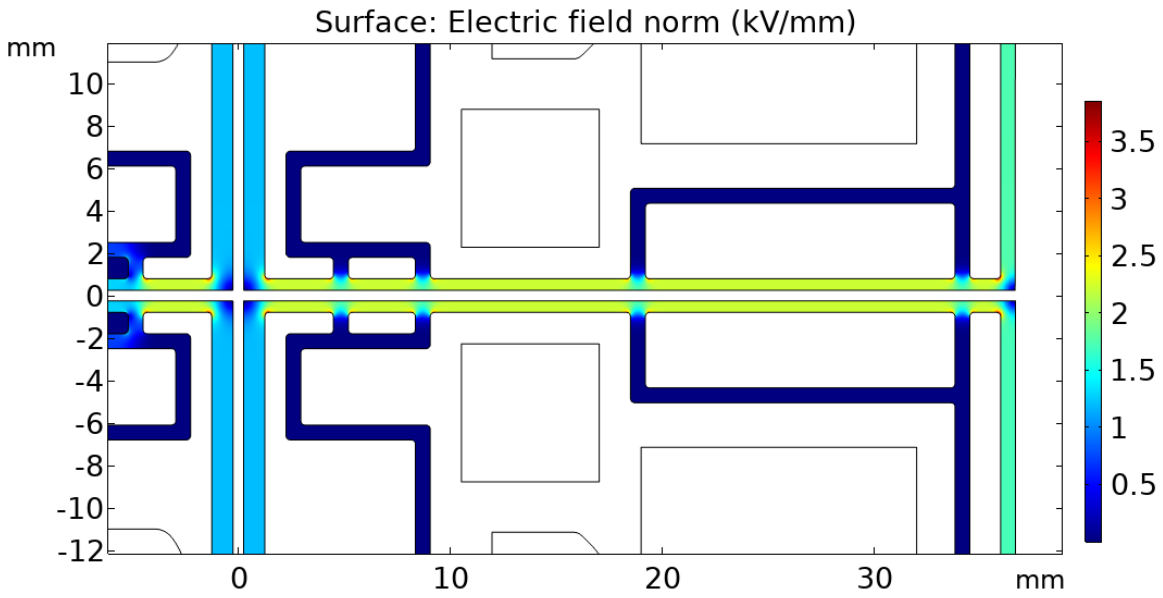


Figure 94. Zoom of right middle area of figure 0.4

Practically no PD activity was detected during single pairs IGBT tests, up to an applied voltage of 1.2 kV_{pk}, both at room and working temperatures.

This is due to the fact that under those conditions, the dielectric is stressed in different locations than before, as shown in Figures 95 and 96, representing the electric field distributions obtained by the 2D model for testing conditions stressing respectively the insulation of top and bottom IGBT pairs (as showed in circuit of figure 56 57).

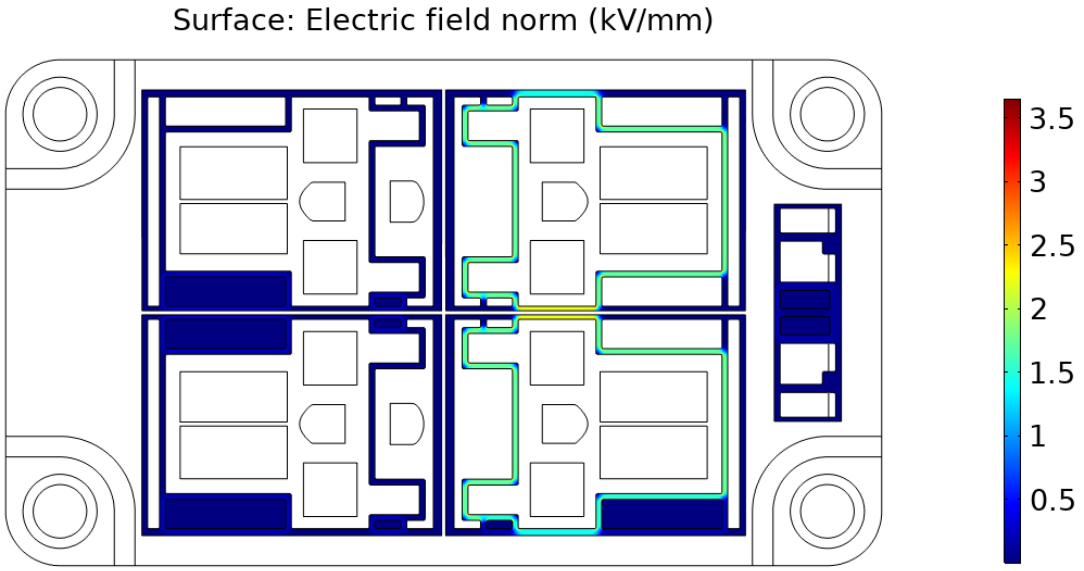


Figure 95. Electric field distribution in single pairs TOP IGBT PD test simulation

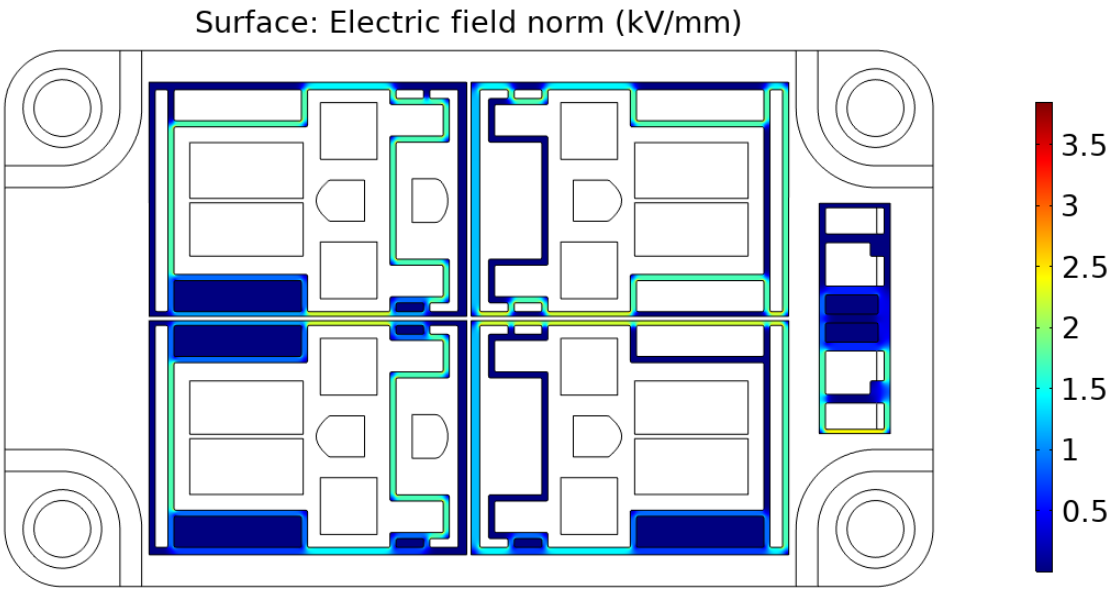


Figure 96. Electric field distribution in single pairs BOTTOM IGBT PD test simulation

To simulate the presence of a cavity, another type of simulation was run. A vertical section model was built at the red segment of horizontal section, as showed in figure 97.

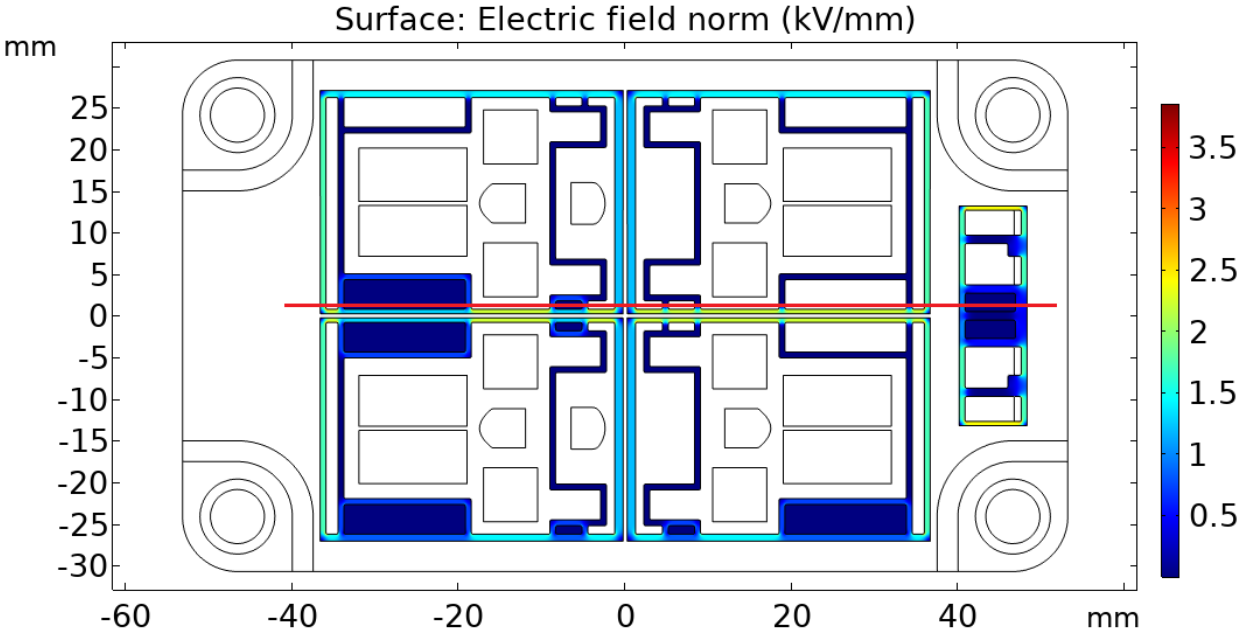


Figure 97. red line represents section line.

The model obtained is represented in figure 98.

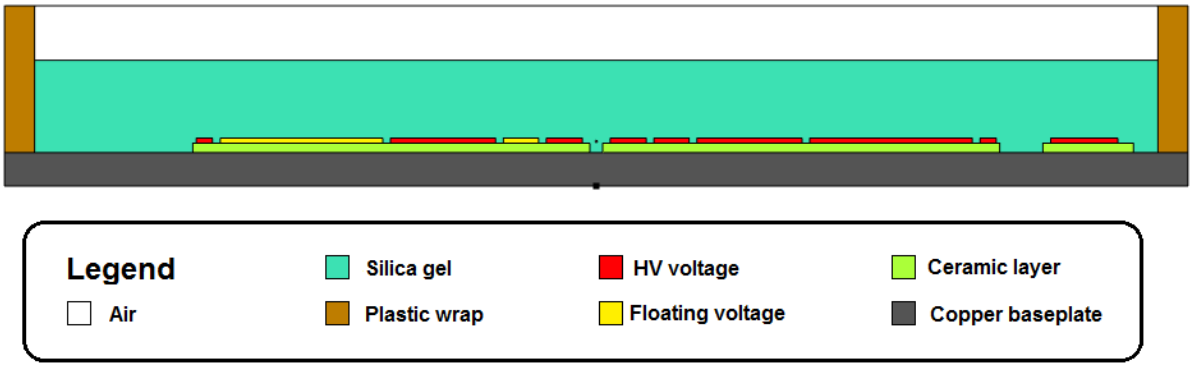


Figure 98. Vertical section of IGBT module

The first case analysed is a circular air cavity with different radius that it's placed inside the silica gel in various point of vertical geometry. All simulation results are shown in table 17 in the appendix. By way of example, one of them is reported in the next images. The cavity is centred, in the middle between two ceramic layers. Its centre has coordinates (0,4) mm and the radius is 100 µm. In figure 99 and 100 are represented respectively electric potential distribution and electric field distribution inside ceramic layer and silica gel of the aforementioned situation.

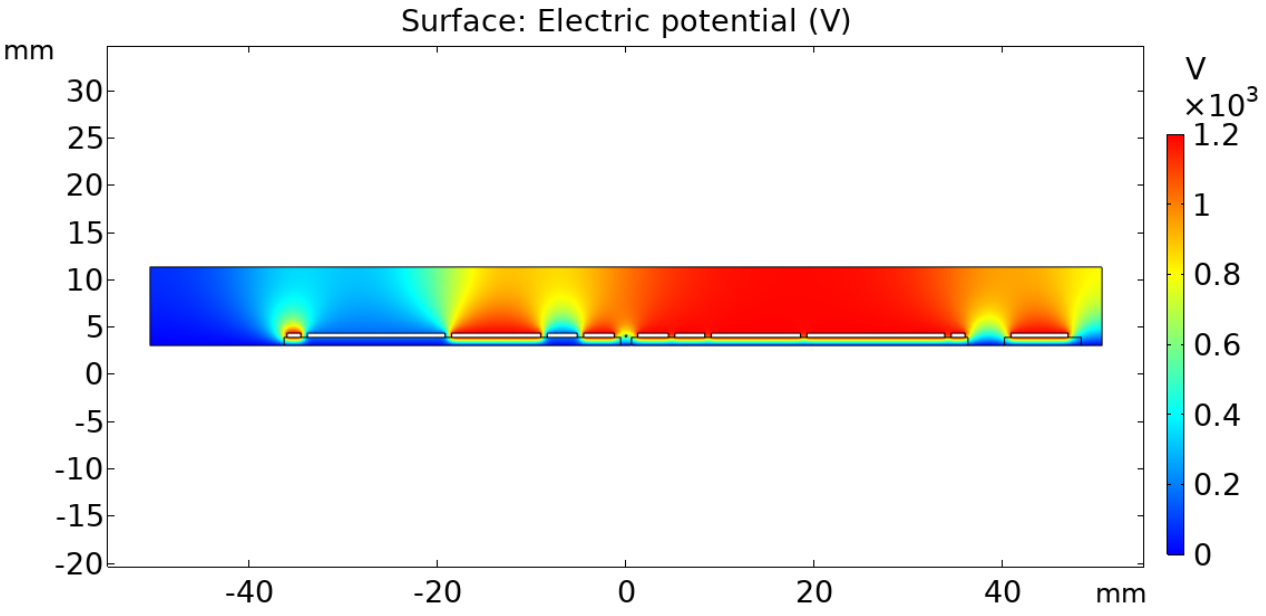


Figure 99. Electric potential distribution in a cavity presence simulation

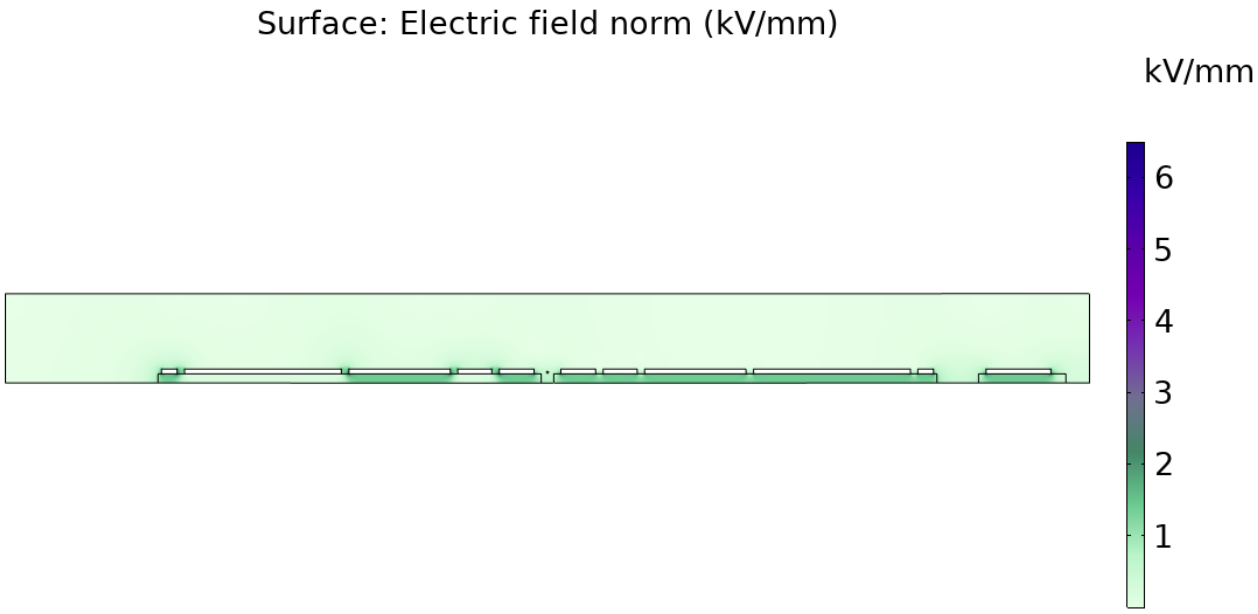


Figure 100. Electric field distribution in presence of cavity simulation

Electric field distribution and maximum and minimum values inside the air bubble are shown in figure 101.

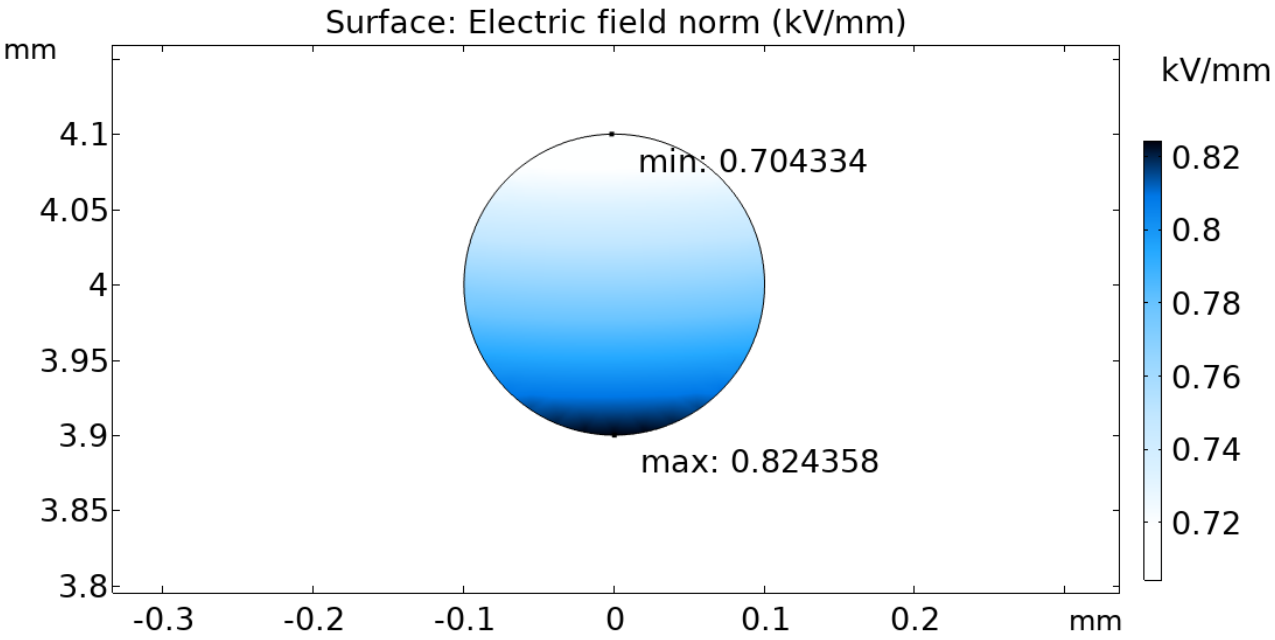


Figure 101. Electric field distribution inside the circular air defect, in the case of cited example

In the case of a circular cavity, maximum electric field inside it are rarely over 4 kV/mm, and thanks to the empirical formula:

$$E_{inc} = 25.2\, p \left(1 + \frac{8.6}{\sqrt{2\, p\, r}}\right) \tag{4}$$

where r is the cavity's radius (expressed in m) and p is the pressure (expressed in Pa), the estimated inception electric field for a cavity with radius of 100 μm is about 7.4 kV/mm.

Different is the case of a semi-circular cavity, which is obviously leaning against a ceramic or copper plate. If air defect is between a grounded or floating plate and a high voltage plate, gradient of electric field along tangential direction is strong enough to cause inception of PD, hence there are a lot of probabilities that partial discharge occurs. An air bubble of this nature is not so unlikely because the silica-gel is quite viscous and in points where the gel doesn't perfectly adhere to surface it has to cover a cavity may form.

An example of a semi-circular air cavity simulation is reported in figures 102 and 103. The cavity centre has coordinates (3.85; 40.70) mm and a radius equal to 100 μm. It is placed on a ceramic layer on which a floating pad in the gate contacts area lies.

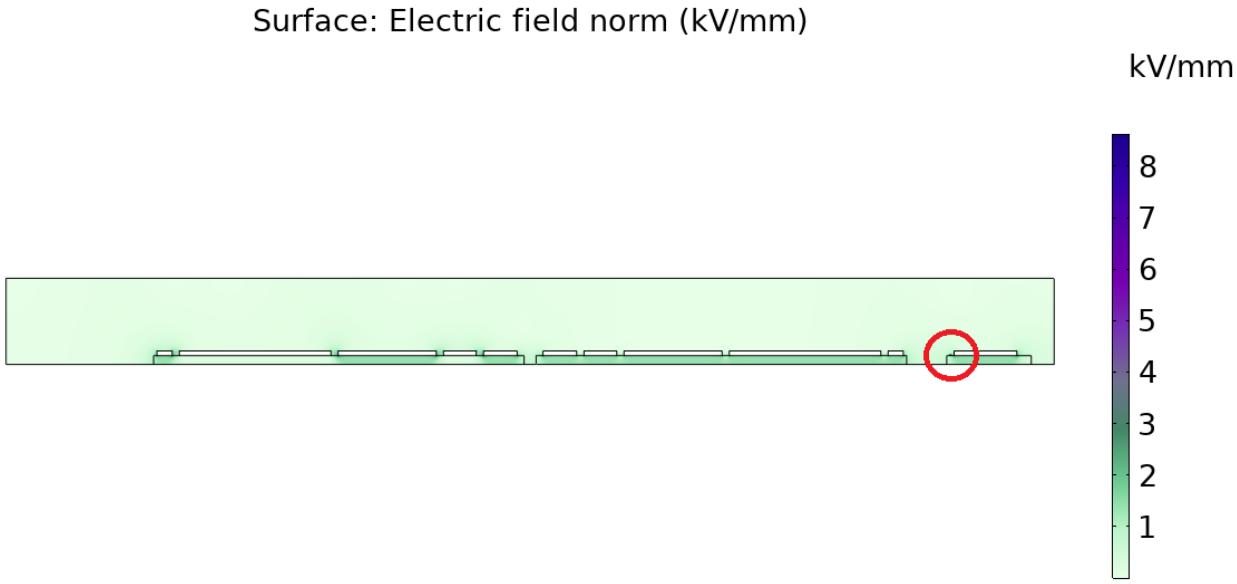


Figure 102. Electric field distribution in presence of cavity simulation, in the case of cited example. The position of the defect is highlighted with the red circle

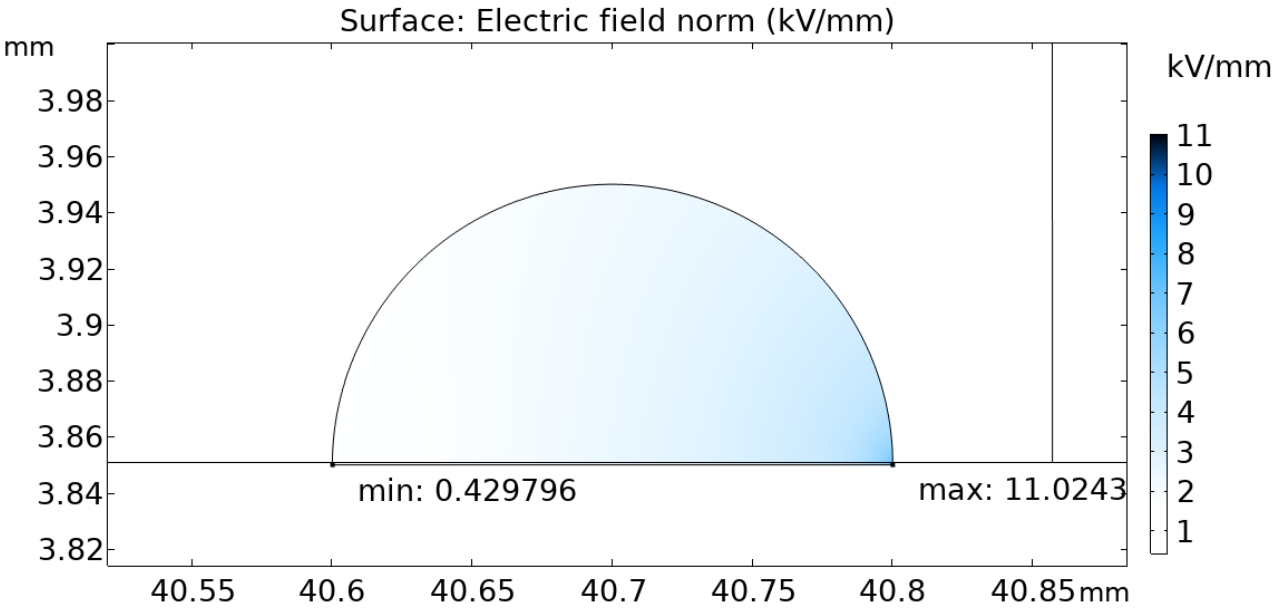


Figure 103. Electric field distribution inside a semi-circular air defect, in the case of cited example

For semi-circular cavity simulations too, obtained results is reported in the table 18 in the appendix.

A more realistic model is realized, representing the IGBT module in a three-dimensional way, to check that electric field values obtained in 2D simulations were similar to 3D ones.

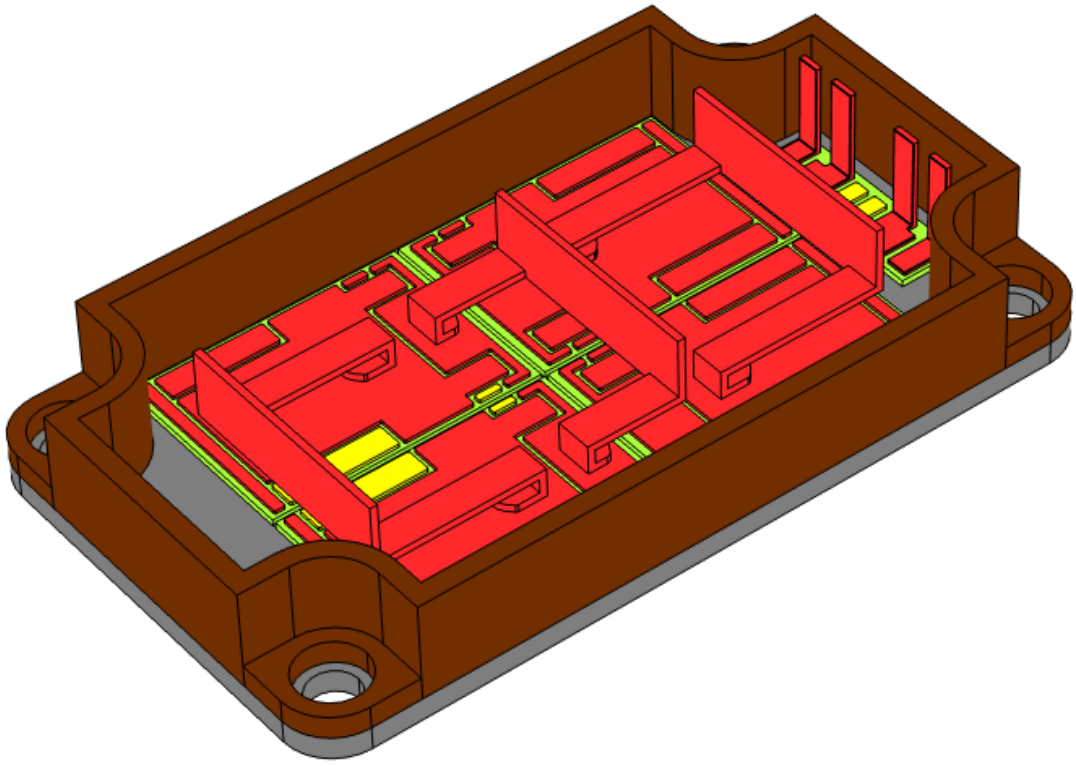


Figure 104. 3D model of IGBT module

Electric field distribution obtained with 3D model are similar to the more approximate ones of 2D model. In particular, critical point positions are in agreement for both simulations (as figure 105 confirms).

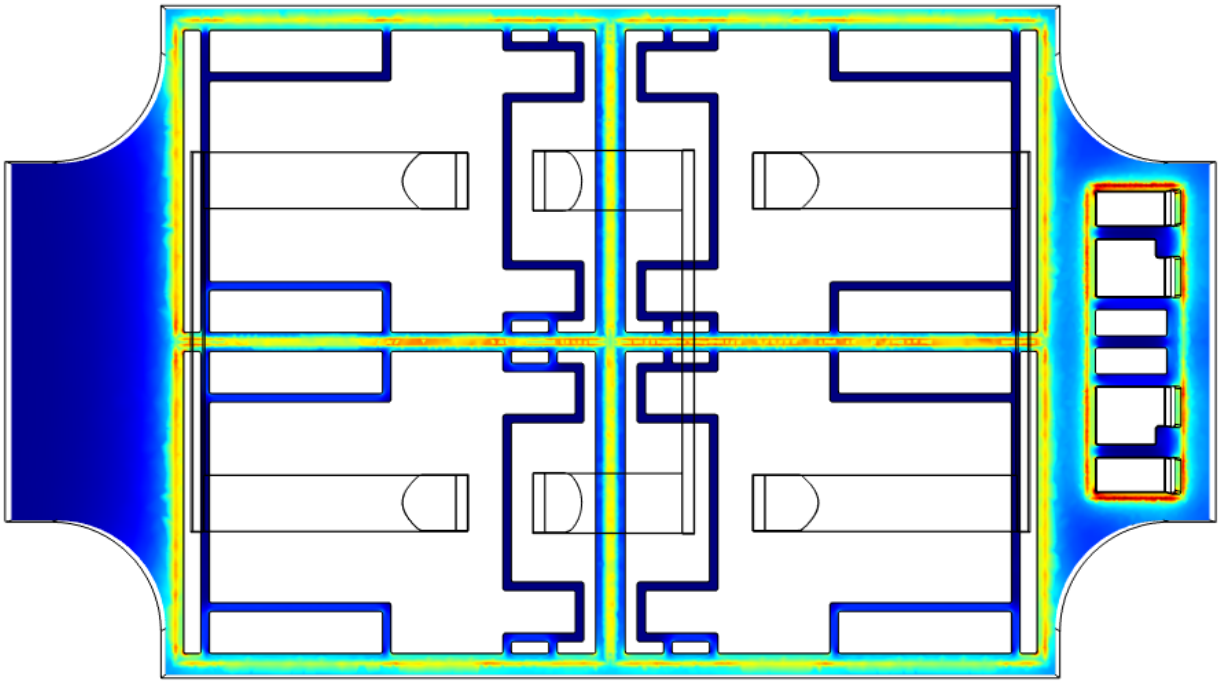


Figure 105. Electric field distribution of a horizontal section of module obtained from 3D model simulation.

Weak points of insulation, thus where electric field is the highest, are located near gate pads and in spaces between two ceramic substrates. This fact is also widely confirmed by the photos taken to view partial discharges, where PD occur close to the gate terminal block (figures 74 - 75).

Conclusion

Power electronics is gaining more and more importance in industry and society. Given the growing number of applications, power electronic systems have to face the most disparate environments and field conditions. Therefore, the issue of reliability has become as fundamental as efficiency for power electronics market. Reliability is the ability of a system or component to perform its required functions under stated conditions for a specified period of time. The requested lifetime of power electronics systems is seldom below 10 years and can reach up to 30 years.

Within this macro topic, this thesis focused on a specific component, currently one of the most widespread semiconductor devices that is IGBT module, in particular on its insulation system. The first step was to study in depth the problem of component's reliability through detailed research of possible and most frequent failure modes.

After that, two main types of tests were carried out. They are measurement of PDIV and PD activity, under different waveforms and temperatures and measurement of leakage current and conductivity at working temperature. Statistical data post-processing was realized, in order to evaluate the conductivity and partial discharges relative quantities such as PDIV, with a view to finding a correlation between electrical parameters and the state of health of IGBT modules.

PD tests had different circuit configurations to stress both the insulation of entire module and IGBT and anti-parallel diode single block. In the first test, almost all modules were affected by PDs but in the second one no PD were detected. PDIV is certainly affected by aging, but other known factors as for example internal geometry and circuit configuration of IGBT module and

unknown factors such as temperature and humidity storage and working conditions contribute to determine its value.

A PRPD pattern analysis was also made to understand what type of discharges affects the insulation. It reveals that there are different types of defects in the insulation because both internal and superficial partial discharges were detected, and the former are more common.

As far as conductivity tests are concerned ageing acts on leakage current increasing it. Further studies and simulations are needed to understand which part of the insulation is involved, i.e. if silica gel affects the measurement or if the detected conductivity is to be only attributed to the ceramic layer of DBC.

Obtained results are in general promising, but further investigations on a larger dataset have to be conducted in order to create or improve a life prediction algorithm based on PDIV and conductivity value.

Software simulations were also run to support measurement results. The aim of these simulations was to observe electrical field distribution inside insulation to find out critical points, in which there are more probabilities a PD occurs. Simulation results showed that electrical field step up in silica gel filled spaces between two adjacent ceramic layers, close to gate terminal pad and obviously at copper layer sharp edges.

Appendix

Table 15. Characteristics and conductivity value of IGBT modules

Name	Model	Application	Ageing	Conductivity [S/m]
A1	KT4	Buck/Booster	Aged	8.03E-15
A2	KT4	Buck/Booster	Aged	6.38E-15
A3	KT4	Buck/Booster	Aged	4.83E-15
A4	KT4	Buck/Booster	Aged	4.79E-15
N1	KT4	\	New	4.60E-15
N2	KT4	\	New	8.18E-15
N3	KT4	\	New	5.98E-15
N4	KT4	\	New	5.14E-15
1	KE4	Inverter	Aged	7.70E-15
2	KE4	Inverter	Aged	9.01E-15
3	KE4	Inverter	Aged	7.79E-15
4	KE4	Rectifier	Aged	7.07E-15
5	KE4	Rectifier	Aged	6.06E-15
6	KE4	Rectifier	Aged	5.85E-15
7	KE4	Rectifier	Aged	6.53E-15
8	KE4	Rectifier	Aged	6.06E-15
9	KE4	Rectifier	Aged	6.74E-15
10	KE4	Rectifier	Aged	5.96E-15
11	KE4	Rectifier	Aged	6.41E-15
12	KE4	Rectifier	Aged	6.23E-15
13	KE4	Inverter	Aged	5.96E-15
14	KE4	Inverter	Aged	6.20E-15
15	KE4	Inverter	Aged	7.72E-15
16	KE4	Inverter	Aged	6.98E-15
17	KE4	Inverter	Aged	6.86E-15
18	KE4	Inverter	Aged	7.58E-15
19	KT4	Buck/Booster	Aged	1.05E-14
20	KT4	Buck/Booster	Aged	1.08E-14
21	KT4	Buck/Booster	Aged	1.20E-14
22	KT4	Buck/Booster	Aged	1.03E-14
23	KT4	Buck/Booster	Aged	1.30E-14
24	KT4	Buck/Booster	Aged	1.11E-14
25	KT4	Buck/Booster	Aged	1.25E-14
26	KT4	Buck/Booster	Aged	1.26E-14
27	KE4	Rectifier	Aged	7.59E-15
28	KE4	Rectifier	Aged	7.19E-15
29	KE4	Rectifier	Aged	9.93E-15
30	KE4	Inverter	Aged	8.04E-15
31	KE4	Inverter	Aged	8.94E-15
32	KE4	Inverter	Aged	8.88E-15
33	KT4	Buck/Booster	Aged	7.74E-15
34	KT4	Buck/Booster	Aged	8.45E-15
35	KT4	Buck/Booster	Aged	9.18E-15
36	KT4	Buck/Booster	Aged	8.28E-15
37	KT4	Buck/Booster	Aged	7.77E-15
38	KT4	Buck/Booster	Aged	8.49E-15
39	KT4	Buck/Booster	Aged	8.87E-15
40	KT4	Buck/Booster	Aged	8.10E-15
N5	KE4	\	New	4.35E-15
N6	KE4	\	New	3.44E-15
N7	KE4	\	New	4.28E-15
N8	KE4	\	New	6.11E-15
N9	KE4	\	New	4.84E-15
N10	KE4	\	New	6.67E-15

Table 16. Average PDIV value for each IGBT module

Name	PDIV [kV] IGBT module		
	Sinusoidal voltage		Square voltage
	Room temperature	Working temperature	Working temperature
A1	1.34	1.26	1.32
A2	1.27	1.09	1.23
A3	1.27	1.22	1.36
A4	1.24	1.25	1.33
N1	1.48	1.20	1.43
N2	1.36	1.25	1.33
N3	1.43	1.37	1.58
N4	1.29	1.23	1.34
1	1.68	1.71	> 2 kV
2	1.18	> 2 kV	> 2 kV
3	1.89	1.98	> 2 kV
4	> 2 kV	> 2 kV	> 2 kV
5	1.41	1.45	1.53
6	1.55	1.64	1.78
7	1.51	1.39	1.53
8	1.57	1.48	1.56
9	1.86	1.64	1.78
10	1.52	1.30	1.31
11	1.42	1.33	1.34
12	1.42	1.30	1.61
13	1.68	1.58	1.75
14	1.53	1.48	2.21
15	1.59	1.52	1.97
16	1.65	1.60	1.51
17	1.52	1.43	2.01
18	1.91	1.94	> 2 kV
19	1.38	1.27	1.45
20	1.46	1.27	1.30
21	1.35	1.28	1.37
22	1.36	1.26	1.41
23	1.39	1.32	1.33
24	1.34	1.16	1.32
25	1.34	1.29	1.42
26	1.46	1.36	1.52
27	1.51	1.59	2.01
28	1.60	1.60	1.60
29	1.56	1.49	1.95
30	1.48	1.46	1.66
31	> 2 kV	> 2 kV	1.85
32	1.97	> 2 kV	> 2 kV
33	1.48	1.50	1.83
34	1.47	1.45	1.64
35	1.50	1.44	1.45
36	1.50	1.46	1.65
37	1.71	1.92	2.16
38	1.53	1.77	2.52
39	1.58	1.46	1.96
40	1.60	1.43	1.75
N5	> 2 kV	> 2 kV	> 2 kV
N6	> 2 kV	> 2 kV	> 2 kV
N7	> 2 kV	> 2 kV	> 2 kV
N8	> 2 kV	> 2 kV	> 2 kV
N9	> 2 kV	> 2 kV	> 2 kV
N10	> 2 kV	1.69	1.95

Table 17. Circular air cavity simulation results

Coordinate of the center (x axis) [mm]	Coordinate of the center (y axis) [mm]	Radius [um]	Applied voltage [kV]	Maximum electric field [kV/mm]	Maximun electric field inside the cavity [kV/mm]	Minimum electric field inside the cavity [kV/mm]	Difference between maximum and minimum [kV/mm]
-36.2800	4.0000	100	1.2	6.564	1.766	1.258	0.508
-36.1700	4.0000	100	1.2	7.501	2.270	1.451	0.819
-36.1200	4.0000	100	1.2	7.827	2.550	1.566	0.984
-36.0570	4.4000	100	1.2	6.501	2.208	1.149	1.059
-36.0570	4.3500	100	1.2	6.413	2.845	1.240	1.605
-36.0570	4.0000	100	1.2	9.617	3.001	1.564	1.437
-36.0070	4.4000	100	1.2	6.405	2.899	1.171	1.728
-35.2305	5.0000	100	1.2	6.404	0.698	0.587	0.111
-35.2305	4.8000	100	1.2	6.404	0.811	0.695	0.116
-35.2305	4.4000	100	1.2	6.405	0.902	0.575	0.327
-35.2305	4.5000	100	1.2	6.488	0.908	0.845	0.063
-19.2000	4.4100	100	1.2	6.412	3.481	1.194	2.287
-19.1000	4.0000	100	1.2	6.852	1.936	1.165	0.771
-19.0500	4.0000	100	1.2	7.181	1.954	1.476	0.478
-19.0500	4.3000	100	1.2	6.498	2.438	1.657	0.781
-18.8500	4.3000	100	1.2	6.500	2.125	1.663	0.462
-18.8500	4.0000	100	1.2	8.350	2.413	1.811	0.602
-18.6500	4.3000	100	1.2	7.039	2.789	1.763	1.026
-18.6500	4.0000	100	1.2	9.497	3.423	2.325	1.098
-18.6000	4.4000	100	1.2	6.747	2.764	1.429	1.335
-18.6000	4.0000	100	1.2	10.923	3.844	2.088	1.756
-18.5500	4.4000	100	1.2	7.112	3.583	1.378	2.205
-18.5000	4.4100	100	1.2	7.304	3.964	1.274	2.690
-6.7720	8.0000	100	1.2	6.499	0.085	0.076	0.009
-6.7720	6.0000	100	1.2	6.502	0.281	0.250	0.031
-6.7720	5.5000	100	1.2	6.507	0.369	0.332	0.037
-6.7720	5.0000	100	1.2	6.485	0.456	0.423	0.033
-6.7720	4.4000	100	1.2	6.407	0.478	0.305	0.173
-6.7720	4.5000	100	1.2	6.500	0.489	0.474	0.015
-5.0400	4.0000	100	1.2	7.169	1.978	1.483	0.495
-4.8400	4.0000	100	1.2	8.347	2.411	1.818	0.593
-4.6400	4.0000	100	1.2	9.473	3.417	2.322	1.095
-4.6000	4.0000	100	1.2	12.447	3.735	2.285	1.450
-2.8700	4.4000	100	1.2	6.391	0.254	0.157	0.097
-2.8700	4.5000	100	1.2	6.500	0.260	0.242	0.018
-1.1000	4.0000	100	1.2	7.991	2.608	1.464	1.144
-1.0000	4.0000	100	1.2	7.000	2.096	1.301	0.795
-0.9000	4.0000	100	1.2	6.495	1.738	1.152	0.586

0.0000	4.0000	1	1.2	6.411	0.772	0.759	0.013
0.0000	4.0000	10	1.2	6.498	0.777	0.755	0.022
0.0000	5.0000	100	1.2	6.494	0.272	0.204	0.068
0.0000	4.8000	100	1.2	6.487	0.358	0.272	0.086
0.0000	4.4000	100	1.2	6.496	0.581	0.462	0.119
0.0000	4.0000	100	1.2	6.488	0.824	0.704	0.120
0.0000	3.6000	100	1.2	6.489	1.033	0.933	0.100
0.0000	3.5000	100	1.2	6.499	1.073	0.984	0.089
0.0000	3.1000	100	1.2	6.410	1.093	0.729	0.364
0.0000	3.4000	100	1.2	6.503	1.103	1.029	0.074
0.0000	3.2000	100	1.2	6.502	1.113	1.084	0.029
0.0000	4.8000	1000	1.2	6.477	0.914	0.057	0.857
1.0000	4.0000	100	1.2	7.568	2.093	1.304	0.789
1.1000	4.0000	100	1.2	7.974	2.606	1.461	1.145
4.5900	4.4000	100	1.2	6.499	0.315	0.085	0.230
4.5900	4.0000	100	1.2	8.616	2.072	0.708	1.364
4.6000	4.0000	100	1.2	7.112	2.012	0.702	1.310
4.8400	4.4000	100	1.2	6.499	0.261	0.079	0.182
4.8400	4.0000	100	1.2	6.499	1.404	0.671	0.733
5.0800	4.0000	100	1.2	8.149	2.016	0.702	1.314
5.0900	4.4000	100	1.2	6.499	0.314	0.090	0.224
5.0900	4.0000	100	1.2	7.684	2.073	0.708	1.365
36.0570	4.4000	100	1.2	6.499	1.513	0.757	0.756
36.0570	4.0000	100	1.2	9.245	2.809	1.382	1.427
36.1570	4.4000	100	1.2	6.499	1.196	0.758	0.438
36.1570	4.0000	100	1.2	7.097	2.168	1.332	0.836
36.2185	4.4000	100	1.2	6.499	1.099	0.743	0.356
36.2185	4.0000	100	1.2	6.590	1.871	1.232	0.639
38.2185	5.0000	100	1.2	6.499	0.351	0.312	0.039
38.2185	4.8000	100	1.2	6.499	0.392	0.350	0.042
38.2185	4.4000	100	1.2	6.414	0.477	0.434	0.043
38.2185	4.0000	100	1.2	6.499	0.558	0.518	0.040
38.2185	3.1000	100	1.2	6.499	0.617	0.396	0.221
38.2185	3.6000	100	1.2	6.499	0.619	0.589	0.030
38.2185	3.5000	100	1.2	6.499	0.629	0.603	0.026
38.2185	3.2000	100	1.2	6.499	0.633	0.607	0.026
38.2185	3.4000	100	1.2	6.499	0.635	0.614	0.021
40.2185	4.4000	100	1.2	6.499	0.817	0.639	0.178
40.2185	4.0000	100	1.2	6.499	1.151	0.861	0.290
40.2185	3.9500	100	1.2	6.406	1.187	0.837	0.350
40.6570	4.4000	100	1.2	6.499	1.300	0.803	0.497
40.6570	4.0000	100	1.2	8.068	2.468	1.518	0.950
40.6570	3.9500	100	1.2	10.009	2.717	1.605	1.112
40.7570	4.4000	100	1.2	6.499	1.639	0.809	0.830
40.7570	4.0000	100	1.2	10.737	3.144	1.242	1.902
40.7570	3.9500	100	1.2	14.986	4.138	1.793	2.345
43.8770	4.4000	100	1.2	6.406	0.144	0.093	0.051

43.8770	5.0000	100	1.2	6.499	0.146	0.141	0.005
43.8770	4.6000	100	1.2	6.499	0.150	0.147	0.003
46.9970	4.4000	100	1.2	6.592	1.900	0.953	0.947
46.9970	4.0000	100	1.2	10.630	3.352	1.690	1.662
46.9970	3.9500	100	1.2	13.555	4.368	1.938	2.430
47.0970	4.4000	100	1.2	6.499	1.496	0.941	0.555
47.0970	4.0000	100	1.2	8.003	2.647	1.681	0.966
47.0970	3.9500	100	1.2	9.729	2.889	1.760	1.129
47.4970	4.4000	100	1.2	6.499	0.969	0.749	0.220
47.4970	4.0000	100	1.2	6.499	1.368	1.055	0.313
47.4970	3.9500	100	1.2	6.406	1.398	1.047	0.351
47.9970	4.4000	100	1.2	6.499	0.669	0.560	0.109
47.9970	4.0000	100	1.2	6.499	0.845	0.694	0.151
47.9970	3.9500	100	1.2	6.406	0.861	0.689	0.172
48.3970	4.4000	100	1.2	6.499	0.522	0.459	0.063
48.3970	3.6000	100	1.2	6.406	0.530	0.432	0.098
48.3970	4.0000	100	1.2	6.499	0.585	0.503	0.082
48.4970	4.4000	100	1.2	6.499	0.494	0.440	0.054
48.4970	3.6000	100	1.2	6.499	0.522	0.491	0.031
48.4970	4.0000	100	1.2	6.499	0.535	0.482	0.053

Table 18. Semi-circular air cavity simulation results

Coordinate of the center (x axis) [mm]	Coordinate of the center (y axis) [mm]	Radius [um]	Applied voltage [V]	Maximum electric field [kV/mm]	Maximun electric field inside the cavity [kV/mm]	Minimum electric field inside the cavity [kV/mm]	Difference between maximum and minimum [kV/mm]
-46.000	3.00	100	1200	6.406	0.049	0.000	0.049
-40.000	3.00	100	1200	6.406	0.209	0.000	0.209
-37.000	3.00	100	1200	6.410	1.320	0.001	1.319
-36.480	3.00	100	1200	6.369	2.179	0.001	2.178
-36.380	3.00	100	1200	6.407	2.159	0.001	2.158
-36.180	3.85	100	1200	12.487	9.198	0.326	8.872
-36.119	3.85	100	1200	16.340	12.462	0.391	12.071
-36.058	3.85	100	1200	57.116	45.715	0.558	45.157
-36.057	3.85	100	1200	75.050	75.026	0.559	74.467
-36.057	3.85	50	1200	17.562	12.167	0.786	11.381
-36.057	3.85	10	1200	13.285	7.554	1.112	6.442
-36.027	3.85	50	1200	21.928	16.737	0.939	15.798
-35.807	4.30	50	1200	6.408	2.511	0.002	2.509
-35.807	4.30	100	1200	6.892	3.308	0.001	3.307
-35.231	4.30	50	1200	6.411	1.444	0.001	1.442
-35.231	4.30	100	1200	6.408	1.461	0.001	1.460
-34.604	4.30	100	1200	55.522	51.506	0.004	51.502
-34.604	4.30	50	1200	8.977	4.178	0.004	4.174
-34.404	3.85	100	1200	94.077	94.077	1.222	92.855
-34.404	3.85	50	1200	18.416	15.055	1.446	13.610
-34.154	3.85	100	1200	9.784	7.915	0.960	6.955
-34.154	3.85	50	1200	9.190	6.431	1.012	5.419
-33.904	3.85	100	1200	23.726	23.726	0.890	22.836
-33.904	3.85	50	1200	7.219	3.914	0.944	2.969
-18.850	3.85	100	1200	10.421	6.965	0.962	6.003
-18.850	3.85	50	1200	9.648	5.724	1.019	4.705
-18.600	3.85	100	1200	81.925	81.925	1.225	80.700
-18.600	3.85	50	1200	25.185	13.026	1.463	11.564
-1.150	3.85	100	1200	66.355	66.355	0.465	65.890
-1.150	3.85	50	1200	16.644	10.090	0.727	9.363
-0.950	3.85	100	1200	9.175	6.118	0.576	5.542
-0.950	3.85	50	1200	8.351	5.019	0.542	4.477
0.000	3.00	100	1200	6.403	1.718	1.165	0.554
40.500	3.85	100	1200	8.596	5.792	0.464	5.327
40.700	3.85	100	1200	20.895	11.024	0.430	10.595

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