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Accuracy and Behaviour of Capacitive Voltage Transformers

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“One measurement is worth a thousand expert opinions.”

-- Donald Sutherland

Acknowledgements

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Table of Contents

List of Figures

Chapter 1

Chapter 2

Chapter 3

List of Tables

Chapter 1

Chapter 3

List of Abbreviations and Acronyms

AC	Alternating Current
CT	Current Transformer
CVT	Capacitive Voltage Transformer
DC	Direct Current
DFT	Discrete Fourier Transform
DSO	Distribution System Operator
EHV	Extra High Voltage
EMU	Electromagnetic Unit
FE	Frequency Measurement Error
FFT	Fast Fourier Transform
GUI	Graphical User Interface
HV	High Voltage
I/O	Inputs and Outputs
IT	Instrument Transformer
LPIT	Low Power Instrument Transformer
PhE	Phase Angle Error
PHIL	Power Hardware-In-the-Loop
PLL	Phase-Locked Loop
PMU	Phasor Measurement Unit
PPS	Pulse Per Second
PQ	Power Quality
PTP	Precision Time Protocol
RAE	Relative Amplitude Error
RCP	Rapid Control Prototyping
RFE	ROCOF Measurement Error
RMS	Root Mean Square
RT	Real-Time
RTS	Real-Time Simulator
SV	Sampled Value
THD	Total Harmonic Distortion
VT	Voltage Transformer
TF	Transfer Function

AC	Accuracy Class
LPVT	Low Power Voltage Transformer
PD	Partial Discharge
PSD	Power Spectral Density

Introduction

Operating the electricity grid under the desired rated conditions is one of the most challenging issues for the system operators. By introducing the Renewable electricity generation, non-linear loads and rise of electric car charging, the power grids faced with more perturbances and this affects the power quality of the system. Consequently, the appropriate monitoring, identification and resolution must be determined. In order to be able to control the system we need to be aware of the operating condition of the grid and the value of the electrical quantities, voltages and currents. Then having a dynamic model of a system, where the energy could flow in both directions and the waveforms could be distorted, accuracy of the measurement devices becomes a vital issue. Instrument Transformers as the key measurement devices in the grid provide us the value of voltages and current of the system that can be used for the protection control, billing and other purposes. In case of high voltage transmission network (≥132KV), the Capacitive Voltage Transformer (CVT) were developed as an alternative to the inductive transformers featuring lower weight, smaller dimension, easier installation in harsh environments, lower costs and larger bandwidth. The CVT secondary voltage is scaled down according to the predefined ratio in the steady state.
During the transient where the system is faced with PQ issues the output voltage of CVT will be affected by the perturbances due to the energy storage elements and there will be a deviation in the scaled down secondary voltage signal in the CVT

In the beginning, the working principle, structure and the components of the CVT is discussed and the possible phenomenon in the CVT related to the transient conditions will be explained. Eventually, the characteristics of the simulation will be discussed.

Figure 1: EHV Substation – FIATO Substation

Chapter 1: Capacitor Voltage Transformer

1.1 CVT Structure, Components and Physical Construction

1.1.1 Basic principles

We always need to make a balance between the cost and the accuracy of the system in order to be able to construct and operate an electrical system. Inductive transformers provide a reasonable characteristic of measuring in low voltages in measuring purposes but at high voltages (above 100kV) the cost of the insulation becomes dominant. Thus, Capacitive Voltage Transformers (CVT) are considered a proper alternative considering their low cost and simpler manufacturing principles.
In an ideal condition, the output waveform signal of a CVT should correspond the input signal specification which is somehow true for the steady-state condition by an accurate design of the device. On the other hand, due to the presence of the non-linear components, capacitors and inductances, during the transient the output voltage will show some deviations.

CVT Applications:

- **Measuring of voltage:** scale down the transmission voltage for metering, protection and control purposes.
- **Transient Recovery Voltage (TRV):** When installing near to HV/EHV Circuit Breakers, CVT's own High Capacitance rises C/B short line performance fault / Transient Recovery Voltage
- **Insulating:** Providing a secure insulation for the control room operators from the HV network and LV circuits
- **HF Transmissions:** Power Line Carrier (PLC) coupling.
  A CVT coupled with a wave trap is used to make a high impedance to the carrier wave high-frequency communication entering into unwanted destinations typically substation. The normal range of carrier wave communication is 150KHz to 800KHz while the power system components are designed to work in 50 or 60 HZ. Then two coupled components are located at the sending and receiving end of substations.

Figure 2: Capacitive Voltage Transformer

1.1.2 Components

The Capacitive Voltage Transformer is consisting of three main components as the capacitive potential divider, inductive element and auxiliary transformer.

In order to step down the line voltage to an intermediate-level voltage the coupling capacitors C1 and C2 are used where functioning as a voltage divider. Base on the design characteristics C1 has a lower capacitance and most of the voltage is dropped across it. For instance, in a 400 KV C1 has a value of 104 pF. Then at the output of C2 we will have typically 5 to 20 KV, usually owing 2,000 pF in 400KV systems.

Our aim is to scale down the voltage without changing its characteristics. Presence of capacitors cause a phase shift between the primary and the secondary voltages at the system frequency. Then a compensation reactor is used to eliminate the coupling capacitor reactance.

In order to achieve the final desired voltage level at the output terminals of a CVT, a step-down transformer is used to reduce further the intermediate-level voltage produced by coupling capacitors to the nominal voltage of the relay.

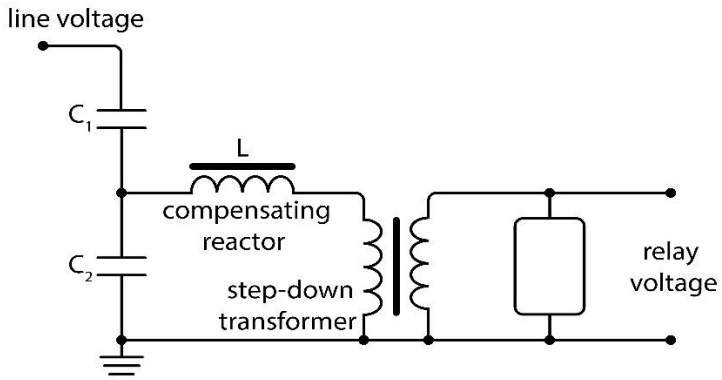


Figure 3: Generic CVT Structure

The compensating reactor and step-down transformer have iron cores. Besides introducing copper and core losses, the compensating reactor and step-down transformer also produce ferroresonance due to the nonlinearity of the iron cores. CVT manufacturers recognize this ferroresonance phenomenon and include a ferroresonance-suppression circuit. This circuit is normally used on the secondary of the step-down transformer. While this circuit is required to avoid dangerous and destructive over voltages caused by ferroresonance, it can aggravate the CVT transient. Whether or not this suppression circuit aggravates the CVT transient depends upon the suppression circuit design. [2]

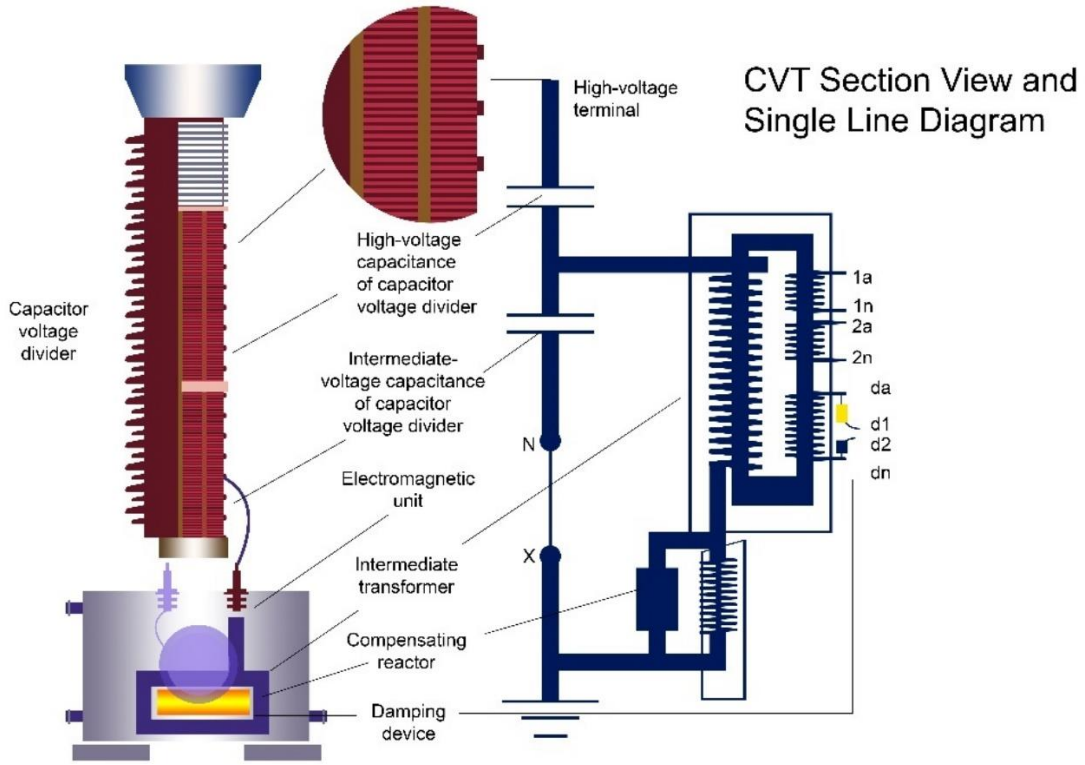


Figure 4: CVT Section View and Single Line Diagram

CVT consists of at least four terminals: High voltage connection at the top, a ground connection and two secondary terminals which connect to the instrumentation or protective relay. In other words, CVT is composed of two primary assemblies, the high voltage capacitor sections, and the base box, housing the electromagnetic components.

Figure 5 Description:

1. H.V. Terminal
2. Porcelain Insulator
3. Base Box
4. Top Cover
5. Terminal Box
6. Lifting hole

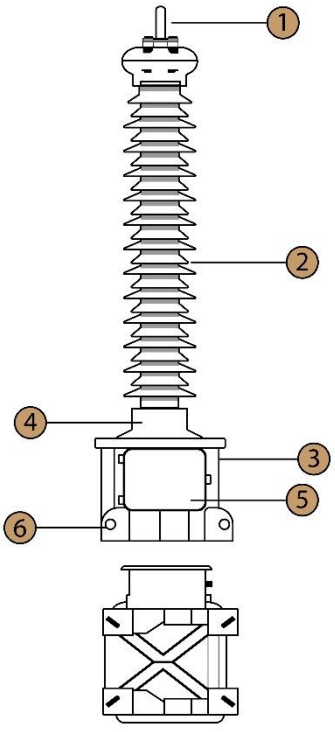


Figure 5: CVT Parts

Each capacitor section includes series capacitors elements placed in porcelain shells in an airtight process and sealed. High quality polypropylene film/paper is used as the dielectric and impregnated with a highly processed synthetic fluid. During the variation of the ambient temperature the synthetic fluid can be expanded maintaining the hermetic sealing.

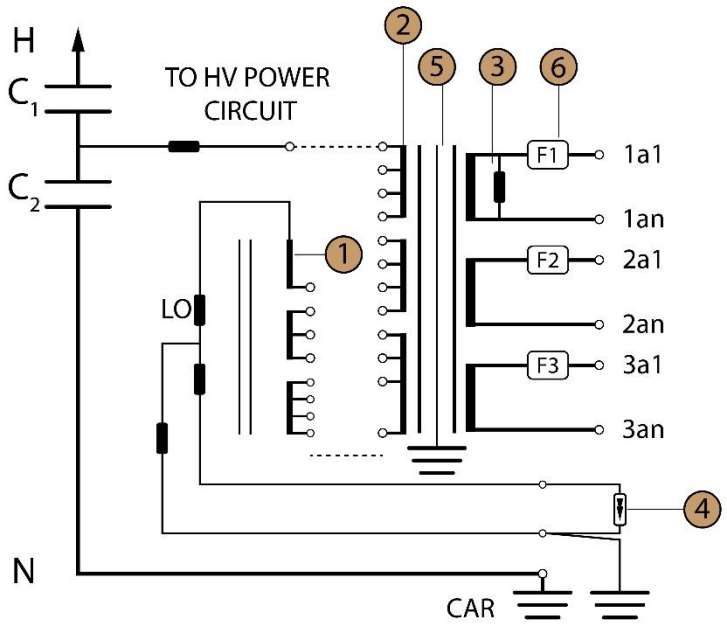


Figure 6: CVT Typical Schematic diagram

Figure 6 Description:

1. Series Reactor
2. Intermediate Transformer
3. Filter
4. Protective Gap
5. Faraday Shield
6. Fuses

The final output voltage is provided by the intermediate transformer which is placed in the base box within series compensating reactor and ferroresonance control circuit. The box contains mineral oil for protection of the components from the environmental deterioration.
Ferroresonance phenomenon due to the nonlinearity of the iron cores can be controlled by designing a magnetic circuit having low flux density and a saturable controlled damping circuit connected across the secondary winding.
Then we can note that the electromagnetic unit consists of

- an inductive transformer,
- a series reactor
- auxiliary elements.

Capacitive Voltage Transformers are built and installed as a single-pole unit; thus, the connection will be between phase and earth. The higher the voltage level is, the more price-competitive the capacitive type becomes in comparison with wounded transformers.

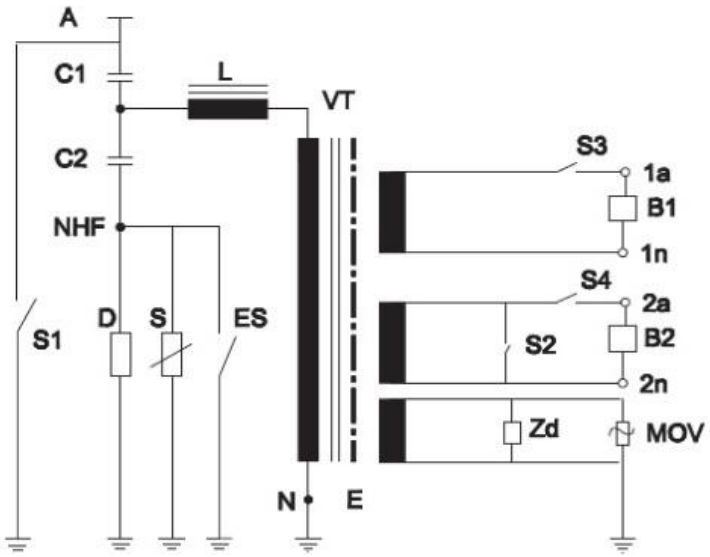


Figure 7: Schematic diagram of the typical 400 kV CVT Adapted from [7]

CVT model composed of capacitive voltage divider (C1 and C2), compensating reactor (L), intermediate transformer (VT), over voltage protection device (S), drain coil (D), metal oxide varistor (MOV), ferroresonance suppression device (Zd), earth switch (ES), and burdens B1, B2. [7]

1.1.2.1 Coupling Capacitors

The main parameters of the coupling capacitors could be described as their voltage dividing principle and insulation.

Coupling capacitors consist of two group of capacitors called C1 and C2 function as a voltage divider. Capacitor C1 is usually made of series connected capacitors to reach a high voltage drop across it. It means there will be small voltage drop on C2 and consequently the required insulation level of the voltage transformer reduces. This makes CVTs more economical with respect to the wound voltage Transformer (WVT) under high voltage (over 100 KV).

The number of capacitor units depends on the applied primary voltage level. For instance, for a 400 KV CVT, the C1 is designed by connecting in series the capacitances to reach such a small value as 104 pF. The voltage drop on C2 will be typically 5 to 20 KV having a capacitance 2,000 pF. The CVT capacitance is represented by two values: one for the equivalent capacitance above the intermediate voltage point (point a in Fig. 8) and the other for the equivalent capacitance below the intermediate voltage point.

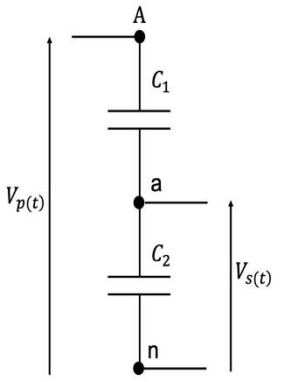


Figure 8: Coupling Capacitor

Considering V1 and C2 the voltages across the coupling capacitances C1 and C2, and as the potential transformer is connected across the line to ground V_p (phase voltage) can be calculated as below:

$$V_p = V_{line} / 1.732$$

Hence V_1 as the Voltage across the Capacitor C1 can be calculated:

$$V_1 = V_P \left(\frac{C_2}{C_{1+C_2}}\right)$$

And V_2 as the Voltage across the Capacitor C2 can be calculated:

$$V_2 = V_P \left(\frac{C_1}{C_{1+C_2}}\right)$$

Series-connected capacitor elements are housed in sealed porcelain or composite insulator shells. The capacitor elements consist of aluminium foil, are insulated with a high-quality polypropylene film and paper insulation, and are filled with highly processed synthetic oil. Each CVT section includes an expansion chamber to allow the oil to expand and contract with changes in temperature. The tap voltage is taken from the lowest capacitor section and fed to the base of the unit. The base houses the compensating reactor, step-down transformer, and ferroresonance suppression circuitry. A pressure relief mechanism is designed to relieve excessive pressure. Manufacturers boast of explosion-proof designs with new models. However, older CVTs that are aging have exploded and pose safety concerns. [3]

Old capacitors were insulated by mineral oil-impregnated kraft paper. It is concluded that the increased ratio error was caused by the insulation material, which is prevented in modern CVTs by using polypropylene film. Although this insulation material is a proper substitute for kraft paper, investigations on ten impaired CVTs demonstrated that the polypropylene film was the major insulation for these CVT capacitor elements. Consequently, the CVT increased error is not completely prevented even by using better insulation materials. [9]

1.1.2.2 Compensating Reactor

As it is known connecting of reactive components such as capacitors or inductors cause phase shift in the electrical systems. In order to prevent such phenomenon in CVTs an inductive component called compensating reactor is connected to the middle point of the coupling capacitors and in series with the burden. Then existence of the reactor and the reactance of the stepdown transformer theoretically can cancel the effect of C1 and C2 at system frequency.

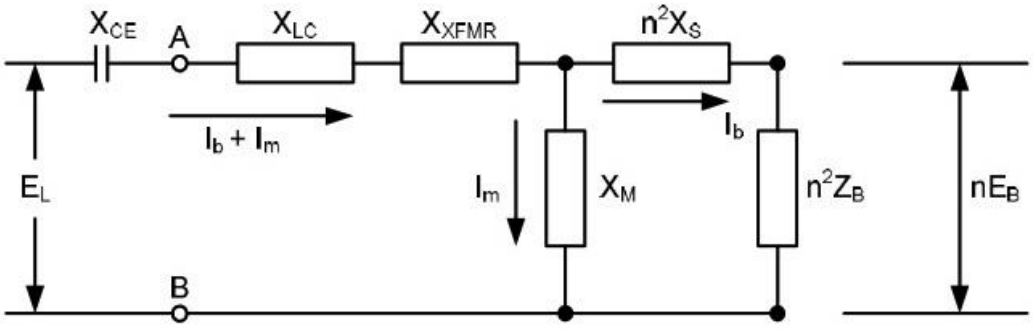


Figure 9: Equivalent Circuit Adopted from [3]

All the components are reflected to the high side of the step-up transformer.

The following definitions apply to Fig. 9:

EL is the intermediate or tap voltage.

XCE is the Thévenin equivalent capacitance.

XLC is the equivalent compensating reactance.

XXFMR is the leakage inductive reactance of the step-down transformer.

XM is the magnetizing reactance of the transformer.

n2 XS is the combined transformer capacitance and ferroresonance suppression reactance reflected to the high side.

Ib + Im is the primary current.

Im is the transformer excitation current.

Ib is the burden current.

n2 ZB is the burden reflected to the high side.

n EB is the output voltage. [3]

Fig. 10 shows the relationship between the primary voltage (EL), the primary current (Ib + Im), and the voltages across XCE and n2 ZB. With a resistive or unity power factor burden and with XL + XXFMR + XM = XCE at the nominal system frequency, the primary current (Ib + Im) is in phase with the primary voltage (EL). The voltage across the reactive components, however, is 90 degrees out of phase with the primary current. [3]

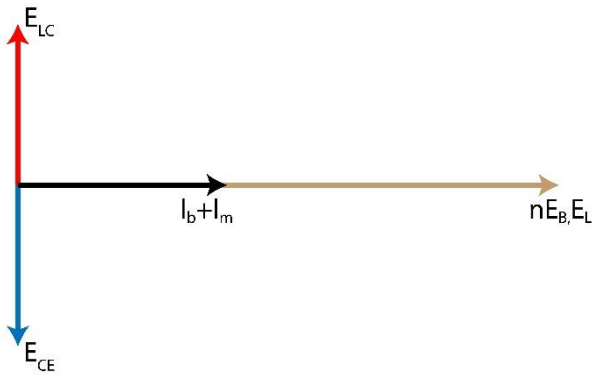


Figure 10: Phasor Relationship Between Components of a CVT

The current taken by the burden is negligible compared with the current passing through the series-connected capacitors. Though, as the burden current becomes larger the ratio error and phase error appear. Using of an adjustable compensation through tuning makes the reactor able to resonant at the supply frequency with sum of the two capacitors and eliminate the error. [11]

Calculation of the value of the inductance of the compensation reactor:

$$L = \frac{1}{\omega^2 (C_1 + C_2)}$$

The value of inductances is adjustable. The inductance compensates the voltage drops occurs in the transformer because of the reduction of the current from the potential divider. But, in actual practice, the compensation is not possible because of the inductance losses.

1.1.2.3 Step-down Transformer

The reduced voltage by the coupling capacitors is fed to the step-down transformer. It is an inductive transformer with iron core and its output can be used to supply CVT burden, protective relay, or meter. The step-down transformer is placed in the base box with the other parts.
The capacitors placed near to the ground have higher capacitance in comparison with the one located near the transmission lines. The high value of capacitance means the impedance of that part of the potential divider becomes low. Therefore, low voltage pass to the auxiliary transformer. The step-down transformer further decreases the voltage. The meter used for measuring the low value of voltage is resistive, and the potential divider is capacitive. Thereby, the phase shift occurs, and the output will be affected. To overcome this problem, the inductance is placed in series with the auxiliary transformer. The number of turns on the primary and secondary windings of the step-down transformer are defined by N_1 and N_2.

The voltage turn ratio of the transformer is expressed as

$$\frac{V_0}{V_1} = \left[\frac{C_2}{C_2 + C_1}\right] * \frac{N_2}{N_1}$$

1.1.2.4 Ferroresonance-suppression circuit

The step-down transformer and the compensation reactor equipped with iron cores used for the further decrease of the voltage and also compensate the shift phasing caused by the capacitors. Apart from the copper and core losses introduced by their iron cores, ferroresonance phenomenon is another issue that we need to deal with. Ferroresonance is caused due to the nonlinearity of the iron cores and can be calculated in advance. Series connection of the CVT capacitances and the inductance of the compensating reactor and the auxiliary transformer creates a possible resonant circuit and generation of subharmonic oscillation of 3^{rd} mode. Power system disturbances such as variation of the voltages or transformer saturation can bring the circuit to the saturation. The aim is to prevent the stabilization of such subharmonics and moreover their fast damping. Then a ferroresonance-suppression circuit on the secondary side of the auxiliary transformer is used to avoid dangerous over voltages cause by ferroresonance phenomenon.
In continue we will see that using of a ferroresonance-suppression circuit can amplify the transient of CVT and a careful design should be taken into the account.

Basically, two main types of ferroresonance suppression circuits are used in CVTs as it showed in Fig. 11 and Fig. 12.

Active Ferroresonance-Suppression Circuits

Active ferroresonance-suppression circuits (AFSC) consist of a LC parallel tuning circuit with a loading resistor, capacitors and inductors, which are both active energy storage devices. The LC tuning circuit resonates at the system frequency and presents a high impedance to the fundamental voltage. The loading resistor is connected to a middle tap of the inductor to increase the resonant impedance of the circuit. For frequencies above or below the fundamental frequency (off-nominal frequencies), the LC parallel resonant impedance gradually reduces to the resistance of the loading resistor and attenuates the energy of off-nominal frequency voltages. [2]

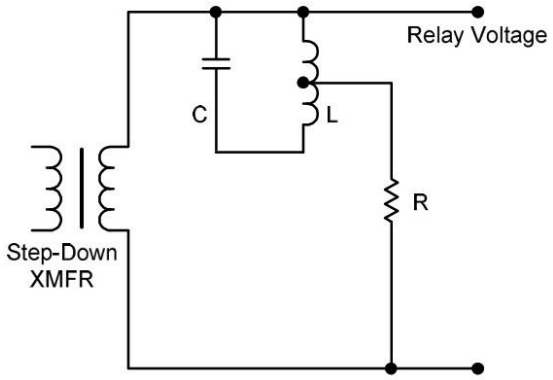


Figure 11: Active Ferroresonance-Suppression Circuits. Adopted from [2]

The AFSC performs like a band-pass filter and introduces added time delay in the CVT secondary voltage output. [3]

Passive Ferroresonance-Suppression Circuits

Passive ferroresonance-suppression circuits (PFSC) have a permanently connected loading resistor Rf, a saturable inductor Lf, and an air-gap loading resistor R. Under normal operating conditions, the secondary voltage is not high enough to flash over the air gap, and the loading resistor R has no effect on the CVT performance. Once a ferroresonance oscillation exists, the induced voltage flashes over the gap and shunts in the loading resistance to attenuate the oscillation energy. Lf is designed to saturate at about 150% of nominal voltage to further prevent a sustained ferroresonance condition. [2]

In contrast, the passive ferroresonance suppression circuit (PFSC) uses resistance. The resistive load does increase the primary current, which causes a higher capacitor voltage. However, compared with the AFSC, the PFSC has little effect on the transient.

In Fig. 12 and Fig. 13, observe that the PFSC CVT more closely replicates the ideal ratio voltage. [3]

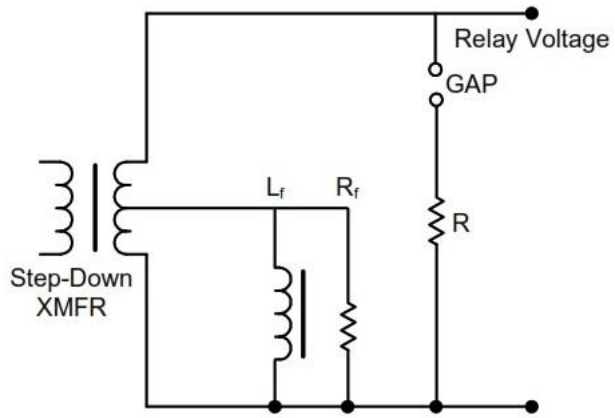


Figure 12: Passive Ferroresonance-Suppression Circuits. Adopted from [2]

The CVT is equipped with over voltage protection device and ferroresonance suppression circuit to be protected against the high voltages caused by the probable resonance. The CVT FSC may be passive or active based on whether this circuit stores energy or not and these can be based on the working principle categorized as:

1) series resonance type,
2) power frequency blocking type,
3) fast saturation type,
4) electronic type, [8]

1.2 Transient Response

Capacitive Voltage Transformers (CVTs) thanks to their cheaper manufacturing costs are common in high-voltage transmission line applications. As the power systems are equipped with faster and more secure protective relays the concerns about the poor transient response of CVTs increases. For instance, Solid-state and microprocessors relay due to their high-speed operating can respond to a CVT transients. When a fault occurs the CVT output may not follow the primary voltage closely. This is due to the presence of the energy storage elements as stack capacitors and the tuning reactor of CTV that are not able to change instantaneously their charge or flux. This energy needs to be dissipated and the CVT generates transients that affect the performance of protective relays. The transients are basically controlled by the parameters of the CVT itself and the point on wave at which the fault occurs.
Distance relays are used as the protecting equipment that operates based on the distance of the fault point on the transmission line. The reduction of the fundamental component of the fault voltage during CVT transient results in a decrease of the calculated line impedance. If the fundamental voltage reduction is large enough the zone 1 distance relay will react and pick up for out-of-section faults.
Considering a fault occurring in the defined portion of protective relay at zone 1, then the effect of CVT transient on the impedance calculation is tolerable. Otherwise for a fault outside of the relay defined area if the relay picks the fault up the transient of CVT is not tolerable.

The compensating reactor is tuned by a CVT manufacturer to ensure zero phase shift between the primary and secondary voltages, and from this perspective, the inductance of the reactor is a constant value dependent only on the capacitances used to set-up the divider.
The shunt parameters of the step-down transformer practically do not contribute to the CVT transients during fault conditions when the voltage collapses.
Consequently, the transients are basically controlled by the following factors:

1. Coupling Capacitor Value
2. Point on the Voltage Wave at the Time of the Fault
3. Excitation current of the intermediate transformer
4. Design of the ferroresonance suppression circuit (active or passive).
5. Burden
6. System Impedance Ratio (SIR)

1.2.1 Parameters Affecting the Transient Response of a CVT

1.2.1.1 Coupling Capacitor Value

A Capacitive Voltage Transformer is composed of a number of capacitor units connected in series. Depending on the applied voltage on the primary side of CVT the number of capacitor units can be chosen. The CVT capacitance is defined by two values: one for C1 which is the equivalent capacitance above the intermediate voltage point (C_1) and the other for the equivalent capacitance below the intermediate volage point (C_2). Then ($C_1 + C_2$) which is the Thevenin equivalent capacitance is distinguished form the total capacitance($\frac{C_1.C_2}{C_1+C_2}$) which is given by the manufacturers.

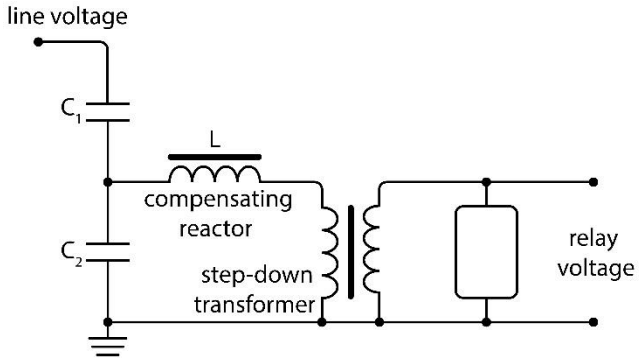


Figure 13: Generic CVT Structure

Examining the equivalent circuit shown in Fig. 13 in order to select the magnitude of the Tap and Stack Capacitances.

$$X_{CE} = \frac{1}{2.\pi.f.C_E}$$

Increasing the magnitude of C_E as the result the capacitive reactance becomes smaller. Having a constant burden, the primary current remains the same. As the voltage drop across the equivalent capacitance is lower, the smaller will be the discharge transient. Therefore, form point of view of the magnitude of the CVT transient, one should recommend CVTs with higher sum of the stack capacitances for supplying the distance relays. On the other hand it should be considered that increasing the value of C_E also increases the duration of the transient and also CVTs with higher capacitances are more expensive.
Typically, the sum of the stack capacitances is in the range of 100nF. From this perspective, CVTs are classified as of “normal-C”, “high-C” and “extra-high-C” types. [5]

As it is said the high capacitance value in a CVT decreases the CVT transient in magnitude. This can be seen by comparing the CVT transient plots of Figure 14 and Figure 15 for a fault initiated at a voltage zero. Figure 15 shows the transient response of a CVT with four times total capacitance of that shown in Figure 14.

When testing distance relays, one should consider a CVT model of the high-C type first. It is, however, necessary to test a given relay using different types of CVTs**.**[5]

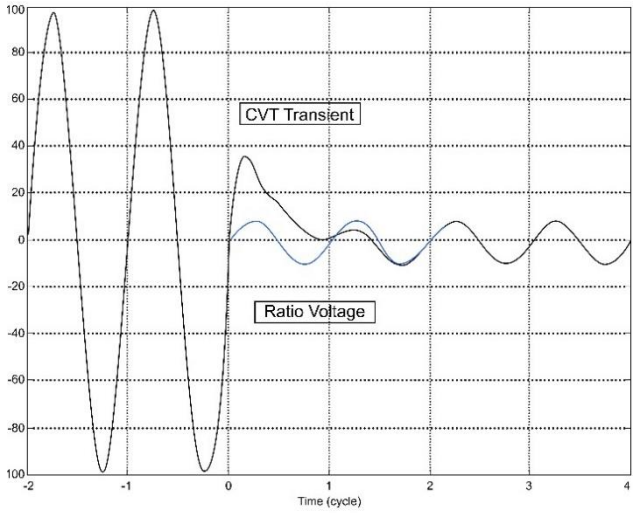


Figure 14: CVT Transient Response with a Fault at Zero Voltage. Adapted from [2]

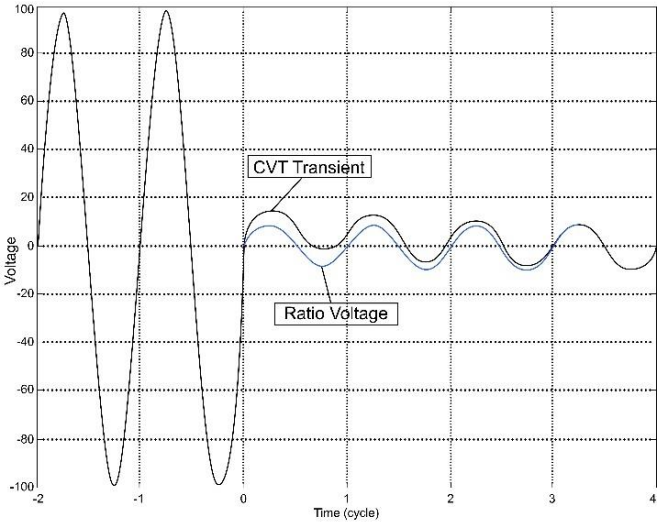


Figure 15: Transient Response of a High-Capacitance CVT with a Fault at Zero Voltage. Adapted from [2]

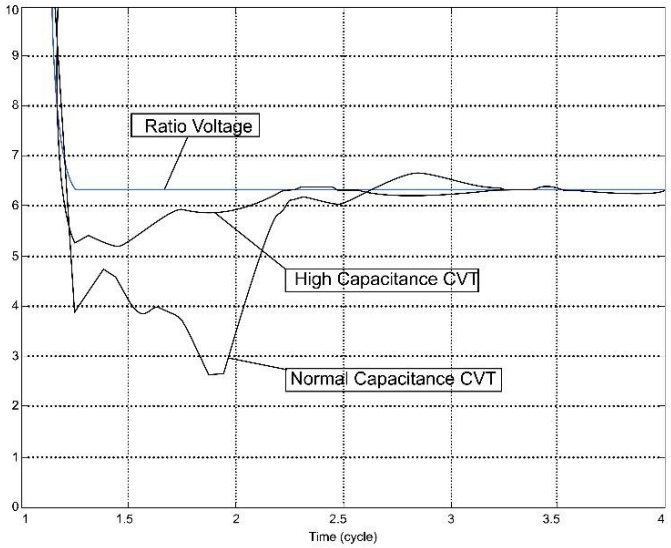


Figure 16: Transient Response of Normal and Hight Capacitances. Adapted from [2]

1.2.1.2 Point on the Voltage Wave at the Time of the Fault

Characteristics of the CVT transient is dependent on the initiation of the fault point-on-wave (POW). In fact, the CVT transients show different behaviour for faults occurring at voltage peaks and voltage zeros. Figure 17 and Figure 18 demonstrate two CVT transients for zero-crossing and peak POW fault initiation. For ease of comparison an ideal CVT voltage output (ratio voltage) has been shown in each figure.

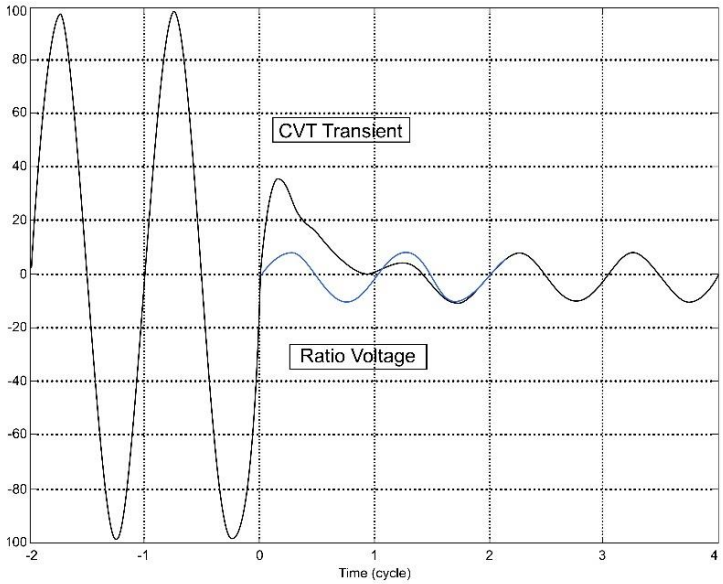


Figure 17: CVT Transient Response with a Fault at zero-crossing. Adapted from [3]

Figure 17 shows a CVT transient with a fault occurring at a voltage zero. It can be seen that the CVT output does not follow the ideal output until 1.75 cycles after fault inception.

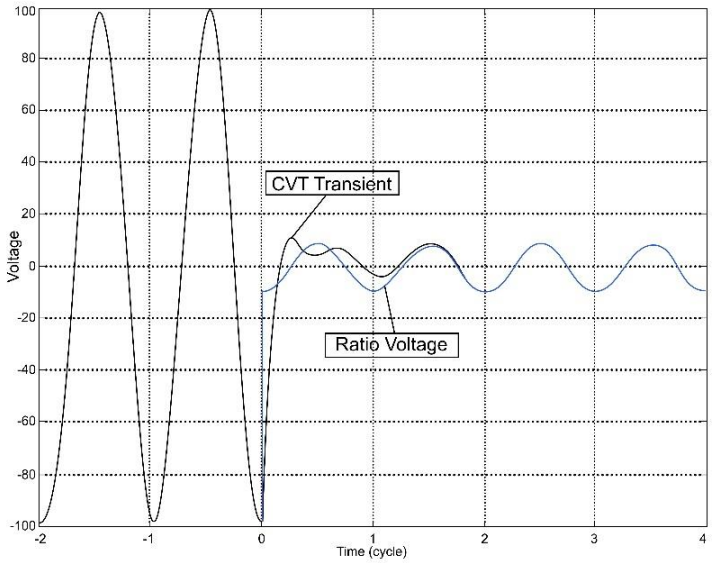


Figure 18: CVT Transient Response with a Fault at peak POW fault initiation Adapted from [3]

For a fault occurring at a voltage peak as it can be seen in the Figure 18 the CVT output does not follow the ideal output. For this case the transient lasts about 1.25 cycles.
For the other cases other than a voltage peak or voltage zero the behaviour of the CVT transient will take a wave shape in between those shown in Figure 17 and Figure 18.

To fully understand this phenomenon, we consider again the figure 9 as the equivalent circuit of a CVT where all the components were reflected to the high side of the set-up transformer.
In essence, the energy stored in the compensating reactor is the same as the energy stored in the effective capacitance. The voltage and energy stored in the capacitor are at a maximum at a voltage zero crossing. The energy must be discharged at the time of the fault, and this produces the maximum transient voltage. The energy stored in the inductor is at a maximum at a voltage and primary current peak. Because the amount of energy stored in the reactive components is the same, we examine the effect of the time constants.

Using the typical parameters from a 230 kV CVT, we can calculate the time constant of each element:

$$\tau_{C_E} = n^2 Z_B C_E = 30.644\ [ms]$$
$$\tau_{L_C} = \frac{L_c}{n^2 Z_B} = 0.189\ [ms]$$

where:
CE is the CVT equivalent capacitance, equal to 276.9 nF.
LC is the CVT equivalent compensating reactance, equal to 20.954 H.
n2 ZB as the burden reflected to the high side is 110 kΩ.

It is evident that the worst-case or longest transient response occurs when the maximum energy is stored in the capacitor or when the primary voltage is at a zero crossing. We will see that the magnitude of the capacitance has a similar effect on transient duration. Fig. 7 and Fig. 8 show the outputs of a CVT for faults that occurred at voltage zero (zero crossing) and at voltage maximum, respectively. [3]
From a statistical point of view faults appear more often at voltages large enough to initiate the insulation breakdown (i.e., close to the maximum point on wave). However, when testing distance relays one must not neglect faults initiated at the zero crossing as they may “occur” when switching onto a fault. [5]

1.2.1.3 Excitation current of the intermediate transformer

Transient response of a Capacitive Voltage Transformer depends on composing components. For instance, the isolation of the burden from the coupling capacitors is defined by the turns ratio of the step-down transformer. A higher turns ratio decreases the primary current by magnifying the burden. The shape and the duration of CVT transients change depending on the different loading on the CVT coupling capacitors due to different transformer ratios. In essence, the smaller the current, the less energy is stored in the capacitor.
From the burden point of the view, the capacitance and the inductance are reflected to the secondary by the inverse of the turns ratio squared. Then the transformers with larger turns ratio (e.g., 15 kV to 20 kV/66.4 V) will produce transients with lower magnitude and longer duration.

As mentioned in 1.1.2.2 the current is at non-unity power factor. Consequently, sub nominal frequency oscillations can occur and requiring larger currents can generate greater transients. Therefore, CVT transformers should designed to minimize the excitation current.

1.2.1.4 Design of the ferroresonance suppression circuit (active or passive)

During the overvoltage conditions the core of the step-down transformer is saturated. Such a condition causes sub synchronous oscillation. It means non-linear oscillations can appear when the operating point of the magnetizing characteristic of the step-down transformer is shifted to the saturation region. Therefore, ferroresonance suppression circuits are designed to prevent such a phenomenon in CVTs. CVTs are equipped with such a circuit to avoid stabilization of the subharmonics and also a fast damping of the oscillations. Practically, the ferroresonance circuit provides an additional path – apart from the burden- for the dissipating of the energy stored on the reactive components of the CVT. Thus, the damping circuit has a significant impact on the transient characteristics of the CVT.

Two generic models of ferroresonance suppression circuits can be considered.

In the first model a series resistance with a parallel LC branch is considered. At the nominal frequency (50 Hz or 60 Hz) the LC branch behaves as an open circuit. At the off-nominal frequencies some currents start flowing in the LC subcircuit and the energy dissipates in the series resistor. This model is called "Active ferroresonance Suppression Circuit' (AFSC) and acts like a band-pass filter and introduces extra time delay in the CVT secondary output. Power electronic elements are utilized for constructing the active circuits. The energy storage elements in the AFSC contribute to the severity of the CVT transient.

In the second design a resistor and saturable inductor are connected together with a flash-over air gap. Then the RL circuit can be considered as a permanent burden on the secondary side of the CVT. Such a design increases the V A loading of the intermediate step-down transformer. For the same burden specification, the CVT with PFSC requires a bigger intermediate step-down transformer. Moreover, the saturation of the inductor will be at about 150% of the nominal voltage. By triggering the airgap above that level another resistor is introduced to the circuit to provide more damping action. This anti-resonance circuit is called "Passive ferroresonance Suppression Circuit" (PFSC)

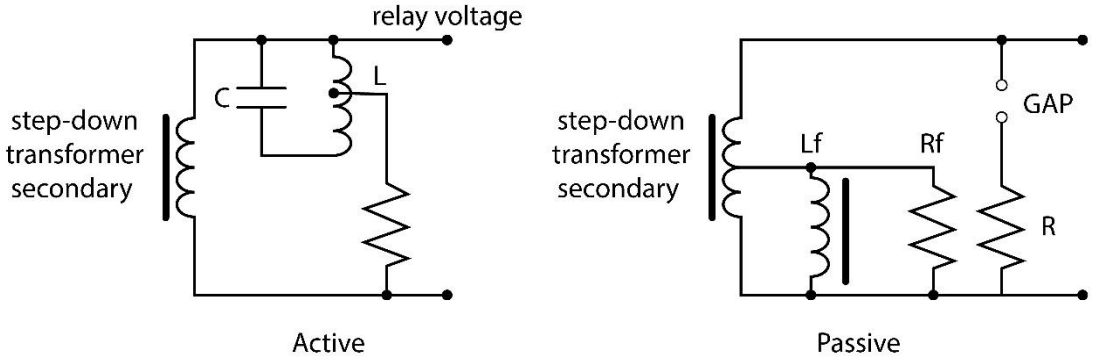


Figure 19: Ferroresonance Suppression Circuits (active and passive)

At the nominal operating condition of CVT, the majority components of the PFSC are isolated from the CVT output. Hence the PFSC has a small impact on the CVT Transient Behaviour and has a less distorted output voltage. For distance relay testing purposes selection of AFSC can be considered as a more severe case.

Considering two Capacitive Voltage Transformers faced with a unique fault and equipped with AFSC and PFSC. The different behaviour of the CVTs for the same fault and using different ferroresonat suppression circuit can be seen in the Figure 20 and Figure 21.

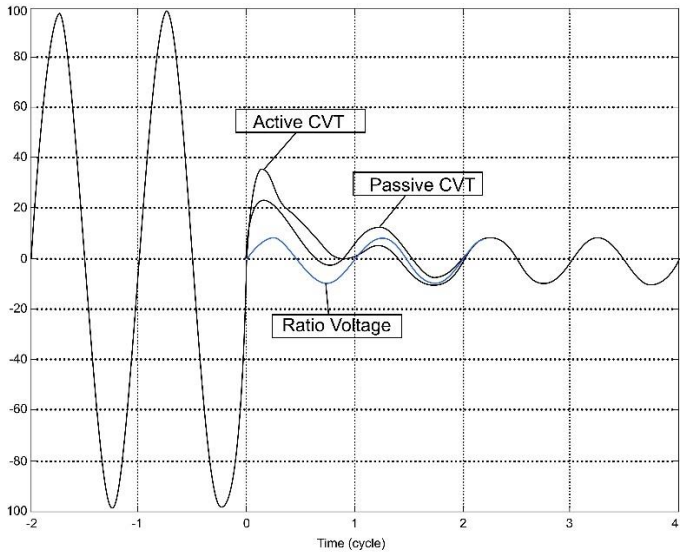


Figure 20: Response of CVTs Equipped with PFSC and AFSC

It can be noted that the CTV with a PFSC has a better, less distorted transient response with respect to the CVT with an AFSC. In other words, the fundamental magnitude will be closer to the true fundamental magnitude when the distortion is small.

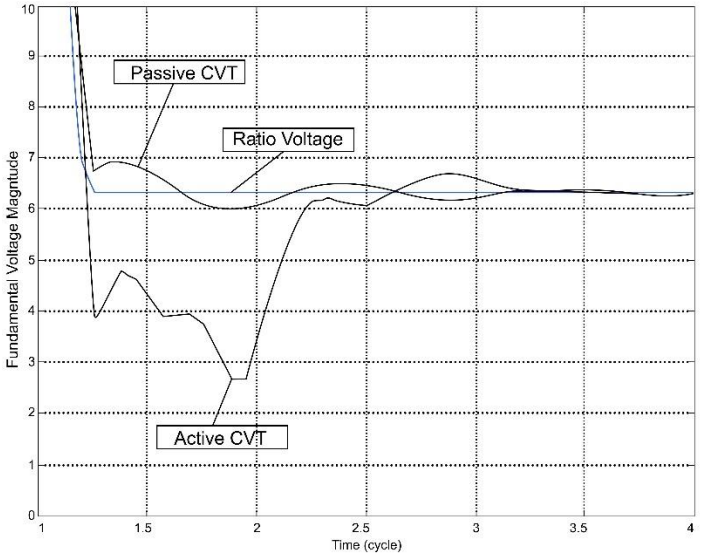


Figure 21: PFSC and AFSC in Comparison with CVT Fundamental Voltage Magnitude

1.2.1.5 Burden

The Capacitive Voltage Transformer transient specifications is characterized by the magnitude and the phase angle of the connected burden. The burden of the CVT is one of the dissipating paths for the energy stored on the reactive components. Hence better CVT performance is obtained when CVT is under full load condition.

For an open circuit CVT, the transformer excitation current is the only current flowing in the CVT circuit. Then the stored energy across the reactive components, coupling capacitor and the inductive component of the compensation reactor and the step-down transformer will be relatively small value. By increase of the burden, the current is composed of the load current and the excitation current. Therefore, the energy stored on the reactive components is increased. In fact, the greater is the burden, the greater will be the energy storage and consequently the transient at zero crossing fault initiation will be aggravated.

Considering different characteristics of the burden the behaviour of the CVT will be changed. For Connecting a pure resistive load having unity power factor, the damping effect will be optimized and the time constant will be changed while the resistive burden does not store energy. In case of an inductive burden, the power factor declines and at a sub nominal frequency the transient response of the CVT will be perturbated with some oscillations.

In order to achieve the optimum performance of the CVT it is recommended to go under full load condition. Electromechanical relays having higher burden can naturally load the CVTs. In turn, the burden for microprocessor-based relays in the modern applications is two to three orders of magnitude smaller in VA than the burden defined by ANSI C93.1 and demonstrating more resistive characteristics (larger in ohms). ANSI C93.1 defines the burden to be used for CVT testing and includes inductive reactance. Therefore, it is recommended that the CVT be fully loaded when using digital relays to avoid extensive transients.
When testing distance relays, one should consider not only the rated burden of a CVT, but also test distance relays with CVTs operating on a small load. [5]

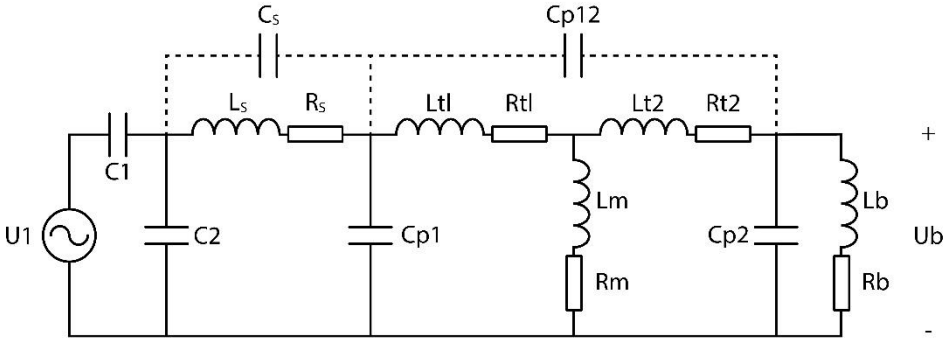


Figure 22: CVT Equivalent Circuit including the Burden and the Stray Capacitances

Further explanation regarding the equivalent circuit of figure 22 is given in the chapter two and the component and their impact on the functionality of the circuit will be discussed.

1.2.1.6 System Impedance Ratio (SIR)

The fault voltage magnitude level is a significant factor affecting the severity of the CVT transients. The smaller is the fault voltage level, the greater and longer will be the transient. The System Impedance Ratio directly effects the fault voltage level for a fault at a given location.
In order to detect faults occurring at the grid, certain information should be provided for the protection devices at the power system to be able to take necessary actions. The length of the line is a vital step in setting the protection relays. The length of a line can be determined by Physical distance, impedance, or its source impedance ratio (SIR). The SIR is the ratio of the source impedance, ZS, to the line impedance, ZL. With reference to the IEEE C37.113, IEEE Guide for Protective Relay Applications to Transmission Lines, the line length based on SIR is classified as follows:

- Long line (SIR < 0.5)
- Medium line (0.5 < SIR < 4)
- Short line (SIR > 4) [14]

Distance Relays face severe problems in coexistence of CVT transients and high value of SIRs. Considering a solid fault which is a short circuit fault with impedance (Z_f) equal to zero occurring at the reach point of the relay, the voltage at the relay location can be approximated by the below equation:

$$V_{fault} \cong \frac{V_{nominal}}{1 + SIR}$$

The table 1 can be obtained by using the above equation. The fault voltage magnitude [pu] is determined for a range of SIRs. Reach of distance relay is defined as line protection covered by relay in terms of length or impedance of the line. Then the reach of relay is Z as it is expected to protect the entire line. But due to absence of residual compensation, the relay is not only able to protect the whole line rather it is protecting only a part of line say 90% of line. This means the effective reach of relay has decreased. This is why; we say relay is under reaching. As the
SIR increases the fault voltage at the reach point drops to very small values. The magnitude of
the CVT transient, in turn, remains constant (independent from the SIR) as the energy accumulated in the CVT is a straight function of the pre-fault voltage. As the SIR increases the fault voltage at the reach point drops to very small values. The magnitude of the CVT transient, in turn, remains constant (independent from the SIR) as the energy accumulated in the CVT is a straight function of the pre-fault voltage. This results in extremely unfavourable signal to noise ratios (as for the protection-oriented measurements when the speed counts). As illustrated in Figure 7, for example, the magnitude of the noise components may be 10 times larger than the magnitude of the 60Hz operating signal. The noise dominates the signal for 1.5 to 2 cycles. [5]

SIR	0.1	1	5	10	20	30
$V_{fault}[pu]$	0.91	0.50	0.17	0.09	0.05	0.03

Table 1: Fault Voltage as a function of SIR. Adopted from [5]

The unfavorable signal to noise ratio contributes to both transient overreach and slow operation of distance relays. Certainly, such extreme proportions occur for high SIRs.

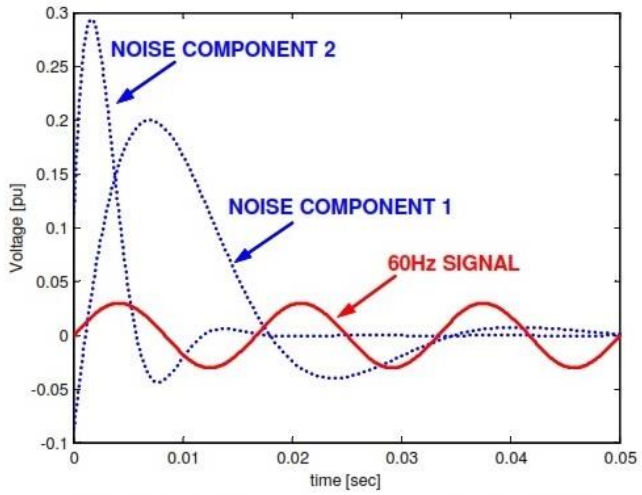


Figure 23: Illustration of the signal-to-noise ratio for the CVT transients (Fault at zero crossing) and high SIRs (30). Adopted from [5]

Traditionally, vendors specify their distance relays up to the SIR of 30 (sometimes 50 or 60). Such high values are not applicable for longer lines in heavily interconnected systems. There are, however, situations when the high SIRs are a fact. They include:

- Short lines adjacent to busbars in a long corridor linking the generation and load areas.
- Lines in weak systems such as in developing countries.
- Distance back-up on short lines for current differential or phase comparison schemes. [5]

We must keep the SIR value in mind when assessing the influence of CVT transients on a distance relay.[2]

1.3 Harmonic Voltage Measurements by CVTs

Powe quality assessment can be considered as one of the crucial requirements of the electricity supply system management. Therefore, standards and recommendations such as IEEE 519, IEC 61000-4-30 and 61000-4-7 and UK, Engineering Recommendation G5/4 require measurements up to the 50th harmonic were introduced in power quality measurement and monitoring. Flicker standard IEC 61000-4-15 require measurement of modulating frequency between 0.5 Hz to 33 Hz. Considering Capacitor voltage transformers with reliable and accurate performance they can be considered as dominant technology for voltage measurement at transmission voltage levels. Conventional inductive transformers have limited frequency response and their frequency response becomes unacceptable above 500 Hz (CIGRE Working Group 36) which is below the below the frequency limit established in the major standards.
Capacitor Voltage Transformer having a reliable insulation and a large electric field strength margin is preferred for measurement purposes particularly above 110 KV. Nowadays, CVTs are widely used in substations of 35 KV and higher levels due to their reduced cost and the size in comparison with the inductive transformers. On the other hand, CVTs have their weaknesses such as poor transient response or not being able to measure harmonics of the power system. In fact, the harmonic components in the grid actual situation cannot be reflected by CVTs since they are essentially tuned to the system frequency and they do not have a uniform (flat) frequency response. Therefore, there will be a large error at the secondary voltage signal of CVT. Hence, the national standard GB/T 14549-1993 “grid harmonic” appendix D7 states that “a CVT cannot be used for harmonic measurement,” and IEC standards and other related technical reports are also provided. The working point deviation of series resonant circuit and stray capacitances at primary side of the intermediate transformer and compensation reactor are two main factors affecting the harmonic transmission characteristics of CVT. There is the possibility to use other interface devices between EHV systems and instrumentation, such as capacitor or resistive dividers to do the task of harmonic measurement. Such devices are expensive options in terms of cost and space in substations since they cannot be used for supplying relays and meters. Besides, capacitor or resistive dividers require regular calibration.

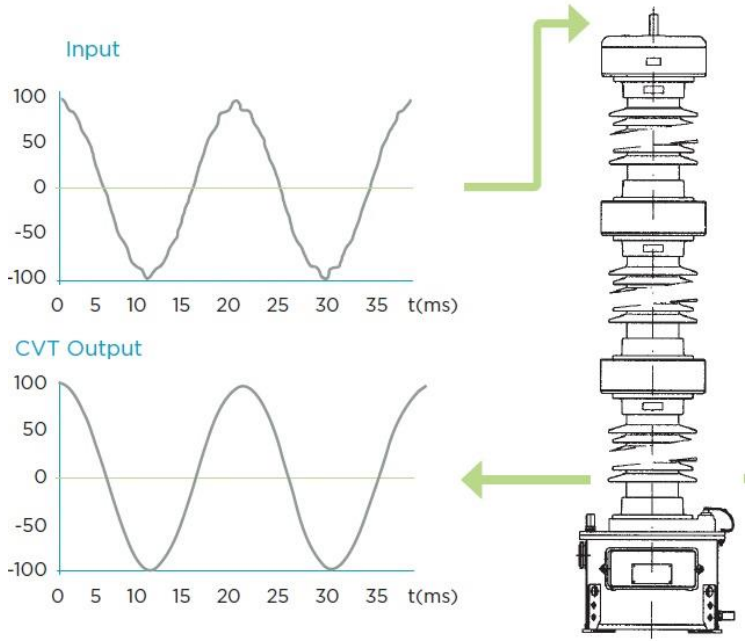


Figure 24: Comparison between input and output voltage of CVT concerning Harmonic Transmission Adopted from [30]

Considering the advantages of CVTs in comparison with VTs particularly at high voltage levels, there are various solutions to meet the requirements of the power system concerning harmonic measurements. Here two possible approaches were described. The first one is based on the calculation of the transfer function without any other devices. The second approach is using a Power Quality sensor for completion of functionality of CVTs. Hence, we try to perceive accurate grid harmonic levels and exact voltage distortion data through CVT by using of CVT Transfer Function (TF) to compensate for the CVT response at the harmonic frequency reference. Then by considering an equivalent circuit model of CVT and calculation of the equivalent impedance relation between the output and input voltage of CVT can be expressed by a transfer function.

1.3.1 Equivalent Circuit Model of CVT

In order to analyze and calculate the harmonic transmission characteristics of CVT, an equivalent circuit model is considered, as shown in Figure 29. The transformer leakage reactance was normalized to compensation reactance since were in resonance with equivalent capacitance of divider.

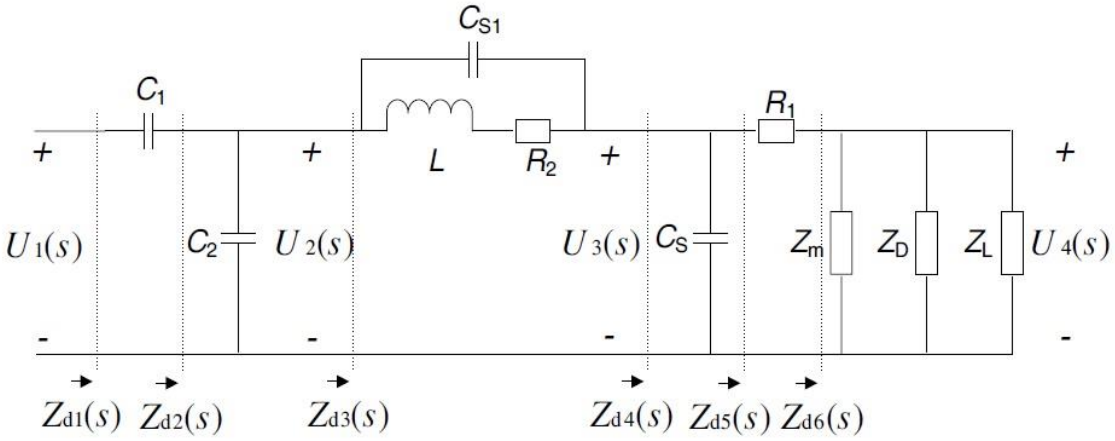


Figure 25: Equivalent Circuit Model for Transfer Function Calculation. Adopted from [17]

C1 and C2:	high-voltage capacitor and medium-voltage capacitor respectively
L:	Compensation Reactor
Zm:	The excitation impedance of intermediate transformer
ZD:	The equivalent impedance of damper
ZL:	The load impedance
	(Zm, ZD and ZL were normalized to the primary side)
R1:	leakage resistance of the intermediate transformer
R2:	Resistance of the compensation reactor
CS:	Equivalent stray capacitances of the primary side of intermediate transformer
CS1:	Equivalent stray capacitances of the compensation reactor
U1(s):	The primary voltage
U2(s), U3(s):	Intermediate node voltages
U4(s):	The output voltage normalized to primary side
Zd1(s) ~ Zd6(s)	equivalent impedances corresponding to different ports

The equivalent impedance Calculation

The equivalent impedance of different ports in Figure 29 can be calculated as below:

$$Z_{d6}(s) = Z_m(s) \parallel Z_D(s) \parallel Z_L(s)$$

$$Z_{d5}(s) = Z_{d6}(s) + R_1$$

$$Z_{d4}(s) = Z_{d5}(s) \parallel \frac{1}{sC_{s1}}$$

$$Z_{d3}(s) = Z_{d4}(s) + \{(R_2 + sL)) \parallel \frac{1}{sC_{s1}})\}$$

$$Z_{d2}(s) = Z_{d3}(s) \parallel \frac{1}{sC_2}$$

$$Z_{d1}(s) = Z_{d2}(s) + \frac{1}{sC_{s1}}$$

The voltage equations can be written considering Up and Us are primary and secondary side voltage of CVT, and N is the ratio of intermediate transformer; s = jω, ω is angular frequency. In order to avoid complex calculation, the transfer function can be obtained by using of MATLAB Simulink. The equivalent impedances of different ports step by step are calculated and easily we can receive the frequency characteristics of the transfer function G(s). The compensation for the errors in the output signal will become possible and the harmonic measurement in EHV systems over the frequency range specified in standards.

The use of the transfer function for error compensation has three main disadvantages:

1. In order to get the transfer function, the offline test should be carried out.
2. The test must be performed for all types and models of CVTs in the system where the harmonic measurement is necessary.
3. The information of Burden is a part of the calculation. Therefore, for various burdens there will be different errors and the proper frequency curve must be selected for the CVT response modification.

1.3.2 PQ sensor

The other possibility is to using another device as a Power Quality sensor Can be retrofitted to in service CVTs or installed in new units. It is able to measure harmonics or flicker over a wide bandwidth from sub synchronous to high frequencies. The reasonable cost and the speed of installation can be considered as its advantages.

Chapter 2: Accuracy of Capacitive Voltage Transformers

2.1 Parameters Influencing CVTs Accuracy

The instrument transformers used in power system must be in agreement with the rated operating condition. The rated and distorted condition of the grid is adopted by EN 50160 and IEEE 519. These standards define the limits and the thresholds for the grid quantities. Instrument Transformer is associated with an accuracy class that determines its performance. In fact, accuracy is evaluated by two parameters:

1. Ratio Error ε

$$\varepsilon = \frac{k_r V_2 - V_1}{V_1}$$

2. Phase Displacement Δφ

$$\Delta\varphi = \hat{V}_2 - \hat{V}_1$$

Where V_1 and V_2 are the primary and secondary rms voltages in the rated frequency and k_r is the rated transformation ratio of the device under test. Respectively, $\hat{V}_1$ *and* $\hat{V}_2$ are 50 Hz phase components of the primary and secondary voltages. In addition, each ε and Δφ computation is associated with a temperature measurement of the working environment.
By monitoring these two parameters the accuracy behaviour of the ITs in a long-time interval can be understood.

2.1.1 Design Characteristics Influencing Accuracy of CVTs

2.1.1.1 Capacitive Divider

As is well known, the accuracy of the instrument transformers is affected by transformer design, external phenomena and the operating conditions.
The capacitive divider of CVTs must be designed and modelled in a way to have an accurate performance. So far, an ideal representation of a capacitive divider was assumed. In order to have a better model the non-idealities of the capacitor should be considered.

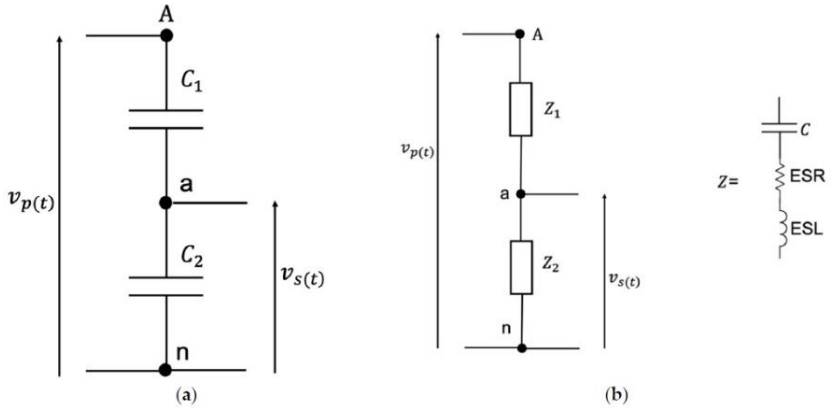


Figure 26: Ideal and Non-ideal Representation of Capacitive Divider. Adopted from [22]

As it can be seen the capacitor is modelled as an impedance including two additional components: an equivalent series inductance (ESL) representing parasitic inductance and an equivalent series resistor (ESR) to model the heat dissipated due to the metallic parts and electrodes in the capacitor. ESL depends on the application frequency and may cause the auto-resonance phenomenon of the capacitor and change the operation condition.

2.1.1.2 Stray Capacitance - Parasitic Effects

Parasitic capacitance or stray capacitance is an unavoidable phenomenon that occurs when parts of an electronic component or circuit are close to each other. The electric charge can be stored on electrical conductors at different voltage level and is considered as capacitance effect. Stray capacitance has a significant effect on the harmonic transmission characteristics of CVTs.

During operating at harmonic frequencies, the original model structure of the CVT changes. Its internal stray capacitance interacts with capacitance and inductance in the main circuit and as a result there will be a greater error on the secondary measurement signal.

CVT Components and the effect of Stray Capacitance

The shape and size of internal components are determined by the manufacturer and the relative position between the conductors is defined. The environmental factors affect the medium between conductors and consequently the stray capacitance.

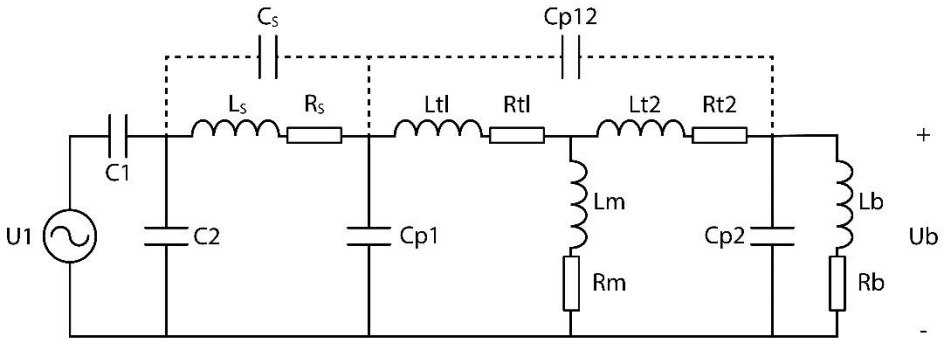


Figure 27: CVTequivalent circuit including stray capacitances

A. Compensation Reactor Stray Capacitance

The compensation reactor with an adjustable airgap is used for the compensation of the phase shift caused by the coupling capacitor. Variation of each tap with amount of ±2%, causes the variation of CS of the compensation reactor at about ±2%. From the below equation the equivalent distributed capacitance for a reactor with n layer winding can be calculated.

$$C_x = \frac{4(n-1)\,\varepsilon_r \varepsilon_0 l\, D\, N}{3\, n^2 d}$$

C_x: Reactor equivalent distributed capacitance
l : average length
D: diameter of the conductor cross-section
d: the distance between layers
N: number of turns in each layer

B. Intermediate Transformer Stray Capacitance

The intermediate transformer winding and the compensation reactor have a similar structure. Thus, the distributed capacitance parameters of the intermediate transformer winding can also be calculated through the above equation. In order to improve the antiferromagnetic resonance, the core is made by a high-quality cold-rolled silicon steel sheet. For the primary winding ±5% of the regulation winding is considered for C_{p1}, C_{p2}, and C_{p12}. Therefore, the stray capacitance on intermediate transformer primary side can affect the entire frequency of the CVT amplitude transfer characteristic

It will be the same effect caused by stray capacitance of the coupling capacitance between the primary side and the secondary side while stray capacitance to the ground on the secondary side of the intermediate transformer has no effect on the harmonic transmission characteristics of the CVT.

As conclusion it can be said that the existence of the stray capacitances affects amplitude and frequency characteristics curve of the CVT and causes larger error measurements. For instance, C_s affects the frequency range after the extreme value point of the CVT amplitude transfer characteristic. C_{p1} and C_{p12} affect the entire frequency range of the CVT amplitude transfer characteristics, while C_{p2} does not have any effect on the harmonic transmission characteristics of the CVT.

2.1.1.3 Dielectric

CVTs shows an overall acceptable running situation. For a safe and reliable operation, we need to consider defects such as manufacturing quality, oil shortage, insulation aging.
In both DC and AC voltages the dielectric loss can be occurred in form of heat in real dielectrics. In case of the applied DC voltage across the insulation material the leakage current arises and cause heating of the insulation material. Considering AC voltages, currents of periodic polarization are added to the leakage current. The heat produced in the materials can lead to a deterioration of the insulation properties of the material or Electrical breakdown in large values of the released thermal

energy. Hence, the quality of insulation material must be tested during manufacturing and exploitation process in order to be able to detect the probable defects.
The real insulation material can be considered as a capacitor including capacitance C_x and active resistance R_x. Considering U as the external voltage and W as the electrical energy stored the below equation can be defined:

$$W = \frac{C_x U^2}{2}$$

For a certain time t, the thermal energy caused by leakage currents is defined as following

$$Q = \frac{U^2}{R_x}$$

The equivalent circuit of capacitor the parameters C_x and R_x can be connected in series for small losses or parallel for larger losses. In the following the power dissipation of a parallel equivalent is given.

$$P_a = U \,.\, I_R = U \,.\, I_c \,.\, tg\ \delta = U \,.\, \frac{U}{X_c}\ tg\ \delta = U^2\, \omega\, C_x \,.\, tg\ \delta$$

Where $X_c = {}^{1}/_{\omega\, C_x}$, δ is dielectric loss angle and ω is the angular frequency of the applied sinusoidal voltage U.

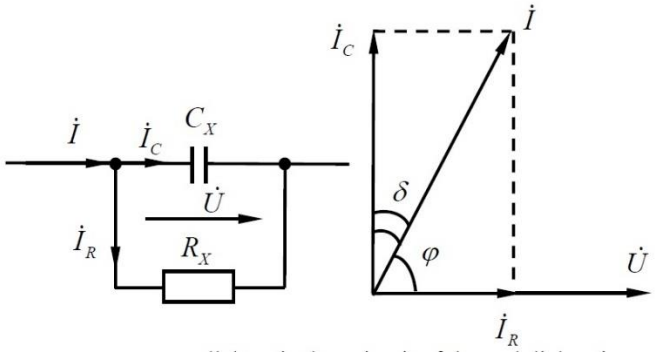


Figure 28: Parallel equivalent circuit of the real dielectric (capacitor) Adopted from [26]

In the material used in high voltage applications, high frequency devices the dielectric losses are more significant. The reason is that the value of dielectric loss is proportional to the square of voltage and frequency. Consequently, the materials used in high frequency-voltage operation must differ by small values of loss angle and dielectric constant to have low value of the power dissipated in the material. Considering the inner insulation dielectric loss and the outer surface leakage current in CVTs we can achieve a new equivalent circuit. The capacitive divider cannot be assumed purely capacitive.
In the proposed equivalent circuit C_{11}, C_2, and C_3 representing the high-voltage capacitance, and C_{12} belongs to the low-voltage capacitor. Temperature and dielectric breakdown are main factors affecting the equivalent capacitance. For temperature rises the equivalent capacitance decreases since a capacitor has a negative temperature coefficient. R_{11}, R_{12}, R_{21}, and $R_{31}$are the insulation resistances of each segment. Increase of the dielectric loss factor represents a decrease in insulating resistance. When temperature increases, the dielectric loss of capacitor will first decrease and then increase. Therefore, the corresponding insulation resistance will first increase and then decrease. R_{13}, R_{22}, and

R_{32} are the surface equivalent resistances. Increase of leakage current represents decrease of surface resistance. The main factors influencing the surface resistance is environmental contamination and humidity.

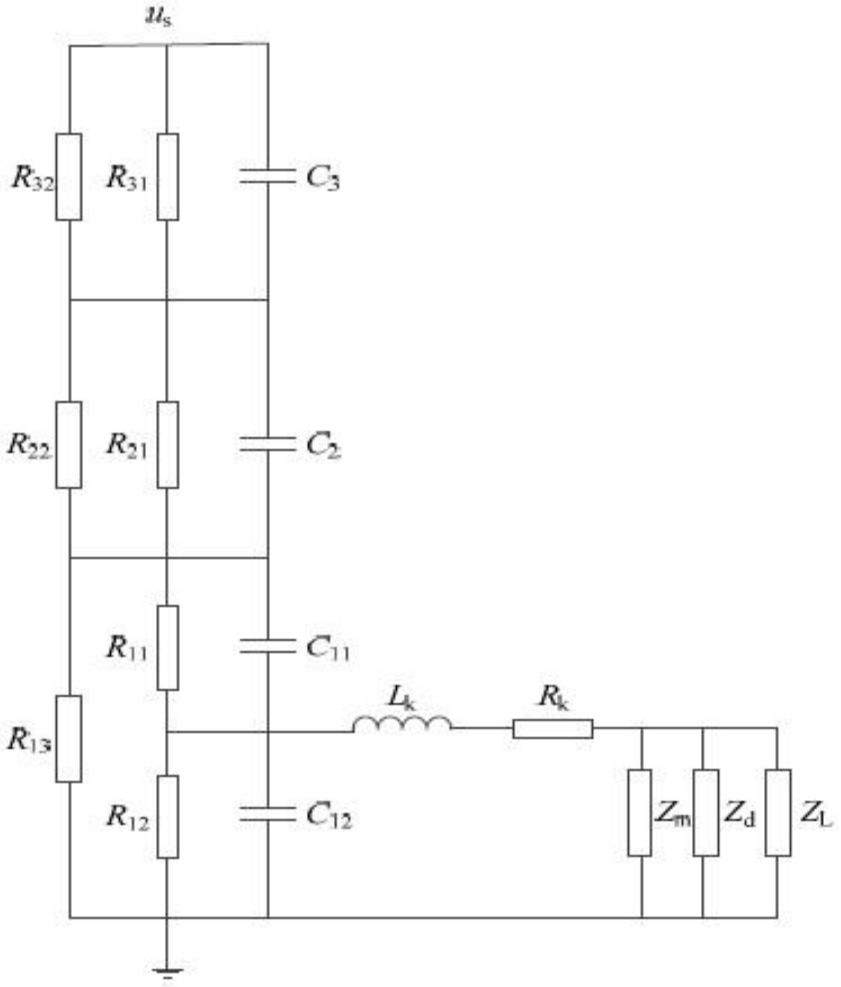


Figure 29: Proposed circuit model of a CVT including inner insulation dielectric loss and the outer surface leakage current. Adopted from [21]

When contamination and humidity in the atmosphere increases, the surface leakage current of a capacitive divider will increase, which represents the decrease in surface resistance. The electromagnetic unit, Lk, is the sum of compensation reactor reactance and leakage reactance of the transformer, which can be used to resonate with equivalent capacitance of the voltage divider C_0, $L_k = 1/(\omega^2 C_0)$. R_k is the sum of tuning reactor resistance and short circuit resistance of the transformer; Z_m is the excitation impedance of the transformer; Z_d and Z_L are the impedance of the damper and load which are recalculated to the primary side of the step-down transformer.

2.1.2 External Phenomenon Influencing Accuracy of CVTs

In addition to the design parameters the external factors are significant in the behaviour of the ITs. Factors like temperature, humidity, electric fields and pressure should be considered when assessing a CVT in operation.

2.1.2.1 Ambient temperature

The effect of ambient temperature can be investigated by considering the device in two different parts:

a. Capacitive Divider
Temperature can be considered as the one of the most influencing parameters that affects a Capacitive divider. For the high or low temperature (compared to the rated one 20-25 °C, the accuracy of the divider goes outside of its accuracy class (AC) limits. Based on the tests done in [23] at the rated and low frequency, temperature effect is almost negligible. It is worth mentioning that the self-resonance phenomenon is affected by temperature variation. For instance, the resonance frequency moves from almost 90 kHz at 20 °C to 80 kHz at both −5 °C and 40 °C temperatures. It can be concluded that the secondary capacitor of the divider shows a temperature dependency. It should be noted that the main dielectric material of the capacitor is insulating oil, which can ignore the influence of humidity, but the influence of temperature on the dielectric constant cannot be ignored. Then considering $C = \varepsilon S/d$ as formula of capacitance plates, the size and position of the conductors remains the same and humidity and ambient temperature don't affect the capacitive divider. The main dielectric material of the capacitor is insulating oil, which can ignore the influence of humidity, but the influence of temperature on the dielectric constant cannot be ignored. The capacitance temperature coefficient is generally less than or equal to -4×10^{-4}/K. When the ambient temperature changes ±40°C, it may bring about a change of 3.2% in dielectric constant, which will directly affect the accuracy of harmonic transmission of CVT. [13]

b. Inductive Transformer
The inductive transformer contains copper windings and the core made up of high-quality cold-rolled silicon steel sheet to improve the antiferromagnetic resonance characteristics. Presence of core losses (Eddy current loss and Hysteresis loss) and copper loss due to the resistance of the windings results in heat production at the intermediate transformer.
For and inductive transformer the so-called transformer temperature rise is the average temperature rise of windings above the ambient temperature and it must be less than the design rated value for safety reasons.

2.1.2.2 Ambient Humidity

In figure 28 the surface equivalent resistance is represented by R_{13}, R_{22}, and R_{32}. The surface resistance decreases as the leakage current increases. The most crucial factors affecting the surface resistance are environmental contamination and humidity.

2.1.2.3 Electric fields

Error characteristics of CVT is affected by numerous factor such as temperature, humidity, frequency, ambient electric field, secondary load and so on. In substations where the concentration of power equipment layout increases the ambient electric fields effect on the error characteristics of the CVT becomes significant. As it is discussed in chapter 1 the main components of a CVT can be considered as the capacitive divider and Electromagnetic Unit (EMU). In fact, locating the EM unit in a metal box in actual operations, a perfect electromagnetic shielding effect is provided. Therefore, the ambient electric field has little effect on the EM unit and can be ignored in this section. On the other hand, the capacitive divider is directly exposed to the external environment.

Actual voltage division ratio:

$$K_r = \frac{C_1 C_2}{C_1}$$

Existence of stray capacitances between capacitive divider and the other equipment near to CVT causes a deviation on the actual division ratio. [27]

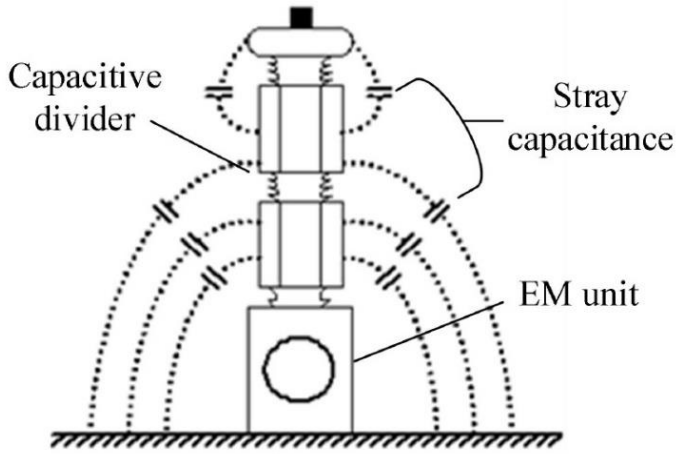


Figure 30: Effect of ambient electric field Adopted from [27]

2.1.2.4 Pollution

The accuracy of a CVT is influenced by pollution which results in external creepage currents. Considering a several parts of porcelain insulator in a CVT, different creepage current can be assumed on each part. This affects the ratio error as the voltage dividing is affected by the creepage currents. Higher the capacitance lower will be the sensitivity to pollution.

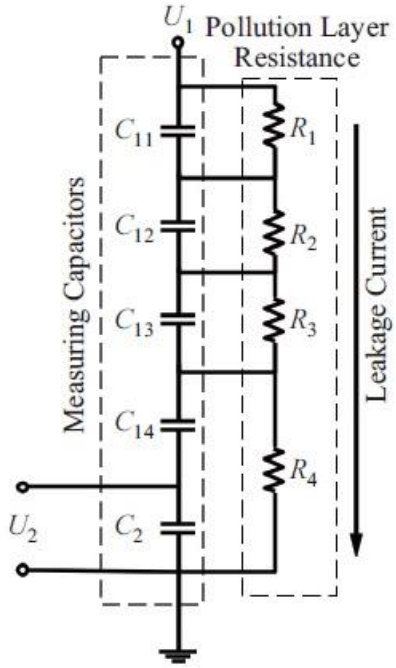


Figure 31: Modelling of Pollution layer resistances. Adopted from [28]

The effect of leakage current on an uneven pollution layer can be modelled as the figure 3**0** by using of pollution layer resistances.

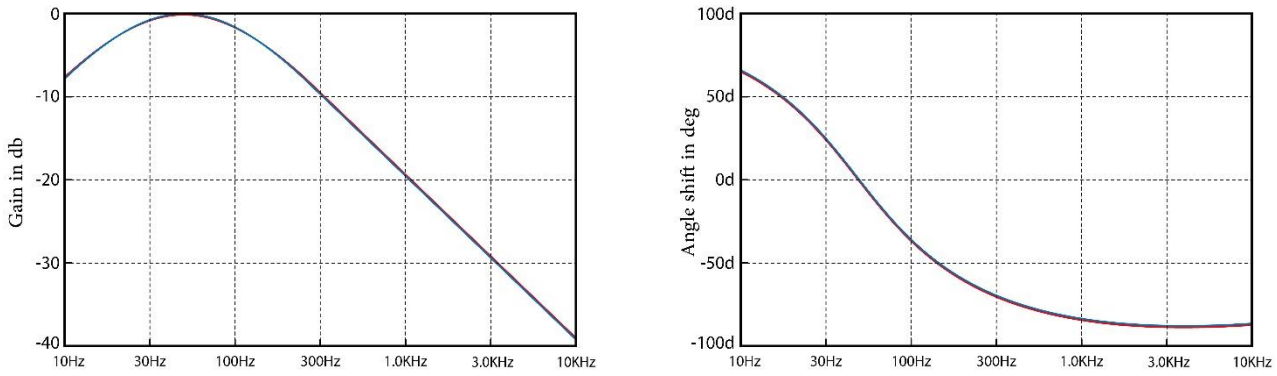
2.1.3 Operating Conditions Influencing Accuracy of CVTs

2.1.3.1 Frequency

The frequency response of CVT is represented by its gain (in decibels or dB) and phase angle (in radians or degrees) plotted against frequency (in radians/sec or Hertz). These plots are known as the magnitude or amplitude response and the phase angle response respectively. In general, a magnitude gain of unity (1.0) and phase angle shift of zero (0°) degrees for the wide range of frequencies is an ideal frequency response. For capacitive voltage transformers, it is difficult to obtain the ideal frequency response. The gain curve is obtained by plotting the gain values at different frequencies according to the relationship:

gain dB = 20*log10(*gain*),
the unity *gain* (1.0) of ideal response is equivalent to zero gain in dB as 20*log10(*1*) = 0.

The magnitude response of the CVT varies with the frequency, i.e., the gain is not constant at all frequencies. The gain curve is flat and represents the unity gain at normal operating frequency. Hence, the performance is good under the steady state condition. However, the response of CVT is deviating from unity gain for other frequencies. Therefore, the output signal is not an exact replica of the input signal for other frequencies. In this paper, to care of switching transients occurring in the system, the frequency response of CVT is considered up to 10kHz



a) Magnitude vs Frequency Plot

b) Phase angle vs Frequency Plot

Figure 32: Typical CVT frequency response. Adopted from [12]

The typical magnitude response of the CVT is shown in Fig. 24 (a). At normal operating frequency, the gain curve is flat and unity i.e., the output signal is same as the scaled down input signal. For the sub synchronous frequencies, the gain is less than unity i.e., the output signal is less than the input signal in terms of magnitude. There is attenuation in the output signal for DC and sub synchronous components of the signal. For the higher order frequencies, the attenuation is more. The phase response of the CVT is shown in Fig. 24(b). The phase response of the CVT varies with the frequency. For the rated frequency there is no phase difference between the input and output signal i.e., zero phase shift (0°). In case of sub synchronous frequencies, the output signal leads the input signal in phase. In case of higher order frequencies, the output signal lags the input signal. The phase curve is almost linear till 300Hz and it remains almost constant for frequencies above 300 Hz.

1.3.1 Factors Influencing CVT Frequency Response

There are three major factors that influence the CVT frequency response:
1. Ferroresonance Suppression Circuit (FSC)
2. CVT Design parameters
3. Burden.

1.3.1.1 Ferroresonance Suppression Circuit (FSC)

The FSC is one of the major components which affects the frequency response of CVT. There are two types (active FSC and passive FSC) of FSC designs widely used. The active type of FSC comprises of inductance, capacitance and loading resistor. This forms an LC parallel circuit in series with resistor tuned to fundamental frequencies at which it offers very high impedance. The permanent connection of the active type FSC gives undesirable frequency response for other system harmonic frequencies. The passive FSC consists of saturable inductor (150% of normal voltage) and loading resistor which remains inactive, i.e., “passive”, for all conditions other than the ferroresonance. Therefore, the frequency response of passive FSC is better than active FSC. [12]

The resistance value of the ferroresonance suppression circuit is another factor that influences the frequency response of CVT. Generally, the value of ferroresonance suppression resistance (Rf) is less than the burden. Hence, it will have loading effect on the CVT. The active FSC is considered for studying the effect of Rf on the CVT frequency response. The Fig. 25(a). shows the magnitude response of the CVT with different ferroresonance suppression resistances. The lower value of Rf results in more attenuation of the output signal and the magnitude curve improves with the increase in the Rf value, i.e., the loss of signal is reduced with higher value of Rf.

The output signal leads the input signal for the sub synchronous frequencies and it lags the input signal for higher order frequencies as shown in Fig. 25(b). The phase response of CVT is comparatively better with increase in Rf value for non-fundamental frequencies. It is observed that the magnitude and phase responses of the CVT improves with increase in the value of the ferroresonance suppression resistance. However, the change in the phase response is minimal with the change in Rf value. [12]

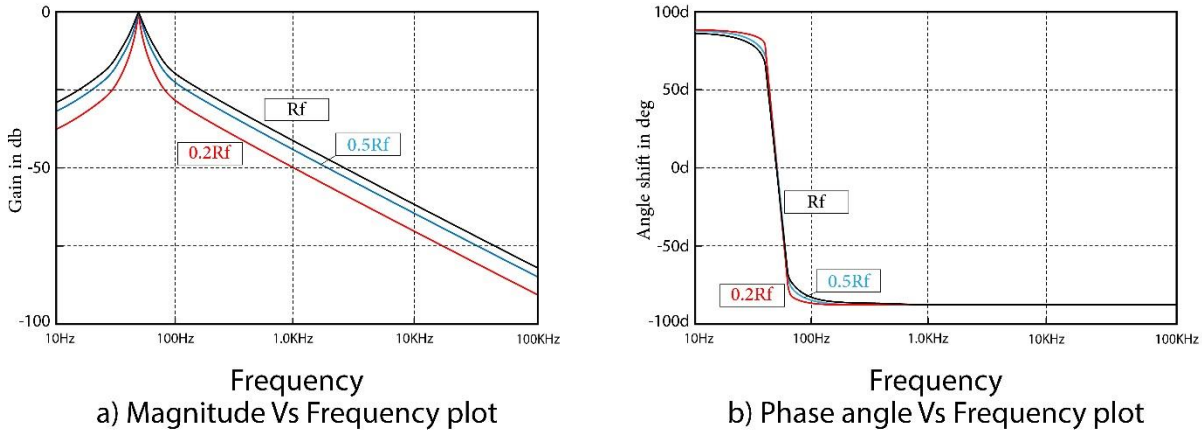


Figure 33: CVT frequency response with variation of Ferroresonance suppression resistance. Adopted from [12]

1.3.1.2 CVT Design parameters

The various design parameters of CVT that have influence on its frequency response are:

1. Ratio of Step-Down Transformer

The increase in the turns ratio of the step-down transformer will result in higher value of secondary current for a given burden impedance and increase in the loading of step-down transformer. Therefore, for a given burden, the increase in the turns ratio results in better magnitude response.

2. Stack capacitance

The frequency response with the variation of the value of capacitance is shown in Fig. 5. For sub synchronous frequencies, the magnitude response is better with increase in the value of capacitance as shown in Fig. 26(a). The increase in the capacitance value gives better phase response for sub synchronous frequencies as shown in Fig. 26(b). It is observed that there is no change in the magnitude and phase response with the variation of capacitance for the higher order frequencies.

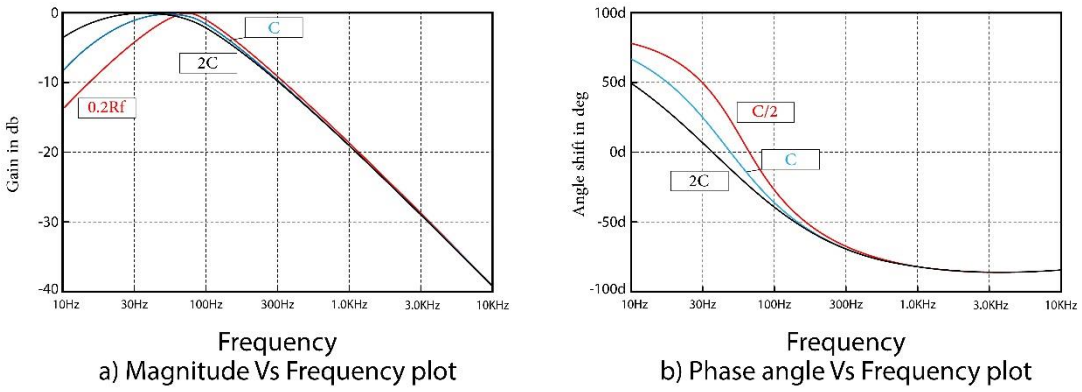


Figure 34: CVT frequency response with variation of Capacitance. Adopted from [12]

1.3.1.3 Burden

The burden which is generally connected external to the CVT is also plays a significant role in determining its frequency response. The effect of composition (power factor) and magnitude of the burden are considered for study.

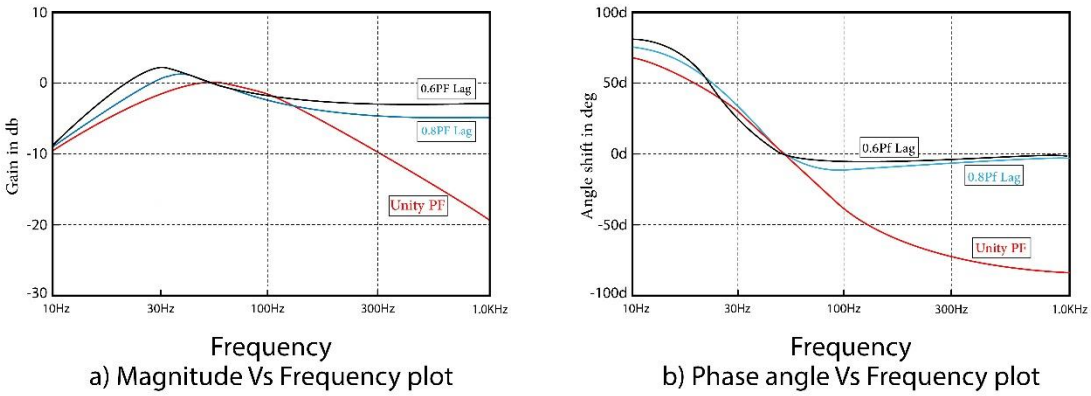


Figure 35: CVT frequency response with variation of Burden power factor. Adopted from [12]

The effect of the burden power factor on frequency response of the CVT is shown in Fig. 27. Generally, the unity power factor burdens or 0.8 lagging power factor burdens are used in the field. The 0.6 lagging power factor burden is considered for illustrative purpose only. The magnitude response is better in case of burden with lower power factor as shown in Fig.27(a). The phase response improves with the increase in burden power factor for sub synchronous frequencies but the phase response worsens with increase in burden power factor for higher order frequencies as shown in Fig.27(b).

In case of 0.8 lagging power factor burden for certain range of sub synchronous frequencies, the gain curve crosses the zero dB point i.e., the gain is more than unity. The gain curve is becoming flat for frequencies more than 50Hz. In case of unity power factor burden, the gain curve is flat and unity for the normal operating frequency and the attenuation is more for higher frequencies compared to other power factor burdens.

In case of unity power factor burden there is comparatively lower phase shift for sub synchronous frequencies but the phase shift is comparatively more for higher order frequencies. For 0.8 lagging pf burden, there is comparatively more phase shift observed for sub synchronous frequencies but the phase shift is comparatively lesser and remains almost constant for higher frequencies.

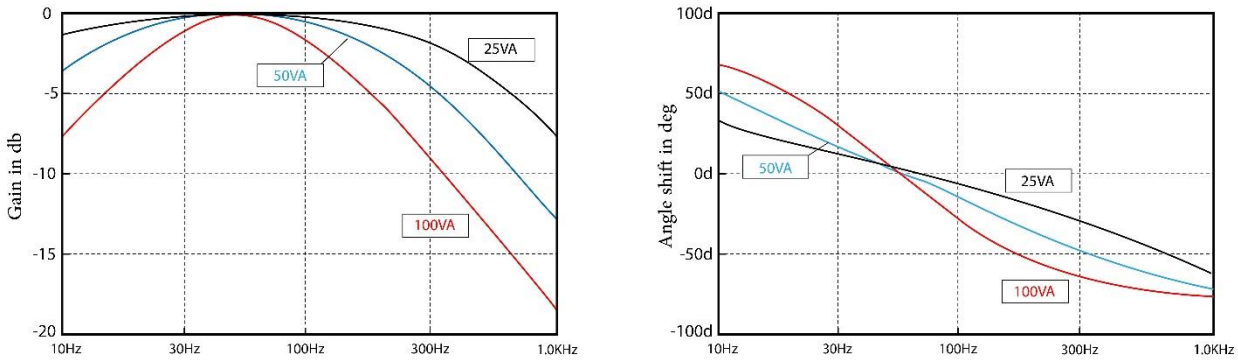


Figure 36: CVT frequency response with variation of Burden magnitude. Adopted from [12]

The effect of burden magnitude (VA with unity power factor) on frequency response of the CVT is shown in Fig. 7. The Fig.7(a) infers that the magnitude response of the CVT is becoming flat for wide frequency band near the rated frequency by decrease in the burden VA. The Fig. 7(b) infers that the shift in the phase angle is decreasing and becoming flat near the rated frequency by decrease in the burden VA. The magnitude and phase responses of the CVT are improving with decrease in the VA of the burden as shown in Fig.7(a) and Fig. 7(b). [12]

It must be noted that the intermediate core losses, eddy current and hysteresis losses, are directly proportional to the operating frequency and as the frequency increases the power dissipated more and converted to heat.

Chapter 3: Simulation

3.1 Equivalent Circuit and Parameters

In order to understand better the behavior of capacitive voltage transformers, the equivalent circuit according to the actual structure is set up and can be examined in MATLAB Simulink.

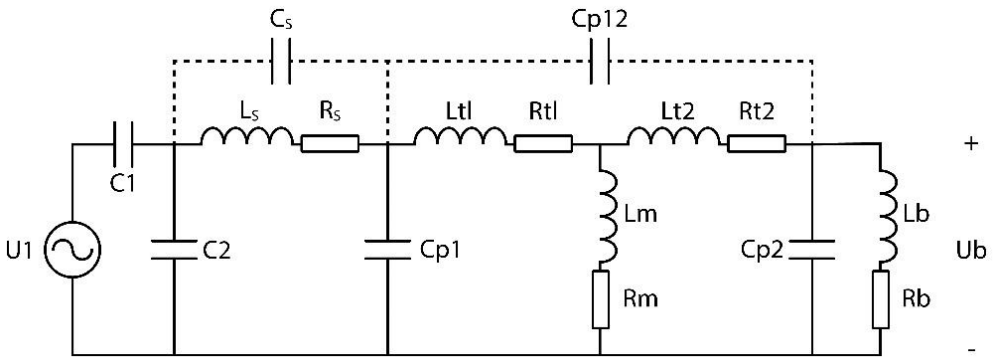


Figure 37: CVT Equivalent Circuit with stray capacitances. Adopted from [13]

Parameter	Description
U1	primary voltage
U2	secondary voltage
C1	Capacitance
C2	Capacitance
LS	Reactance of the compensation reactor
RS	Resistance of the compensation reactor
Lt1	equivalent leakage inductance of the intermediate transformer primary side
Rt1	equivalent leakage resistance of the intermediate transformer primary side
Lm & Rm	intermediate transformer excitation impedance
Lt2	equivalent leakage inductance of the intermediate transformer secondary side
Rt2	equivalent leakage resistance of the intermediate transformer secondary side
CS	stray capacitance of compensation reactor
Cp1	primary side stray capacitance of the intermediate transformer
Cp2	stray capacitance to the ground on the secondary side of the intermediate transformer
Cp12	coupling capacitance between the primary side and the secondary side
Rb & Lb	Load impedance

Table 2: CVT Parameters Description. Adopted from [13]

3.2 Modelling of the CVT equivalent circuit can be done through three main approaches:

1. Using MATLAB Simulink blocks to represent the equivalent transfer function
2. Using built-in Simscape blocks of Electrical components
3. Using built-in Transfer block (validating the first two approaches)

CVT Equivalent Circuit Modelling by Transfer Function

In order to find the transfer function of the system the following steps can be followed:

a. Find the equations describing the system
b. Identify the system input and output variables
c. Take Laplace Transform of these equations, assuming zero initial conditions
e. Find the ratio of the output to the input (Laplace Transform).

Defining the impedances of Figure 30:

$Z_1 = s * L_b + R_b$, $Z_2 = s * L_{t2} + R_{t2}$,

$Z_3 = s * L_{t1} + R_{t1}$, $Z_4 = s * L_s + R_s$,

$Z_5 = {}^{1}/_{s(C_1+C_2)}$, $Z_6 = {}^{1}/_{s * C_s}$,

$Z_7 = {}^{1}/_{s * C_{p1}}$, $Z_8 = {}^{1}/_{s * C_{p12}}$,

$Z_9 = {}^{1}/_{s * C_{p2}}$

The transfer function without considering the effect of stray capacitances can be driven as below:

$$H_1(s) = \frac{Z_1}{Z_1 + Z_2 + Z_3 + Z_4 + Z_5}$$

The transfer function without considering the effect of stray capacitances can be driven as below:

$$H_2(s) = \frac{[Z_1 \| Z_9 + (Z_2 + Z_3) \| Z_8] \| Z_7 \| Z_4 \| Z_6}{[Z_1 \| Z_9 + (Z_2 + Z_3) \| Z_8] \| Z_7 \| Z_4 \| Z_6 + Z_5}$$

AS the study object the CVT with the model TYD100/3 -0.01H was selected in the simulation study process.

Parameter	Value
U1	$100/\sqrt{3}$ KV
U2	$100/\sqrt{3}$ V
C1	0.01257μF
C2	0.04885μF
LS	164.96H
N1	≈ 10000T
N2	≈ 45T
e_t	1.3 V/T
CS	80.3 pF
Cp1	80.5pF,
Cp2	11.1pF
Cp12	80pF
Load	100 VA / 0.8

Table 3: CVT model TYD100/3 -0.01H parameters' values [13]

3.3 Stray Capacitance calculation:

The equivalent distributed capacitance of a U-shaped row winding induction coil with n layers based on electromagnetic field theory is calculated as following:

$$C_x = \frac{4(n-1)\,\varepsilon_r \varepsilon_0 l\, D\, N}{3\, n^2\, d}$$

Where: l is the average length, D is the diameter of the conductor cross-section, d is the distance between layers, and Nis the number of turns in each layer.

a. Compensation Reactor

Compensation Reactor Parameters	
n	10
N	300
l	82.4mm
D	0.25mm
d	0.18mm
ε_r	2.2

Table 4: CVT model TYD100/3 -0.01H – compensation reactor parameters [13]

The capacitance of the compensating reactor is calculated as 80.3 pF.

$C_s = 80.3$ pF

b. Intermediate Transformer

Considering similar structure with the compensation reactor the same equation can be used for calculation of the stray capacitances.

Intermediate Trans. Parameters	
n	16
N	650
l	58.6mm
D	0.25mm
d	0.18mm
ε_r	2.2

Table 5: CVT model TYD100/3 -0.01H – Intermediate Transformer Parameters [13]

Consequently, the followings are defined:

$C_{p1} = 80.5\text{pF}$
$C_{p2} = 11.1\text{pF}$
$C_{p12} = 80\text{pF}$

The influence of the Stray Capacitances is shown by dashed line in the figure. For the simplicity the equivalent impedance of the damper is neglected.

Primary winding voltage of intermediate transformer can be driven by using a capacitance divider:

$$U_p = U_1 \frac{C_1}{(C_1 + C_2)} = 12{,}997.4\ [V]$$

In continue the behavior of CVT under different operating conditions is evaluated:

a. Existence of Noise at the input voltage

b. Existence of Noise at the frequency

c. Existence of Thermal Noise

3.4 Application the Equivalent Circuit in MATLAB Simulink

This section builds a MATLAB/Simulink simulation model based on the CVT equivalent circuit model, as shown in Figure 31.

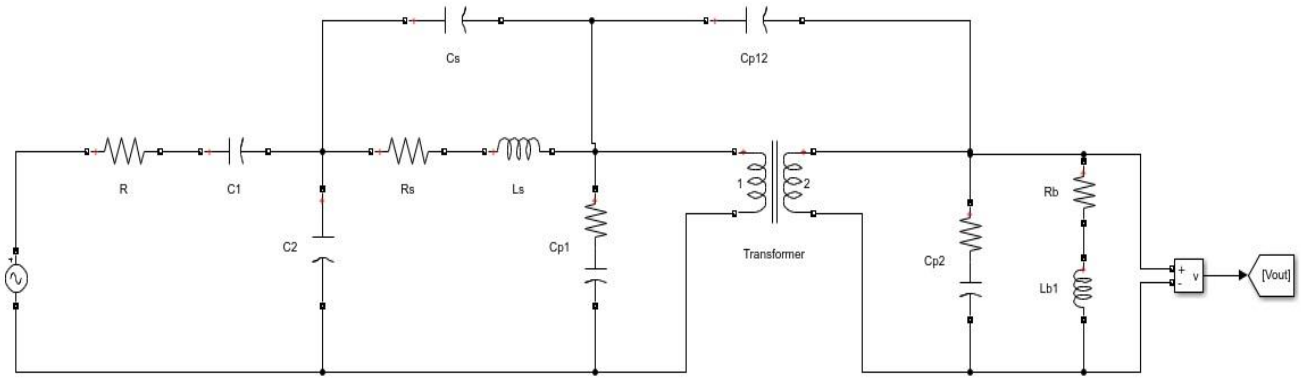


Figure 38: CVT Equivalent Circuit – MATLAB Simulink

3.4.1 Modelling of the capacitive divider

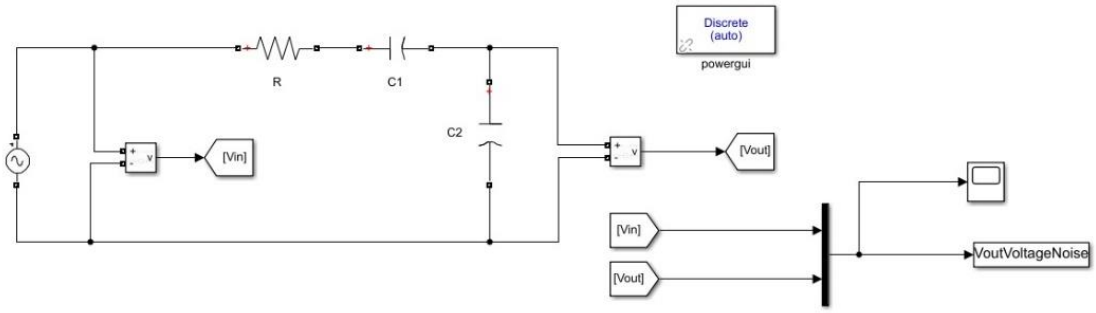


Figure 39: Input voltage and output of Capacitive divider

The plot shows the input voltage signal and the output of the capacitive divider

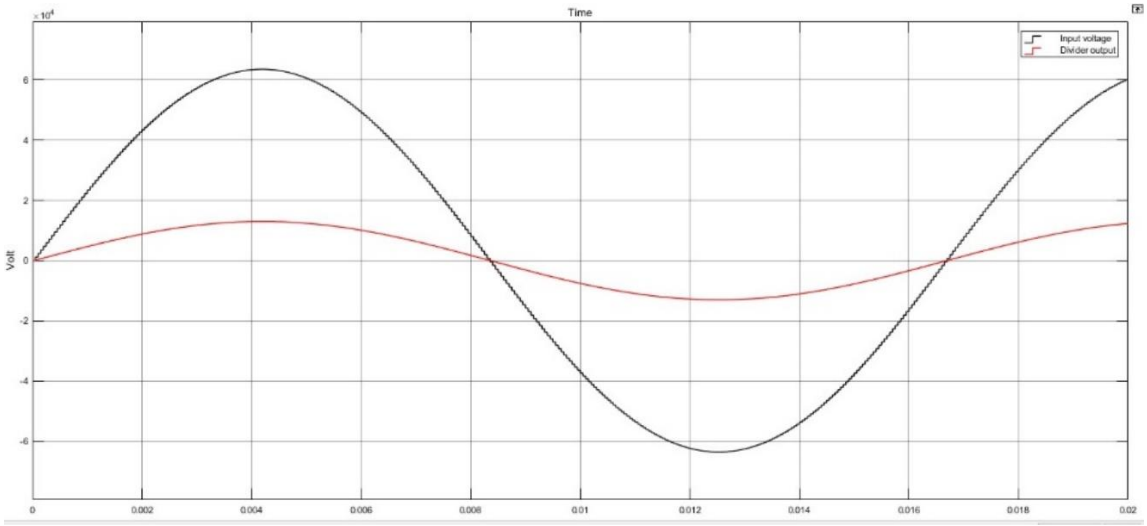


Figure 40: Input voltage (black) and output (red) of Capacitive divider signals

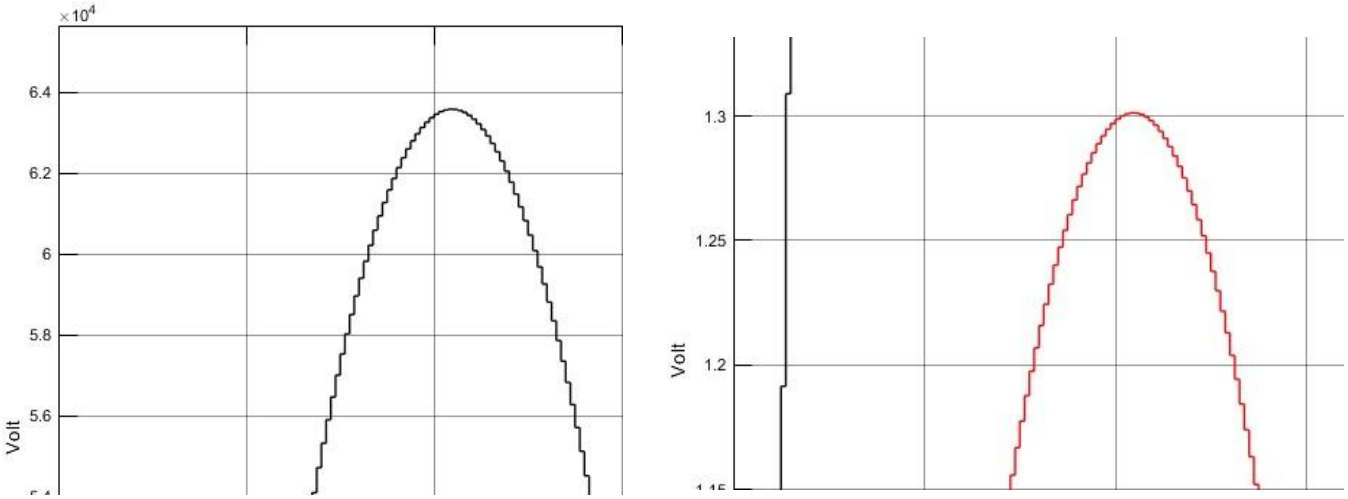


Figure 41: Input voltage and output of Capacitive divider signals-values

Input voltage

$$(110/1.73) * 1000 = 63{,}580\ [v]$$

Output of capacitive divider

$$U_p = U_1 \frac{C_1}{(C_1 + C_2)} = 12{,}997.4\ [v]$$

3.5 Existence of Noise at the input voltage

At this part two identical CVT model outputs are compared to realize the effect of the input voltage noise on the output of the CVT. The CVT equivalent circuit considered as the subsystem for the simplicity of the diagram and are represented by CVT1 and CVT2 at the figure 41.

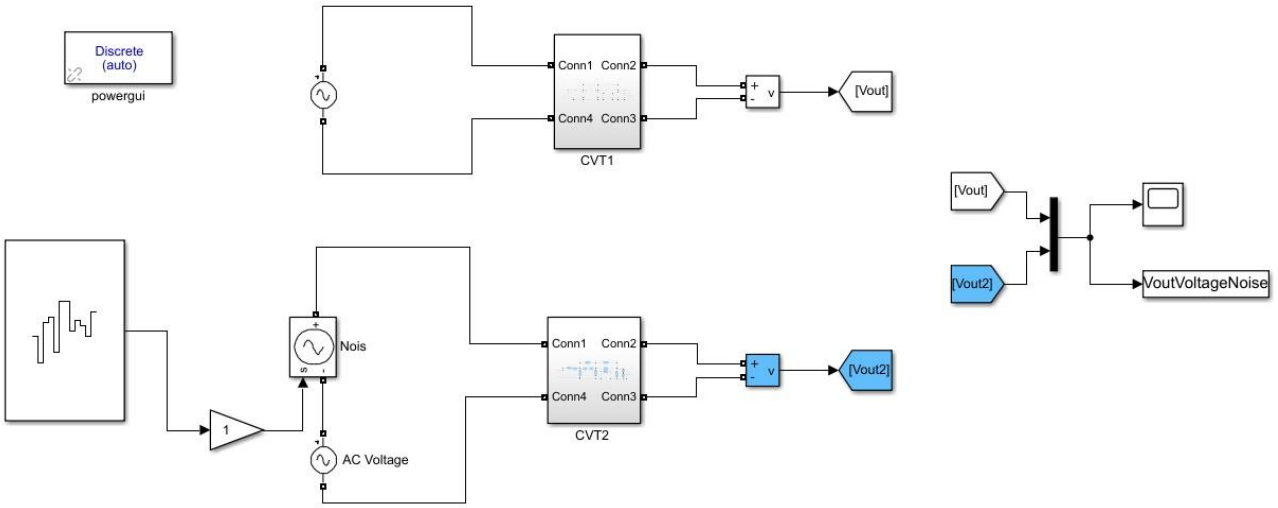


Figure 42: Simulation of input voltage (with and without noises)

3.5.1 Introduction of additional components for producing the noise at the input voltage

In order to create a noise in the supply voltage of CVT a Band-limited white noise block, a gain block and a controlled voltage source block can be used. Then considering the main circuit and having a second circuit where the noise is applied may give us the possibility to make comparison between the behavior of the CVT in normal condition and during the fault simultaneously.

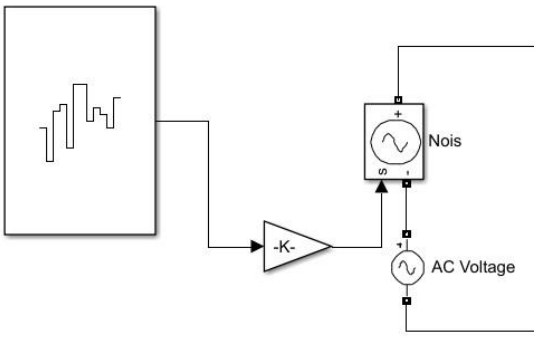
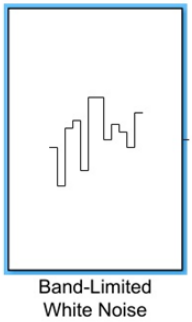


Figure 43: Noise Circuit – Input Voltage Noise

a. Band-limited white noise block:

This block used to generate distributed random numbers that are suitable for use in continuous or hybrid systems. It has a correlation time of zero defining that there is no correlation between two variables. It produces a random signal with equal intensity at different frequencies resulting in flat Power Spectral Density (PSD) and a total energy of infinity.



Therefore, by using of this block we will be able to simulate the effect of a random sequence with a correlation time smaller than the time constant of the system (natural bandwidth of the system).

Figure 44: Band-limited white noise block

b. Gain

The gain block is connected at the output of the band-limited white noise block and is used to multiply the value by a constant gain. Its value can be changed according to the requirement of the simulation.

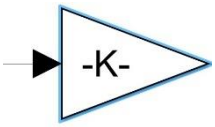


Figure 45: Gain Block

C. Controlled Voltage Source

The Controlled Voltage Source block converts a Simulink® input signal into an equivalent voltage source. The generated voltage is driven by the input signal of the block. The controlled voltage source block can be initialized with AC or DC voltages.

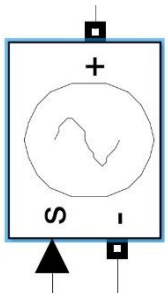


Figure 46: Controlled Voltage Source Block

3.5.2 Analysis of the obtained signals:

By using of Fast Fourier Transform (FFT) analyses provided by Powergui (Graphical User Interface), the output voltages can be observed. The value of Total Harmonic Distortion (THD) determines the value of the included harmonics at the output of the CVT. Harmonics have frequencies that are integer multiples of the waveform's fundamental frequency. For example, given a 60Hz fundamental waveform, the 2nd, 3rd, 4th and 5th harmonic components will be at 120Hz, 180Hz, 240Hz and 300Hz respectively. Thus, harmonic distortion is the degree to which a waveform deviates from its pure sinusoidal values as a result of the summation of all these harmonic elements. The ideal sine wave has zero harmonic components. In that case, there is nothing to distort this perfect wave. It is vital to have lower THD values since it implies lower current peaks, less dissipated heat, lower electromagnetic emissions and less core loss in motors. Unwanted distortion can increase the current in power systems which results in higher temperatures in neutral conductors and distribution transformers. Higher frequency harmonics cause additional core loss in motors which results in excessive heating of the motor core Considering a periodic voltage its harmonic frequencies are the component in the signal having integer multiplies of the frequency of the main signal. The outcome of Fourier analysis of a periodic signal determines the harmonic distortion of the main signal.

While there is no national standard dictating THD limits on systems, there are recommended values for acceptable harmonic distortion. IEEE Std 519, "RECOMMENDED PRACTICES AND REQUIREMENTS FOR HARMONIC CONTROL IN ELECTRICAL POWER SYSTEMS" provides suggested harmonic values for power systems:

"Computers and allied equipment, such as programmable controllers, frequently require ac sources that have no more than 5% harmonic voltage distortion factor [THD], *with the largest single harmonic being no more than 3% of the fundamental voltage. Higher levels of harmonics result in erratic, sometimes subtle, malfunctions of the equipment that can, in some cases, have serious consequences."* [29]

Calculating Total Harmonic Distortion

THD is defined as the ratio of the equivalent root mean square (RMS) voltage of all the harmonic frequencies (from the 2nd harmonic on) over the RMS voltage of the fundamental frequency (the fundamental frequency is the main frequency of the signal.

$$\mathrm{THD} = \frac{\sqrt{\sum_{n=2}^{\infty} V_{n^2\_rms}}}{V_{fund\_rms}}$$

V_{n_rms} is the RMS voltage of the n^{th} harmonic.

V_{fund_rms} is the RMS voltage of the fundamental frequency

The formula above shows the calculation for THD on a voltage signal. The end result is a percentage comparing the harmonic components to the fundamental component of a signal. The higher the percentage, the more distortion that is present on the mains signal.Since the amplitudes of the

harmonics are needed to calculate the THD, Fourier analysis can be used to help determine THD. To see this application of Fourier analysis, let's look at the simple example of a 50% duty cycle square wave. The Fourier series representation of a 50% duty cycle square wave is the following:

$$V_{square}(t) = \frac{4}{\pi} \sum_{n=1,3,5,\ldots}^{\infty} \frac{\sin(2n\pi f t)}{n}$$

At this section the goal is to evaluate the effect of voltage noise on the CVT behavior. Therefore, different values of gain can be considered. Higher the value of gain, higher will be the random noise portion at the supply voltage.

The simulation is done in four different gain values as below and then by using of Powergui the Fast Fourier Transformation (FFT) is determined.

Selected Gain values: 10, 100, 500 and 10,000. (At gain 1 the output will be identical.)

a. Gain=10: The value of the gain is set to 10 and the output of two circuits can be compared.

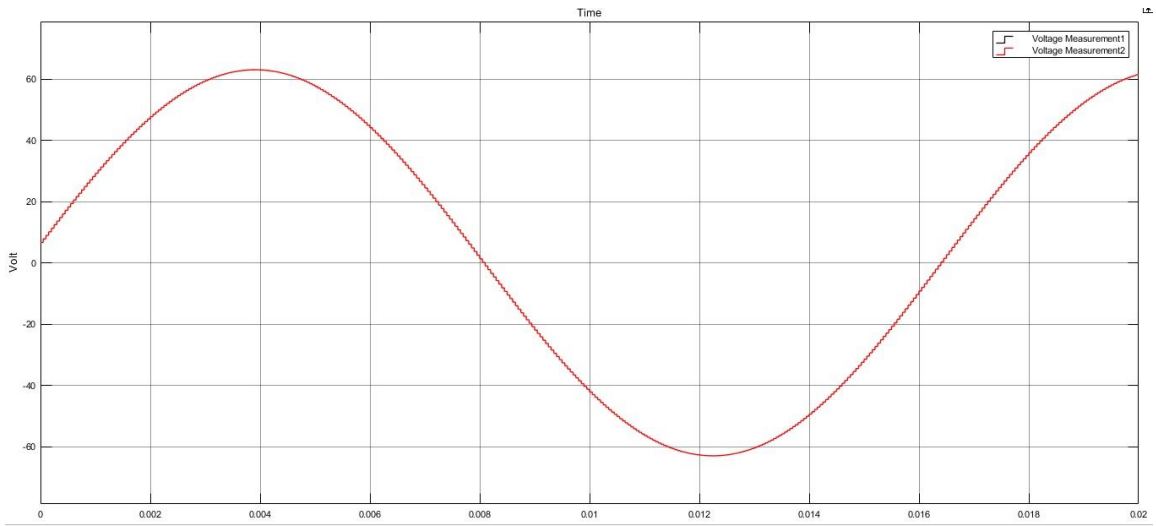


Figure 47: Output voltages – Gain: 10

Figure 46 represents the output voltages of two circuits. The black color represents the output of main equivalent circuit and the red curve shows the output of the circuit affected with white noise at gain chosen at 10. As it can be seen at this level the two voltage curves are identical.

Main circuit Analysis

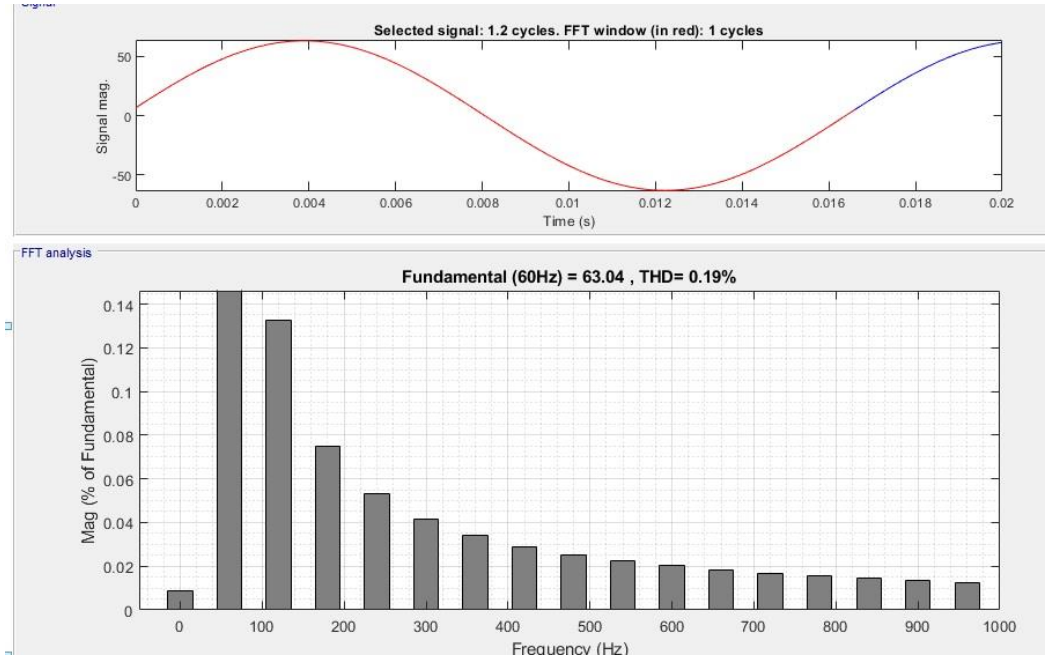


Figure 48: FFT Response – Main Circuit

Figure 47 represents the FFT analysis of the output voltage of the main circuit.

The Total Harmonic Distortion is 19%.

```
Sampling time      = 5e-05 s
Samples per cycle  = 333
DC component       = 0.005634
Fundamental        = 63.04 peak (44.58 rms)
THD                = 0.19%

     0 Hz   (DC):          0.01%     270.0°
    60 Hz   (Fnd):       100.00%       5.8°
   120 Hz   (h2):          0.13%       3.7°
   180 Hz   (h3):          0.07%       3.4°
   240 Hz   (h4):          0.05%       3.5°
   300 Hz   (h5):          0.04%       3.8°
   360 Hz   (h6):          0.03%       4.1°
   420 Hz   (h7):          0.03%       4.6°
   480 Hz   (h8):          0.03%       5.0°
   540 Hz   (h9):          0.02%       5.5°
   600 Hz  (h10):          0.02%       5.9°
   660 Hz  (h11):          0.02%       6.4°
   720 Hz  (h12):          0.02%       6.9°
   780 Hz  (h13):          0.02%       7.4°
   840 Hz  (h14):          0.01%       8.0°
   900 Hz  (h15):          0.01%       8.5°
   960 Hz  (h16):          0.01%       9.0°
  1020 Hz  (h17):          0.01%       9.5°
  1080 Hz  (h18):          0.01%      10.0°
  1140 Hz  (h19):          0.01%      10.6°
  1200 Hz  (h20):          0.01%      11.1°
  1260 Hz  (h21):          0.01%      11.6°
  1320 Hz  (h22):          0.01%      12.1°
  1380 Hz  (h23):          0.01%      12.7°
  1440 Hz  (h24):          0.01%      13.2°
  1500 Hz  (h25):          0.01%      13.7°
  1560 Hz  (h26):          0.01%      14.3°
  1620 Hz  (h27):          0.01%      14.8°
  1680 Hz  (h28):          0.01%      15.3°
  1740 Hz  (h29):          0.01%      15.9°
  1800 Hz  (h30):          0.01%      16.4°
  1860 Hz  (h31):          0.01%      16.9°
  1920 Hz  (h32):          0.01%      17.5°
  1980 Hz  (h33):          0.01%      18.0°
  2040 Hz  (h34):          0.01%      18.5°
  2100 Hz  (h35):          0.01%      19.1°
  2160 Hz  (h36):          0.01%      19.6°
  2220 Hz  (h37):          0.01%      20.1°
  2280 Hz  (h38):          0.01%      20.7°
  2340 Hz  (h39):          0.01%      21.2°
  2400 Hz  (h40):          0.01%      21.8°
  2460 Hz  (h41):          0.00%      22.3°
```

Figure 49: Fundamental component and harmonic signals phase and percentage – Main Circuit

Circuit with Noise at the input voltage – Gain: 10

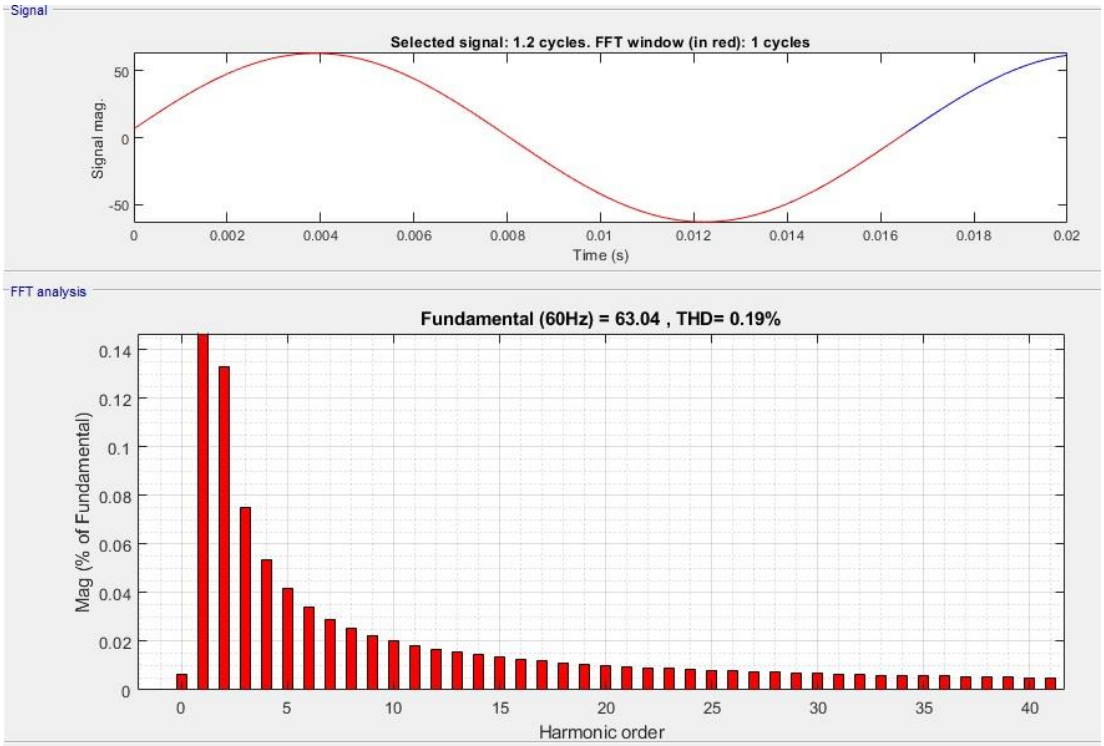


Figure 50: FFT Response – White noise with Gain: 10

Figure 49 represents the FFT analysis of the output voltage of the circuit including the noise with Gain 10

The Total Harmonic Distortion is 19%.

```
Sampling time     = 5e-05 s
Samples per cycle = 333
DC component      = 0.00415
Fundamental       = 63.04 peak (44.58 rms)
THD               = 0.19%

     0 Hz   (DC):          0.01%    270.0°
    60 Hz   (Fnd):       100.00%      5.8°
   120 Hz   (h2):          0.13%      3.7°
   180 Hz   (h3):          0.07%      3.3°
   240 Hz   (h4):          0.05%      3.4°
   300 Hz   (h5):          0.04%      3.6°
   360 Hz   (h6):          0.03%      4.0°
   420 Hz   (h7):          0.03%      4.4°
   480 Hz   (h8):          0.03%      4.8°
   540 Hz   (h9):          0.02%      5.3°
   600 Hz  (h10):          0.02%      5.8°
   660 Hz  (h11):          0.02%      6.3°
   720 Hz  (h12):          0.02%      6.8°
   780 Hz  (h13):          0.02%      7.3°
   840 Hz  (h14):          0.01%      7.8°
   900 Hz  (h15):          0.01%      8.3°
   960 Hz  (h16):          0.01%      8.8°
  1020 Hz  (h17):          0.01%      9.3°
  1080 Hz  (h18):          0.01%      9.9°
  1140 Hz  (h19):          0.01%     10.4°
  1200 Hz  (h20):          0.01%     10.9°
  1260 Hz  (h21):          0.01%     11.5°
  1320 Hz  (h22):          0.01%     12.0°
  1380 Hz  (h23):          0.01%     12.5°
  1440 Hz  (h24):          0.01%     13.1°
  1500 Hz  (h25):          0.01%     13.6°
  1560 Hz  (h26):          0.01%     14.1°
  1620 Hz  (h27):          0.01%     14.7°
  1680 Hz  (h28):          0.01%     15.2°
  1740 Hz  (h29):          0.01%     15.7°
  1800 Hz  (h30):          0.01%     16.3°
  1860 Hz  (h31):          0.01%     16.8°
  1920 Hz  (h32):          0.01%     17.4°
  1980 Hz  (h33):          0.01%     17.9°
  2040 Hz  (h34):          0.01%     18.4°
  2100 Hz  (h35):          0.01%     19.0°
  2160 Hz  (h36):          0.01%     19.5°
  2220 Hz  (h37):          0.01%     20.1°
  2280 Hz  (h38):          0.01%     20.6°
  2340 Hz  (h39):          0.01%     21.1°
  2400 Hz  (h40):          0.01%     21.7°
  2460 Hz  (h41):          0.00%     22.2°
```

Figure 51: Fundamental component and harmonic signals phase and percentage – Gain:10

Circuit with Noise at the input voltage – Gain: 100

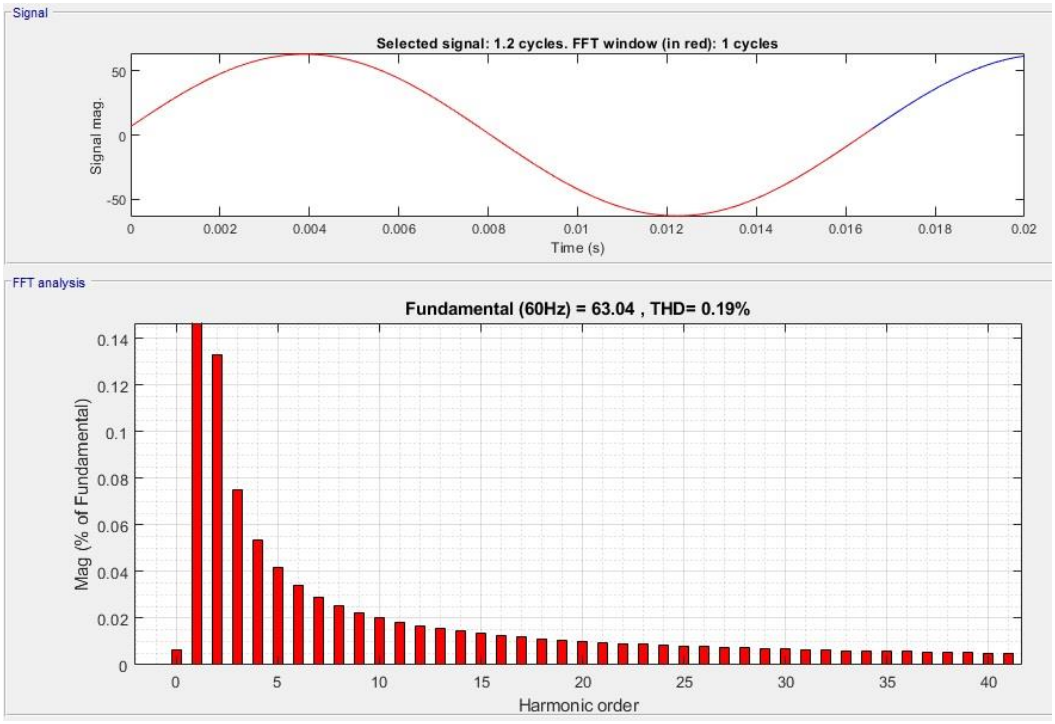


Figure 52: FFT Response – White noise with Gain: 100

Figure 51 represents the FFT analysis of the output voltage of the circuit including the noise with Gain 100

The Total Harmonic Distortion is 19%.

```
Sampling time     = 5e-05 s
Samples per cycle = 333
DC component      = 0.00415
Fundamental       = 63.04 peak (44.58 rms)
THD               = 0.19%

    0 Hz  (DC):          0.01%    270.0°
   60 Hz  (Fnd):       100.00%      5.8°
  120 Hz  (h2):          0.13%      3.7°
  180 Hz  (h3):          0.07%      3.3°
  240 Hz  (h4):          0.05%      3.4°
  300 Hz  (h5):          0.04%      3.6°
  360 Hz  (h6):          0.03%      4.0°
  420 Hz  (h7):          0.03%      4.4°
  480 Hz  (h8):          0.03%      4.8°
  540 Hz  (h9):          0.02%      5.3°
  600 Hz (h10):          0.02%      5.8°
  660 Hz (h11):          0.02%      6.3°
  720 Hz (h12):          0.02%      6.8°
  780 Hz (h13):          0.02%      7.3°
  840 Hz (h14):          0.01%      7.8°
  900 Hz (h15):          0.01%      8.3°
  960 Hz (h16):          0.01%      8.8°
 1020 Hz (h17):          0.01%      9.3°
 1080 Hz (h18):          0.01%      9.9°
 1140 Hz (h19):          0.01%     10.4°
 1200 Hz (h20):          0.01%     10.9°
 1260 Hz (h21):          0.01%     11.5°
 1320 Hz (h22):          0.01%     12.0°
 1380 Hz (h23):          0.01%     12.5°
 1440 Hz (h24):          0.01%     13.1°
 1500 Hz (h25):          0.01%     13.6°
 1560 Hz (h26):          0.01%     14.1°
 1620 Hz (h27):          0.01%     14.7°
 1680 Hz (h28):          0.01%     15.2°
 1740 Hz (h29):          0.01%     15.7°
 1800 Hz (h30):          0.01%     16.3°
 1860 Hz (h31):          0.01%     16.8°
 1920 Hz (h32):          0.01%     17.4°
 1980 Hz (h33):          0.01%     17.9°
 2040 Hz (h34):          0.01%     18.4°
 2100 Hz (h35):          0.01%     19.0°
 2160 Hz (h36):          0.01%     19.5°
 2220 Hz (h37):          0.01%     20.1°
 2280 Hz (h38):          0.01%     20.6°
 2340 Hz (h39):          0.01%     21.1°
 2400 Hz (h40):          0.01%     21.7°
 2460 Hz (h41):          0.00%     22.2°
```

Figure 53: Fundamental component and harmonic signals phase and percentage – Gain:100

Circuit with Noise at the input voltage – Gain: 500

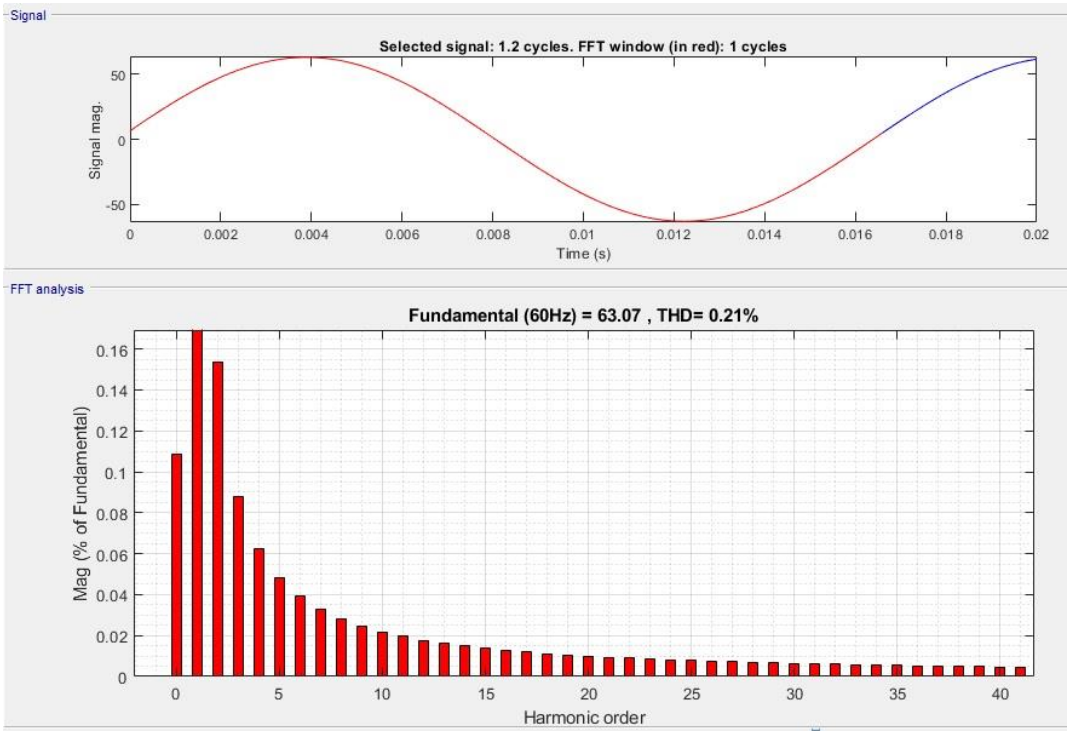


Figure 54: FFT Response – White noise with Gain: 500

Figure 53 represents the FFT analysis of the output voltage of the circuit including the noise with Gain 500

The Total Harmonic Distortion is 21%.

```
Sampling time      = 5e-05 s
Samples per cycle  = 333
DC component       = 0.005634
Fundamental        = 63.04 peak (44.58 rms)
THD                = 0.19%

     0 Hz  (DC):          0.01%    270.0°
    60 Hz  (Fnd):       100.00%      5.8°
   120 Hz  (h2):          0.13%      3.7°
   180 Hz  (h3):          0.07%      3.4°
   240 Hz  (h4):          0.05%      3.5°
   300 Hz  (h5):          0.04%      3.8°
   360 Hz  (h6):          0.03%      4.1°
   420 Hz  (h7):          0.03%      4.6°
   480 Hz  (h8):          0.03%      5.0°
   540 Hz  (h9):          0.02%      5.5°
   600 Hz (h10):          0.02%      5.9°
   660 Hz (h11):          0.02%      6.4°
   720 Hz (h12):          0.02%      6.9°
   780 Hz (h13):          0.02%      7.4°
   840 Hz (h14):          0.01%      8.0°
   900 Hz (h15):          0.01%      8.5°
   960 Hz (h16):          0.01%      9.0°
  1020 Hz (h17):          0.01%      9.5°
```

```
  1080 Hz (h18):          0.01%     10.0°
  1140 Hz (h19):          0.01%     10.6°
  1200 Hz (h20):          0.01%     11.1°
  1260 Hz (h21):          0.01%     11.6°
  1320 Hz (h22):          0.01%     12.1°
  1380 Hz (h23):          0.01%     12.7°
  1440 Hz (h24):          0.01%     13.2°
  1500 Hz (h25):          0.01%     13.7°
  1560 Hz (h26):          0.01%     14.3°
  1620 Hz (h27):          0.01%     14.8°
  1680 Hz (h28):          0.01%     15.3°
  1740 Hz (h29):          0.01%     15.9°
  1800 Hz (h30):          0.01%     16.4°
  1860 Hz (h31):          0.01%     16.9°
  1920 Hz (h32):          0.01%     17.5°
  1980 Hz (h33):          0.01%     18.0°
  2040 Hz (h34):          0.01%     18.5°
  2100 Hz (h35):          0.01%     19.1°
  2160 Hz (h36):          0.01%     19.6°
  2220 Hz (h37):          0.01%     20.1°
  2280 Hz (h38):          0.01%     20.7°
  2340 Hz (h39):          0.01%     21.2°
  2400 Hz (h40):          0.01%     21.8°
  2460 Hz (h41):          0.00%     22.3°
```

Figure 55: Fundamental component and harmonic signals phase and percentage – Gain:500

Circuit with Noise at the input voltage – Gain: 10,000

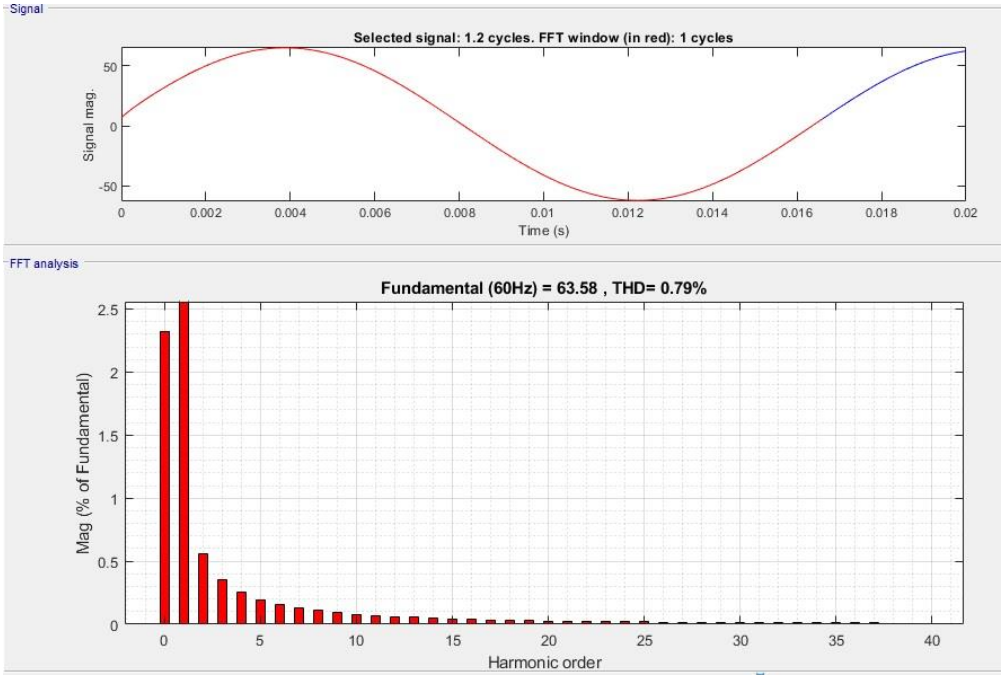


Figure 56: FFT Response – White noise with Gain: 10,000

Figure 55 represents the FFT analysis of the output voltage of the circuit including the noise with Gain 10,000

The Total Harmonic Distortion is 79%.

```
Sampling time     = 5e-05 s
Samples per cycle = 333
DC component      = 1.478
Fundamental       = 63.58 peak (44.96 rms)
THD               = 0.79%

     0 Hz   (DC):          2.33%     90.0°
    60 Hz   (Fnd):       100.00%      5.8°
   120 Hz   (h2):          0.56%     -5.2°
   180 Hz   (h3):          0.35%    -12.6°
   240 Hz   (h4):          0.25%    -18.8°
   300 Hz   (h5):          0.20%    -24.2°
   360 Hz   (h6):          0.16%    -29.2°
   420 Hz   (h7):          0.13%    -33.8°
   480 Hz   (h8):          0.11%    -38.0°
   540 Hz   (h9):          0.09%    -41.8°
   600 Hz  (h10):          0.08%    -45.3°
   660 Hz  (h11):          0.07%    -48.5°
   720 Hz  (h12):          0.06%    -51.4°
   780 Hz  (h13):          0.05%    -54.1°
   840 Hz  (h14):          0.05%    -56.6°
   900 Hz  (h15):          0.04%    -58.9°
   960 Hz  (h16):          0.04%    -61.1°
  1020 Hz  (h17):          0.03%    -63.1°
  1080 Hz  (h18):          0.03%    -64.9°
  1140 Hz  (h19):          0.03%    -66.6°
  1200 Hz  (h20):          0.03%    -68.3°
  1260 Hz  (h21):          0.02%    -69.8°
  1320 Hz  (h22):          0.02%    -71.2°
  1380 Hz  (h23):          0.02%    -72.5°
  1440 Hz  (h24):          0.02%    -73.8°
  1500 Hz  (h25):          0.02%    -75.0°
  1560 Hz  (h26):          0.02%    -76.1°
  1620 Hz  (h27):          0.02%    -77.2°
  1680 Hz  (h28):          0.01%    -78.2°
  1740 Hz  (h29):          0.01%    -79.2°
  1800 Hz  (h30):          0.01%    -80.1°
  1860 Hz  (h31):          0.01%    -81.0°
  1920 Hz  (h32):          0.01%    -81.8°
  1980 Hz  (h33):          0.01%    -82.6°
  2040 Hz  (h34):          0.01%    -83.4°
  2100 Hz  (h35):          0.01%    -84.1°
  2160 Hz  (h36):          0.01%    -84.8°
  2220 Hz  (h37):          0.01%    -85.5°
  2280 Hz  (h38):          0.01%    -86.1°
  2340 Hz  (h39):          0.01%    -86.7°
  2400 Hz  (h40):          0.01%    -87.3°
  2460 Hz  (h41):          0.01%    -87.9°
```

Figure 57: Fundamental component and harmonic signals phase and percentage – Gain:10,000

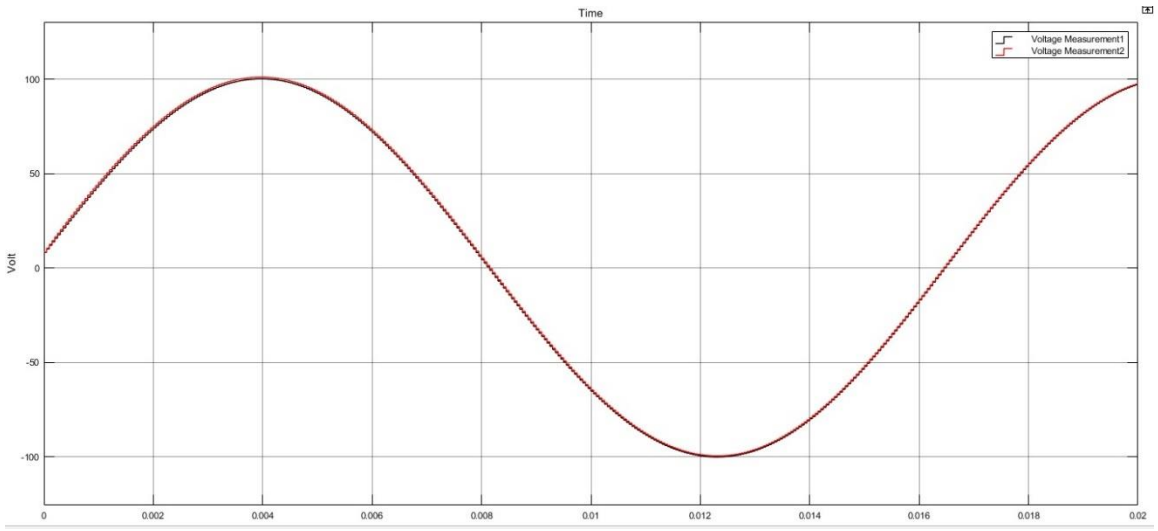


Figure 58: Output voltages – Gain: 2,000

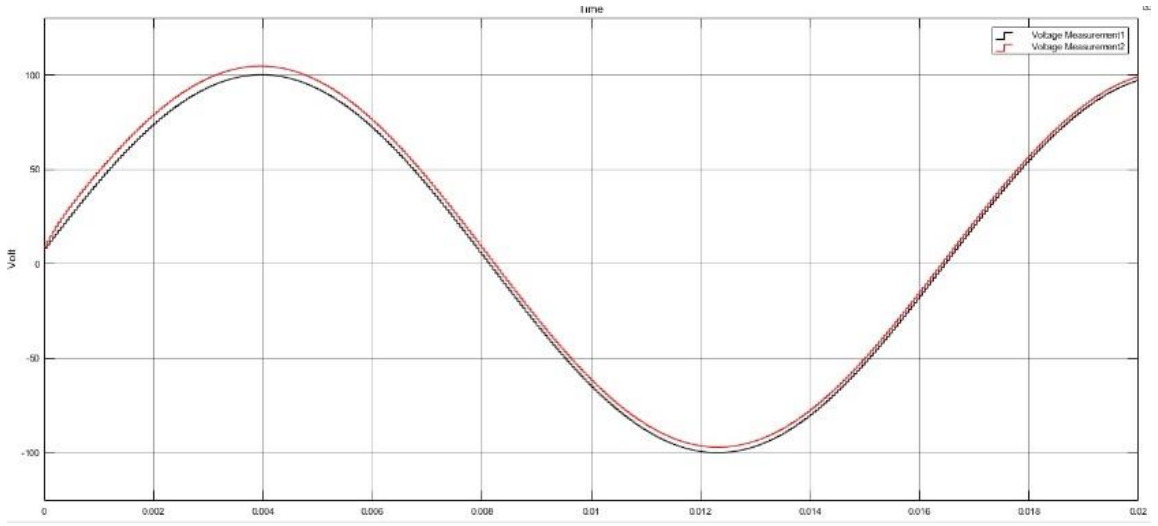


Figure 59: Output voltages – Gain: 10,000

The signals of the main circuit and the circuit with noise at the input voltage are at the same phase until gain 2000. Above that gain they start showing different phase as it can be seen in the figures 57 and 58.

3.6 Existence of Noise at the frequency

At this section the frequency noise was modelled at the input and again compared with the circuit operating at the steady state conditions.

At this part outputs of two identical CVT models are compared to realize the effect of frequency noise at the input. The CVT equivalent circuit considered as the subsystem for the simplicity of the diagram and are represented by main circuit and circuit with noise at the figure 59.

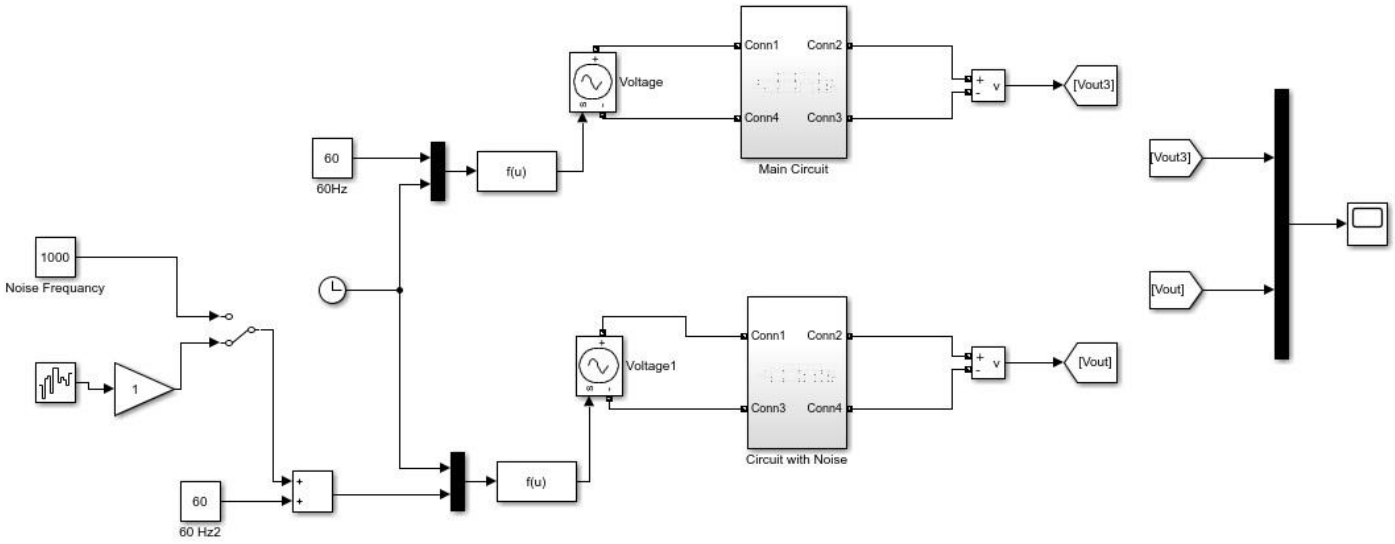


Figure 60: Simulation of input voltage (with and without Frequency noises)

In the main circuit, the frequency (60Hz) was modelled by using a clock and a constant block fed to a function block. Then a variable voltage controller was used to supply the main circuit.

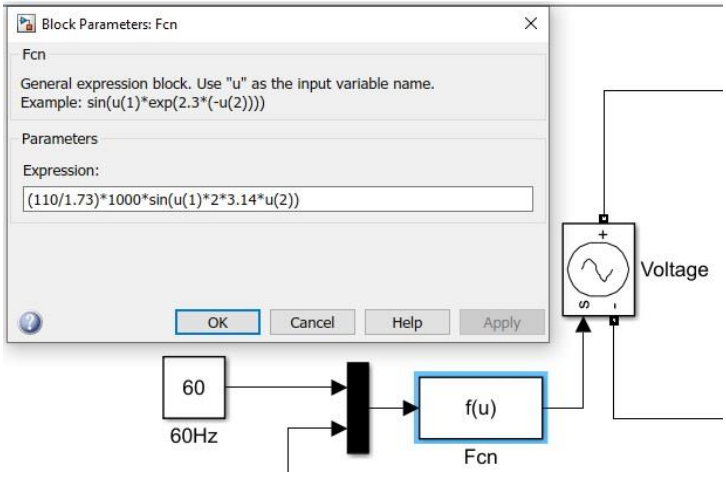


Figure 61: Modelling the Voltage sources – without Noises

For the creating of noise two possibilities are considered that could be selected through the switch. Based on the test requirement a constant noise or a random noise (white noise) can be added to the main frequency of the circuit (60Hz)

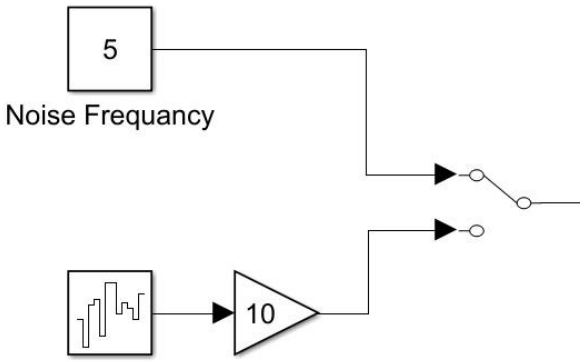


Figure 62: Modelling the Voltage sources – with Noises

3.6.1 Adding a constant frequency value to the supply voltage

a. Constant value: 0

We start the simulation by adding zero constant value and the two output voltages will become identical.

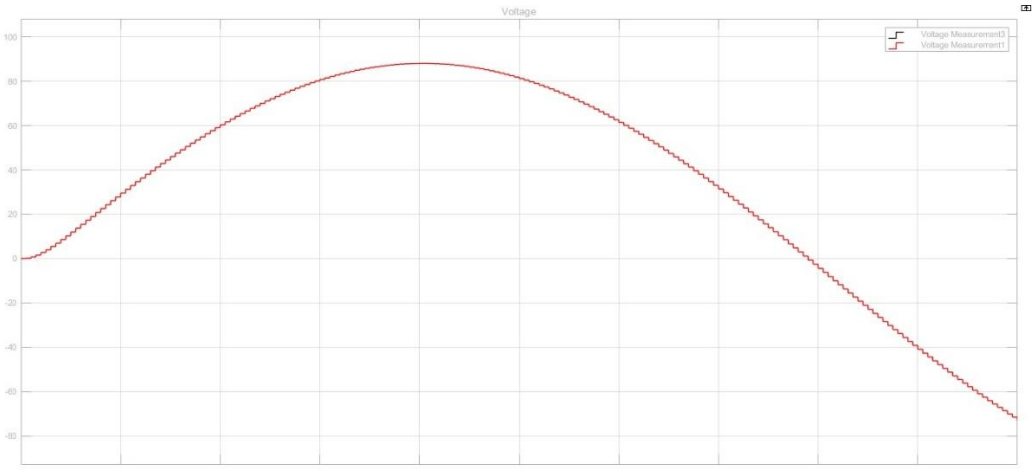


Figure 63: Output voltages of the main (black) and the noise circuits (red) – Additional Frequency: 0 Hz

AS it is expected they have same magnitude and phase angle.

b. Constant value: 5 Hz

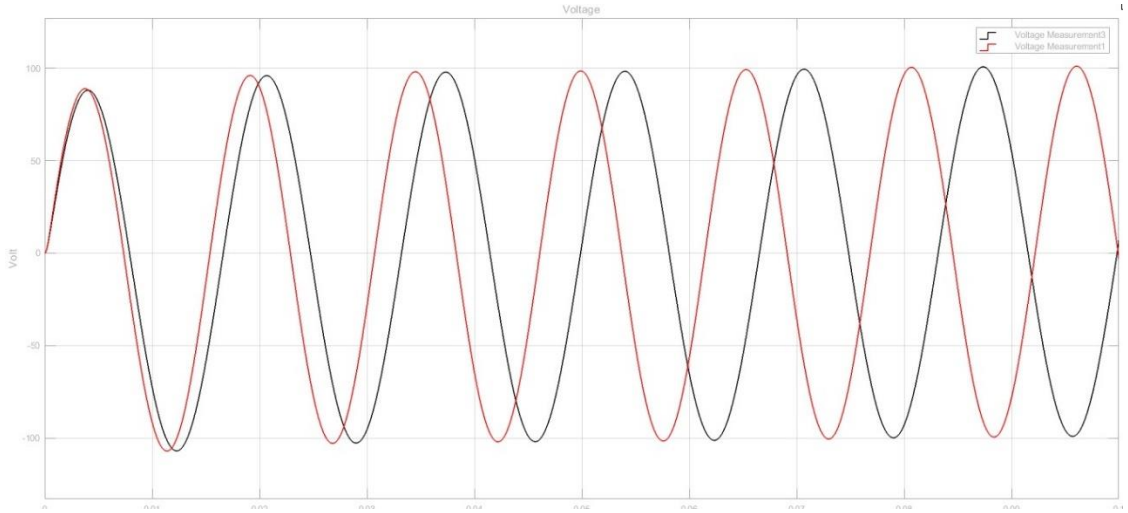


Figure 64: Output voltages of the main (black) and the noise circuits (red) - Additional Frequency: 5 Hz

C. Constant value: 10 Hz

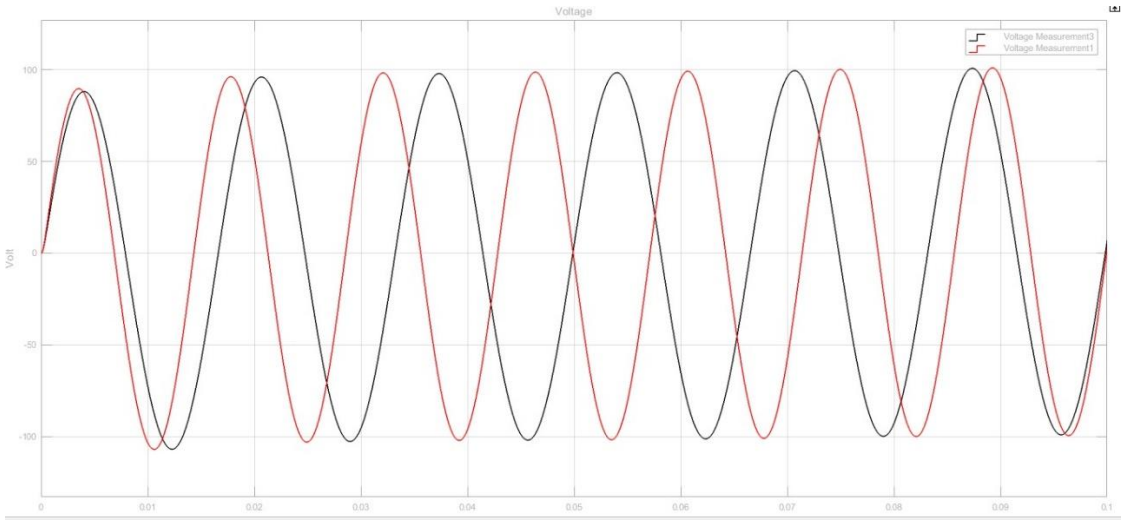


Figure 65: Output voltages of the main (black) and the noise circuits (red) - Additional Frequency: 10 Hz

d. Constant value: 100 Hz

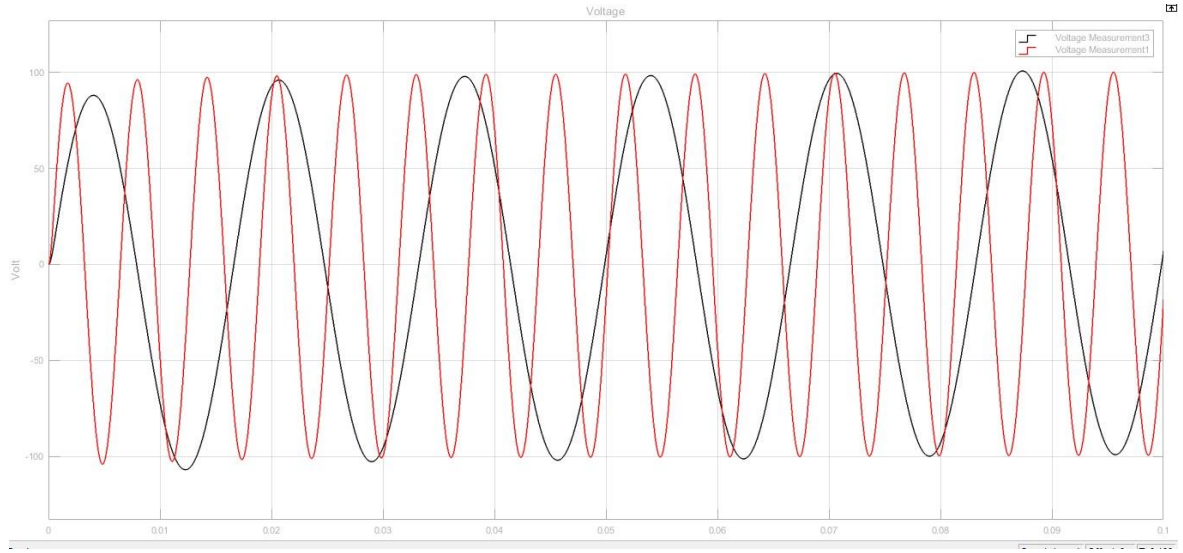


Figure 66: Output voltages of the main (black) and the noise circuits (red) - Additional Frequency: 100 Hz

e. Constant value: 1,000 Hz

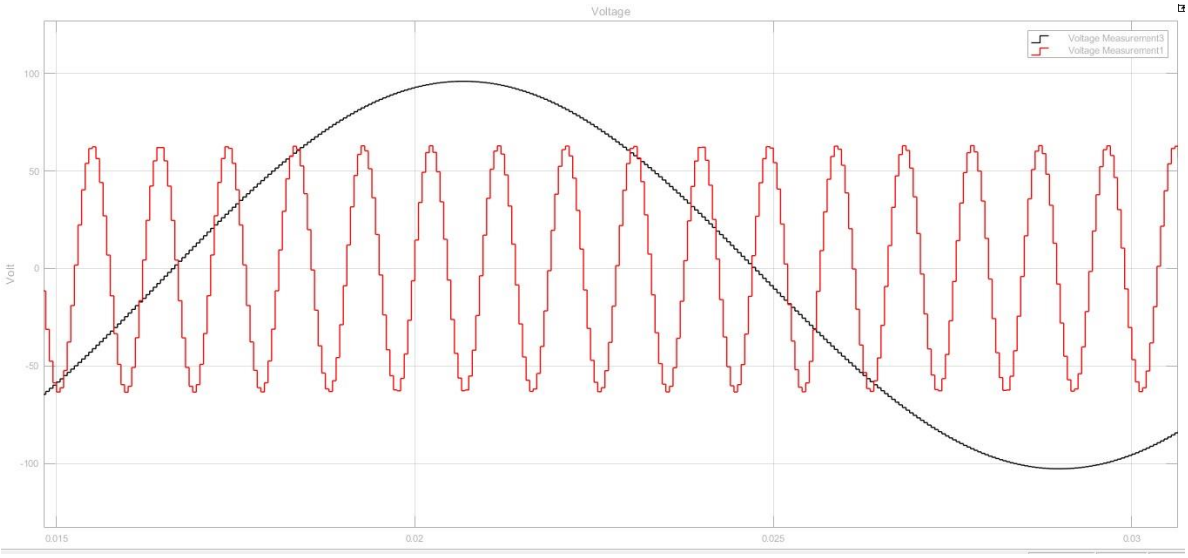


Figure 67: Output voltages of the main (black) and the noise circuits (red) - Additional Frequency: 1000 Hz

By increasing the frequency through the additional frequency block, it can be observed that the magnitude decreases and the distortion becomes more aggravated.

3.6.2 Adding a Random frequency Noise to the supply voltage

At this section a Band-limited white noise and a gain were used to create a noise at the supply voltage. The behaviour of the CVT depending on the value of the gain is shown in the following graphs.

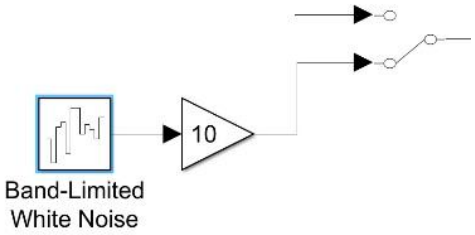


Figure 68: Random Noise (white noise)

a. Gain: 10

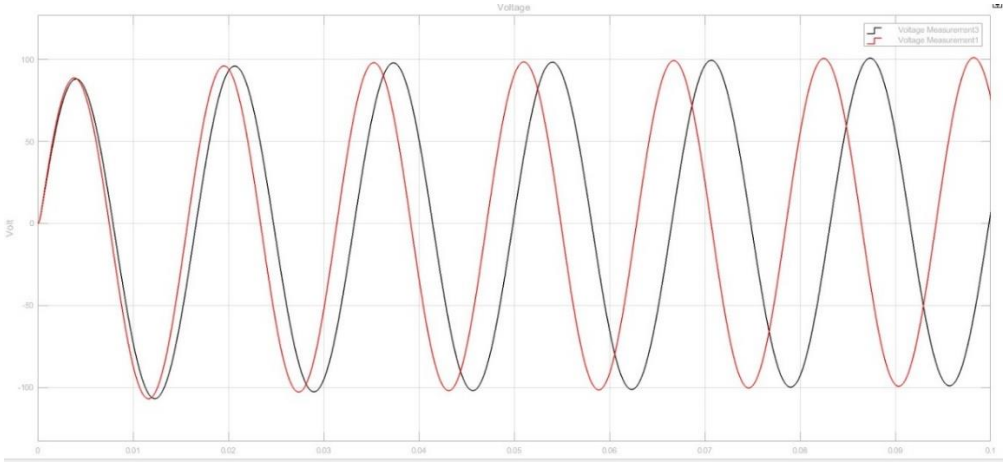


Figure 69: Output voltages of the main (black) and the noise circuits (red) – Random noise Gain: 10

b. Gain: 100

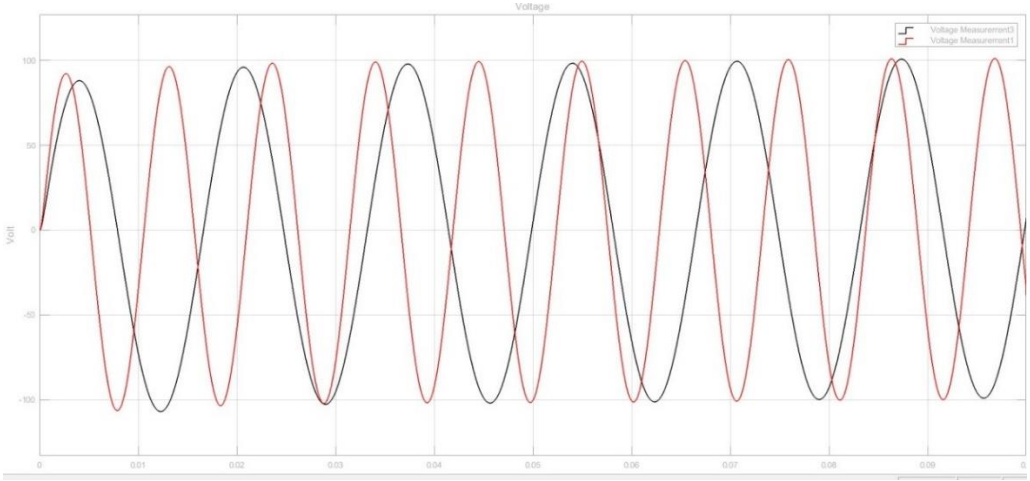


Figure 70: Output voltages of the main (black) and the noise circuits (red) – Random noise Gain: 100

c. Gain: 1,000

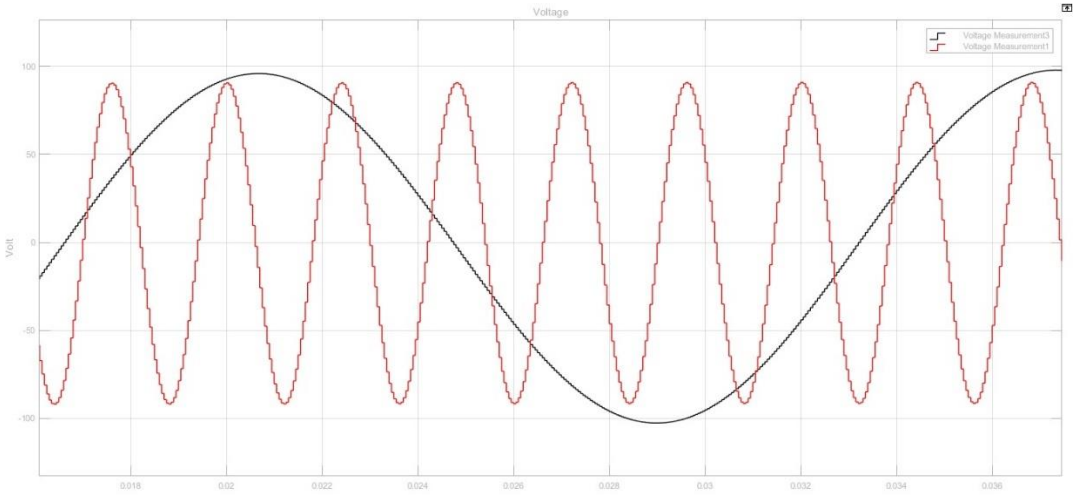


Figure 71: Output voltages of the main (black) and the noise circuits (red) – Random noise Gain: 1000

d. Gain: 10,000

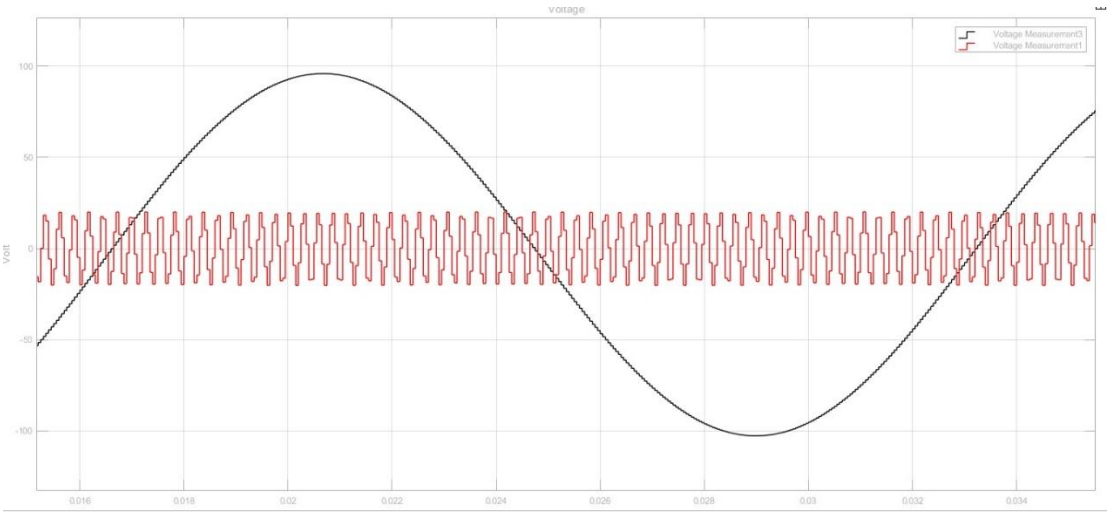


Figure 72: Output voltages of the main (black) and the noise circuits (red) – Random noise Gain: 10,000

By increase of the frequency the impedance will be changed and affects the output of the circuit with noise. $X_c = \frac{1}{2\pi f\, C}$ and $X_L = 2\pi f\, L$

It is noticeable that the core losses of the EMU are directly proportional to the frequency and by increase of the frequency their value increases.

3.7 Existence of Thermal Noise

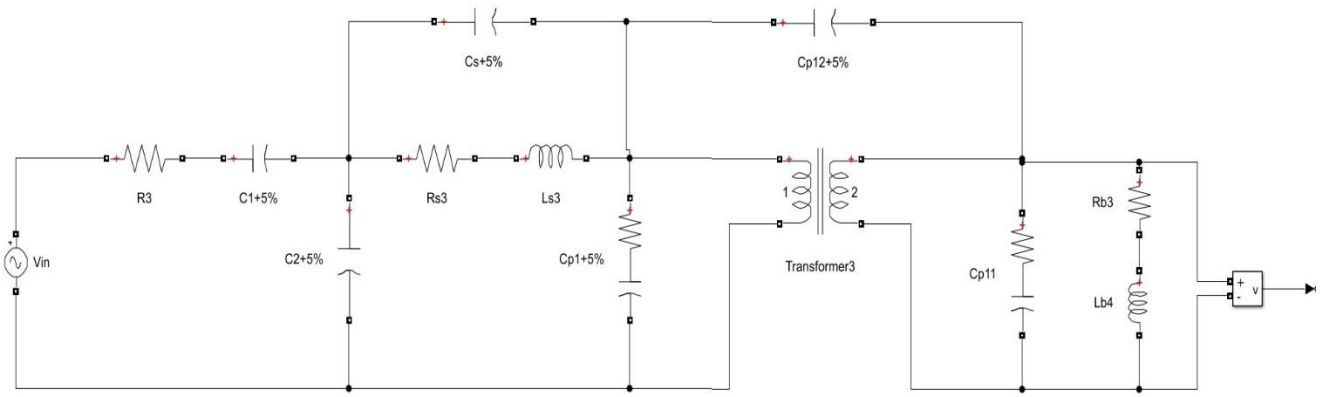


Figure 73: CVT Equivalent Circuit – including effect of Thermal noise

As it is well known, the influence of the thermal noise can be considered as a 5% error on the dielectric of the capacitors. Therefore, for the simplicity of the comparison the value was added to the coupling and the stray capacitances. [13]

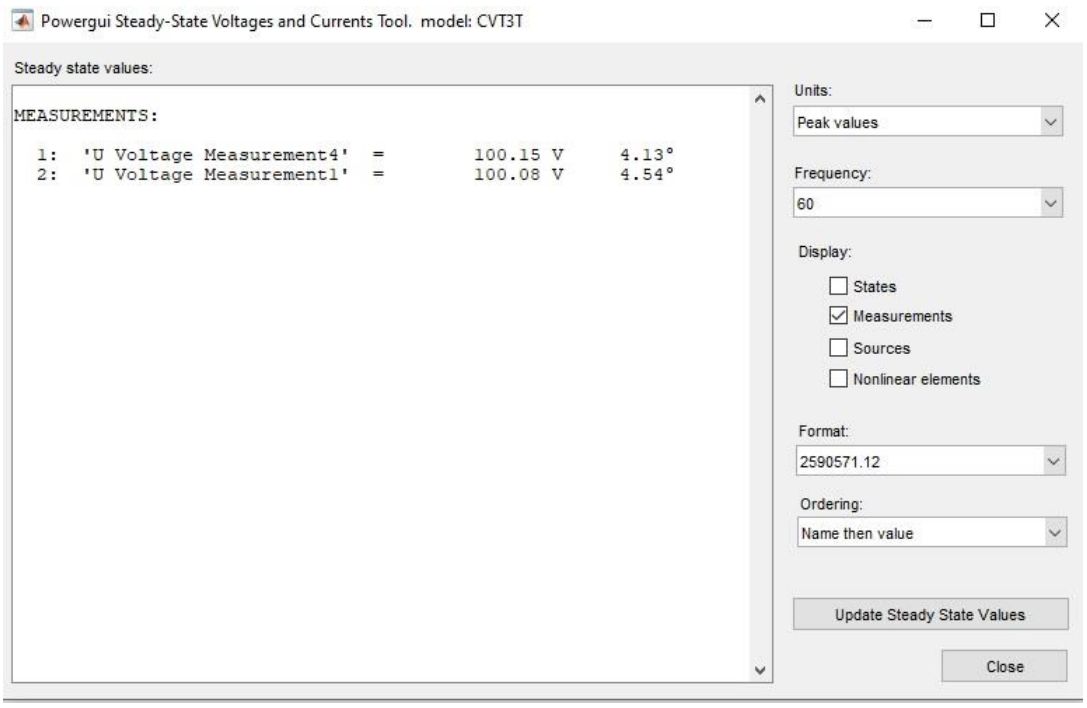


Figure 74: Existence of Thermal Noise – Steady state voltages and currents Tool

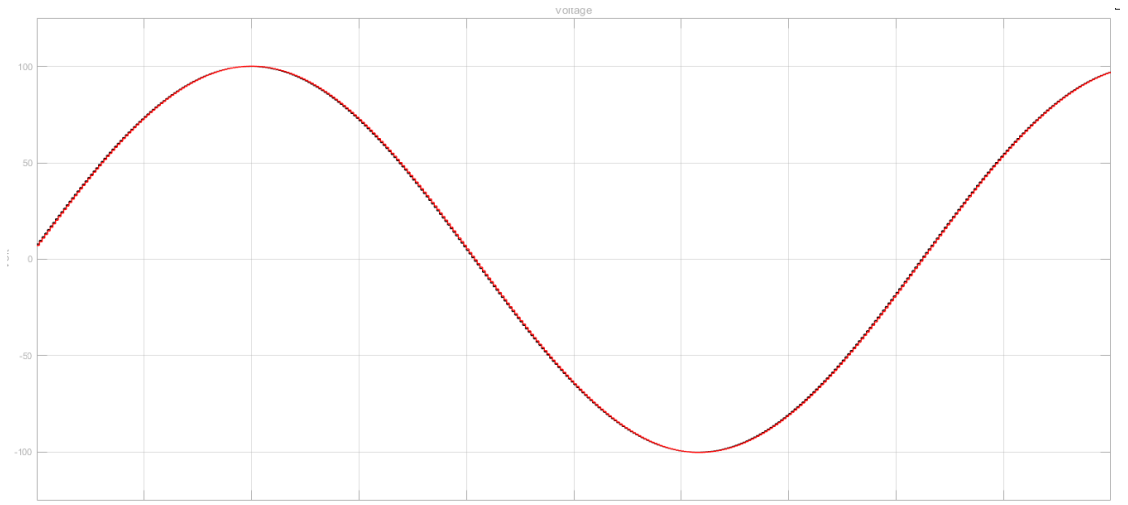


Figure 75: Existence of Thermal Noise – Rated frequency

As it can be seen the increase of the temperature at the rated frequency results a small variation of the phase and amplitude of the output voltages. In fact, behaviour of capacitors over temperature differs with different dielectrics. On an average, Polyester capacitors show an increase in value of up to 2.5 - 3% from room temperature to 85 degrees C, while PP capacitors show decrease of similar amount. Based on the tests done in [23] at the rated and low frequency, temperature effect is almost negligible.

Conclusions

In this dissertation, characteristics and the main parameters affecting the behaviour and accuracy of a Capacitive Voltage Transformer (CVT) were described.

A preliminary discussion was carried out in the first chapter concerning the structure of a CVT and its transient response. The importance of an accurate design of the components for obtaining an output signal similar to the input waveform were discussed. In continue, the weakness of CVT to measure and reflect the harmonics was explained and two solutions were proposed.

Afterwards, in the second chapter the parameters influencing the accuracy of a CVT were considered. Parameters such as is transformer design, external phenomena and the operating conditions have a major influence on the accuracy of the transformer and each one was described.

Eventually, at the third chapter a model of the CVT including stray capacitances was simulated in MATLAB Simulink. For a better understanding of the transformer behaviour three various disturbances were considered and by comparison the output signals of main circuit and the one with a noise the behaviour of CVT was evaluated.

In the first step a voltage noise was added to the supply voltage and the output voltages at different gains were compared. It was observed that due to the presence of non-linear components in a CVT the Harmonic Distortion at the output voltage is increasing as the distortion increases.

Then concerning a frequency noise different waveforms obtained. At the higher frequencies the impedances change and affect the output signal. It is noticeable that due to the presence of electromagnetic components such as intermediate transformer and the compensating reactor, at the higher frequency level the core losses are increased. The eddy current is directly proportional to the square of the frequency and the hysteresis loss is proportional to the frequency which means at high frequencies the amount of losses in the form of heat will rise and the proper design and precautions must be considered.

At the last section, the effect of ambient temperature was simulated. The effect can be considered separately for the capacitive components and the electromagnetic components. Concerning the capacitors, the dialectic specifications are important but in general the influence of the temperature on them at the rated operating condition can be neglected. The electromagnetic unit is located in a box contains mineral oil for protection of the components from the environmental deterioration. The specification of the oil plays a vital role for different operating conditions.

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