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Radiation-sensitive OXide semiconductor Field Effect Transistor (ROXFET): a novel thin-film device for real-time and remote ionizing radiation detection

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Abstract

Nowadays, ionizing radiation detectors find application in a wide range of contexts, spanning from industry to healthcare and security. In this background, the next generation of ionizing radiation sensors require devices that are accurate, light-weight, relatively inexpensive and capable to be read-out in real-time and remotely.

In recent years, research groups at the University of Bologna and the NOVA University of Lisbon (Portugal) have developed Radiation-sensitive OXide-semiconductor Field-Effect Transistors (ROXFET) to be employed as fast, real-time x-ray dosimetry detection systems. The ROXFET operation relies on the principle that, upon exposure to radiation, excitons are generated in the dielectric and separated into hole and electron charge carriers. While electrons are able to diffuse out of the dielectric layer, hole charges get trapped and contribute to the field-effect in the semiconductor channel. Macroscopically, such contribution is observable as a shift in transistor threshold voltage toward negative values, which turns out to be proportional to the absorbed radiation dose.

In laboratory tests, ROXFET devices proved to be sensitive in a wide energy range and capable of providing reliable information about their radiation exposure history. Furthermore, the design of ROXFET can be integrated on a flexible substrate and read in real-time as a passive radio-frequency tag.

Aim of this thesis work was to contribute to the development of the ROXFET technology. To this end, I carried out multiple characterization tests on recently fabricated samples, revealing how they outperformed previously observed radiation sensitivities. Later on, I worked in a clean-room facility to fabricate new ROXFET experimental samples by leveraging the knowledge acquired from previous observations.

Contents

Chapter 1

Introduction

Nowadays, distributed X-ray radiation dosimetry is crucial in diverse areas with significant environmental and human impacts. Nuclear waste management, radiotherapy, or radioprotection devices are only few of the applications that require fast, reliable, light-weight, inexpensive and low-power detection and readout of ionizing radiation doses.

In recent years, research groups at the University of Bologna and the NOVA University of Lisbon (Portugal) have developed Radiation-sensitive OXide-semiconductor Field-Effect Transistors (ROXFET), which represent ideal candidates to be employed as fast, real-time x-ray dosimetry detection systems. ROXFET devices leverage the advantages offered by both amorphous oxide semiconductors (AOSs) and high dielectric constant (*high-k*) insulating oxides. Indeed, AOSs materials such as a-IGZO have been widely investigated for a combination of good electrical performances and the possibility of low-cost large-area fabrication. On the other hand, *high-k* dielectrics such as tantalum oxide (Ta_2O_3) offer both improved TFTs performances and higher radiation cross-section (thanks to the high atomic number of Ta).

Aim of this thesis work was to contribute to the development of the ROXFET technology, either by assessing overall devices performances, understanding the underlying physical processes and improving ROXFET architecture and fabrication methods. The first part of this project took place at the Physics and Astronomy department at the University of Bologna, where I characterized previously fabricated ROXFET devices which differed by fabrication techniques and constructive features. To identify the more promising configurations, I tested transistors' properties via electrical characterizations and radiation sensitivity experiments. To better understand the charge transport mechanism inside ROXFETs, I operated various trials among which Kelvin Probe Force Microscopy (KPFM) analyses and capacitance-voltage (C-V) measurements. The second phase of my work

was held at the CEMOP-CENIMAT laboratories at the NOVA University of Lisbon. There, by leveraging the knowledge acquired from previous measurements and trials, I fabricated new experimental ROXFET devices in a clean-room facility. This part also included the evaluation of possible enhancements of devices architecture, materials choice and fabrication processes.

In *Chapter 1* we will go through a brief introduction on thin film transistors (TFTs), focusing then on amorphous oxide semiconductors (AOSs). Then, we will discuss the working principles and figures-of merit of Radiation-sensitive OXide-semiconductor Field-Effect Transistors.

In *Chapter 2* we will discuss all the techniques involved in the fabrication process of ROXFET devices. In particular, we will focus on all the techniques employed at the CEMOP laboratories, analysing their principles of operation.

In *Chapter 3* we will summarize the characterization techniques employed on the experimental samples. In addition to the standard electrical and radiation sensitivity performances tests, we will see how KPFM and C-V measurements allowed to extract meaningful informations on the ROXFETs.

In *Chapter 4* are presented all the experimental results obtained during this thesis work. We will start from the fabrication process and subsequent characterization of oxide semiconductor thin film transistors. Then, we will review the results concerning the extraction of conduction band tail density of states (DOS) from C-V measurements. Finally, we will go through the radiation detection characterization performed on all available samples.

In *Chapter 5* we will review the main achievements of this thesis work and take a brief insight into future perspectives.

1.1 Thin Film Transistors

1.1.1 Working principle and figures-of-merit

Thin film transistors (TFTs) are three terminal devices in which a semiconductor is placed between two electrodes (called *source* and *drain*) and a dielectric layer is inserted between the semiconductor and a third transversal electrode (known as *gate*).

TFTs' working principle relies on the modulation of the current flowing, through source and drain, across the semiconductor. The current modulation is achieved by the capacitive injection of carriers close to the dielectric/semiconductor interface. This phenomena, known as *field effect*, is turned possible due to the parallel plate capacitor structure formed by the gate electrode, dielectric and semiconductor.

Figure 1.1 shows the most common TFT structures. Such configurations feature are denominated *coplanar*, if the source-drain and the gate electrodes are on the same side of the semiconductor (respect to the dielectric), or *staggered*, if the source-drain and gate on the opposite sides. Moreover, two different arrangements are possible: depending on whether the gate electrode is placed on top or at the bottom of the structure, TFTs can be defined respectively as *top-gate* or *bottom-gate* [1].

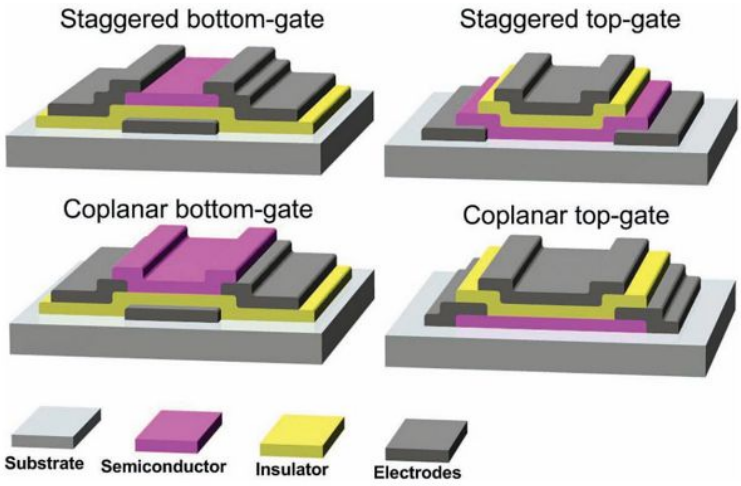

Figure 1.1: Scheme of the most common TFT structures. (Source: [1])

All these structures present both advantages and disadvantages, usually strongly related to the materials used to fabricate the TFTs. For example, the staggered bottom-gate configuration is ideal when applied to

TFTs for displays, as the gate shields the semiconductor from the backlight while avoids shadowing the light emitted by the TFT. On the other hand, in bottom-gate structures the semiconductor surface is exposed to air, factor that can be exploited in certain fabrication processes but may also lead to instability effects, usually requiring the application of a passivation layer. Also, in the case of staggered bottom-gate devices, an insulating film is often deposited on top of the semiconductor layer. Acting as an etch-stopper, this can allow for more accurate etching of the source-drain electrode without damaging the semiconductor surface [1].

TFTs are quite similar to other field-effect devices, such as MOSFETs, in terms of operation and composing layers (Figure 1.2). Nevertheless, some important differences exist:

- **Substrate**. While the TFTs use an insulating substrate (typically glass), in MOSFETs the silicon wafer plays the dual role of semiconductor substrate. Given that the electrons flow in a single crystalline semiconductor, rather than in an amorphous one, MOSFETs ideally provide higher performances.
- **Fabrication temperature**. MOSFETs processing temperature usually exceeds $1000°C$, while TFTs are limited by the softening of the glass substrate around $600°C$.
- **Semiconductor junctions**. MOSFETs feature a p-n junction at the source and drain regions, which is absent in TFTs. This also leads to MOSFETs being operated in inversion mode, while TFTs work in accumulation mode.

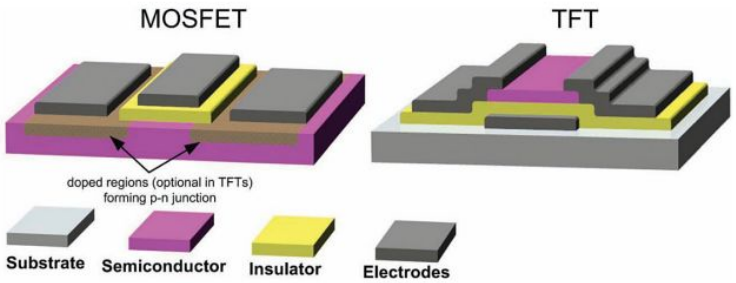

Figure 1.2: Comparison between MOSFET and TFT structure schemes. (Source: [1])

The ideal operation of an n-type TFT can be described by analysing the energy band diagram of the structure comprised by the gate electrode,

the dielectric and the semiconductor, upon the application of different biases to the gate electrode. As represented in Figure 1.3, three different conditions may occur [2]:

- **Equilibrium** ($V_G = 0\,V$). When no bias is applied, the Fermi levels are aligned and the energy bands are in equilibrium.
- **Depletion** ($V_G < 0\,V$). This condition induces an upward bending of the semiconductor energy bands, producing a depletion region at the semiconductor/dielectric interface. Regardless of the drain voltage (V_D) applied, this conditions prevents (almost any) current from flowing between source-drain electrodes (OFF state).
- **Accumulation** ($V_G > 0\,V$). In this case, the downward bending induced on the semiconductor energy bands determines the formation of an accumulation region at the semiconductor/dielectric interface. This enables a current to flow between source-drain electrodes (ON state) when a positive V_D is applied.

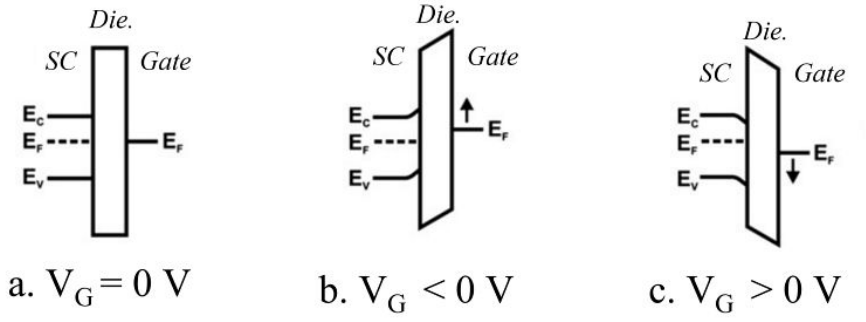

Figure 1.3: Energy band diagrams of an ideal gate electrode/dielectric/n-type semiconductor (SC) structure in different bias conditions: a) equilibrium ($V_G = 0\,V$), b) depletion ($V_G < 0\,V$), c) accumulation ($V_G > 0\,V$). (Adapted from: [2])

Ideally, $V_G = 0\,V$ should represent the threshold voltage V_{th} at which occurs the transition between the OFF/ON states. In real devices, such V_{th} deviates from $0\,V$, as it also function of the gate electrode-semiconductor work function difference, the background carrier concentration of the semiconductor, the charge density residing within the dielectric and the trap density at the interface and within the semiconductor [2].

For an n-type TFT, depending on whether V_{th} is positive or negative, the devices are designated as *enhancement* or *depletion* mode, respectively. Both types are useful for circuit fabrication, but enhancement mode is preferable in electronic switch applications because no V_G is required to achieve the OFF-state, turning easier the circuit design and minimizing power dissipation.

When the transistor is in the ON-state, depending on the value of V_D different operation regimes can be distinguished [2]:

- **Linear regime** $V_D < (V_G - V_{th})$. In this condition, also known as *pre-pinch-off regime*, the drain current I_D can be described as:

$$I_{\mathrm{D}} = C_{\mathrm{i}} \mu_{\mathrm{FE}} \frac{W}{L} \left[(V_{\mathrm{G}} - V_{\mathrm{T}}) V_{\mathrm{D}} - \frac{1}{2} V_{\mathrm{D}}^2 \right] \tag{1.1}$$

  where C_i is the gate capacitance per unit area, μ_{FE} is the field-effect mobility, W is the channel width, and L is the channel length. For very low V_D, the quadratic term can be neglected, yielding a linear relation between I_D and V_D. In this situation, the accumulated charges are considered to be uniformly distributed throughout the semiconductor channel.

- **Saturation regime** $V_D > (V_G - V_{th})$. Also known as *post-pinch-off regime*, it describes a condition in which the accumulation layer close to the drain region becomes depleted (*pinch-off*), leading to the saturation of I_D. In this regime, the drain current I_D can be described as:

$$I_{\mathrm{D}} = C_{\mathrm{i}} \mu_{\mathrm{sat}} \frac{W}{2L} (V_{\mathrm{G}} - V_{\mathrm{T}})^2 \tag{1.2}$$

  where μ_{sat} is the saturation mobility.

The aforementioned equations are based on some assumption. First, according to the *gradual channel approximation*, the gradient of the lateral field within the channel is much smaller than the gradient of the vertical field. This implies that the channel is seen as one-dimensional. Even if this approximation is not valid near the drain electrode, when the transistor is in saturation regime or for short-channel devices, it is still quite accurate as usually L is much larger than the dielectric thickness. Second, while it is assumed that μ_{FE} and μ_{sat} represent constant quantities, especially for TFTs this is not always the case, and their V_G dependence should be taken into account [2].

The electrical performances of TFTs are described by several parameters that are evaluable from the electrical characterization of the devices. Figure 1.4 shows the same I-V transfer characteristic in saturation regime, represented in square-root and logarithmic scales. From these plots can be extracted several parameters representing the figures-of-merit of the transistor [1]:

- I_{ON}/I_{OFF} **ratio**. This value defines the ratio between the maximum (ON state) and the minimum (OFF state) value of the drain current. A large value (usually above 10^6) is desirable to obtain a device to be employed as electronic switch.

- **Threshold voltage** V_{th}. This value corresponds to the gate voltage an accumulation layer forms inside the dielectric, opening a conductive path between source-drain electrodes across the channel. This value can be extracted by a linear extrapolation in the $I_D - V_G$ plot when in linear regime, or from the $\sqrt{I_D} - V_G$ plot when in saturation regime.

- V_{ON} **voltage**. This value represents the gate voltage at which occurs an onset in channel conductivity. Ideally $V_{ON} = V_{th}$, but it often results lower due to band-tails and defects.

- **Sub-threshold swing** S. The value of S represents the necessary ΔV_G to increase I_D by one decade. It is defined as the inverse of the maximum slope of the I-V transfer characteristic.

$$S = \left(\frac{\partial \log (I_D)}{\partial V_G} \bigg|_{\max} \right)^{-1} \tag{1.3}$$

  Typically, S values are around 0.1–0.3 V/dec, with small values resulting in higher switching speeds and lower power consumption. During this thesis work we will also refer to the **sub-threshold slope**, which represents the reciprocal value of the sub-threshold swing.

- **Mobility** μ. The value of μ is related to the efficiency of charge transport in a material and is directly related to to the maximum I_D and the switching speed of the device. The mobility is directly affected by the scattering mechanisms present in the material: lattice vibrations, several types of defects, scattering from dielectric charges and from interface states or surface roughness.
  Three main types of mobility can be calculated, depending on the operative regime:

Effective mobility μ_{eff}. It is obtained from the conductance ($g_d = \dfrac{I_D}{V_G}$) in linear regime (low V_D):

$$\mu_{eff} = \frac{g_d}{C_i \frac{W}{L} (V_G - V_T)} \tag{1.4}$$

Field Effect mobility μ_{FE}. It is obtained from the transconductance ($g_m = \frac{\partial I_{\text{out}}}{\partial V_{\text{in}}}$) in linear regime (low V_D):

$$\mu_{FE} = \frac{g_m}{C_i \frac{W}{L} V_D} \tag{1.5}$$

Saturation mobility μ_{sat}. It is obtained in saturation regime (high V_D):

$$\mu_{sat} = \frac{\left(\frac{d\sqrt{I_D}}{dV_G}\right)^2}{\frac{1}{2} C_i \frac{W}{L}} \tag{1.6}$$

Each methodology has its advantages and drawbacks. Even if μ_{eff} takes into account V_G, it requires the determination of V_{th} that is more sensitive to contact resistances. The latter last issue also verifies for μ_{FE} which, however, can be easily calculated by the derivative of transfer characteristics. Finally, μ_{sat} does not require V_{th} and is less sensitive to contact resistance. However, it describes a situation where the channel is pinched-off, thus its effective length is shorter than L.

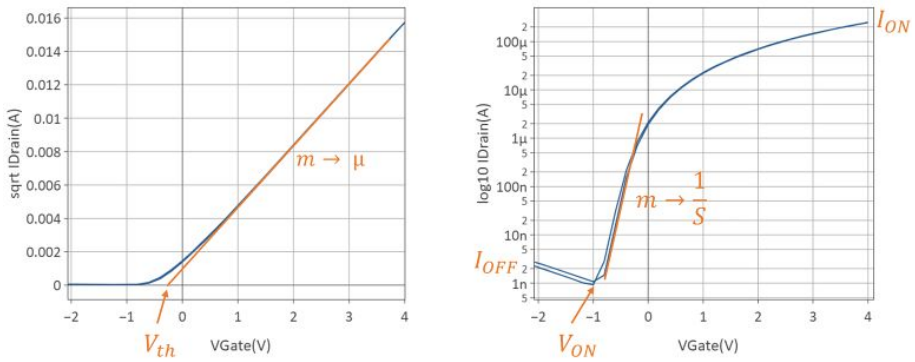

Figure 1.4: Example of a I-V transfer characteristic in saturation regime and representation of the evaluable parameters.

1.1.2 Oxide semiconductor Thin Film Transistors

Over the last two decades, amorphous oxide semiconductors (AOSs) have been employed in the fabrication of devices known as *giant microelectronics*, a broad family that includes solar cells and thin-film transistors for large-area, flexible flat-panel displays. In late 2004, Nomura et al. reported that an amorphous oxide semiconductor with the composition $a-InGaZnO_4$ (a-IGZO) can be applied in the fabrication of flexible, transparent thin film transistors with improved performances respect to conventional TFTs based on $a-Si:H$ and organic materials [3]. Since then, AOSs have been widely tested for flexible displays, non-volatile memories and other electronics applications.

The amorphous oxide semiconductor materials employed in TFTs offer numerous advantageous features, among which [3]:

- **Processing temperature**. Satisfactory operation characteristics can be achieved even with devices fabricated at room temperature. Also, depending on the material's chemical composition, an appropriate temperature condition can be chosen to tune the desired TFT characteristics.

- **High electron mobility**. By tuning the chemical composition, mobilities as high as $50\,cm^2/Vs$ can be achieved.

- **Low operation voltage and OFF current**. Oxides feature electronic structures specific to the ionic chemical bonds, and therefore they form much fewer defect states in the band gap than conventional covalent semiconductors such as silicon. As a result, it is typical to obtain S values of $0.1\,V/dec$, low operation voltages (below $5\,v$) and low OFF currents. Also, by operating in accumulation mode, AOS TFTs do not require any power consumption to maintain the OFF state.

- **Ease of fabrication**. The simple electrodes structures, the absence of p-n junctions, the wide range of possible dielectric materials and the possibility of fabricating at low temperature are only few of the factors that render AOS TFTs relatively easy to fabricate.

Figure 1.5 summarizes the structural condition IGZO films as a function of the chemical composition. At first, we can immediately see that pure Zn_O and In_2O_3 form crystalline films even when deposited at room temperature. This feature is detrimental for large-area fabrication, as the formation of polycrystalline structures leads to poor electrical transport properties due to high density of grain boundaries. On the other hand, the binary oxide

compounds, such as $Zn-In-O$ and $Zn-Ga-O$, form amorphous phases if the mixing ratio of the oxides exceeds a certain threshold value.

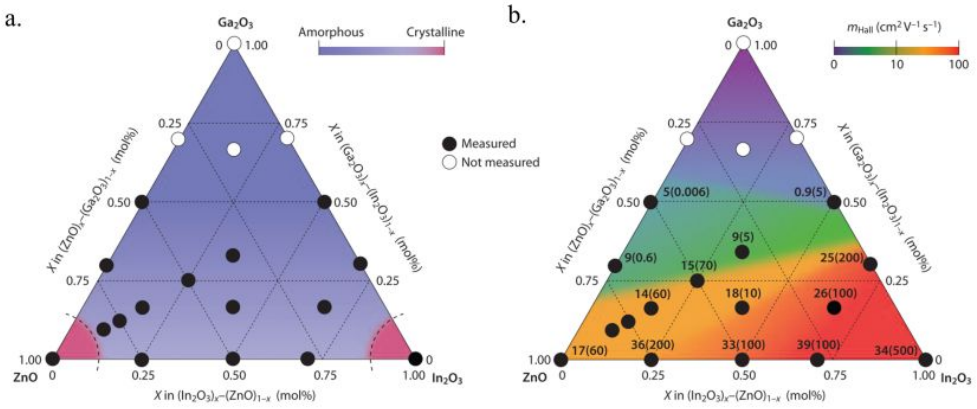

Figure 1.5: Diagram of the a) amorphous formation and b) electron transport properties of In_2O_3-Ga_2O_3-ZnO thin films (deposited at room temperature by pulsed laser deposition). The values in b) denote the electron Hall mobility (cm^2/Vs) with density ($10^{18}\,cm^{-3}$) in parenthesis. (Source: [3])

Originally, it was believed that the properties of amorphous semiconductors were considerably degraded compared with their corresponding crystalline phases. Indeed, this is the case for silicon, whose mobility drops from $1500\,cm^2/Vs$ in its crystalline phase to $2\,cm^2/Vs$ when in the amorphous phase. However, AOSs exhibit much larger electron mobilities, usually even grater than $10\,cm^2/Vs$ (Figure 1.5, b).

Despite the amorphous state, the origin of the high mobility in AOSs was attributed to the electronic orbital structure of the material. As shown in Figure 1.6, the direct overlapping between neighbouring metal s orbitals can occur. This results in the formation of a conducting path for free electrons which is not significantly affected even in a distorted amorphous structure. For example, the conduction band in IGZO is mainly formed by the overlapping of the In $5s$ orbitals, which exhibit isotropic properties. The spherical symmetry of the $5s$ orbitals (Figure 1.6) renders the IGZO material insensitive to structural deformation, and the semiconductor maintains high mobility in the amorphous state [4].

In contrast, as we said, conventional amorphous semiconductors such as $a-Si:H$ exhibit much deteriorated carrier transport properties compared with the corresponding crystalline materials. This is because the chemical bonds in the covalent semiconductors are made of sp^3 or p orbitals with strong spatial directivity. Therefore, the strained chemical bonds in

amorphous structures form rather deep and high-density localized states, causing carrier trapping [3].

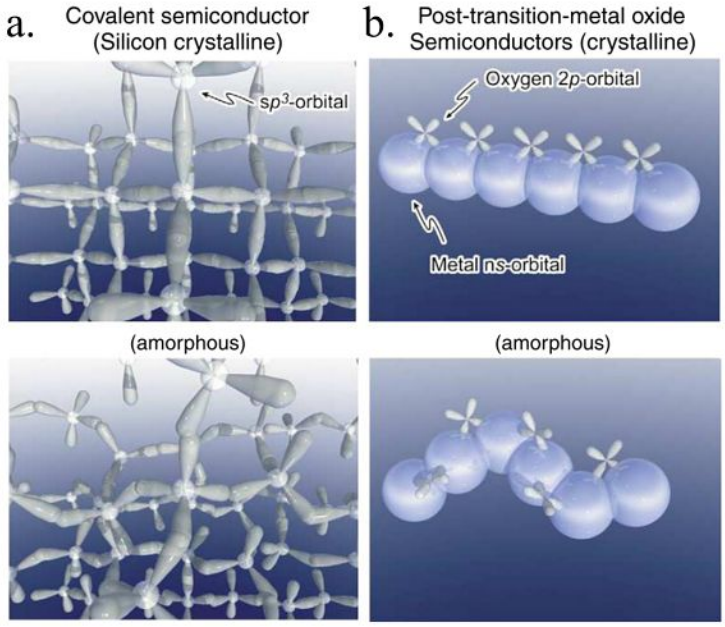

Figure 1.6: Pictorial representation of the orbital structure of the conduction-band minimum in $c-Si$ and in metal oxide semiconductors. (Source: [4])

Indium, gallium, zinc and Tin are the major constituents of good transparent conducting oxides, as their unoccupied s orbitals form the electron transport paths in AOSs. Therefore, these elements represent a fundamental requirement to obtain AOSs with large electron mobilities. To understand the role of the other ions, it is useful to compare systems such as a-IZO and a-IGZO. As seen in Figure 1.5, a-IZO has higher electron mobilities than a-IGZO, but is more difficult to control at the low electron concentrations required for TFTs to ensure a low off-current ($<< 10^{17}\, cm^{-3}$). In this sense the presence of gallium in the conductive IZO host is crucial: Ga-O bonds are much stronger than In-O and Zn-O bonds, meaning that the incorporation of Ga both acts as a network stabilizer and suppresses the generation of mobile electrons (by preventing the formation of oxygen deficiencies). On the other hand, the incorporation of a too high amount of gallium deteriorates the electron mobility, thus requiring a controlled tuning of the relative compositions [3].

1.2 ROXFET: Radiation sensitive OXide semiconductor Field Effect Transistors

Nowadays, ionizing radiation detectors find application in a wide range of contexts, spanning from radiotherapy to nuclear waste management, high-energy physics experiments, and space missions. In all these cases, a fast and accurate detection system is crucial to avoid health or technical safety risks.

The most common real-time radiation detectors are ionization chambers and calorimeters, which however are bulky and require complex electronics or high-voltage operation. Those devices are not suitable, for example, to achieve a spatially resolved irradiation map via a distributed network of detectors, or in medical scenarios where flexibility and high integration density represent fundamental requirements.

Recent studies are focusing on obtaining novel microelectronic dosimeters that feature high charge generation efficiency, the possibility of flexible and large-area fabrication, low-power operation and wireless integrability. To date, such dosimeters consist in diode or transistor structures based on the Complementary Metal-Oxide Semiconductor (CMOS) technology. The operation of these devices relies, upon exposure to ionizing radiation, on the introduction of defects or the trapping of generated charge carriers in the dielectric/semiconductor layers. This results in a measurable shift in device's electrical characteristics, proportional to the absorbed radiation dose [5].

The RADiation-sensitive Field-Effect Transistors (RADFET) represent an example of commercially available microelectronic dosimeters. These RADFET employ a thick silicon oxide layer as a dielectric and a crystalline silicon semiconductor channel, achieving sensitivity to doses ranging from a few hundreds of micro-Grays up to thousands of Grays, thus suitable for many dosimetry applications. RADFET sensitivities are expressed as threshold voltage shift per radiation dose (dV_{th}/dGy) and, depending on oxide thickness and photon energy, range between $0.05 - 0.30\,V/Gy$. Larger sensitivities are achieved when a positive bias is applied to the gate electrode, as the electric field improves the exciton dissociation [5].

The next generation of RADFET dosimeters aims at overcoming the current limitations: a change in materials is required as the sensitivity is currently limited by the low radiation cross-section of silicon oxide, and their integration into dense and flexible structures is incompatible with silicon CMOS technology. Amorphous Oxide Semiconductors (AOSs) such as indium-gallium-zinc oxide (IGZO) and FETs represent a mature technology to be used in RADFET applications. As we saw, they combine highly stable electronic performance, high electron mobilities, ease of fabrication and

compatibility with flexible structures. Moreover, AOSs feature excellent radiation hardness, and the compatibility with a wide range of dielectrics, thus allowing great tunability.

In the next sections, we will go through the details of the project on novel RADFET devices subject of this thesis work, discussing its working principles and potential advantages.

1.2.1 Presentation of the project

In recent years, a researchers team from the University of Bologna and the NOVA University of Lisbon have collaborated in the realization of Radiation-sensitive OXide semiconductor Field-Effect Transistors (ROXFET). In its latest version, this TFT technology employs IGZO as a amorphous oxide semiconductor and tantalum oxide (Ta_2O_5) inside the dielectric.

We already discussed the advantages offered by AOSs in terms of ease of fabrication and excellent electrical and mechanical properties. All these combine with the use of Ta_2O_5, which provides:

- **Increased ionizing radiation cross section**. As Figure 1.7 highlights, the interaction or X-rays with matter predominantly occurs via Photoelectric effect. The interaction probability τ is given by:

$$\tau \propto \frac{Z^n}{E^3} \tag{1.7}$$

  where Z is the atomic number of the material and n is a factor varying between 3 and 4, depending on the radiation energy (represented by E) [6]. Thus, the replacement of Si ($Z = 14$) with Ta ($Z = 73$) allows in principle to obtain much higher sensitivities thanks to an increased detection probability.

- **Increased dielectric constant**. Given the low-temperature deposition conditions, it can be expected that lower quality interfaces may introduce defects and trap states that deteriorate the electrical performances. As a solution, materials with a high dielectric constant (*high-k*) compensate these drawbacks by providing higher gate-semiconductor capacitance. This was demonstrated to improve the TFT performances, by decreasing the sub-threshold slope and the operating voltage [8].

- **Ease of fabrication**. Ta_2O_5 layers can be deposited at relative low temperatures (around $200°C$) as for the AOS and conductive layers. Moreover, the combination with other components such as SiO_2 or Al_2O_3 allows to improve interface properties, reducing the number of trap states, and to increase the bandgap, reducing leakage currents [8].

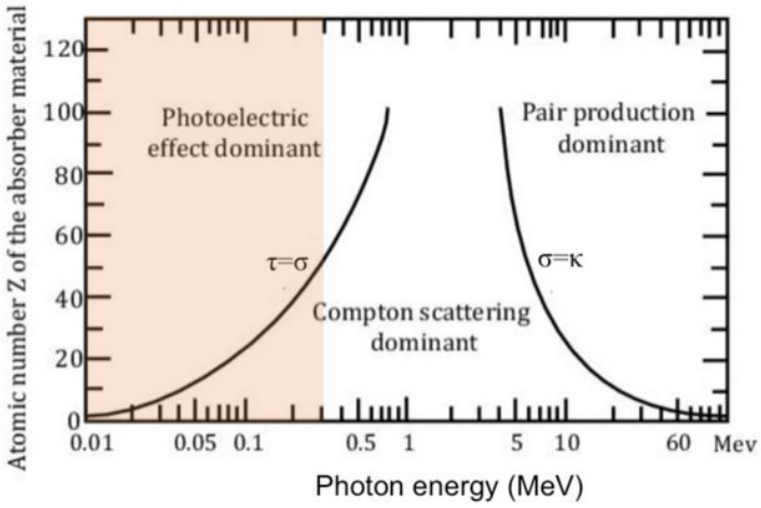

Figure 1.7: Relative interaction probability depending on elemental atomic number Z and the photon energy E. The shaded area corresponds to the X-rays range. (Adapted from: [7])

During radiation detection tests, ROXFET devices exhibited the same positive space charge accumulation observed in RADFETs, but with an order-of-magnitude increased sensitivity when operated without any bias applied (passive mode). In addition, the ROXFET sensors can be fabricated into arrays and on flexible plastic substrates. Finally, if associated to a low-cost radio-frequency identification (RFID) chip, such sensors can be employed as passive real-time operated radiation detectors and dosimeters [5].

1.2.2 ROXFET working principle and figures-of-merit

The working principle of ROXFET devices is presented in Figure 1.8. Upon exposure to ionizing radiation, excitons are generated inside the dielectric (which has the highest interaction probability thanks to its high atomic number). Then, excitons separate into electron and hole charge carriers that populate the conduction and the valence bands of the dielectric. Electrons are mobile in the oxide layer and hence diffuse out of the device through the gate contact. Instead, hole charges get trapped and lead to the build-up of a positive ionization charge close to the dielectric/semiconductor interface. Consequently, as the positive space charge in the dielectric contributes to the field effect in the semiconducting channel, the transistor threshold voltage (V_{th}) shifts toward negative values. The ΔV_{th} amount is proportional to the total radiation dose (ΔGy) absorbed by the device, providing integrated

information about the radiation exposure history.

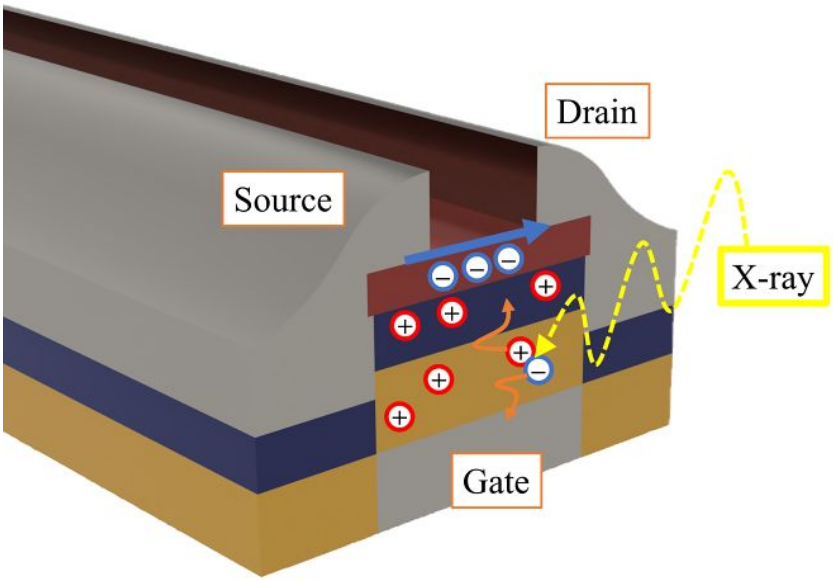

Figure 1.8: Cross section of a ROXFET device and schematic representation of its working principle.

From tests performed on first prototypes, ROXFET devices demonstrated [5]:

- **High radiation sensitivity**. Calculated as $\frac{dV_{th}}{dGy}$, represents the shift in threshold voltage obtained after a known absorbed dose. The observed $(3.4 \pm 0.2)\, V/Gy$ sensitivity corresponds to an order-of-magnitude increase respect to reference results from the literature.

- **Radiation hardness**. Upon exposure to ionizing radiation, no other TFT parameter such as sub-threshold slope or mobility is affected. This confirms the radiation sensitivity of the transistor structure and its stability during operation.

- **Stable measurement**. When irradiated, the device response in terms of V_{th} shift is fast (within seconds or less). Then, the threshold voltage tends to return to its initial value, but on a much longer time scale (several minutes or hours). This ensures good accuracy when the readout is performed in real-time or immediately after exposure.

- **Device re-usability**. The tendency to recover the initial V_{th} value suggests that an annealing of positive ionization charges in the dielectric takes place. It was observed that annealing time can be shortened by increasing temperature or by applying electric fields across the dielectric. In this way, it is possible to easily reset the dosimeter to its initial state and to reuse the device.

- **Real-time and remote operation**. The accumulation of charges in the dielectric, at the base of the device's operation, takes place even when no bias is applied to the device. This allows ROXFET to be combined with a RFID chip, both passively operated by a RFID reader (Figure 1.9). Upon request of the RFID reader, the integrated RFID tag probes the channel impedance (Z) of the ROXFET, wirelessly returning its value to the reader. Whether a detectable irradiation has occurred, the measured impedance has decreased as a result of the negative V_{th} shift. By means of a proportion, this measurement can be associated with a specific radiation dose. This approach allows to realize low-cost x-ray dosimeter tags that can be operated remotely and in real time, allowing automatized read-out, enabling immediate decision-making and preventing any exposure hazard.

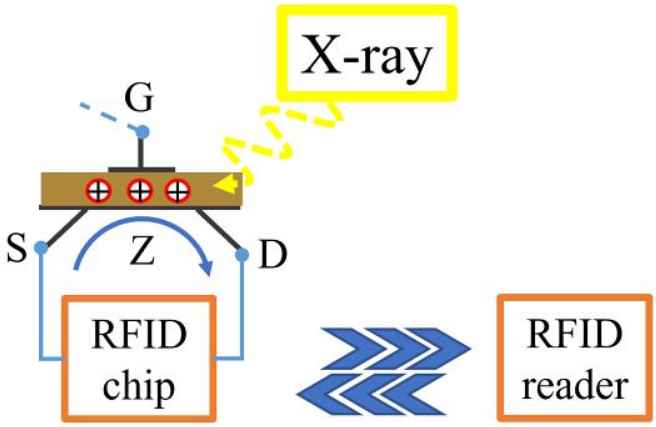

Figure 1.9: Schematic representation of the ROXFET-RFID integration. The RFID chip probes the impedance Z between source and drain, wirelessly operated by a reader. The gate contact might be connected in several different configurations to the RFID chip.

Chapter 2

Fabrication processes

In this chapter we will focus on the the process involved in the fabrication of thin film transistors, which is summarized by the diagram in Figure 2.1. We will describe the techniques and apparatuses employed during this thesis work, in terms of both characteristics and physical working principles. We will go through the different photo-lithography approaches, the deposition techniques and subsequent etching processes, and will conclude with annealing treatments.

During this thesis work, we performed fabrication activities at the CEMOP facility of the NOVA University of Lisbon. In Chapter 4.1 we will discuss how we put into practice the fabrication workflow presented here.

2.1 Optical lithography

Optical lithography, or photolithography, is one of the techniques which might be employed to realize nano-scale devices with a bottom-up approach. Two different approaches are available: mask-based or projection-based. The former features relatively high throughput and the possibility to achieve resolutions down to few μm, while the latter has lower throughput but potentially higher resolution (down to few tens of nm) [9].

Initially, the substrate is covered with photoresist, a photosensitive solution whose chemical and physical properties change after being illuminated from a UV source. By selectively illuminating regions of the photoresist, it is possible to obtain a real-size 2-dimensional pattern on the surface of the substrate.

In the following sections I will describe the steps involved in the optical lithography process.

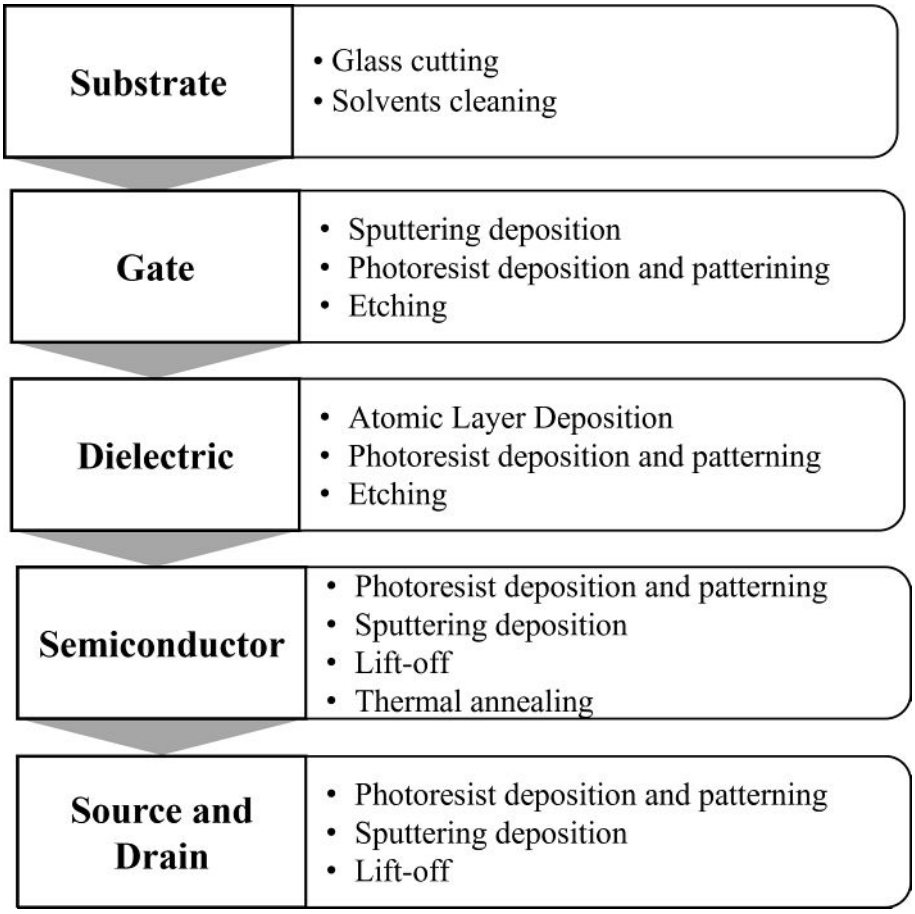

Figure 2.1: Workflow employed for the TFT fabrication.

2.1.1 Spin coating

Spin coating is a widely used method for photoresist deposition. It is relatively simple, fast and inexpensive as it only requires a high-speed rotating chuck operated in ambient condition. The substrate is retained to the chuck by a vacuum pump and, depending on the substrate area, a sufficient photoresist amount is deposited at the wafer center. The rapid acceleration up to thousands of revolutions per minute (rpm) spreads the liquid toward the edges, expelling ed over the edges any excess amount.

While standard photoresist is usually around $1\,\mu m$ thick, spin-coated thicknesses may vary from $0.1\,\mu m$ up to $500\,\mu m$.

The film thickness depends mainly on resist viscosity (ν) and spin

speed (ω), according to

$$t \propto \sqrt{\frac{\nu}{\omega}} \tag{2.1}$$

but also on other factors such as acceleration, ambient conditions, solvent drying rate or surface tension [10].

The photoresist solution is mainly composed by:

- Base resin, which determines the mechanical and thermal properties;
- Photoactive compound, which determines sensitivity to radiation;
- Solvent, which controls viscosity.

2.1.2 *Soft baking* or *Pre-baking*

Immediately after spin coating follows a *soft baking*, or *pre-baking*, which consists in placing the coated substrate on a hot plate. This step allows to improve photoresist adhesion and to evaporate most of the solvent.

In order to obtain uniform and reproducible results, the bake temperature and duration need to be optimized, since a too high temperature would decompose the photoactive compound and lead to lower sensitivity under illumination [10].

2.1.3 Pattern alignment and exposure

Every micro fabricated device is usually composed by several different layers (in this case: electrical contacts, dielectric, semiconductor), each of whom can be represented by its 2-dimensional imprint. During the design phase, the properly sized graphical representation of every layer to be fabricated is encoded in a GDS file. Such files also contain the details about the designed model, and can be easily visualized and edited with computer software (such as KLayout [11]).

For this work, in order to transfer the desired pattern from the digital model to the surface of the substrate, we employed a direct-writing lithography method. In such a technique, the substrate with the photoresist ready to be patterned is secured onto the x-y moving stage of a micro-writer (Figure 2.2). A laser write head is optically focused on the surface of the underlying substrate and projects a pulsed UV light beam controlled by the micro-writer. The control unit of the micro-writer interprets the GDS models and transforms it into a series of lines, which are reproduced onto the substrate by sliding the x-y stage and selectively pulsing the laser write-head

(Figure 2.3). Photoresists are usually sensitive to wavelengths in the UV - visible blue range (below 450 nm) [10]. Indeed, the fabrication room requires a special yellow light illumination so to prevent damaging the patterned photoresist layer.

The change in chemical and physical properties of the photoresist, induced by the selective UV irradiation, allow in the subsequent fabrication steps to obtain a full-dimension pattern of the desired layer.

Once exposed, the substrates undergo another baking step, which leads to the diffusion of photo-generated molecules responsible for the solubility difference between exposed and unexposed photoresist. This diffusion also smooths out optical interference effects. This post-exposure baking step is fundamental in the so-called *chemically amplified resists*, where the UV exposure only initiates the polymerization process, generating catalyst molecules that only activate during the baking step [10].

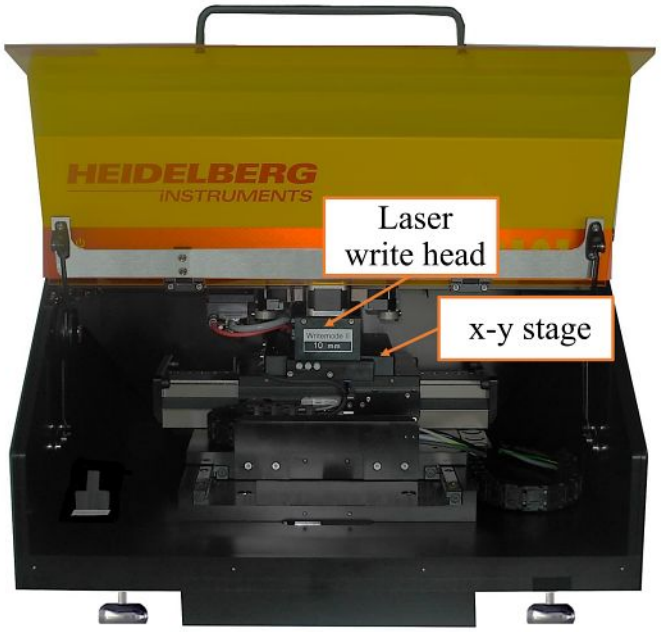

Figure 2.2: Heidelberg Instruments μPG101 laser micro-writer employed for optical lithography.

The micro-fabrication of devices nearly always requires the stacking of several differently patterned layers. In such cases, the photoresist deposition and patterning is repeated throughout the fabrication process, and every newly deposited pattern must be perfectly aligned with the underlying features already present. To this end, the photoresist patterning model should

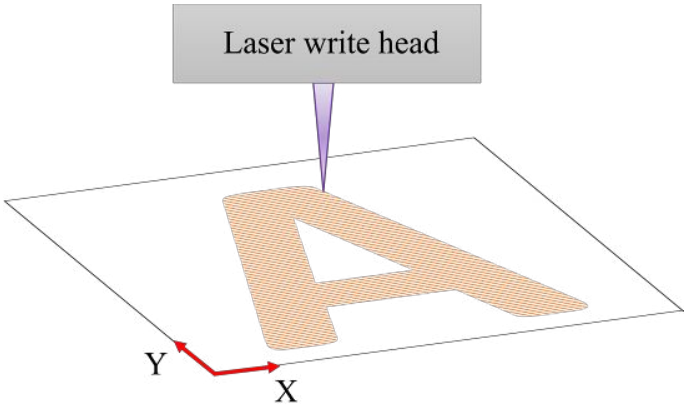

Figure 2.3: Working principle of laser writing.

foresee some pattern alignment symbols (Figure 2.4) placed at fixed coordinates in every layer. In this way, by taking (at least) two of these symbols as calibration points before the exposure, it is possible to obtain an optimal alignment of the layers stack.

Figure 2.4: Alignment pattern employed to fabricate all ROXFET samples. Six of these patterns are distributed on the sample, three on the left corner and three on the right. The center of the right symbol corresponds to the calibration point, while the left cross (if present) identifies the two symbols at mid-height of the sample.

2.1.4 Development

After the exposure procedure, the substrates undergo a development treatment. Depending on the photoresist used, different developer solutions are available.

In the following I will present two different approaches employed in this thesis work: the *conventional* method and the *lift-off* method.

Conventional photolithography

In this procedure, summarized in Figure 2.5, the photoresist layer has been deposited on top of the thin film layer. After the exposure step, a bath in a developer solution is able to dissolve the positive (negative) photoresist regions that were (were not) illuminated with UV light. The so obtained photoresist pattern will protect the underlying deposited material during the following etching phase.

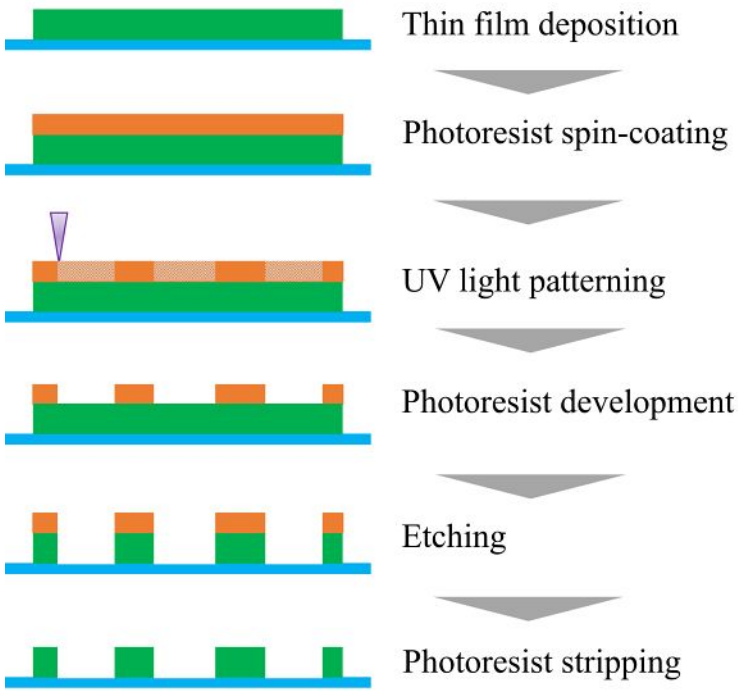

Figure 2.5: Steps composing the conventional photolithography process.

As we saw, both positive and negative photoresist are available. Usually, in the case of positive resist, the base resin is soluble in alkaline developers, while the photoactive compound acts as an inhibitor. Thus, unexposed resist is non-soluble in the developer. Upon illumination, the photoactive component undergoes a reaction that forms an acidic compound, rendering soluble the resist combined with it [10].

Instead, with negative resists, the exposed area can become insoluble by becoming cross-linked either via free radical or acid-catalysed polymerization, a process that increases its molecular weight. It has to be notice that the cross-linking that stabilizes the negative photoresist also makes its removal difficult in the following steps [10]. Also, since only the stabilized

regions remain to protect the underlying material, the exposure template should be designed as a *negative* of the desired pattern (Figure 2.6).

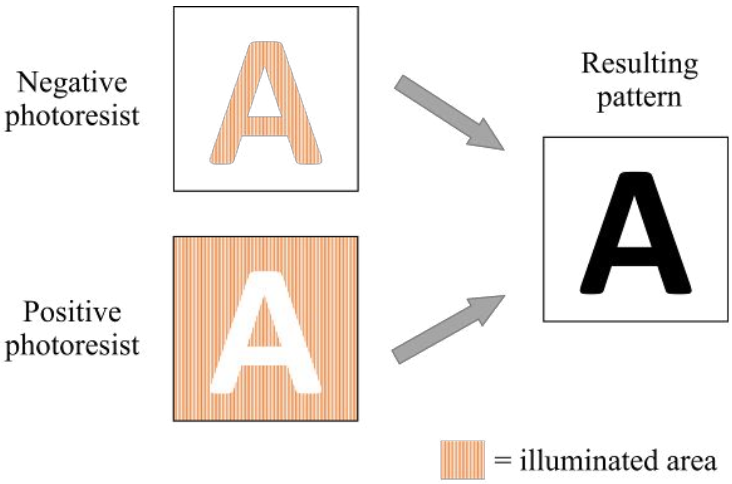

Figure 2.6: Comparison between positive photoresist and negative photoresist. In order to obtain the same final pattern (e.g. the *A* letter), the two photoresist types require complementary exposure patterns.

In photolithography rework is easy: if a visual inspection indicates that the resist pattern is faulty or misaligned, the photoresist can be easily stripped and lithography repeated. However, rework becomes nearly always impossible once the subsequent etching has taken place and the pattern has been transferred into the underlying layer [10].

After the etching, all the remaining photoresist has to be stripped from the substrate. To this end, specific solvents or a simple acetone bath dissolve the photoresist leftovers, leaving the underneath patterned layer and, eventually, ready for the following fabrication steps.

Lift-off photolithography

In this alternative approach, summarized in Figure 2.7, the photoresist layer has been deposited and patterned with UV light before (below) the thin film layer. After the photoresist development, performed as in the conventional process, follows the deposition of the thin film material. Then, the photoresist is stripped by specific developers or a simple acetone bath. During this step, both the resist and the above material are removed, leaving the desired pattern on the substrate.

As in conventional photolithography, rework is easy as photoresist can be easily stripped and lithography repeated. Again, if the overlying material has ben deposited, any reprocessing is extremely challenging [10].

The lift-off results preferable compared to the conventional process as, by not requiring any etching step, it prevents damaging the eventual previously deposited layers. On the other hand, this technique leads to less defined structures, more residues and it can be used only to pattern layers thinner than the resist thickness [10].

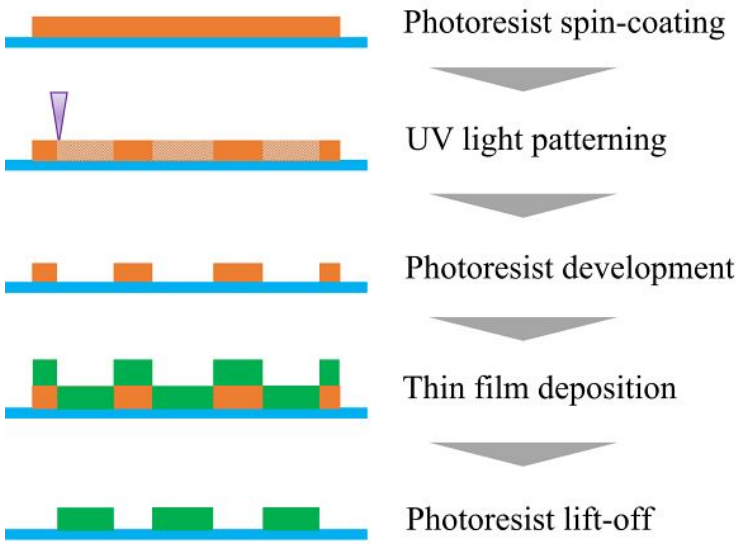

Figure 2.7: Steps composing the lift-off photolithography process.

2.2 Deposition

Two typical thin film deposition principles, both employed in this thesis work, are physical vapour deposition (PVD) and chemical vapour deposition (CVD). The distinction between the two arises from the fact that, while CVD features a chemical reaction (i.e. a change in the chemical properties of the precursors), PVD is characterized by a purely *mechanical* process.

Although both approaches contain many possible variants, in the following we will focus only on those employed in this thesis work.

2.2.1 Magnetron sputtering deposition

The working principle of physical vapour deposition relies on particles ejection from a solid target material and their following transport (in vacuum) to the substrate surface. PVD is divided into two categories depending on the technique used to evaporate the solid source materials into the vapour phase: thermal evaporation and sputtering.

Compared to other thin-film deposition methods, sputtering is characterized by several advantages: low substrate temperatures (down to room temperature), good adhesion of films on substrates, high deposition rate (up to $12\,\mu m\,min^{-1}$), great film thickness uniformity and density, relatively cheap and easy to control deposition method, possibility to deposit a broad range of materials and good scalability to large areas [12].

This deposition technique is based on the use of plasma, a gas-like phase in a dynamic condition where neutral gas atoms, ions, electrons and photons simultaneously exist. Figure 2.8, shows the working principle of this the sputtering technique. A vacuum chamber contains two electrodes: the cathode, to which is attached the target (the material to be deposited), and the anode, generally grounded and covered by the substrate. The chamber also has an inlet for an inert gas: Argon is typically employed due to its low cost and high cross-section.

To start the sputtering process, an electric field is created between the two electrodes. Due to this field, ever present electrons are accelerated towards the anode and eventually excite or ionize the neutral gas atoms along their path. In the first case, the excited Argon atom returns to the original electronic configuration, emitting a photon and giving rise to the characteristic glow discharge. If instead Argon undergoes ionization, the Ar^+ ions are accelerated towards the cathode electrode and, releasing their energy, sputter the surface of the target. This phenomena releases neutral target atoms and creates new free electrons: while the former travel towards the substrate, the latter contribute to the continuation of the plasma by

forming new Ar^+ ions.

The neutral particles ejected by the target would travel in a straight line but, due to the sputtering chamber pressure (usually from 1 to 10 $mTorr$), they often experience collisions before reaching the substrate. This phenomena, known as thermalization, has both positive and negative consequences. Indeed, on the one hand, the sputtered particles reduce their energy (cool down) before reaching the substrate, avoiding to the damage of the sample and decreases the re-sputtering rate (re-ejection from the substrate). On the other hand, these collisions decrease the number of atoms reaching the substrate, determining a lower sputtering rate.

The sputtering yield, representing the average number of atoms ejected from the target per incident ion, depends on various factors: the ion incident angle, the kinetic energy of the ions, the masses ratio between ions and target atoms, the threshold posed by surface binding energy of atoms in the target and, eventually, the crystalline orientation of the target [13]. In order to successfully deposit material on the substrate, such sputtering yield has to be higher than the unity.

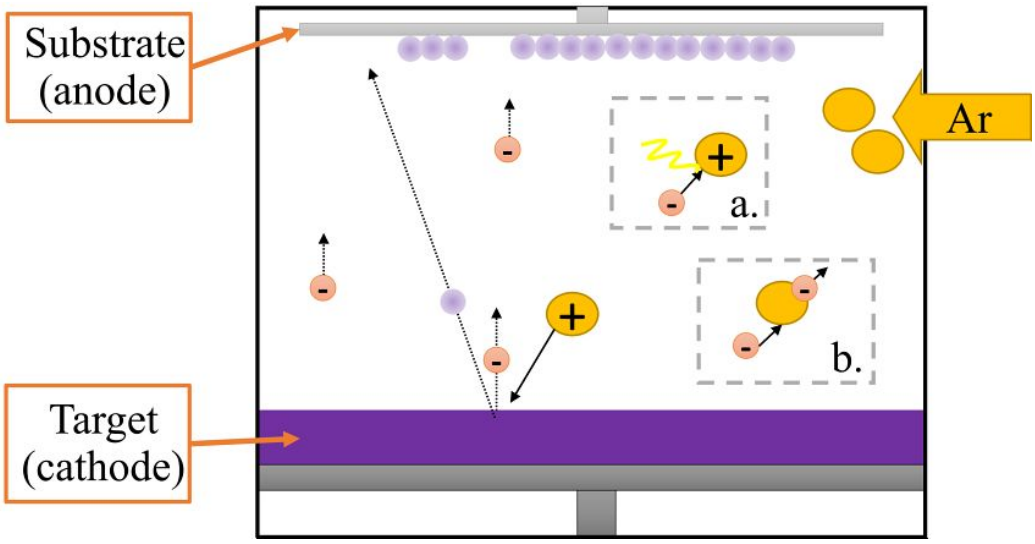

Figure 2.8: Schematic representation of the sputtering process. An Ar^+ sputters the target surface, releasing an atom that travels towards the substrate and a free electron. Inside the dashed boxes: a) glow discharge after Ar^+ relaxation, b) ionization of an Ar atom by a free electron.

Nowadays, the three main sputtering techniques are: DC, radio

frequency (RF) and magnetron.

- **DC sputtering**. It is the simplest configuration, which features a DC bias between the cathode and the anode. As insulators are not able to supply sufficient secondary electrons to sustain the gas ionization, such materials are not compatible with this technique.

- **RF sputtering**. This variation overcomes the previous limitations by supplying a high frequency voltage to the target (usually at $13.56\,MHz$). This setup employs an impedance-matching network between the power supply and the electrodes, blocking capacitors and an asymmetric electrode configuration induces (with the target area much smaller than the anode's one). These expedients induce a further negative DC bias on the target, creating the conditions for sputtering to occur even when employing insulator target materials [13].

- **Magnetron sputtering**. The two previous techniques present two main issues: they have a low deposition rate and may provoke overheating and substrate damage due to the strong electron bombardment. Magnetron sputtering, as an enhancement the RF technique, tackles these issues by implementing magnets behind the target. This solution produces a toroidal field capable of trapping the free electrons right above the target surface (Figure 2.10). Therefore, these electrons are prevented from bombarding the substrate and, at the same time, they enhance the ionization probability of neutral gas molecules, resulting in higher sputtering rates. A disadvantage posed by magnetron sputtering technique is the poor target utilization, as the preferential erosion occurs in the areas defined by the magnetic field (Figure 2.9).

Figure 2.9: Example of an eroded ZnO target. It is clearly visible the effect of the electrons confinement in specific regions due to the magnetic field.

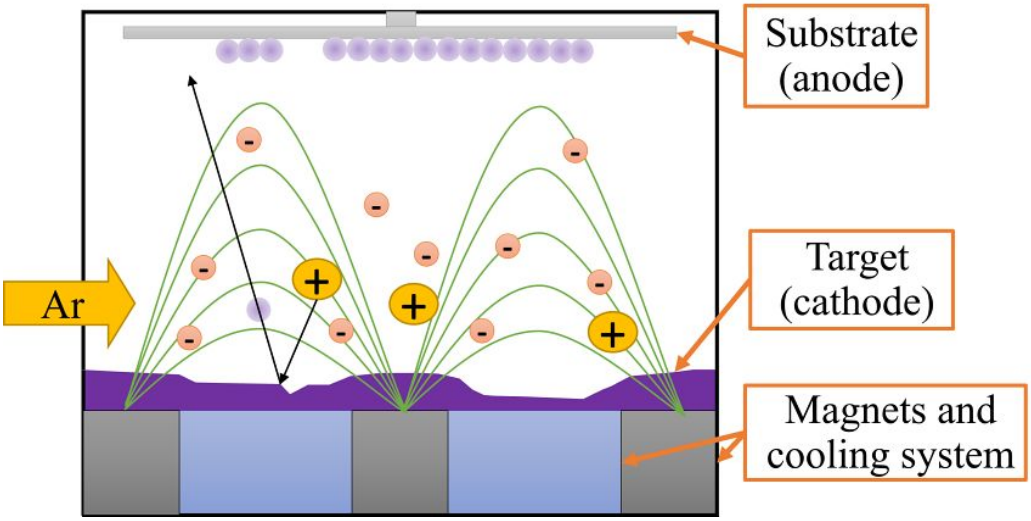

Figure 2.10: Simplified schematic representation of the magnetron sputtering process.

2.2.2 Atomic layer deposition

In chemical vapour deposition (CVD) techniques, a chemical reaction forms the basis of the deposition process. Although many variations exist, all CVD processes consist of: bringing the source materials (precursors) in the gas phase into the deposition chamber, enabling the chemical reaction (e.g. heating, plasma, etc.) and diffusing the precursors to the substrate's surface. Here, precursors react and bind to the surface forming a film, while reaction by-products are desorbed and pumped away. Given the fact that CVD processes employ gas phase materials and feature a chemical reaction, they are strongly dependent on pressure and temperature conditions inside the deposition chamber. Employing chemical vapour deposition techniques, thin films can be grown at a rate 0.1–10 nm/s [10].

Among existing CVD processes, in atomic layer deposition (ALD) technique films are deposited one atomic layer at a time, offering great thickness control and the ability to excellently coat any surface reproducing its morphology. Furthermore, ALD is free of homogeneous gas phase reactions, that are one of the main mechanisms of irreproducibility in CVD. Indeed, as only one gas is introduced at a time, gas phase reactions between precursors are impossible [10].

The working principle of ALD is schematized in Figure 2.11. Atomic layer deposition works in pulsed mode: inside the deposition chamber, chem-

ical bonds are formed between the precursor gas molecules and the atoms already present on the substrate's surface. Once all possible reaction sites are occupied, no more reactions can take place and a purging nitrogen pulse removes all excess precursor molecules. Then, a pulse of the second precursor is introduced and reacts with the previous layer. Similarly, the surface saturates as chemical bonds are formed, and excess precursor and by-products are purged away. The cyclical repetition of precursor and purge pulses allows to deposit thin films one atomic layer at-a-time.

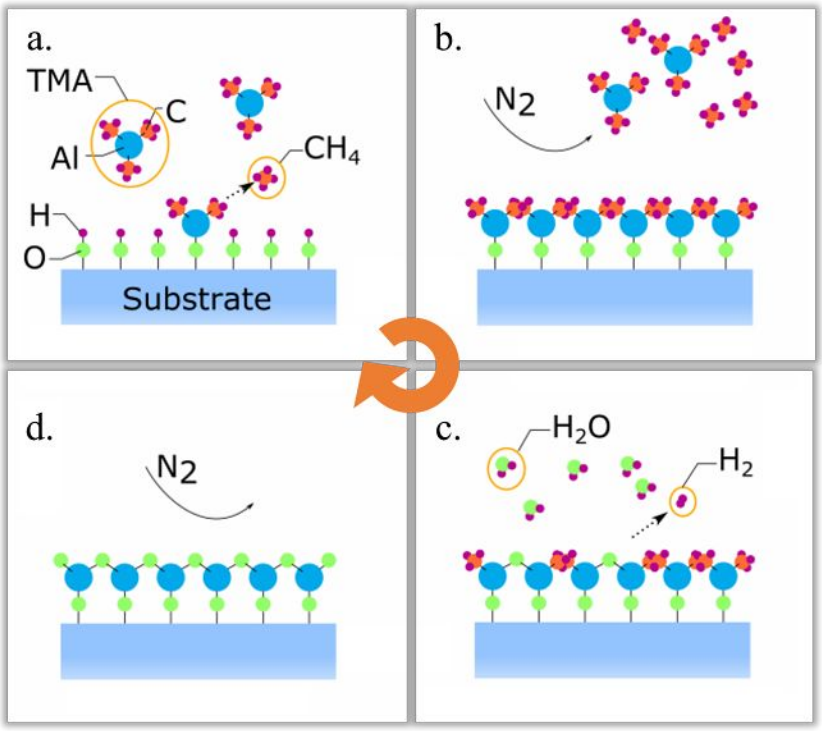

Figure 2.11: Schematic representation of an ALD cycle for the deposition of Al_2O_3. The steps represent: a) pulse of first precursor (TMA) saturating the available binding sites, b) purge of excess precursor and by-products with N_2 flow, c) pulse of second precursor (H_2O) saturating the available binding sites, d) purge of excess precursor and by-products with N_2 flow. These four step compose a single ALD cycle, which is repeated several times to deposit one atomic layer at-a-time of the desired material. (Adapted from: [14])

The layer thickness is simply given by the number of pulses times the monolayer thickness, and practical growth rates range are around $0.1\,nm/cycle$. When considering the deposition rates, one has to take into account the time required by purging cycles between the pulses. In general, rates of a few

nanometers per minute are typical for ALD processes [10].

In theory, with ALD one monolayer per pulse is deposited, but in sub-monolayer growth is also possible. One explanation is the so-called steric hindrance, that is the inability to move of an atom in a molecule due to the proximity of other atoms. Indeed, as large precursor molecules take up space, it is impossible for another precursor molecule to come close enough, rendering some reaction sites inaccessible. It is important to notice that both monolayer and sub-monolayer deposition are self-limiting, which is the key to controlling the deposition [10].

2.3 Etching

As previously discussed in Section 2.1.4, in conventional photolithography the photoresist protects the areas where the underlying material needs to remain, while open areas are etched.

In every etching process, the unprotected material can be both chemically or physically eroded. While only some materials can be chemically etched, all materials can be physically etched by energetic ions bombardment. This also applies to the photoresist, reason for which it is important to achieve selectivity: the etchant should remove the unprotected layer much faster than it attacks the photoresist layer [10].

Etching is often divided into two classes: wet etching and dry etching. For this thesis work, we employed both wet etching and plasma etching techniques, with this latter as part of the wider group of dry etching processes. The distinction between the two arises from the reactions involved [10]:

- **Wet etching** solid + liquid etchant $\rightarrow$ soluble products.
- **Plasma etching** solid + gaseous etchant $\rightarrow$ volatile products.

In both classes, several processes must take place for the etching to proceed [10]:

- Transport of etchants to the surface (flow and diffusion);
- Surface processes (adsorption, reaction, desorption);
- Removal of product species (diffusion and flow).

In the following, we will focus on the two techniques employed for this thesis work.

2.3.1 Wet etching

Wet etching employs liquid etchants to remove material from the substrate's uncovered areas. Upon exposure of the thin film material to the etchant, a chemical reaction (typically for insulators, a reduction-oxidation) consumes the original reactants producing new ones. All the reaction products are dissolved in the etchant solution and, as the full layer thickness is eroded, only the protected patterned layer remains on the substrate.

The velocity at which a *first order* chemical reaction occurs, expressed as $molar\,concentration/s$, is given by [15]:

$$\begin{aligned} reaction\,velocity &= k \cdot [X] \\ &\propto e^{(-E_a)/(k_b\,T)} \cdot [X] \end{aligned} \tag{2.2}$$

where E_a is the activation energy (required to overcome the initial energetic barrier preventing the reaction), $k_b = 1.38 \cdot 10^{-23}\,J/K$ is the Boltzmann constant, T is the temperature and $[X]$ is the concentration of the reactant (the etchant). Thus, both temperature and concentration are determinant in for the etching rate, which can also be influenced by two different reaction dynamics [10]:

- **Surface reaction-limited process**. A low surface reaction velocity determines the etching rate, which can be increased by increasing etchant concentration but not by stirring. The usual activation energy varies between $30 - 90\,kJ/mol$.
- **Transport reaction-limited process**. When the surface reaction is fast, the rate is then determined by etchant availability (i.e. transport of reactant by convection and diffusion) and can be increased with agitation and stirring. The usual activation energy varies between $5 - 25\,kJ/mol$.

The wet etching tends to be isotropic, which means that it occurs indistinctly in all spatial direction (Figure 2.12). As a consequence, this process also attacks the material under the resist (undercutting) up to a distance equal to the thickness of the film itself. When the dimensions of the patterned structures decrease below $\sim 1\,\mu m$, such undercutting can become seriously detrimental.

Some of the advantages of wet etching are its excellent material selectivity and the high etch rate ($10 - 100\,nm/min$). Moreover, compared to dry etching, the necessary equipment is relatively inexpensive as it only requires a heated quartz bath filled with the etchant solution. On the other hand, several problems might be present. Indeed, the product substances

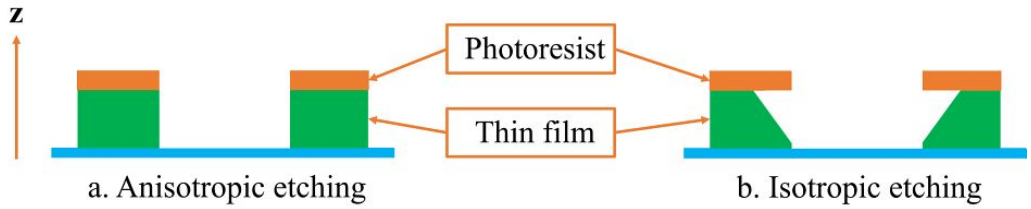

Figure 2.12: a) Anisotropic etching, with a preferential vertical direction. b) Isotropic etching, taking place in any spatial direction.

may catalyse or inhibit the chemical reaction that is taking place, and the eventual endothermic/exothermic nature may influence the process temperature [10].

2.3.2 Plasma etching

Dry etching techniques employ either plasmas or etchant gasses to erode the unprotected areas of the substrate. The process that takes place can involve ionized particles with high kinetic energy, chemical reactions or a combination of both.

The term dry etching is often used as a synonym for plasma etching, even if there are dry methods that do not involve plasma formation. There are mainly three different kinds of dry etching mechanisms [16]:

- **Sputtering**. The interaction is purely physical, involving momentum transfer. It typically employs highly energetic positive ions (e.g. Ar^+) bombarding the sample. When ions strike and transfer their energy to surface atoms, material is removed as these latter are ejected from the surface. This process is highly anisotropic, but it is slow and lacks of material selectivity as it requires high ions energies.

- **Purely chemical**. In this process, an etchant gas reacts with the substrate material, creating volatile products that escape from the surface and are pumped out of the chamber. This kind of procedure is the most material selective but also non-directional (isotropic).

- **Ion-enhanced energy-driven mechanism**. These processes, such as reactive ion etching (RIE), combine both physical and chemical etching mechanisms. In RIE (Figure 2.13), samples are kept in vacuum and reactive gases are ionized and accelerated so to bombard the sample

surface. The ionization occurs thanks to an AC bias (usually a RF at $13.56\,MHz$) between two electrodes, while the acceleration is a consequence of a negative DC bias ($\sim\ -100\,V$). The etching occurs as a combination of the ion bombardment and the chemical reaction promoted by energy transfer, forming volatile products that escape from the surface. Pressure, temperature, RF power, and gas flows all influence the final etching result. This technique combines good material selectivity and high level of anisotropy, avoiding the undercutting problem (Figure 2.12) characteristic of wet processes.

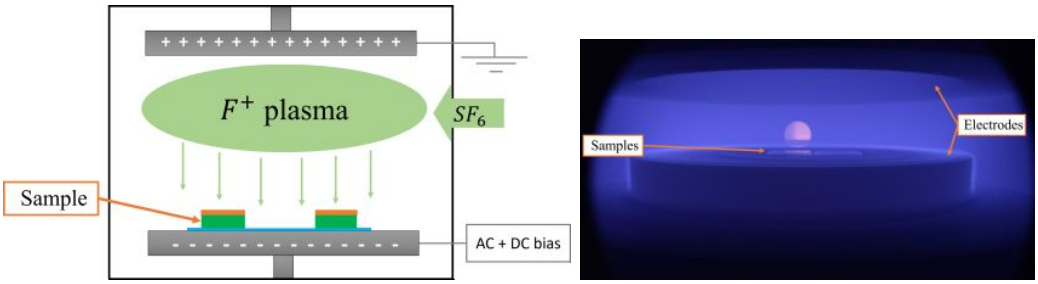

Figure 2.13: On the left, schematic representation of the Reactive Ion Etching process. The AC bias between the two electrodes ionizes the SF_6 gas, while the negative DC bias accelerates the F^+ ions towards the sample to be etched. On the right, picture of two samples undergoing RIE.

Among the advantages, dry etching requires only small amounts of reactant gases, while wet etching requires the disposal relatively large amounts of liquid chemical wastes. Also, dry etching features an anisotropy not available in wet etching. On the other hand, the process is relatively more expensive and also generates by-products that are toxic or polluting.

2.4 Thermal annealing

Post-deposition processes are able to modify several key features of the fabricated devices. Thermal treatments, known as thermal annealing, offer numerous advantages: reduce electron traps density in the bulk and at the interfaces [17], release the mechanical stress accumulated, promote the formation of a crystalline phase from an amorphous one [18], and even modify the interfaces, by annihilation of surface states or inter-diffusion of different elements.

In thin film transistors fabrication, a rapid thermal annealing (RTA) treatment has proven to be beneficial in terms of electrical performances of the devices. By removing donor-like defect states at the semiconductor/metal interface induced by the ion bombardment during sputtering, the TFTs showed an improved mobility, a smaller sub-threshold swing and a higher on/off ratio [17].

Rapid thermal annealing can be performed in three alternative methods: by switching on powerful halogen lamps (Figure 2.14), by rapidly transferring the sample into a hot zone, or using lasers [10]. RTA represents an improvement respect to standard thermal annealing treatments, as it can be performed controlling the thermal budget (i.e. the heat transferred to the sample) and gaseous impurities. Also, process duration is reduced to seconds (or even milliseconds), instead of minutes or hours. This also helps to reduce diffusion of dopants or impurities, as the diffusion length l_{RMS} and process duration t are related as $l_{RMS} \propto \sqrt{t}$.

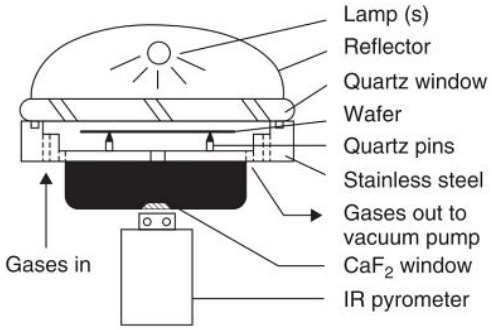

Figure 2.14: Schematic representation of the components of a halogen lamp based RTA system. The *wafer* represents the sample to be thermally annealed. (Source: [10])

Chapter 3

Characterization processes

In this chapter we will go through the characterization techniques that we employed on the experimental samples. To start, we will review the setup employed to perform standard electrical characterization measurements, such as I-V transfer and output characteristics. Then, we will discuss how C-V measurements can be performed in order to probe the density of states inside thin film transistors. Finally, we will see the principles of KPFM measurements and some of the informations that can be achieved.

3.1 Electrical characterization measurements

3.1.1 Standard electrical characterization

We performed the standard electrical characterization of the ROXFET samples to extract I-V transfer characteristics both in linear ($V_D < V_G - V_{th}$) and saturation ($V_D > V_G - V_{th}$) regimes. To this end, we employed a specifically manufactured apparatus available at the Physics and Astronomy department at the University of Bologna. The instrumentation was composed by a sample holder and a multiplex (MUX) based on the ADG333A chip [19]. The multiplexer was also directly interfaced to a KEYSIGHT B2912A source measure unit (SMU) [20]. The SMU was able to control the multiplexer, switching the available channels while measuring in series all the devices present on the sample. Through a control software on a computer, we ran the measurements and extracted the experimental data (Figure 3.1).

This experimental apparatus was fully compatible with the measurements we aimed at performing, as it showed noise background currents below $50\,pA$ in a $[-10\,V\,;\,10\,V]$ operative range.

The standard characterization procedure, performed on each sam-

ple, consisted in the acquisition of:

- 3 consecutive I-V transfer characteristics, in saturation regime, on all of the 9 devices on the sample. This allowed us to determine the appropriate V_G range and which devices were working. Also, as it was known that such TFTs experience V_{th} shift in the first few measurement cycles, by repeating the measure we ensured that the devices had reached stability before the proper data acquisition.
- I-V transfer characteristics, in saturation and then linear regime, only selecting the working devices.
- Output characteristic, only selecting the working devices.

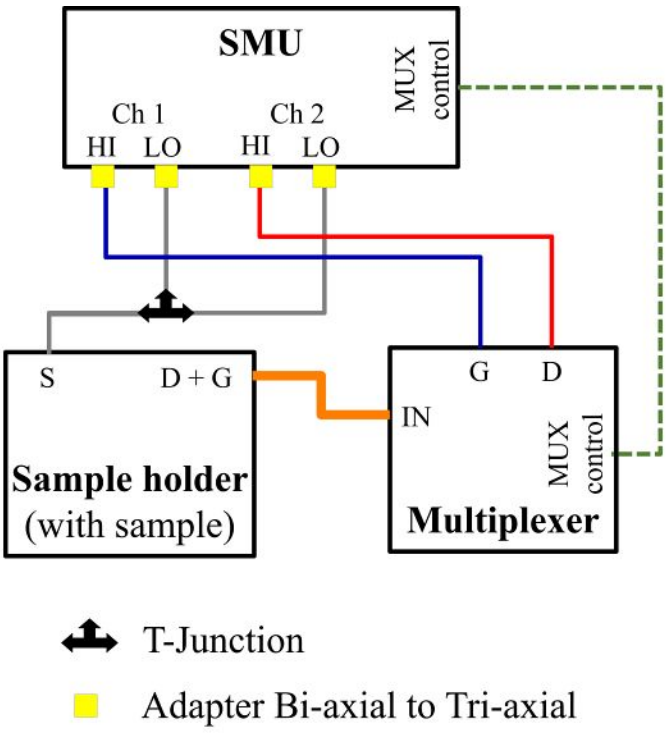

Figure 3.1: Setup employed for the electrical characterization measurements. With the sample placed on the sample holder, the common source was directly connected with bi-axial cable to both SMU Low channels. Instead, all the drain and gate pads were connected with a ribbon connector to the multiplexer input. Also the two MUX output channel were connected to the SMU High channels with bi-axial cables. The power connections (MUX and SMU) and the USB connection to PC for the SMU are not represented.

3.1.2 Capacitance-voltage measurements and density of states determination

Capacitance-voltage measurements (C-V) are widely used in TFTs electrical characterization for determining several parameters such as: dielectric oxide thickness, doping, flat-band voltage, work function and density of states at the interfaces [21]. In this thesis work, we employed such measurements to determine the TFTs capacitances and the sub-bandgap density of states (DOS) at the semiconductor-dielectric interface, according to the work described in [22].

To this end, we employed the experimental setup schematized in Figure 3.2. A Zurich Instruments MFLI Lock-in Amplifier [23] was able to provide AC signals up to $5\,MHz$ with a DC offset of $\pm 10\,V$.

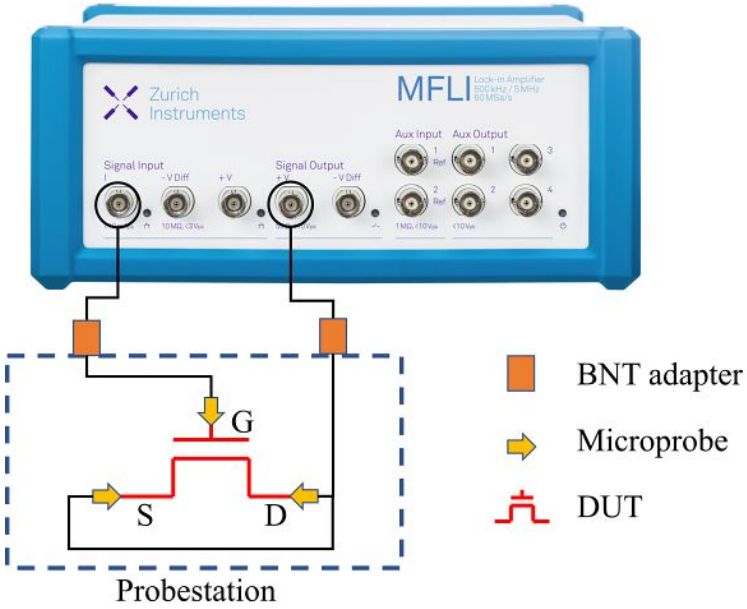

Figure 3.2: Schematic representation of the setup employed for C-V characterization measures. The sample was placed inside a probe station and the device under test (DUT) was electrically contacted. We employed BNT adapters for bi-axial cables to perform the connections with the Lock-in amplifier. (Source of the device picture: [23])

In order to extract the capacitance of a TFT device, the aforementioned setup can be employed to provide a sinusoidal AC signal of known frequency (f) and root-mean-square amplitude ($V_{in\,RMS}$). The frequency should be selected inside the operative range of the Lock-in amplifier. Then,

a measurement is performed by acquiring the input current ($I_{out\,RMS}$) while sweeping the gate voltage in a range in which occurs the on/off switch of the TFT. The impedance as function of gate voltage ($Z(V_G)$) can be calculated as:

$$Z(V_G) = \frac{V_{in\,RMS}}{I_{out\,RMS}(V_G)} \tag{3.1}$$

Then, since $\omega = 2 \cdot \pi \cdot f$ and $Z = \dfrac{1}{\omega \cdot C}$, we obtain the capacitance $C(V_G)$ as:

$$C(V_G) = \frac{1}{\omega \cdot Z(V_G)} = \frac{I_{out\,RMS}(V_G)}{\omega \cdot V_{in\,RMS}} \tag{3.2}$$

Known the length (L) and width (W) of the TFT's channel, the capacitance per unit area can be written as:

$$C_{area}(V_G) = \frac{C(V_G)}{W \cdot L} \tag{3.3}$$

The aforementioned procedure, if repeated at several fixed frequencies, allows to perform a multi-frequency C-V characterization. We employed such technique to determine the sub-bandgap density of states (DOS) at the semiconductor-dielectric interface [22]. In Appendix A is presented the derivation that relates the capacitance measurement ($C(V_G)$) to the density of states $g(E)$, in which E is the energy scale and V_G is the voltage applied to the gate electrode.

3.1.3 Positive bias stress tests on reference TFT devices

During the application of a bias voltage, thin film transistors may undergo changes in their threshold voltage for several different reasons, which include electron or hole trapping at the interfaces, or the creation of donor states [24]. Positive bias gate stress (PBGS) tests are commonly employed to observe and quantify such effect. A PBGS test consists in applying, generally for few hours, a constant positive voltage to the gate, while keeping the source grounded. At regular intervals, the bias is interrupted just for the time of acquiring a I-V transfer characteristic in linear regime. These measures are fundamental to later extract V_{th} and determine how it has shifted over time, but they also inevitably perturb the stress procedure. For this reason, transfer characteristics should be performed as few and as quick as possible. During the stress application, by also providing a small fixed bias to the drain (usually $V_D \approx 0.1\,V$), it is possible to monitor the drain-source current I_{DS}, which tracks the evolution of the threshold voltage shift.

Normally, we can expect that the threshold voltage shifts *towards* the applied bias, and then tends to recover the original value upon removal of the external stress. The trend relating V_{th} vs. *time* can be fitted with a power function, usually the exponential

$$V_{th}(V) = A \cdot exp(-t(s)/\tau) + B \tag{3.4}$$

where A and B are parameters while τ is a time constant. From that, we can extract the characteristic time constant τ_{stress} of the device [25]. Analogously, a $\tau_{recovery}$ constant can be determined if the previously mentioned procedure is continued while applying no bias to the gate. Ideally, for common applications a transistor should have a large τ_{stress} (small V_{th} drift under stress) and small $\tau_{recovery}$ (fast recovery of the stress effect).

In order to perform PBGS tests, we employed the experimental setup available at the CEMOP facility, which features a Cascade Microtech EPS 150 probe station [26] connected to a KEYSIGHT B1500A semiconductor parameter analyser [27] (Figure 3.3).

Figure 3.3: Setup for electrical characterizations available at the CEMOP department of the NOVA University of Lisbon.

3.2 KPFM measurements

The Kelvin probe force microscopy (KPFM) technique aims at producing a high spatial resolution map of the work function or surface potential of a sample. In recent studies, KPFM was used to image the potential distribution on surfaces with sub-nanometer resolution, making KPFM the ideal method for characterizing the electrical properties of nanostructures [28].

Kelvin probe force microscopy is primarily based on the instrumentation of an atomic force microscopy (AFM) system. The AFM employs a cantilever with a tip that can operate three different modes: contact, intermediate (tapping) and non-contact.

In contact and intermediate mode operations, the AFM tip directly touches the sample surface. When sweeping the surface, either the cantilever deflection or oscillation amplitude is monitored and used as a feedback signal to re-adjust the cantilever according to a set-point. At each spatial point, the cantilever vertical displacement necessary to reach the set-point directly provides an information about the sample topography. Moreover, when in tapping mode, the analysis of the oscillation amplitude variation in terms of an harmonic oscillator model can describe the direct tip-sample interaction force [28].

In non-contact mode, while the cantilever is oscillated close to its resonant frequency, the AFM tip never touches the surface. While scanning the surface, the tip–sample interaction is altered as their relative distance changes (according to an harmonic oscillator model), leading to a change in cantilever's resonance frequency. A feedback system regulates the cantilever vertical displacement to keep the set-point frequency constant, allowing the topography of the sample surface to be acquired. In this operation mode, the AFM detects the force gradient between tip and sample rather than force itself, a factor that provides have higher spatial resolution when compared to other modes [28].

The Kelvin probe force microscopy technique measures the local contact potential difference (CPD) between the sample surface and the AFM tip operated in non-contact mode. Indeed, as the measured CPD is strongly affected by a short-range force between tip and sample, it is specifically referred as the local CPD. While standard Kelvin probe methods provide results averaged over the whole sample surface, KPFM is able to detect local variations in CPD with a resolution of $10\,nm$ or higher [28].

The contact potential difference (V_{CPD}) between the tip and sample can be expressed as:

$$V_{CPD} = \frac{\Phi_{tip} - \Phi_{sample}}{q_0} \tag{3.5}$$

where Φ_{tip} and Φ_{sample} are, respectively, the work functions of the sample and tip, while q_0 is the elementary charge. As shown in Figure 3.4, when the AFM tip is brought close to the sample surface, an electrostatic force arises between the two as a consequence of the difference in energy of the Fermi levels. Equilibrium is reached upon alignment of the Fermi levels, obtained as a tunnelling electron current starts to flow when the is close enough to the surface. As a consequence, a V_{CPD} forms between the two, also resulting in an electrostatic force. By applying an external voltage bias (V_{DC}) with the same magnitude of V_{CPD} but opposite sign, such force can be nullified. At this stage, known the V_{DC} applied (thus V_{CPD}) and the tip work function (Φ_{tip}), it is possible to obtain the local Φ_{sample} (Equation 3.5). Thus, it is possible to obtain a map of the local CPD (or work function) from the V_{DC} applied while scanning the surface of the sample.

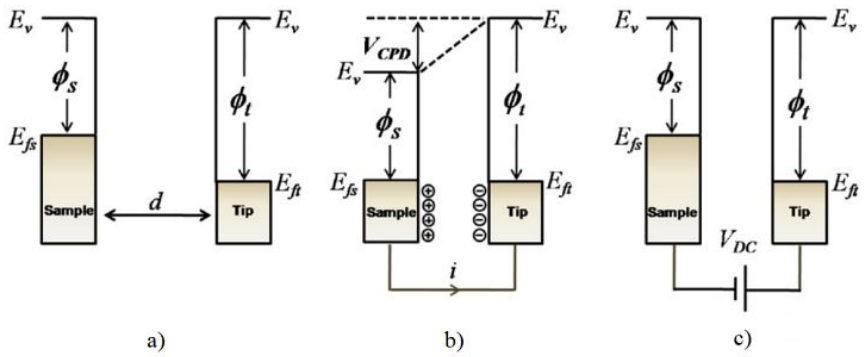

Figure 3.4: Electronic energy levels of the sample and the AFM tip for three cases: a) tip and sample are distant and with no electrical contact, b) tip and sample are close enough for being in electrical contact via a tunnelling current, c) an external bias (V_{DC}) is applied between tip and sample to nullify the CPD and, therefore, the tip–sample electrical force. E_v is the vacuum energy level, while E_{fs} and E_{ft} are, respectively, the Fermi energy levels of the sample and tip. (Source: [28])

According to the tip-sample distance, short-range forces (e.g. van der Waals) overlap with the electrostatic force that underlies the V_{CPD} measurement. Thus, in KPFM, the AFM tip is biased with a combination of the already mentioned DC voltage (V_{DC}) and an AC voltage (V_{AC}) (Figure 3.5). Thanks to this modulation, the V_{DC} component that nullifies the electrostatic force related to CPD can be separated from other forces. It is important to choose the AC signal frequency so to be different from the one of the cantilever oscillation. In this way, no interference occurs between the

two different pulses, allowing the CPD information to be correctly extracted.

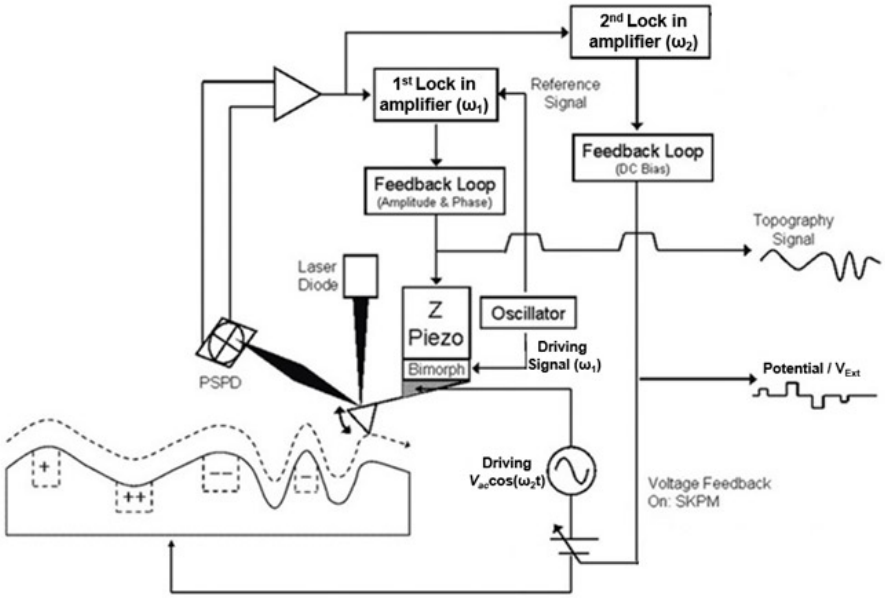

Figure 3.5: Schematic representation of the components of a KPFM system. The dashed line over the sample represents the measured topography, while the +/- regions in the sample are an example of the measurable potential. (Source: [29])

Considers the tip-sample interaction as the one between two capacitor plates ($U = \frac{1}{2}C\Delta V^2$), the electrostatic force (F_{es}) between the AFM tip and the sample can be expressed as:

$$F_{es}(z) = -\frac{1}{2}\Delta V^2 \frac{\partial C}{\partial z} \tag{3.6}$$

where z is the direction normal to the sample surface, ΔV is the potential difference between V_{CPD} and the voltage applied to the AFM tip and $\partial C/\partial Z$ is the gradient of the capacitance between the tip and the sample surface. When both the DA and AC biases are applied to the tip, ΔV corresponds to:

$$\Delta V = V_{tip} - V_{CPD} = (V_{DC} - V_{CDP}) + V_{AC}\sin(\omega_{AC}t) \tag{3.7}$$

Combining the two previous equations, the electrostatic force applied to the tip is:

$$F_{es}(z,t) = -\frac{1}{2}\frac{\partial C}{\partial z}\left[(V_{DC} - V_{CDP}) + V_{AC}\sin(\omega_{AC}t)\right]^2 \tag{3.8}$$

This equation can be divided into three parts:

$$F_{DC} = -\frac{\partial C}{\partial z}\left[\frac{1}{2}\left(V_{DC} - V_{CDP}\right)^2\right]$$

$$F_{\omega} = -\frac{\partial C}{\partial z}\left[\left(V_{DC} - V_{CDP}\right) V_{AC} \sin\left(\omega_{AC} t\right)\right]$$

$$F_{2\omega} = \frac{\partial C}{\partial z}\frac{1}{4} V_{AC}^2 [\cos(2\omega t) - 1] \tag{3.9}$$

Here, F_{DC} induces a static bending of the cantilever, F_{ω} is used to measure the CPD and $F_{2\omega}$ can be applied in capacitance microscopy [28]. Thanks to the AC modulation, a lock-in amplifier can be employed to extract at frequency ω the F_{ω} force component. The output signal of that lock-in amplifier is directly proportional to the difference between V_{CPD} and V_{DC}. Thus, the value of V_{CPD} can be measured by applying a V_{DC} to the AFM tip such that the output signal of the lock-in amplifier is nullified ($F_{\omega} = 0$). In this way, it is possible to map the value of V_{CPD} on the whole sample surface area.

During our experiments, we employed a Park Systems NX10 atomic force microscope [30] available at the Physics and Astronomy department at the University of Bologna. Inside the AFM apparatus, the samples were connected to a KEYSIGHT B2912A source measure unit with the electrical contacts shown in Figure 3.6. We performed the connections to the SMU similarly to what described for the electrical characterization measurements (Section 3.1.1). As an exception, we did not employ the multiplexer as we performed our tests on a single device.

One of the goals of our experiment was to extract the density of states (DOS) of the semiconductor from KPFM measurements, following the principle described by Roelofs et al. in [31]. Among the available techniques to extract the DOS, the KPFM method appears preferable as it can be performed in non-contact mode, thus not affecting the DOS itself.

The operation mechanism is presented in Figure 3.7. When the gate is at flat-band voltage, no electrostatic field is present between the gate and the semiconductor and, therefore, no charges are accumulated. During KPFM measurements, a bias V_{tip} is applied to the tip such that the electrostatic field between tip and surface is nullified.

Subsequently, a positive gate bias can be applied to the transistor, determining the bending of the energy levels and the accumulation of charges at the oxide interfaces that screen the potential seen by the AFM tip. This also determines a shift in the vacuum level (E_{vac}) of the semiconductor, which corresponds to that of the non-contacted AFM tip. Such variation, measured

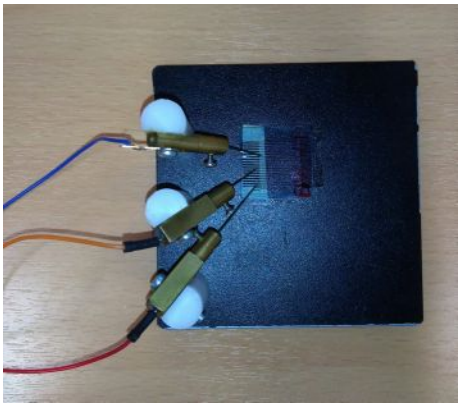

Figure 3.6: Electrically contacted sample inside the mini-protestation. Due to spatial obstructions between the KPFM head and the electrical probes, only one row of the devices matrix was accessible.

by KPFM, can be expressed as $\Delta E_{vac} = q_0 \Delta V_{tip}$, with q_0 the elementary charge.

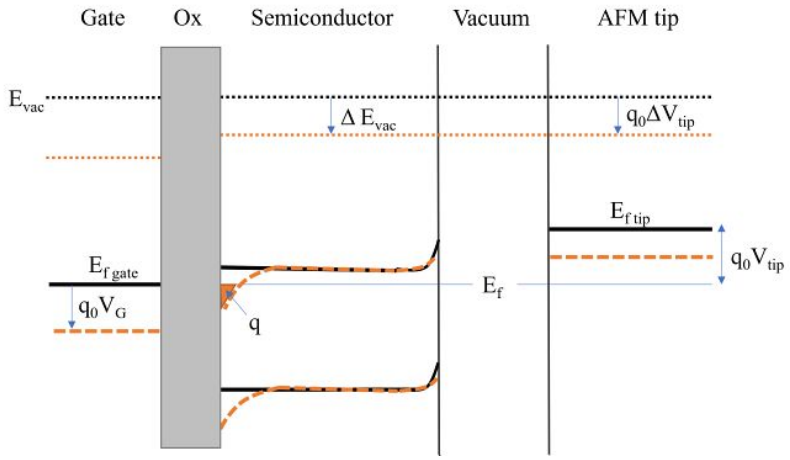

Figure 3.7: Energy band diagram of the KPFM experiment. In solid black is depicted the flat-band potential condition, while in dashed orange the situation when a positive gate bias V_G is applied to the gate. The charges indicated as q accumulate at the semiconductor-oxide interface, as the E_f is kept constant by the contact with source and drain electrodes.

With this procedure, the DOS is extracted from the measured V_{tip} as function of the the gate bias V_G. By increasing the gate bias, the number

of charges Δq accumulated at the semiconductor is given by:

$$\Delta q = C\left(\Delta V_G - \Delta V_{\text{tip}}\right)/q_0 t \tag{3.10}$$

where C is the capacitance per unit area of the dielectric and t is the thickness of the semiconductor. At the same time, the shift of the vacuum level ΔE_{vac} is measured by KPFM. With these information, the DOS at the Fermi level (E_f) can be extracted as:

$$g\left(E_f\right) = \frac{\Delta q}{\Delta E_{\text{vac}}} = \left[\left(\frac{dV_{\text{tip}}}{dV_G}\right)^{-1} - 1\right]\frac{C}{tq_0} \tag{3.11}$$

In Equation 3.11, we have multiplied by a q_0 term so that the DOS is expressed as $eV^{-1}cm^{-3}$. Also, it is important to remember that this equation is valid assuming $T = 0\,K$ and a homogeneous potential distribution across the whole thickness of the semiconductor. When these conditions do not apply, corrective terms must be added [31].

3.3 Radiation sensitivity measurements

After the assessment of the electrical performances of the ROXFET devices, followed the radiation sensitivity characterization, taking advantage of the equipment available at the Physics and Astronomy department at the University of Bologna. This procedure consist in measuring the response of the samples after being exposed to known ionizing radiation doses.

As previously discussed, ROXFET base their working principle on a threshold voltage (V_{th}) shift induced by the interaction with ionizing radiation. In order to produce and monitor such variation, we employed the setup presented in Section 3.1.1 together with a X-ray source (Figure 3.8). During this thesis work, we employed two different radiation source: a Hamamatsu microfocus [32] and a Mo target based X-ray tube. The measurements consisted in a continuous acquisition during which, every $15\,s$ the SMU acquired an I-V transfer characteristics in saturation regime. Each acquisition lasted only $20\,ms$, so to minimize the stress on to the device, thus avoiding any perturbation of the device's state. With the aid of the multiplexer, the SMU was able to measure in series all the devices present on a sample. Finally, with purposely designed Python code, we were able to extract V_{th} associated to each measurement and create a V_{th} vs. $time$ plot.

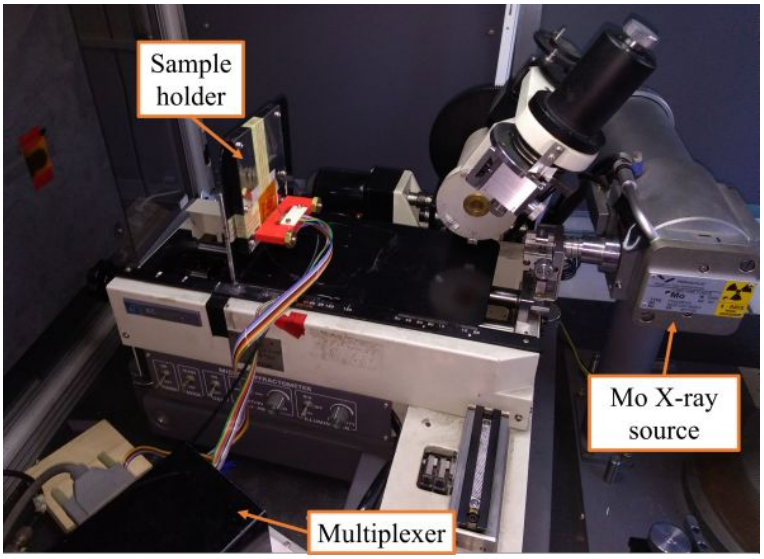

Figure 3.8: Part of the experimental apparatus employed for radiation sensitivity measurements.

The radiation dose can be expressed in Grays (Gy), which represent

the amount of energy deposited in one kilogram of matter ($1\,Gy = 1\frac{J}{kg}$). Thanks to the calibration curves previously determined, we were able to precisely control the radiation dose provided to the sample, by tuning the X-ray source parameters (source current and accelerating voltage) and the source-sample distance.

Multiple tests were performed with this experimental technique:

- **Minimum detectable dose**. This test aims at determining the minimum radiation dose that can be detected by a specific sample. It is carried out by providing increasing radiation doses (over several orders of magnitude) and while monitoring the eventual onset of a V_{th} shift.

- **Radiation sensitivity**. This test consist in quantifying the V_{th} shift induced by a specific radiation dose. The value of sensitivity is calculated as dV/dGy, where dV represents the measured threshold voltage shift and dGy the corresponding radiation dose provided. Such sensitivity, expressed in V/Gy, can be assessed over a wide range of doses, energies and cumulated doses.

- **Maximum cumulated dose**. This test intends to determine the cumulated dose at which the device is no longer able to detect any further irradiation. It is assessed by monitoring how the radiation sensitivity reduces after repeated irradiations of known dose.

- **Devices cross-talk**. In order to exclude possible interactions between devices (cross-talk), all the previously mentioned results can be performed by only irradiating one device at-a-time. To this end, we fabricated a holed $3\,mm$ thick brass mask ($Z \approx 30$), capable of screening 99% of the radiation below $55\,keV$.

Chapter 4

Results and discussion

In Section 4.1, we will go through the process and results from the fabrication performed at CEMOP laboratories in Lisbon. We will start with some positive bias stress tests performed on reference TFT devices, and then move to the details of the fabrication of a new batch of ROXFET samples. This section will conclude with a review of the electrical performances obtained from this batch.

In Section 4.2 we will see how we employed multi-frequency C-V measurements to extract information on the density of states (DOS) inside the semiconductor. This analysis was performed on all sample batches available, and for the newly fabricated batch we also investigates possible variations induced by ionizing radiation.

Finally, in Section 4.3 we study the impact of thin film architecture on radiation detection properties. Starting from and overview of the available TFT structures, we and their electrical performance data, we will analyse at the radiation sensitivity results and look for possible trends.

4.1 Oxide semiconductor thin film transistor fabrication results

4.1.1 Positive bias stress tests on reference TFT devices

The use of Ta_2O_5/SiO_2 multicomponent dielectric in amorphous oxide TFTs, recently investigated by researchers at the NOVA University of Lisbon, demonstrated to provide reliable and high performance devices [25]. During that study, it has been observed that V_{th} instability was more pronounced for the SiO_2-richer devices, implying that these were more defective.

In fact, SiO_2/high-k dielectrics interfaces are known to form defects, mainly due to silicon's strong oxygen affinity that causes oxygen displacement [25]. Alternatively, SiO_2 could be replaced by Al_2O_3, which offers several advantages: a lower oxygen affinity [33], a higher bandgap (of $9.9\,eV$ instead of $9\,eV$) and a higher dielectric constant (≈ 10 instead of 3.9) [34].

In order to investigate the potential improvement offered by Al_2O_3, we performed positive bias gate stress (PBGS) test as described in Section 3.1.3. We employed three previously fabricated samples with different dielectric composition: only Al_2O_3, only Ta_2O_5 and a multilayer combination of the two. For a consistent comparison, they all had W/L channel dimensions of $20/20\,\mu m$.

To perform the PBGS tests, we electrically contacted one of the TFTs inside the probe station (Figure 4.1) and then applied the following procedure:

- Acquire one I-V transfer characteristic in linear regime (I-V linear), in order to extract V_{th} of the sample.
- Set V_S to ground, $V_D = 0.1\,V$ and $V_G = 1 - V_{th}$.
- Start the PBGS protocol (the stress phase): I-V linear $\rightarrow 15min$ PBGS $\rightarrow$ I-V linear $\rightarrow 15min$ PBGS $\rightarrow$ I-V linear $\rightarrow 30min$ PBGS $\rightarrow$ I-V linear $\rightarrow 60min$ PBGS $\rightarrow$ I-V linear $\rightarrow 60min$ PBGS $\rightarrow$ I-V linear.
- Set $V_G = V_S$ to ground.
- Repeat the previous PBGS protocol (the recovery phase).

In this way, we were able to monitor the threshold voltage shift over a three hours stress period, followed by a three hours recovery phase. As a variation, we might have selected V_G in a different way, for example by fixing it to a constant value (thus fixing for all the samples the electric field present across the dielectric).

An example of the data acquired during PBGS measurements is represented in Figure 4.2. The time constants extracted for all the different conditions are reported in Table 4.1. From a time constant perspective, the Ta_2O_5-only condition was the one with best performances during both stress and recovery. On the other hand, such device was the only one experiencing an anomalous V_{th} shift, i.e. the threshold voltage is shifting in the opposite *direction* respect to the applied gate bias. The mechanisms that are normally used to explain this behaviour are: charge trapping/de-trapping from the gate dielectric, ionic migration within the dielectric (as a slow polarization of the dielectric material) or the creation of defects [25].

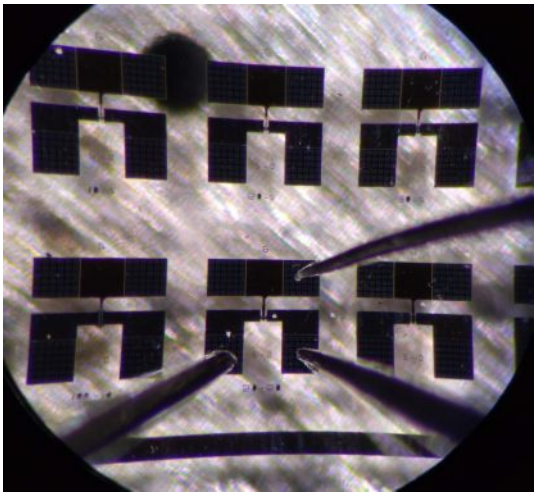

Figure 4.1: Picture of one of the reference TFTs employed for PBGS tests.

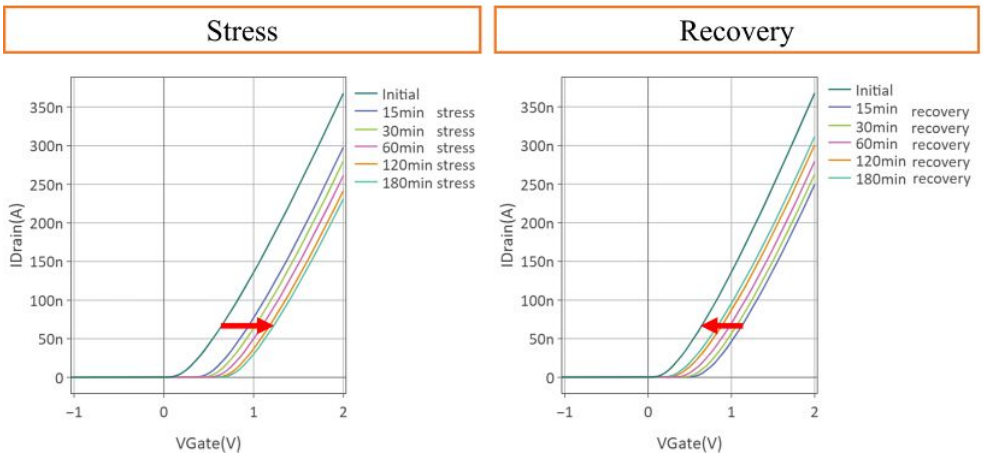

Figure 4.2: I-V transfer characteristics acquired during the stress and recovery phases of the Multilayer sample. It is possible to notice that the curves shift in the expected direction and that after three hours of recovery the TFT had not yet returned to the initial pre-stress state.

The analysis of the drain-source current (I_{DS}) measured during PBGS allows to guess how the V_{th} has shifted over time. Indeed, an I_{DS} decrease can be linked to a decreased channel conductivity, and therefore to a threshold voltage shifting towards higher voltages. The opposite is true if an I_{DS} increase is observed. Figure 4.3 compares the drain-source currents measured during our experiments. Overall, the trends confirm the normal/anomalous behaviour that we observed from the I-V transfer charac-

Sample	$\tau_{stress}(s)$	$\tau_{recovery}(s)$	V_{th} **shift**
Al_2O_3	$8.5 \cdot 10^2\, s$	$3.1 \cdot 10^3\, s$	Normal
Ta_2O_5	$1.4 \cdot 10^4\, s$	$2.1 \cdot 10^3\, s$	Anomalous
$Multilayer$	$1.4 \cdot 10^3\, s$	$4.1 \cdot 10^3\, s$	Normal

Table 4.1: Time constants extracted for the three different dielectric configurations.

teristics. Of particular interest is the fact that the Ta_2O_5 sample experiences a normal V_{th} shift in the first $\sim 50 - 100\, s$, before inverting its trend into an anomalous shift. Moreover, the slope of the I_{DS} trends is identical during all stress applications.

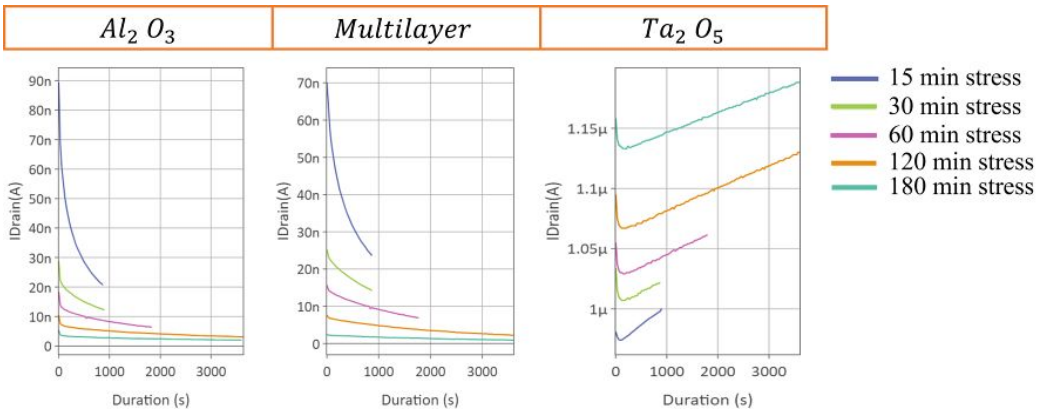

Figure 4.3: Trend of the I_{DS} measured during the application of a positive gate bias.

While for Al_2O_3-only and Multilayer samples the dominant effect associated with stress might be the electrons trapping at the semiconductor-dielectric interface, for the Ta_2O_5-only sample two competing effects might be present (one *normal* and one *anomalous*). This observation led to the proposal of possibly tune the Al_2O_3/Ta_2O_5 relative dielectric composition, so to determine the condition for which the two competing effects cancel out each other. In the following Section 4.1.2 we will see how this idea was applied while planning the fabrication of a new batch of samples.

4.1.2 Fabrication process of new ROXFET devices

Based on the knowledge acquired from previously fabricated devices, we planned the fabrication of new samples. The goal of this new batch was to incorporate different ratios of Ta_2O_5 and Al_2O_3 in a bi-layer dielectric stack to evaluate the impact in ROXFET stability. We decided to employ the ALD technique due to the superior quality of the final devices, in terms of either reproducibility, electrical performances and radiation sensitivity. Also, for a more meaningful comparison, we decided to reproduce the identical ROXFET fabrication model that was already employed for previous devices.

As previously said, the new batch would feature a $100\,nm$ thick dielectric composed as a bi-layer stack of Ta_2O_5 and Al_2O_3 (Figure 4.4). A previous study by the research group at CEMOP department showed that the incorporation thin SiO_2 layer at the semiconductor/dielectric interface improved both dielectric reliability and device performances [25]. Instead of it, we decided to employ Al_2O_3 for two main reasons: first, in order to compare its performances with those already measured with SiO_2 and second, because Al_2O_3 has a higher static dielectric constant k (9 instead of 4.9 of SiO_2 [35]).

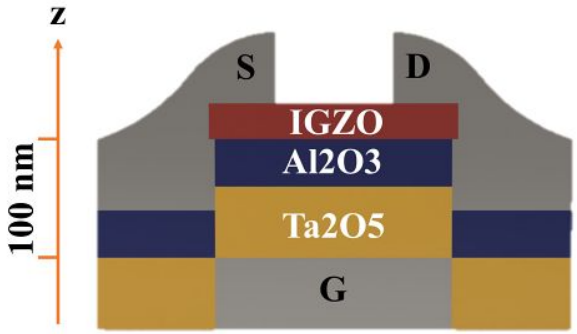

Figure 4.4: Representation of the vertical cross-section of a ROXFET device.

The Table 4.2 summarizes the fabrication we performed at CEMOP. We produced 5 pairs (10 samples total) of ROXFET devices varying the relative thickness of the two dielectric components, while keeping the rest of the process unchanged. We chose to fabricate pairs of (identical) samples in order to assess the reproducibility of the process.

Figure 4.5 shows one of the TFT devices at the end of the fabrication process.

Sample ID	Ta_2O_5 **thickness** (nm)	Al_2O_3 **thickness** (nm)
Ta20 (A,B)	20	80
Ta40 (A,B)	40	60
Ta60 (A,B)	60	40
Ta80 (A,B)	80	20
Ta100 (A,B)	100	-

Table 4.2: To assess reproducibility, we fabricated two identical samples (A,B) for each condition. Each sample contains 9 TFT devices. In the following, we will identify these samples, for example, as Ta20A - device 1.

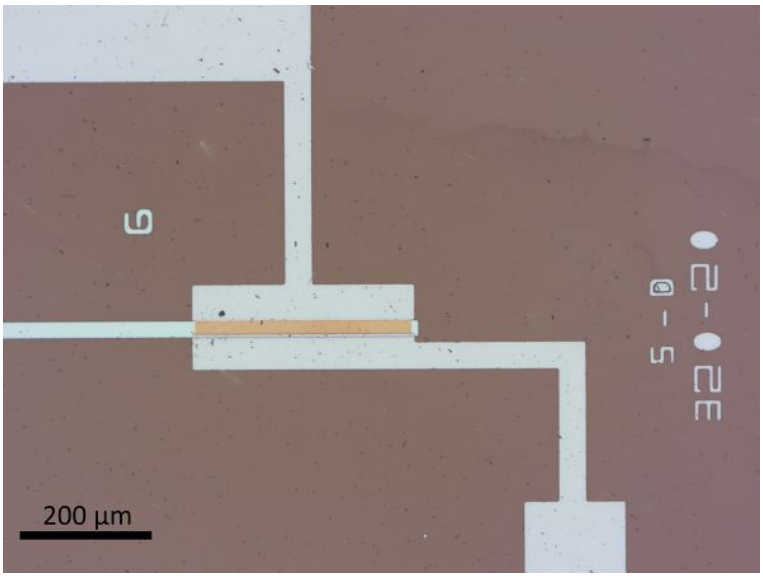

Figure 4.5: Optical microscope image of one of the devices at the end of the fabrication process.

4.1.3 Substrate preparation

We obtained the substrates by cutting $3 \times 3\,cm$ Corning Glass squares. Then, glass substrates followed a standard cleaning process, composed by:

- $10\,min$ Acetone ultrasonic bath,
- $10\,min$ Isopropyl alcohol (IPA) ultrasonic bath,
- Rinse in ultra pure water and blow dry with nitrogen flow,
- $20\,min$ baking on hotplate at $120°C$.

The two solvent baths and the final rinse guaranteed that the glass surface was free from dust and contaminants. Instead, the baking on hotplate ensured that the substrates were completely dry before moving to the next fabrication steps.

4.1.4 Photoresist patterning

In order to pattern each of the thin film layers we employed a Heidelberg Instruments μPG101 laser micro writer (Figure 4.6). The following Table 4.3 summarizes the parameters used in this fabrication step.

Figure 4.6: Heidelberg Instruments μPG101 laser micro writer employed for optical lithography.

Layer	**Photoresist type**	**Exposure parameters**
Gate	Negative (AZ nLof 2020)	$28\,mW$, 81% speed
Dielectric	Positive (AZ ECI 3012)	$34\,mW$, 90% speed
Semiconductor	Positive (AZ ECI 3012)	$22\,mW$, 90% speed
Source - Drain	Positive (AZ ECI 3012)	$22\,mW$, 90% speed

Table 4.3: Details on the photoresist patterning process. Common to all layers: $20\,mm$ write head, light filter OFF, unidirectional exposure mode.

During this thesis work we employed two different photoresists: the AZ ECI 3012 positive photoresist [36] and the AZ nLof 2020 negative photoresist [37]. Also, for both photoresists we used AZ 726 MIF as developer [38]. In order to deposit a $1.2\,\mu m$ thick photoresist layer, we employed a SUSS MicroTec spin coater (Figure 4.7) with the settings listed in Table 4.4.

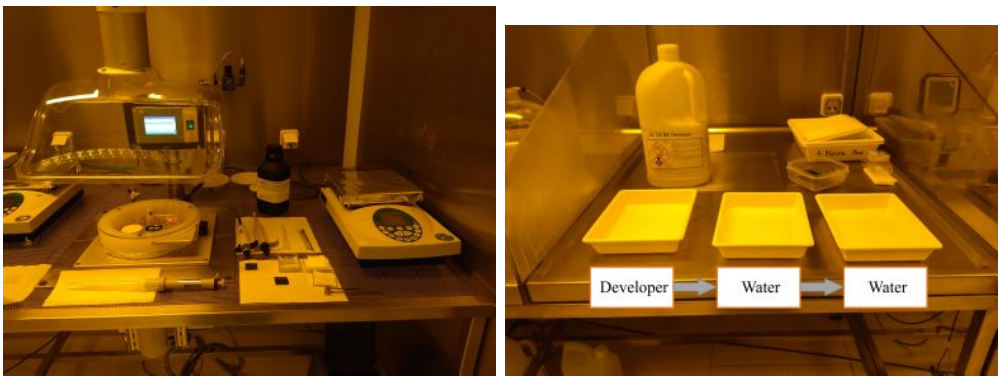

Figure 4.7: Instrumentation available at CEMOP clean room facility. On the left, photoresist spin coater and hotplate. On the right, photoresist development tools.

Layer	**Coating**	**Spin coater parameters**
Gate	Single	$30\,s$ @ $4000\,rpm$
Dielectric	Double	$10\,s$ @ $1000\,rpm$ + $20\,s$ @ $2000\,rpm$
Semiconductor	Single	$10\,s$ @ $2000\,rpm$ + $20\,s$ @ $4000\,rpm$
Source - Drain	Single	$10\,s$ @ $2000\,rpm$ + $20\,s$ @ $4000\,rpm$

Table 4.4: Details on the photoresist spin coating process. Common to all layers: $2000\,rpm/s$ acceleration.

For the AZ ECI 3012 positive photoresist we employed the following routine:

1. Resist spin coating (Table 4.4)
2. Soft baking on hotplate ($1\,min$ @ $90°C$)
3. Micro writer patterning (Table 4.3)

4. Baking on hotplate ($1\,min$ @ $110°C$)

5. Development in AZ 726 MIF bath ($\sim 80\,s$, then rinse in two ultra pure water baths and blow dry with nitrogen flow)

Similarly, for the AZ nLof 2020 negative photoresist we employed the following routine:

1. Resist spin coating (Table 4.4)

2. Soft baking on hotplate ($2\,min$ @ $110°C$)

3. Micro writer patterning (Table 4.3)

4. Baking on hotplate ($2\,min$ @ $110°C$)

5. Development in AZ 726 MIF bath ($\sim 40\,s$, then rinse in two ultra pure water baths and blow dry with nitrogen flow)

The only exception to the previous routines was when dealing with the dielectric's photoresist layer. Indeed, as the subsequent etching process would have been particularly damaging, we decided to increase the resist thickness. To do so, we repeated twice the steps 1-2 of the previous routine before moving to the patterning step. Furthermore, we increased the power of the micro writer laser source (Table 4.3) in order to properly expose the higher thickness layer.

After the development step, with the aid of an optical microscope we verified that the photoresist had been successfully patterned. Indeed, any residue might have compromised the following fabrication steps (as in Figure 4.8) and thus had to be removed by soaking the sample in the developer bath for few more seconds.

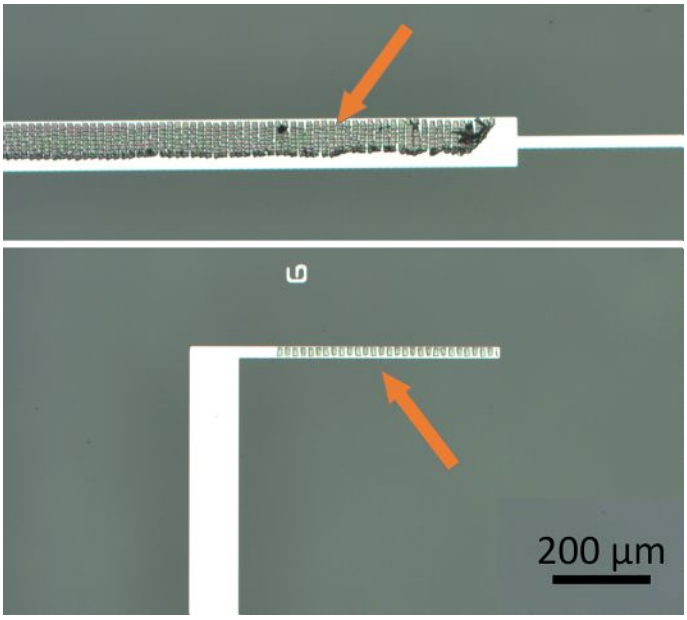

Figure 4.8: Optical microscope images of some positive photoresist residues after development.

4.1.5 Sputtering deposition

During the TFTs fabrication, we employed RF magnetron sputtering technique to deposit the Molybdenum electrodes (Gate, Source and Drain) and the a-IGZO semiconductor channel. At the CEMOP fabrication facility, we employed the two sputtering systems AJA ATC-1300F and AJA ATC 1800-S from AJA International (Figure 4.9) [39].

The deposition of the Molybdenum electrodes requested the following conditions:

- Chamber pressure: $1.7\,mTorr$ (plasma started at $20\,mTorr$)
- Target: Mo
- Gas flow: $50\,sccm\,Ar$
- Temperature: room temperature (no intentional substrate heating)
- Deposited thickness: $60\,nm$
- Pre-sputtering: Yes

Instead, we deposited the a-IGZO semiconductor layer with $2:1:1$ atomic ratio by operating the system under the following conditions:

- Chamber pressure: $2.3\,mTorr$ (plasma started at $20\,mTorr$)
- Targets: In_2O_3, Ga_2O_3, ZnO (co-sputtering)
- Gas flow: $14\,sccm\,Ar$, $2\,sccm\,O_2$
- Temperature: room temperature (no intentional substrate heating)
- Deposited thickness: $30\,nm$
- Pre-sputtering: Yes

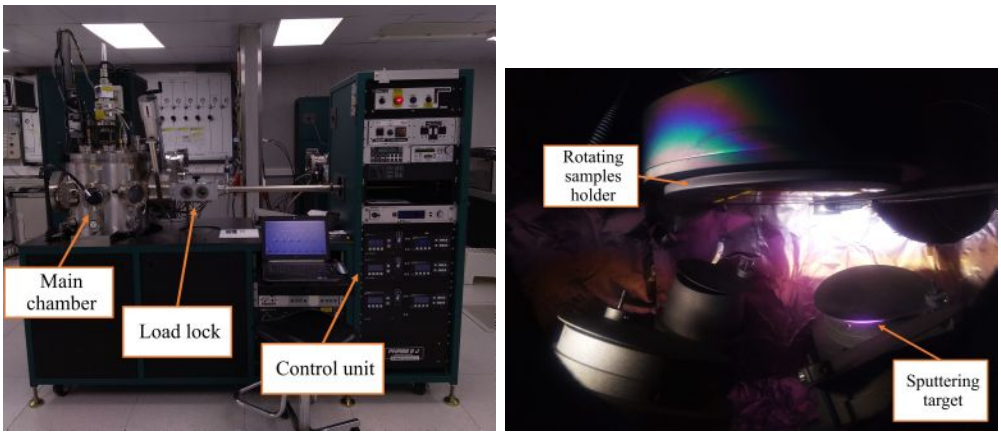

Figure 4.9: Instrumentation available at CEMOP clean room facility: AJA ATC 1800-S sputtering equipment (left) and detail of its main deposition chamber (right).

4.1.6 Atomic layer deposition

We employed the atomic layer deposition (ALD) technique to fabricate the dielectric layer. At the CEMOP fabrication facility, we employed a Beneq TFS 200 ALD system [40] (Figure 4.10). The information on the chemical reaction precursors that we employed are listed in Table 4.5.

Layer composition	**First precursor**	**Chemical formula**	**Growth rate**
Ta_2O_5	Tantalum(V) Ethoxide [41]	$Ta_2(OC_2H_5)_{10}$ (gaseous)	$0.556\,\mathring{A}/cycle$
Al_2O_3	Tri-methyl-aluminum [42]	$(CH_3)_3Al$ (liquid)	$1.053\,\mathring{A}/cycle$

Table 4.5: Summary of precursors employed during ALD fabrication. In both cases, we employed water (H_2O, liquid) at room temperature as second precursor.

The ALD process is highly automatized: the whole system follows a coded sequence of operations (the *recipe*), in which the user only has to tune the number of cycles required to reach the desired film thickness.

To deposit the Ta_2O_5 layer, we run the system under the following conditions:

- Precursor temperature: $160°C$
- Main chamber temperature: $225°C$
- ALD cycle: $200\,ms$ $Ta_2(OC_2H_5)_{10}$ pre-chamber load $\rightarrow$ $50\,ms$ wait $\rightarrow$ $200\,ms$ $Ta_2(OC_2H_5)_{10}$ pre-chamber release + $200\,ms$ line purge $\rightarrow$ $5000\,ms$ N_2 purge $\rightarrow$ $3000\,ms$ H_2O pulse $\rightarrow$ $5000\,ms$ N_2 purge.

Instead, to deposit the Al_2O_3 layer, we run the system under the following conditions:

- Precursor temperature: room temperature
- Main chamber temperature: $200°C$
- ALD cycle: $150\,ms$ TMA pulse $\rightarrow$ $650\,ms$ N_2 purge $\rightarrow$ $150\,ms$ H_2O pulse $\rightarrow$ $1000\,ms$ N_2 purge.

In each process, we simultaneously deposited (Figure 4.10):

- 2 ROXFET substrates (Mo layer on glass substrate, gate patterned),

- 4 test substrates (Mo layer on glass substrate, plain),
- 1 Si wafer fragment.

Figure 4.10: Instrumentation available at CEMOP clean room facility: Beneq TFS 200 ALD equipment[40] (left) and detail of some samples inside the main chamber (right).

We prepared the test substrates as phantoms of the real ROXFET samples. In this way, we could use these samples to perform trials of the following etching tests without damaging the final devices. In addition, the Si wafer fragment was used to carry out a quality check of the deposited thin film. Thanks to the homogeneity and the known properties of the Si surface, we used the Horiba-Jobin Yvon ellipsometer available at CENIMAT department (NOVA University) to measure the thickness of the deposited layer.

4.1.7 Etching

During this thesis work we employed several etching techniques, as reported in Table 4.6.

Layer	Etching technique
Gate	Plasma etching (SF_6)
Dielectric Ta_2O_5	Plasma etching (SF_6)
Dielectric Al_2O_3	Wet etching (H_3PO_4)
Semiconductor	Lift-off
Source - Drain	Lift-off

Table 4.6: Overview of the etching techniques employed for each deposited layer.

After the complete etching of the gate layer and the dielectric bi-layer of ROXFET samples, we removed residual photoresist with a $20\,min$ acetone bath on an oscillating plate (to facilitate resist dissolution without damaging the deposited layers), followed by a rinse in ultra pure water and drying with nitrogen flow. As the dry etching step hardens the photoresist layer, we sometimes observed residues under optical microscope. In such cases, we repeated the aforementioned process by re-soaking the samples in acetone and gently sweeping them with a brush.

Plasma etching

We employed a Trion PHANTOM III reactive ion etching (RIE) system [43] to perform dry etching of the Molybdenum gate layer and the Ta_2O_5 dielectric layer. According to numerous studies, RIE with SF_6 gas is the ideal process in terms of etching rate and quality for both Mo [44] and Ta_2O_5 [45] materials.

The RIE process on PHANTOM III is fully automatic, with the etching parameters easily selectable from the touchscreen interface. For both aforementioned layers, we operated the etching system under the following conditions:

- Pressure: $50\,mTorr$
- RIE radio frequency power: $60\,W$
- Gas flow: $10\,sccm\,SF_6$
- Temperature: room temperature

For the gate layer, the process time was approximately 300 s (0.2 nm/s etching rate). We then inspected each sample under optical microscope looking for Mo residues. Eventually, an extra 120 s process was enough to fully etch the sample. In this case, being the only layer on the substrate protected by photoresist, we did not need to accurately tune the process duration to prevent over-etching.

Instead, the etching of the Ta_2O_5 dielectric layer requested more attention, as the underlying Mo would have been compromised in case of over-etching. To determine the correct process time of each of the different Ta_2O_5 thickness configurations, we employed some test substrates (Figure 4.11) fabricated alongside the real ROXFET samples. By exposing only few lines at a time (while protecting the others with pieces of glass) we repeatedly tested various etching durations trying to identify the best condition. To determine whether the etching was complete, we placed the samples under optical microscope and measured the impedance of the patterned surface with a multimeter. Indeed, the ideal etch would fully remove the Ta_2O_5 layer without affecting the underlying conductive layer. Once found the proper process time, we then moved on to the real ROXFET samples. Table 4.7 summarizes the durations employed for this process.

Ta_2O_5 **thickness** (nm)	**Tested etching duration** (min)	**Proper etching duration** (min)
20	10	3
40	13	8
60	19	9.5
80	30	11.5
100	40	16.5

Table 4.7: Process times employed for the different Ta_2O_5 thicknesses. *Tested* refers to the values determined from test substrates, while *proper* refers to the ones actually used with real samples.

As clearly observable from Table 4.7, the process durations we utilized with real samples were much shorter than expected. This initially lead to some ROXFET samples being over-etched. We then drastically reduced the etching time, preferring to under-etch the samples and then achieve the final results by *smaller* etching steps.

We hypothesized that the observed discrepancy might be due to the fact that we employed normal glass as substrate for the test samples, while Corning glass for the real samples. Although precise data is unavailable, possible differences in both thermal properties and dielectric constants (on

which RIE depends) between the two glass types may have influenced the observed results.

Another issue we encountered during the trials on the test samples is evidenced in Figure 4.12. In some cases, a given etching process duration would lead to over-, proper and under- etching on the same sample. We could not relate this effect to the presence of shadow areas, as it randomly appeared over the exposed region.

As a final note, Table 4.4 explains why we employed a double layer photoresist when performing the dielectric patterning. Indeed, we wanted to ensure that the photoresist layer would have been thick enough to withstand the expected long dry etching processes.

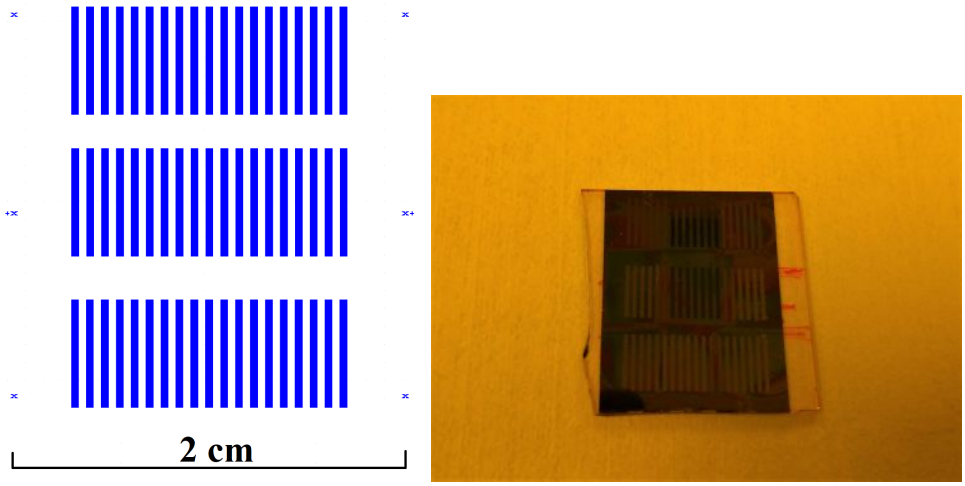

Figure 4.11: On the left, representation of the GDS model used to pattern the test substrate. So to obtain comparable results, we designed this pattern by repeating the main feature (electrical pads) to be etched on the real samples. On the right, a substrate that underwent multiple trials.

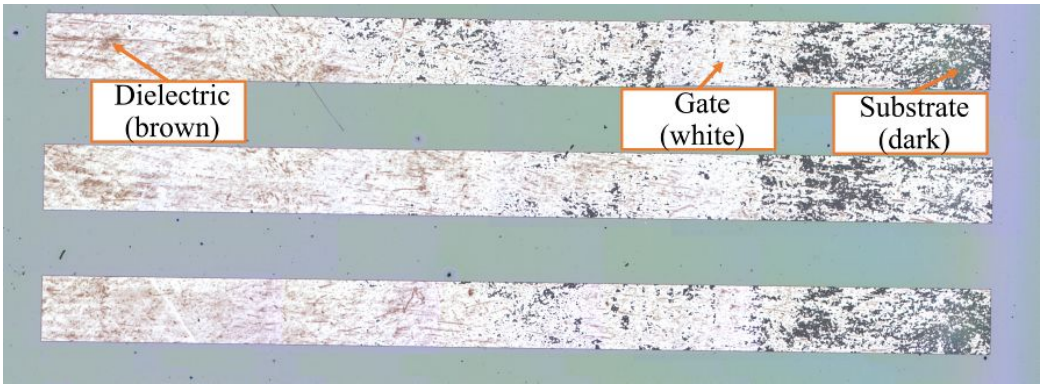

Figure 4.12: Optical microscope image of portion of a test sample after non-uniform dry etching. During a single etching cycle the sample was either under-etched (dielectric still present) and over-etched (underlying substrate exposed).

Wet etching

We employed wet etching to patter the Al_2O_3 layer in the dielectric. The process requires a Phosphoric acid (H_3PO_4) bath kept on a hotplate at $80°C$, and is based on the chemical reaction:

$$Al_2O_3 + 6\,H^+ \rightarrow 2\,Al^{3+} + 3\,H_2O \tag{4.1}$$

which is a surface reaction-limited process, proportional to the first order to $[H^+]$ and with $52\,kJ/mol$ activation energy [46].

Once the H_3PO_4 bath placed on a hotplate had reached the desired temperature, we soaked the samples for $8\,min$. Then, we immediately rinsed them with ultra pure water to interrupt the chemical reaction and blow dried with nitrogen flow.

We determined the process time by performing some tests on the same substrates presented in Figure 4.11. To assess whether the Al_2O_3 layer was successfully etched, we performed a visual comparison using an optical microscope. Indeed, being the Al_2O_3 layer deposited on top of another dielectric layer, we could only rely on the colour change induced by the etching (Figure 4.13). Since the underlying Ta_2O_5 layer was not affected by H_3PO_4 and no damage to the devices would occur in case of undercutting, we decided to fix the process duration to the amount of time require to etch the maximum Al_2O_3 thickness among the samples.

Once completed this etching process, we then performed the dry etching to remove the remaining dielectric layer.

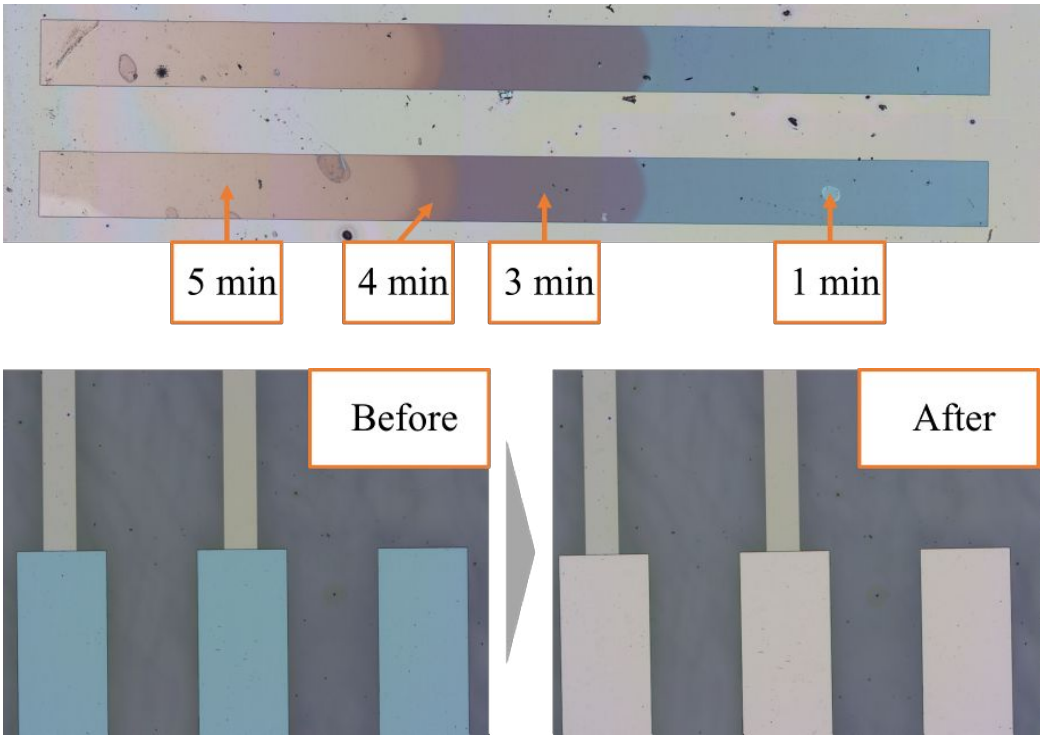

Figure 4.13: Optical microscope images highlighting the effect of wet etching on the Al_2O_3 dielectric layer.

Lift-off

We used lift-off to pattern both the semiconductor and the top electrodes (source and drain) layers. The choice of this technique aimed at preventing over-etching damage to the underlying layers.

To perform this technique we employed an Acetone bath at room temperature (Figure 4.14), in which we soaked the samples for approximately one hour. To facilitate the stripping of the photoresist flakes, we gently swept the samples with a brush when still inside the acetone bath. Then, in order to remove any residue, we moved the samples to an Isopropyl alcohol bath for approximately $30\,min$ and then rinsed with ultra pure water.

However, completed this process, most of the samples were still presenting residues that would have compromised the proper device functionality (Figure 4.15). Thus, we attempted to remove such residues by employing a photoresist stripper (Technistrip P 1316 [47]) bath at $70°C$. This step partially advanced the lift-off process, but did not succeed in fully strip the residues potentially affecting the devices. Ultimately, aided with an optical

microscope, we gently brushed the devices area with a cotton swab soaked in Acetone.

As a comparison, previous fabrications carried out by researchers at CEMOP department only requested an Acetone bath to successfully strip the photoresist layer. This fabrication step might have been damaging for the patterned structures, potentially introducing defects in the semiconductor and dielectric layers.

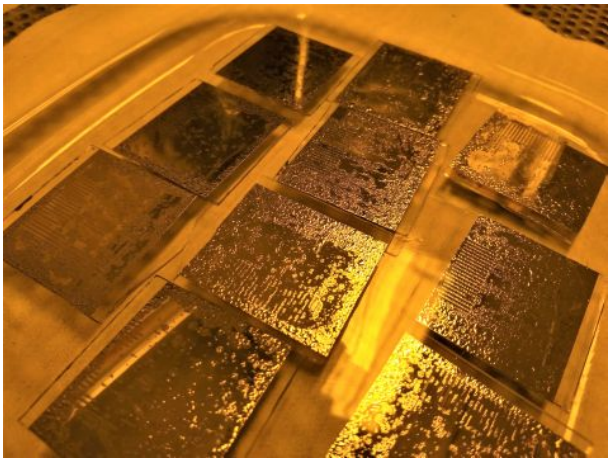

Figure 4.14: Samples in acetone bath during lift-off of the source-drain layer.

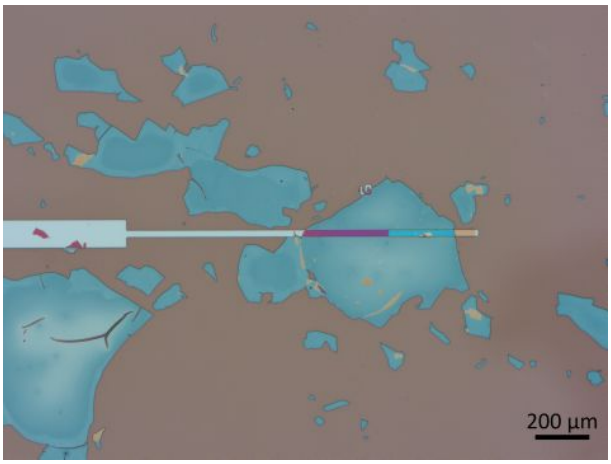

Figure 4.15: Optical microscope image of photoresist residues during semiconductor lift-off. A large resist flake covers the area of one of the devices.

4.1.8 Thermal annealing

After the semiconductor patterning we performed a rapid thermal annealing (RTA) of the samples with the AnnealSys AS-ONE RTA system [48]. The RTA process is highly automatized: once the samples are in place (Figure 4.16), the system carries out the protocol planned by the user.

We operated the thermal annealing system under the following conditions:

- Environment: air, at ambient pressure
- Annealing: $10\,min\,@\,180°C$
- Annealing protocol: Pre-heat to $50°C$ $\rightarrow$ Annealing ($100°C/s$ ramp) $\rightarrow$ Cool down to $75°C$, then to room temperature

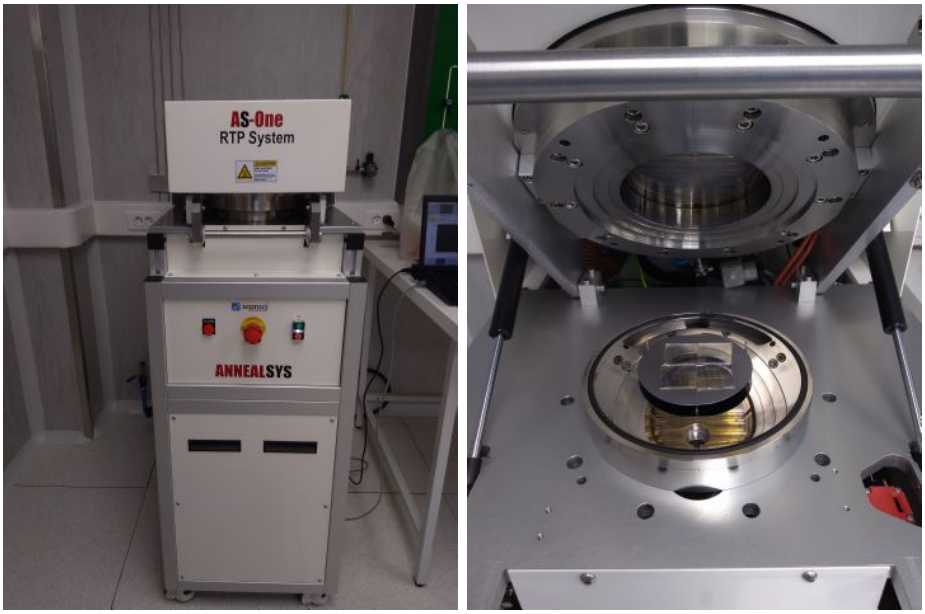

Figure 4.16: On the left, AnnealSys AS-ONE RTA system at CEMOP fabrication facility. On the right, detail of some samples inside the annealing chamber.

4.1.9 Electrical characterization of the newly fabricated devices

Completed the fabrication, we brought the samples to Physics and Astronomy department at the University of Bologna to perform the electrical characterization and radiation sensitivity tests. To perform these measurements, we employed the same techniques already used for the previously fabricated samples. In the following, we will go through the results obtained from the electrical characterization, while other results will be presented in the following sections.

The main results of the electrical characterization of the newly fabricated batch are shown in Figures 4.17 and 4.18, while Figure 4.19 presents the measured leakage currents. Furthermore, an overview of the experimental values obtained for the best performing device in each sample is reported in Table 4.8.

Sample	log_{10} **Leakage**	**On/off ratio**	**V threshold** (V)	**Mobility** $(cm^2/V \cdot s)$	**Sub-threshold slope** (V/dec)
Ta20A	-10	5	1.0	12	0.1
Ta20B	-7	5	0.9	14	0.2
Ta40A	-7	5	0.1	13	0.1
Ta40B	-3	3	0.1	14	0.4
Ta60A	-10	6	0.2	15	0.1
Ta60B	-10	5	0.1	13	0.1
Ta80A	-10	5	0.4	13	0.1
Ta80B	-10	6	0.4	13	0.1
Ta100A/B	-	-	-	-	-

Table 4.8: Overview of the electrical performances of the newly fabricated batch. Values reported are those for the best performing device in each sample.

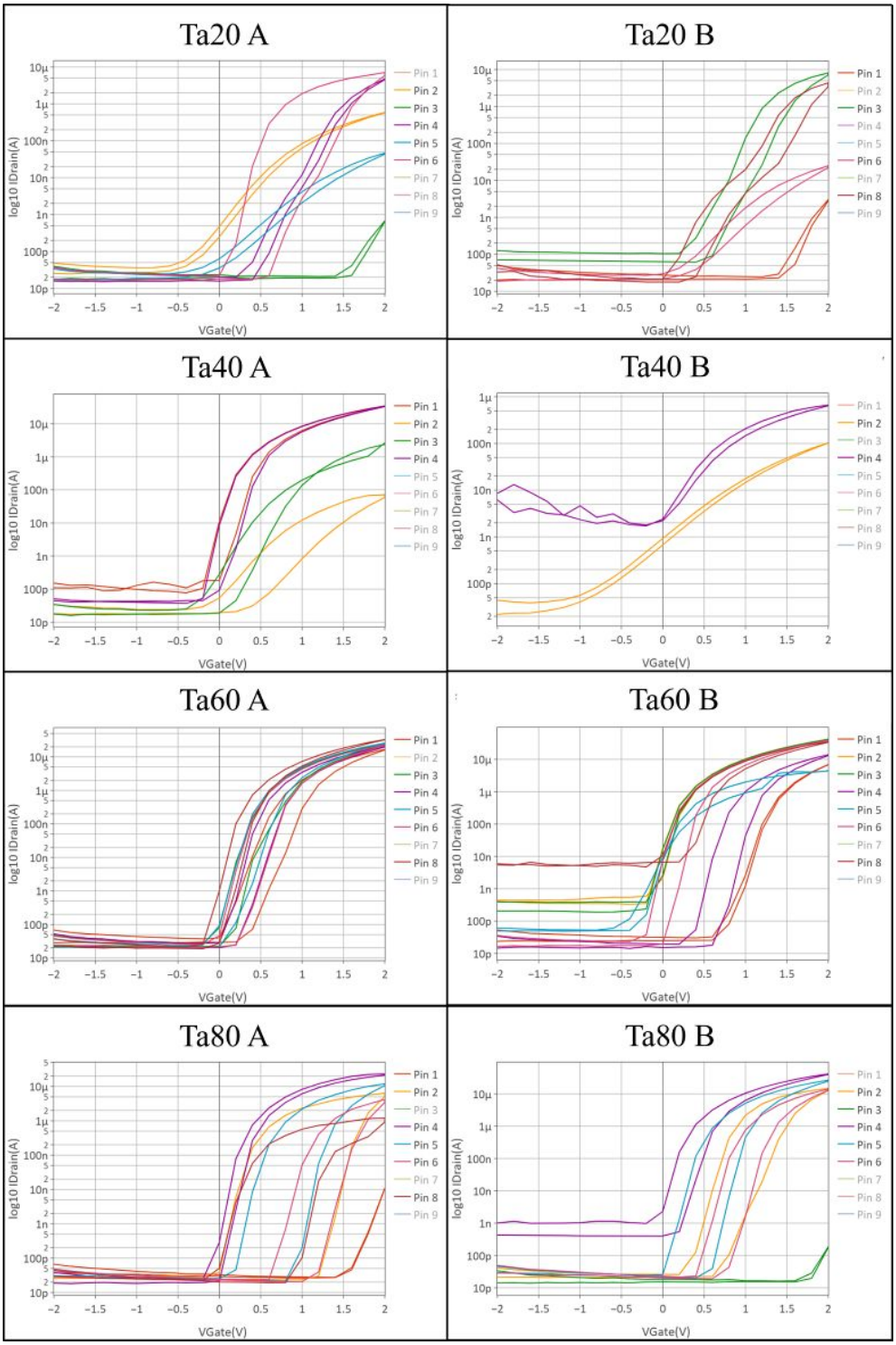

Figure 4.17: Overview of the transfer characteristics in saturation regime ($VD = 3\,V$), log_{10} scale.

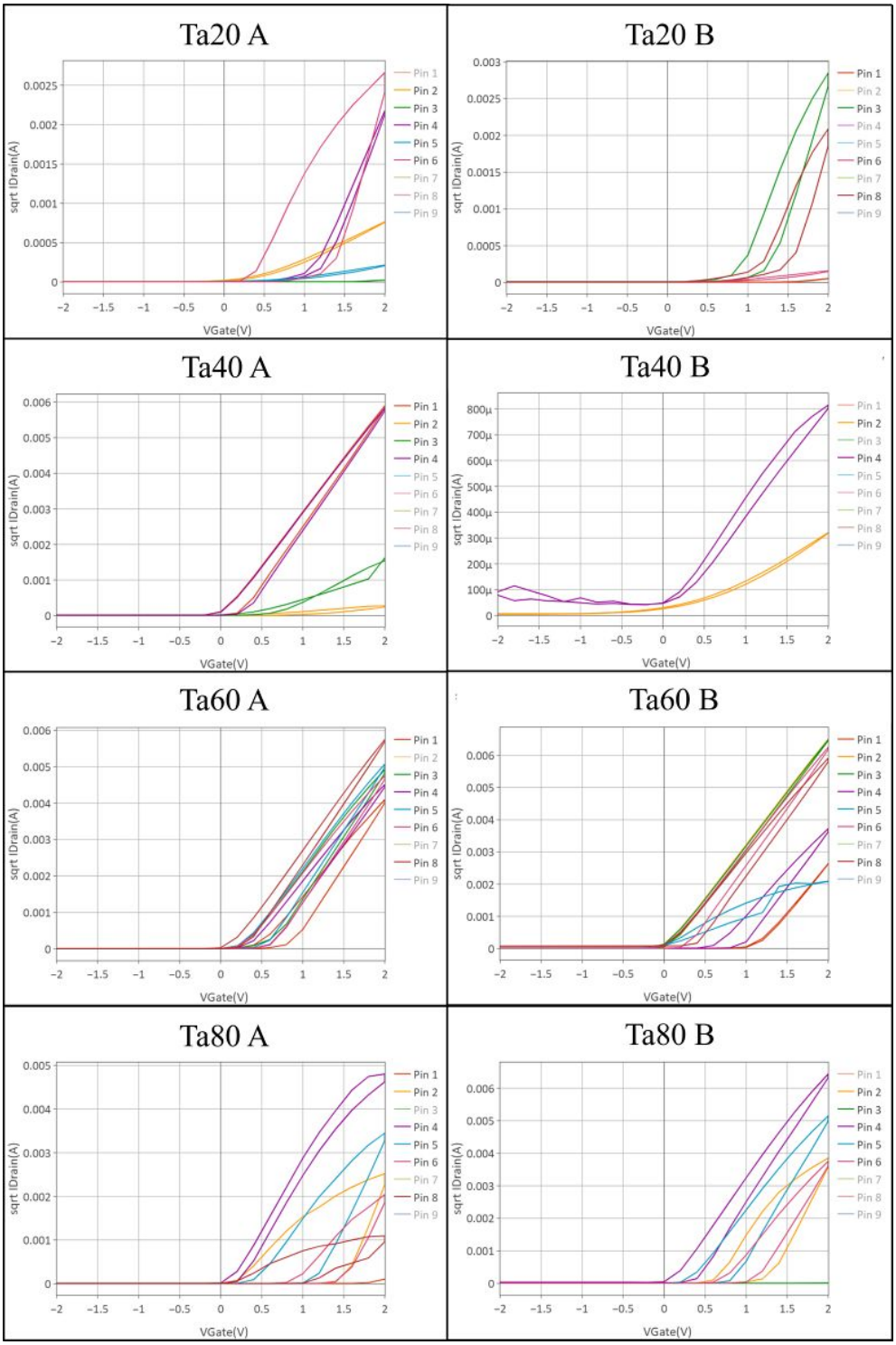

Figure 4.18: Overview of the transfer characteristics in saturation regime ($VD = 3\,V$), square root scale.

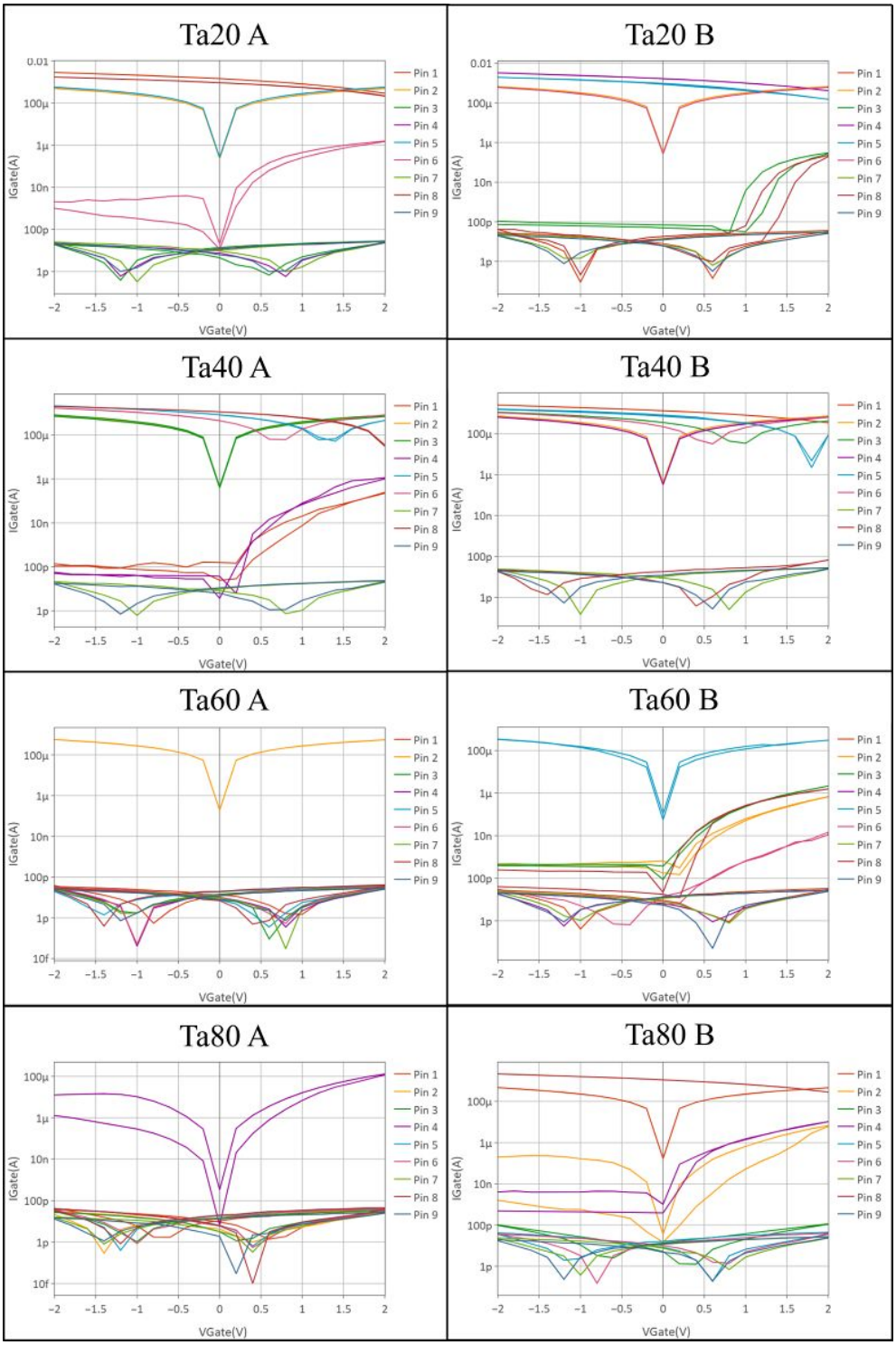

Figure 4.19: Overview of the leakage currents ($VD = 3\,V$), log_{10} scale.

As Figure 4.20 summarizes, most of the devices were not showing a transistor-like behaviour and, among those working, very few presented acceptable leakage currents for practical applications. Although less statistically significant, we can conclude that the *working* devices were compatible with what previously observed on ALD fabricated samples: a threshold voltage between $0\,V$ and $1\,V$ and leakage currents below the nA. Instead, only Ta60A partly shows the reproducibility we expected from ALD. Finally, we may notice that all devices have large hysteresis, which reduces after 2-3 measurement cycles as previously experienced with other TFT devices.

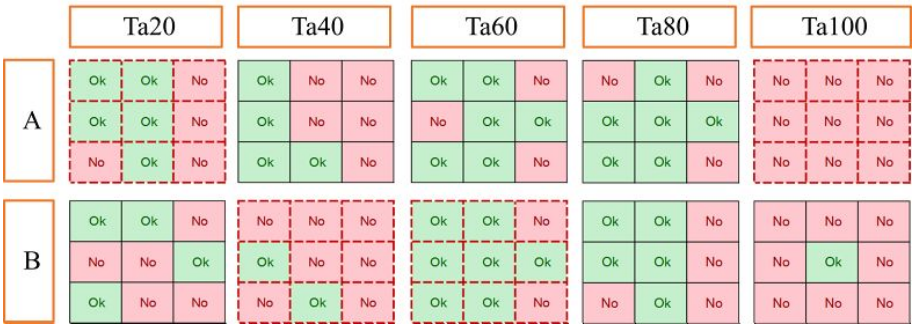

Figure 4.20: Overview of the devices showing a transistor-like behaviour (schematic representation of the 3×3 devices matrix in each sample). However, due to high leakage current, not all of the samples marked as *working* could have a practical application. The samples with red dashed border are those that suffered over-etching during the fabrication process.

4.2 Extraction of conduction band tail DOS from C-V measurements

4.2.1 C-V measurements on previously fabricated batch

We performed C-V characterization measurements on selected devices from ALD LO and ALD Etch samples. For these measurements, we employed a Lock-in amplifier in the setup previously discussed (Figure 3.2).

We acquired multiple C-V characteristics under the following conditions:

- Gate DC offset: sweep from $-5\,V$ to $5\,V$ during each measurement
- Gate AC signal: $10\,mV_{RMS}$, fixed frequency from $10^2\,Hz$ to $10^6\,Hz$ (acquired 3 measurements per decade)

Actually, as we provided both the AC signal and the DC offset to source-drain short circuited (instead of the gate), to obtain the final results we simply had to reverse the sign of the gate voltage. Furthermore, we verified that the phase of the response to the AC signal was always close to 90°, as expected from a capacitor behaviour. These results, an example of which is represented in Figure 4.21, allowed us to extract a dielectric capacitance of $(200 \pm 5)\,nF/cm^2$ for both ALD LO and ALD Etch samples.

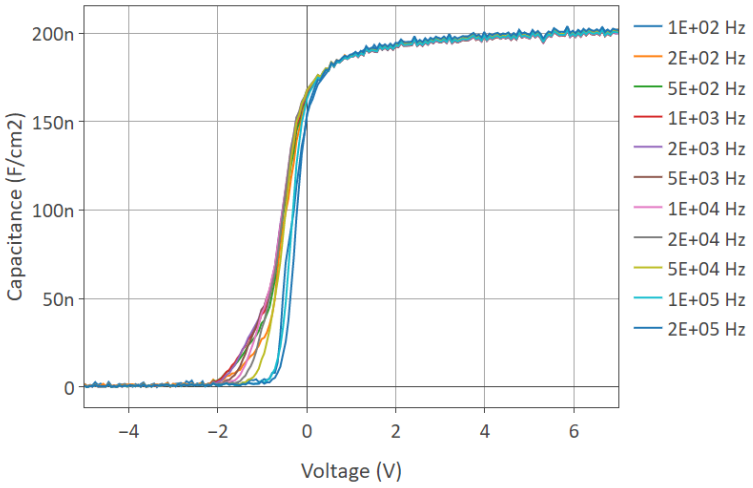

Figure 4.21: Multifrequency C-V data extracted at multiple frequencies for ALD Etch, device 6 sample.

Following the procedure discussed in Appendix A.1, we also employed these data to calculate the density of states (DOS) inside the channel's semiconductor. We will then compare these results with those extracted from KPFM analysis (Section 4.3.1).

Figure 4.22 shows the DOS calculated for a device on the ALD Etch sample. Each line in the plot is associated to the specific frequency of the AC signal at which it was measured. According to this analysis, the density of states starts to increase between $-1\,eV$ and $0\,eV$, reaching its maximum around $1.5\,eV$. Also, we can notice that most of the curves show an initially curved trend, indicating the presence of states at low energies. This effect, as can be explained from Figure A.1, is linked with the feature seen in the capacitance plot between $-2\,V$ and $0\,V$ (Figure 4.21).

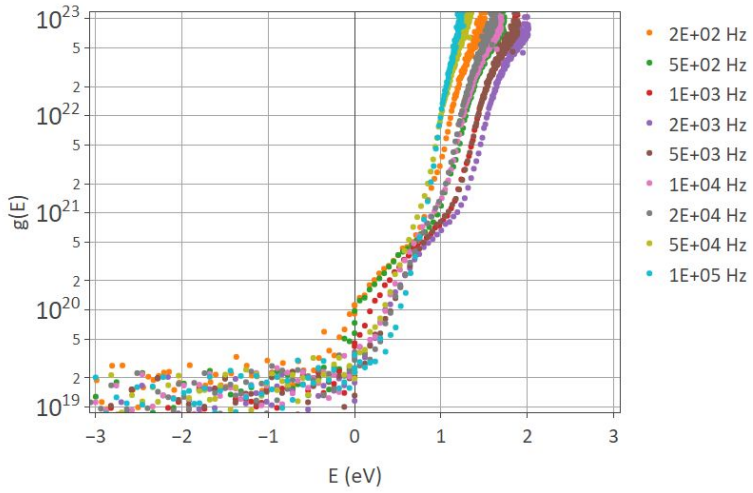

Figure 4.22: Density of states calculated from multi-frequency C-V measurements on ALD Etch sample, device 6.

4.2.2 C-V measurements on newly fabricated batch

We also performed C-V characterization measurements selecting one working device available for each different configuration. For these measurements, we employed a Lock-in amplifier in the setup previously discussed (Figure 3.2).

Analogously to what did before, we acquired multiple C-V characteristics under the following conditions:

- Gate DC offset: sweep from $-5\,V$ to $5\,V$ during each measurement, eventually adapted so to better fit full C-V characteristic
- Gate AC signal: $10\,mV_{RMS}$, fixed frequency from $10^2\,Hz$ to $10^6\,Hz$ (acquired 3 measurements per decade)

Also in this case, we reverse the sign of the gate voltage as we provided both the AC signal and the DC offset to source-drain. Furthermore, we verified that the phase of the response to the AC signal was always close to 90°, as expected from a capacitor behaviour. These results, an example of which is represented in Figure 4.23, allowed us to extract the capacitances listed in Table 4.9.

Sample ID	**Capacitance** (nF/cm^2)
Ta20	70
Ta40	90
Ta60	110
Ta80	140
Ta100	Not measured

Table 4.9: Capacitances calculated, for each different fabrication condition, by averaging the C-V characteristics acquired. The associated uncertainty is $\pm\,10\,nF/cm^2$.

Following the procedure discussed in Appendix A.1, we also employed these data to calculate the density of states (DOS) inside the semiconductor before exposing the ROXFET devices to any ionizing radiation. Then, maintaining a conceptually identical setup, we irradiated each sample with a $200\,mGy$ X-ray dose (peak at $150keV$) using a Hamamatsu microfocus X-ray source. Immediately afterwards we performed again the same C-V characterization procedure, which enabled us to determine the DOS in the semiconductor after irradiation.

The comparison between pre- and post- irradiation DOS is shown in Figures 4.24, 4.25, 4.26 and 4.27. In the case of the Ta20A sample (Figure

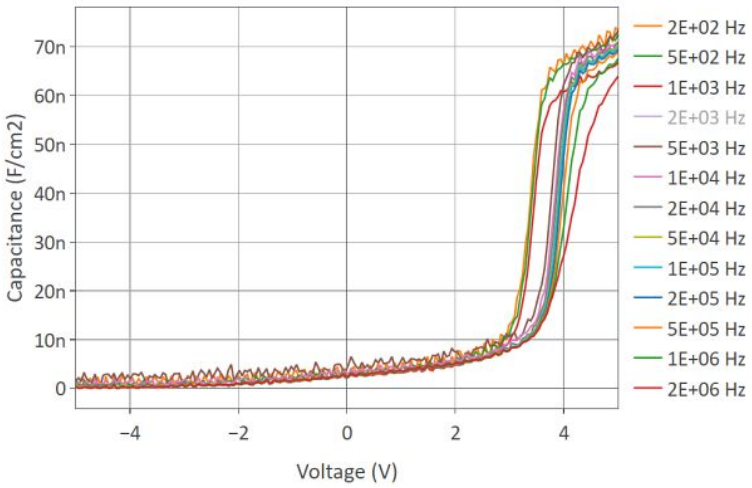

Figure 4.23: Example of C-V data extracted at multiple frequencies for Ta20A, device 1 sample.

4.24), we observed that the exposure to X-rays induced a shift towards higher energies of the density of state. Instead, in all other cases, the irradiation induced a shift of the DOS towards lower energies. In some cases, such as Ta40A (Figure 4.25) and Ta60A (Figure 4.26), we can also notice a change in the shape of the distribution, with a bowing feature appearing right before the onset of the DOS growth.

The increased DOS at lower energy is consistent with the increase in channel conductivity that we normally expected upon irradiation. As we will see in Section 4.3, the anomalous behaviour of the Ta20 sample will also be confirmed from radiation sensitivity measurements.

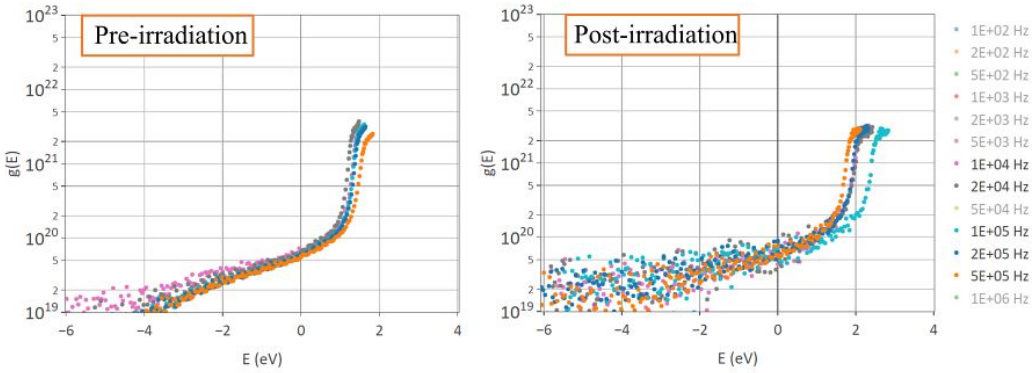

Figure 4.24: Density of states calculated pre- and post- irradiation. The DOS is shifted towards higher energies. (Reference: Ta20A, device 4)

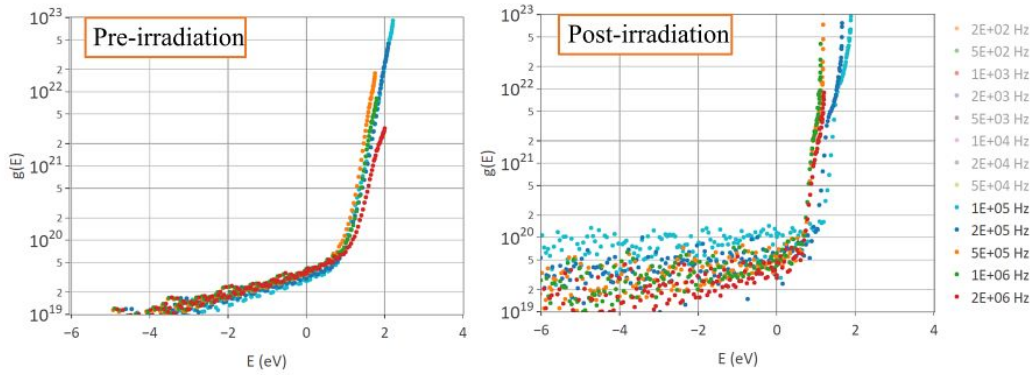

Figure 4.25: Density of states calculated pre- and post- irradiation. The DOS is shifted towards lower energies. (Reference: Ta40A, device 1)

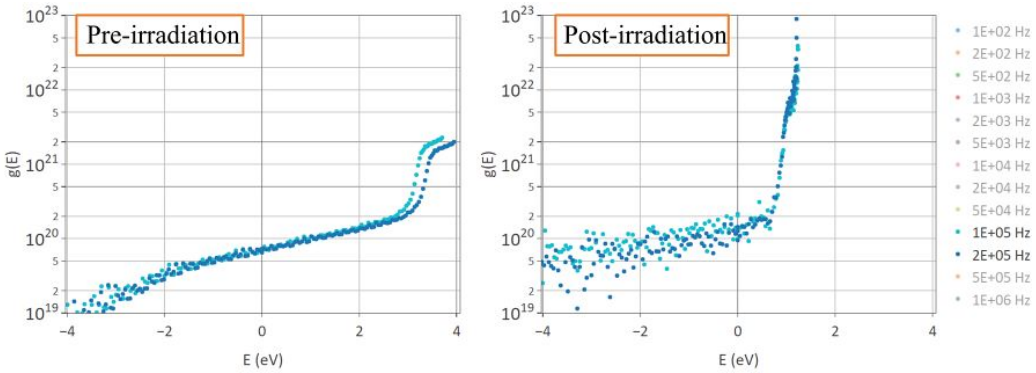

Figure 4.26: Density of states calculated pre- and post- irradiation. The DOS is shifted towards lower energies. (Reference: Ta60A, device 8)

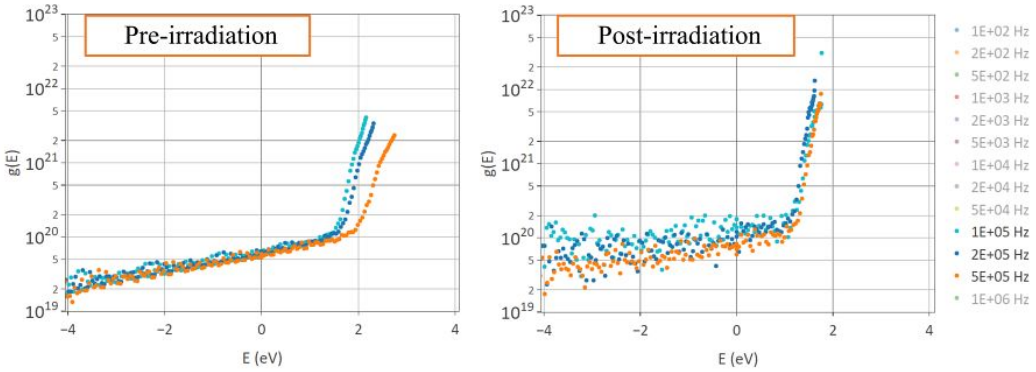

Figure 4.27: Density of states calculated pre- and post- irradiation. The DOS is shifted towards lower energies. (Reference: Ta80A, device 5)

4.3 Impact of oxide semiconductor thin film architecture on radiation detection properties

4.3.1 Overview of the compared TFT structures and their electrical performance data

Part of this thesis work consisted in performing the characterization of a previously fabricated batch of ROXFET samples, proceeding as presented in Chapter 3. These experimental devices had been manufactured by researchers at the CEMOP facility of the NOVA University of Lisbon and then provided to the Physics and Astronomy department of the University of Bologna. Once performed the full electrical and radiation sensitivity characterization, we leveraged this knowledge to plan the fabrication of a new batch that would use the most effective techniques.

The previously fabricated batch consisted of 8 samples, patterned by direct laser writing according to the ROXFET prototype layout (Figure 4.28). Each sample contained a 3×3 matrix of TFTs with a staggered bottom gate structure. As visible from the model, each transistor had its own gate and drain electrical contacts, while the source contact was common to all the 9 devices. Moreover, the model features some test structures useful to investigate eventual faults that may have occurred during the fabrication process.

The structure of the TFTs in this batch consisted of:

- $60\,nm$ Molybdenum gate;
- $380\,nm$ $TaSiO$ multilayer dielectric, deposited by magnetron sputtering at room temperature
  - or -
  $100\,nm$ Ta_2O_5 single layer dielectric, deposited by ALD at $200°C$;
- $30\,nm$ Indium-gallium-zinc-oxide (IGZO) with 2:1:1 atomic ratio semiconductor layer, deposited by co-sputtering at room temperature and patterned by lift-off;
- $60\,nm$ Molybdenum source-drain;
- Parylene-c passivating layer (only 4 samples), deposited by chemical vapour deposition techniques.

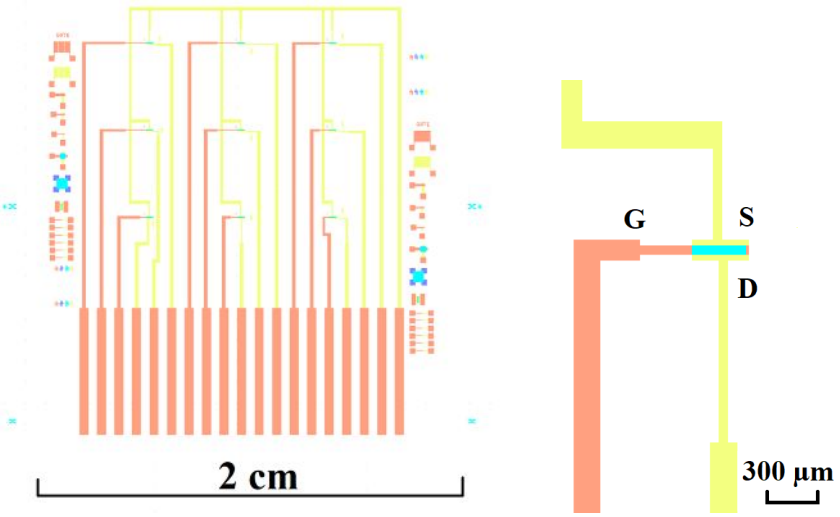

Figure 4.28: On the left, representation of the GDS model used to pattern the ROXFET matrix. On the right, detail of one of the transistors.

The differences among the samples, and their identification names, are presented in Table 4.10.

Sample	Dielectric	Source-drain	Passivation
Etch	$TaSiO$ sputtered	RIE (SF_6)	-
LO	$TaSiO$ sputtered	Lift-off	-
Etch 1g	$TaSiO$ sputtered	RIE (SF_6)	$650\,nm$
LO 1g	$TaSiO$ sputtered	Lift-off	$650\,nm$
Etch 2g	$TaSiO$ sputtered	RIE (SF_6)	$1300\,nm$
LO 2g	$TaSiO$ sputtered	Lift-off	$1300\,nm$
ALD Etch	Ta_2O_5 ALD	RIE (SF_6)	-
ALD LO	Ta_2O_5 ALD	Lift-off	-

Table 4.10: Overview of the differences that distinguish each sample. All samples were also submitted to RTA in air after IGZO patterning ($180°C$, $100°C/s$ heating ramp).

Electrical characterization

The main results of the electrical characterization of the previously fabricated batch are shown in Figure 4.29. Furthermore, an overview of the experimental values obtained is reported in Table 4.11.

Sample	log_{10} **Leakage**	**On/off ratio**	**V threshold** (V)	**Mobility** $(cm^2/V \cdot s)$	**Sub-threshold slope** (V/dec)
Etch	-9.6	6.4	-1.1	5.3	0.5
LO	-10	6.9	-1.7	6.0	0.25
Etch 1g	-10.3	6.6	-1.8	5.7	0.5
LO 1g	-9.9	7.0	-1.3	5.1	0.3
Etch 2g	-10.2	6.3	-3.0	2.7	0.5
LO 2g	-9.8	6.7	-2.4	5.0	0.3
ALD Etch	-10	4.3	-1.5	8.1	0.3
ALD LO	-10.4	5.3	-0.3	8.4	0.2

Table 4.11: Overview of the electrical performances of the previously fabricated batch.

Overall, the samples showed good electrical performances in terms of low leakage currents and high on/off ratio. As negative aspects, most of the devices exhibit some hysteresis while few also had high leakage currents. Also, the LO 1g sample had only 4 over 9 working devices.

Of particular interest are the data regarding ALD LO sample, fabricated with a combination of the ALD and lift-off techniques. It is particularly evident the superiority of this sample, given the excellent reproducibility among devices, the $V_{th} \approx 0\,V$, the absence of hysteresis and the lowest sub-threshold slope. All these condition render the ALD LO the ideal candidate for several reasons. Firstly, a good reproducibility is desirable from the perspective of a final application into a radiation detection device, which requires a calibration and has to be reliable. Secondly, the threshold voltage close to $0\,V$ allows the device to be operated at low voltage, simplifying the integration into a detector. Finally, as the readout of a ROXFET device is ultimately based on a resistance measurement, the combination of low leakage current, no hysteresis and a small sub-threshold slope would, in principle, provide a high accuracy result.

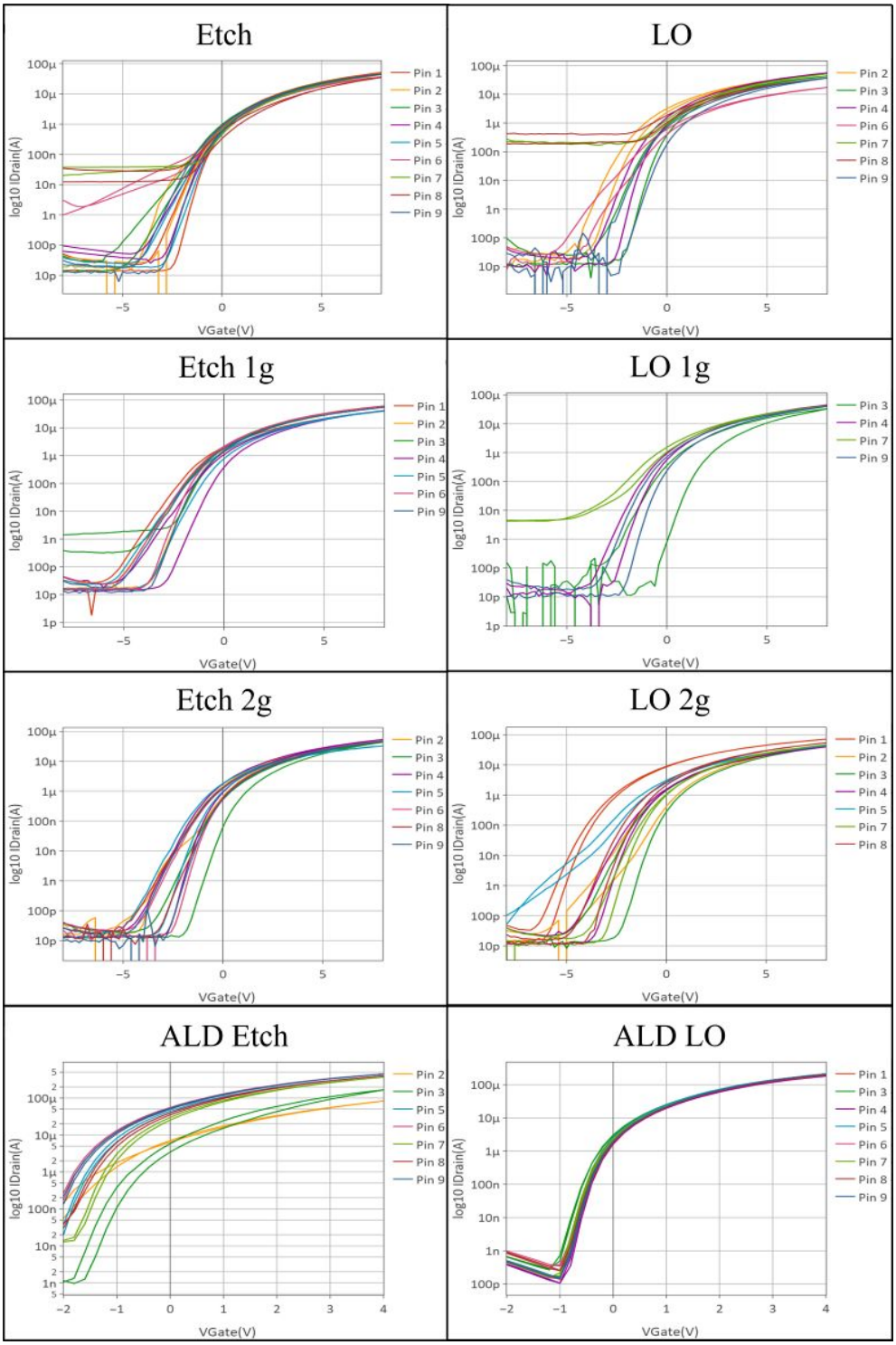

Figure 4.29: Overview of the transfer characteristics in saturation regime ($VD = 3\,V$), log_{10} scale.

KPFM measurements

We performed KPFM experiments on the ALD LO and ALD Etch samples with the setup presented in Section 3.2. We mounted on the AFM system a NSC36 Cr/Au tip, using its B cantilever at $96.1\,kHz$ frequency and $16.5\,nm$ amplitude set-points.

After having made all the electrical connections and tuned the AFM parameters, we acquired KPFM images of a $30 \times 30\,\mu m$ area on the semiconductor surface of one of the TFTs. We selected an AC modulation of the tip bias at $17\,kHz$ and with $2\,V$ amplitude. All the images were acquired while the transistor was operating in linear regime ($V_D = 0.5\,V$ and V_G between $-3\,V$ and $6\,V$) or in saturation regime ($V_D = 6\,V$ and V_G between $-2\,V$ and $5\,V$).

Figure 4.30 shows the KPFM image acquired when all the TFT electrodes were connected to ground. By averaging over the image lines, we observed an average surface potential difference between semiconductor and electrodes of $(0.15 \pm 0.07)\,V$. Thus, we can expect this offset to be present in all later measurements.

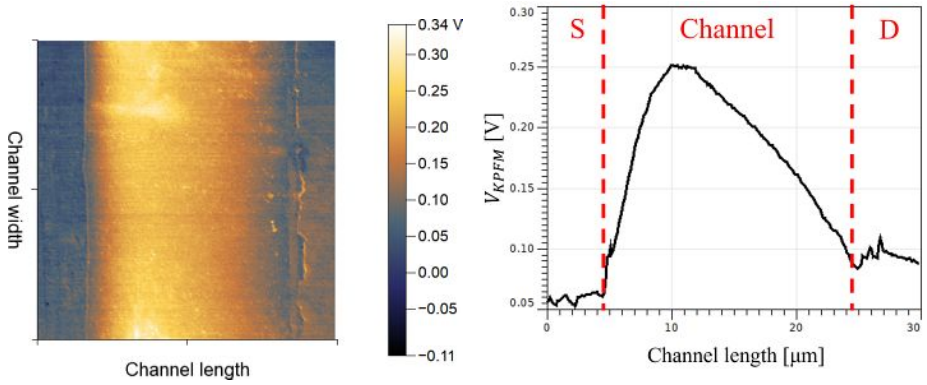

Figure 4.30: On the left, KPFM image acquired at $V_G = V_D = V_S = 0\,V$. On the right, surface potential profile averaged over the channel length.

Figures 4.31 and 4.32 compare the surface potential measured in linear and saturation regime, respectively at $V_G = 0\,V$ and $V_G = 4\,V$. In both cases, from the false-colour scale we can observe the typical trend of a TFT in the two regimes. Indeed, the linear condition tends to have a uniform charge distribution in the channel region. Instead, in the saturation regime it is clearly observable the distribution gradient, with the depletion region next to the drain electrode causing the *pinch-off* of the channel.

During our measurements, one of the TFT devices broke down probably after some interaction with the AFM tip. We later acquired the KPFM

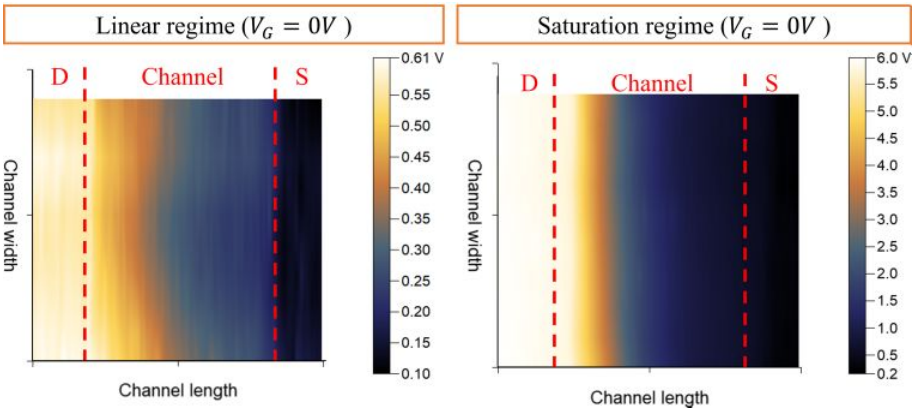

Figure 4.31: KPFM images acquired in linear ($V_D = 0.5\,V$) and saturation ($V_D = 6\,V$) regimes when $V_G = 0\,V$. Reference: ALD Etch sample, device 6.

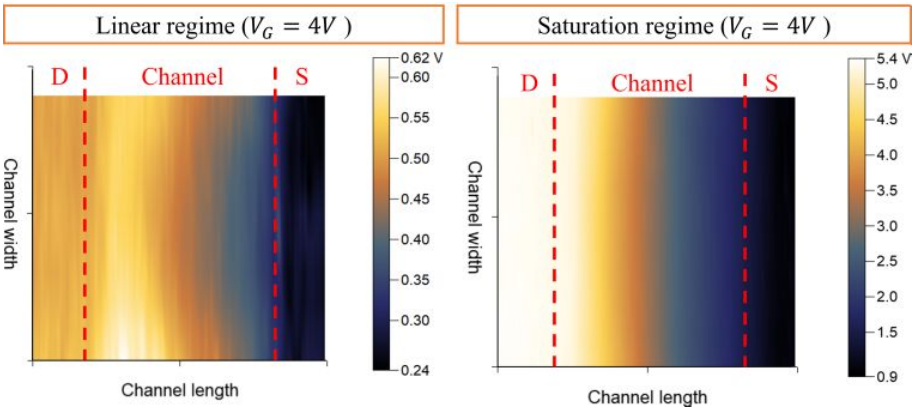

Figure 4.32: KPFM images acquired in linear ($V_D = 0.5\,V$) and saturation ($V_D = 6\,V$) regimes when $V_G = 4\,V$. Reference: ALD Etch sample, device 6.

image in Figure 4.33, in which the defect point is clearly visible.

Following the procedure presented in Section 3.2, we also employed KPFM measurements to extract the density of states in the semiconductor channel. For these measurements, the AFM system was able to control the gate bias, while source and drain were connected to ground. We acquired KPFM images as $1 \times 50\,\mu m$ stripes oriented parallel to the channel width and horizontally centred on it. At each pixel along the stripe, the AFM system measured the surface potential while sweeping V_G between $-3\,V$ and $3\,V$ (Figure 4.34). Then, we extracted the DOS plot in Figure 4.34 employing a Matlab analysis script, prepared by prof. Tobias Cramer according to Equation 3.11.

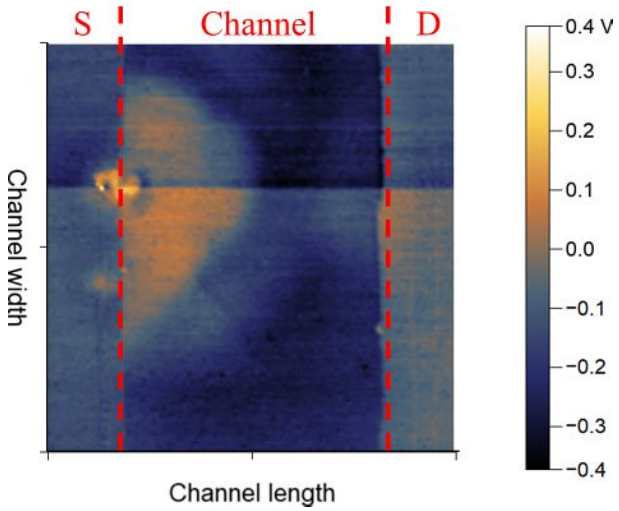

Figure 4.33: KPFM image of a damaged TFT device. Reference: ALD LO sample, device 9.

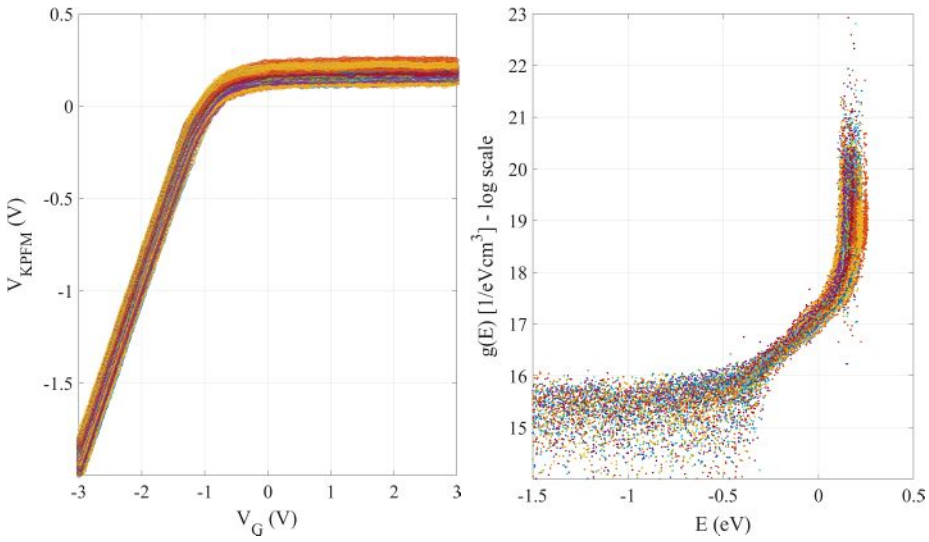

Figure 4.34: On the left: surface potential, acquired as function of the gate voltage, for several positions along the channel. On the right: extracted density of states. Reference: ALD Etch sample, device 6.

Observing the $V_{KPFM}(V_G)$ plot it is possible to notice that, when V_G is below the threshold voltage of the transistor, no charge accumulates inside the channel and the potential seen by the AFM tip is proportional to V_G itself. Instead, as the gate bias increases, charges start to accumulate inside the semiconductor, screening the field generated at the gate.

From the density of states plot, we can observe that the initial DOS is around $10^{16}\,eV^{-1}cm^{-3}$, and that the trend has an increase starting around $-0.3\,eV$. As a comparison, the results obtained from C-V measurements on the same sample (Section 4.2.1) indicated an initial DOS around $10^{19}\,eV^{-1}cm^{-3}$, with an increase starting in the range $[-1; 0]\,eV$ and reaching its maximum when above $1\,eV$. Although the outcomes of the two techniques are not compatible, it is important to notice that between the acquisition of the two datasets several factors may have affected the DOS (exposure to light and ionizing radiation, thermal effects, etc.).

4.3.2 Radiation exposure protocols and results

Radiation sensitivity measurements on previously fabricated batch

After having assessed the electrical characteristics of the ROXFET devices, we measured their radiation detection performances. During our tests, we employed the same setup employed for the electrical characterization (Figure 3.1), plus one of the two ionizing radiation sources: a Mo target based X-ray tube or a Hamamatsu micro focus source. The former was able to provide radiation between $35\,keV$ and $60\,keV$, with a calibrated minimum dose rate of $10\,mGy/s$. Instead, the latter could provide radiation between $40\,keV$ and $150\,keV$, with a calibrated minimum dose rate of $0.125\,mGy/s$. As our samples presented sensitivities to doses even lower than $0.5\,mGy$, for our experiments we mainly employed the Hamamatsu source.

During the first radiation sensitivity characterization, we tested all the available samples by running the Mo target based X-ray tube under the following conditions:

- Radiation energy: $35\,keV$.
- Radiation doses: $20\,mGy$ (1st), $40\,mGy$ (2nd), $60\,mGy$ (3rd).
- Irradiation protocol: $5\,min$ initial stabilization $\rightarrow$ Three irradiations, each followed by a $5\,min$ stabilization $\rightarrow$ $5\,min$ final stabilization.

This procedure allowed us to assess the radiation sensitivity of the samples and how it was influenced by the cumulated dose. The results are represented in Figure 4.35, while Figure 4.36 focuses on the best performing device selected in each sample. The numerical values extracted are listed in Table 4.12.

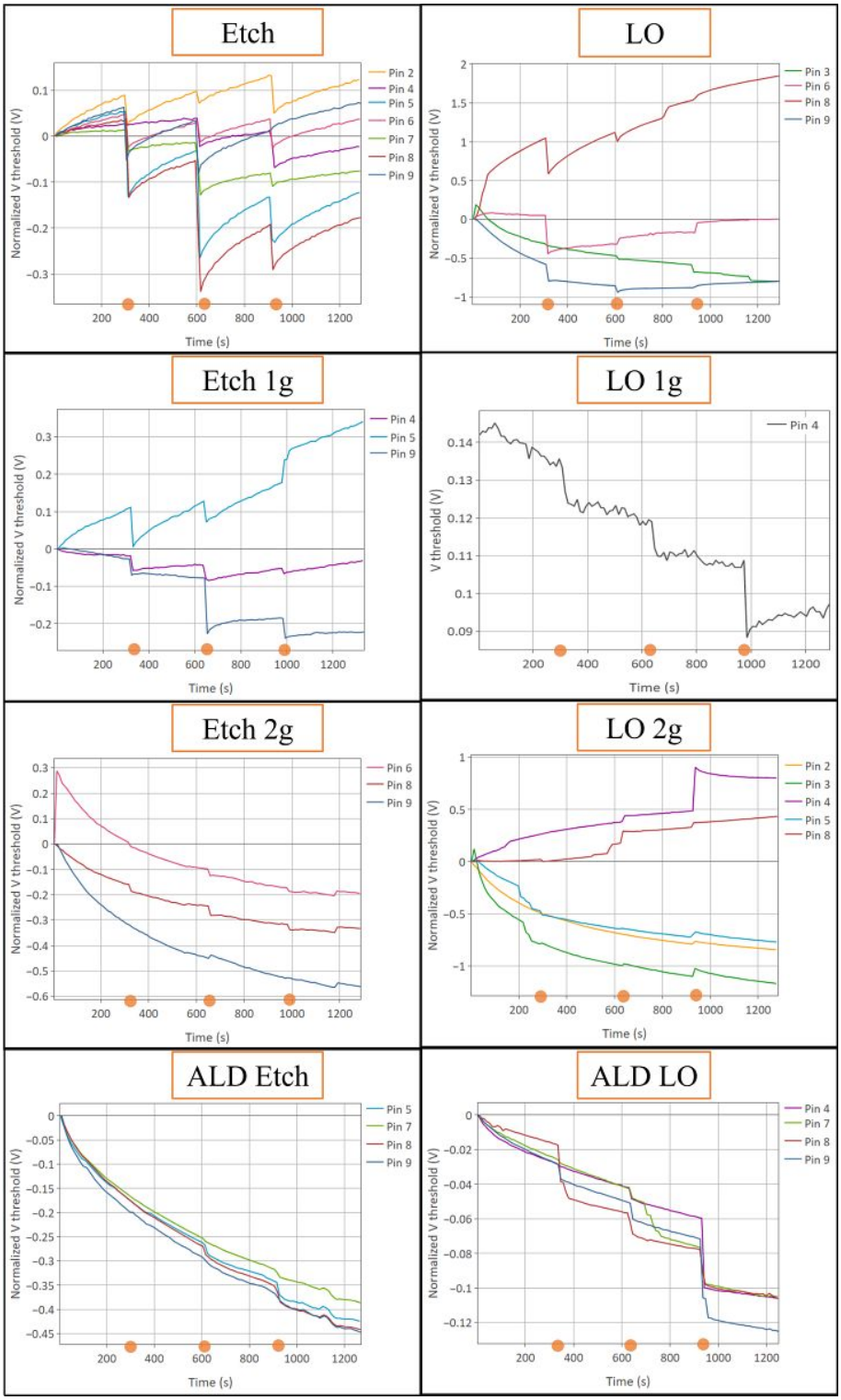

Figure 4.35: Normalized threshold voltage shift, observed during radiation sensitivity tests, for the working devices in each sample. Each orange dot represents an irradiation.

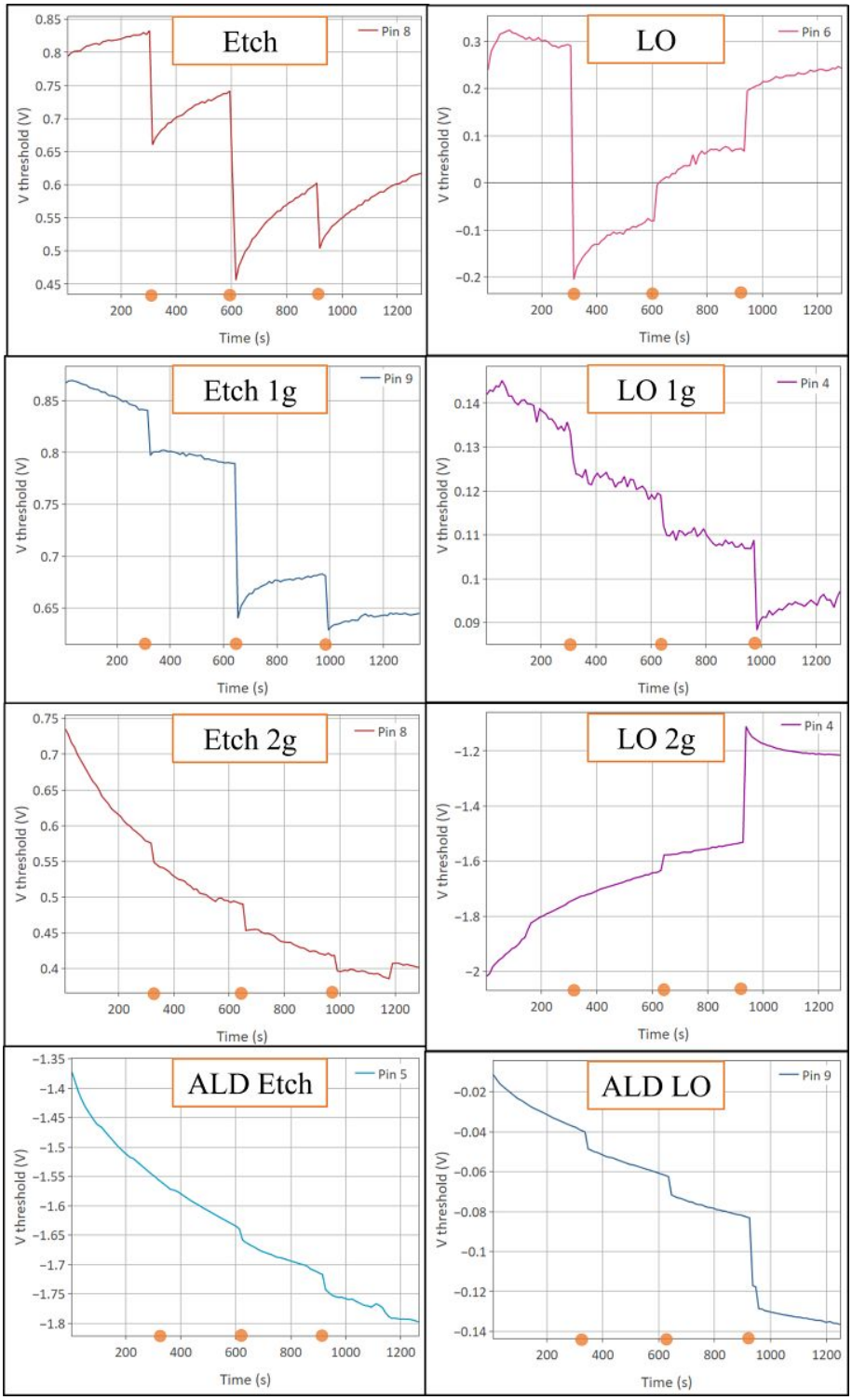

Figure 4.36: Threshold voltage shift, observed during radiation sensitivity tests, for the best performing device in each sample. Each orange dot represents an irradiation.

Sample	**Sensitivity 1st irradiation** (dV/dGy)	**Sensitivity 2nd irradiation** (dV/dGy)	**Sensitivity 3rd irradiation** (dV/dGy)	V_{th} **shift**
Etch	9.1	7.5	1.7	↓
LO	25.7	2.0	2.0	↓/↑
Etch 1g	2.3	3.9	0.9	↓
LO 1g	0.5	0.2	0.3	↓
Etch 2g	1.3	1.0	0.4	↓
LO 2g	N.D.	1.4	7.2	↑
ALD Etch	N.D.	0.5	0.5	↓
ALD LO	0.5	0.2	0.6	↓

Table 4.12: Radiation sensitivities for the best performing device in each sample. A symbol ↓ (↑) indicates a negative (positive) V_{th} shift after irradiation.

From these results we can conclude that all samples were sensitive to radiation. It stands out immediately how Etch and LO samples potentially offer radiation sensitivities much higher than those previously reported in the literature ($3.4\,V/Gy$ [5]). However, while the Etch sample had a negative V_{th} shift upon irradiation, the LO sample presented a mixed behaviour difficult to explain. Furthermore, among the ALD samples, the ALD LO appeared to be unaffected by the cumulated dose and with its threshold voltage behaving as expected. Finally, these trials allowed us to confirm that also Parylene-c passivated samples are radiation sensitive.

We concluded that the Etch and ALD LO samples were particularly promising and deserved further investigation. Thus, we performed new radiation sensitivity tests employing the Hamamatsu micro focus X-ray source. Such device allowed us to provide much smaller doses and vary the X-rays energy in a broader range.

In order to assess the sensitivity to smaller doses, and how that sensitivity was affected after multiple irradiations, we operated the X-rays source under the following conditions:

- Radiation energy: $60\,keV$.
- Radiation doses: $0.5\,mGy$ (4 irradiations).
- Irradiation protocol: $6\,min$ initial stabilization → Four irradiations, each followed by a $6\,min$ stabilization → $10\,min$ final stabilization.

The results of these measurements on Etch and ALD LO samples are represented in Figures 4.37 and 4.38, respectively. For both samples, even ignoring possible outliers, it is particularly interesting how the radiation sensitivity resulted much higher than that previously observed (even up to 20 times more). This suggests that such devices are particularly suitable for doses below few mGys, while they might saturate when exposed to higher amounts or radiation. Moreover, the ALD LO sample appeared more stable than the Etch in terms of sensitivity after repeated irradiations.

In addition to the previous measurements, in order to assess how the sensitivity changed and different radiation energies, we performed further tests by operating the X-rays source under the following conditions:

- Radiation energies: $40\,keV$, $60\,keV$, $90\,keV$, $120\,keV$, $150\,keV$.
- Radiation doses: $0.5\,mGy$ (one irradiation for each energy value).
- Irradiation protocol: $6\,min$ initial stabilization $\rightarrow$ Four irradiations, each followed by a $6\,min$ stabilization $\rightarrow$ $10\,min$ final stabilization.

These results for the Etch and ALD LO samples are represented in Figures 4.39 and 4.40, respectively. In this case, excluding again possible outliers, the radiation sensitivity proved to be much higher than the literature standard. Both the ALD LO and the Etch sample sample appeared to be slightly energy dependent, with the former performing better overall. However, also considering the previous observations, these results might have been partially influenced by the cumulated dose (with the high energy irradiations performed shortly after the low energy ones).

In conclusion, the ALD LO sample resulted to own the ideal characteristics in terms of reproducibility, electrical performances and radiation sensitivity. As discussed in Chapter 4.1, we chose the ALD LO as the standard of reference for the fabrication of future devices.

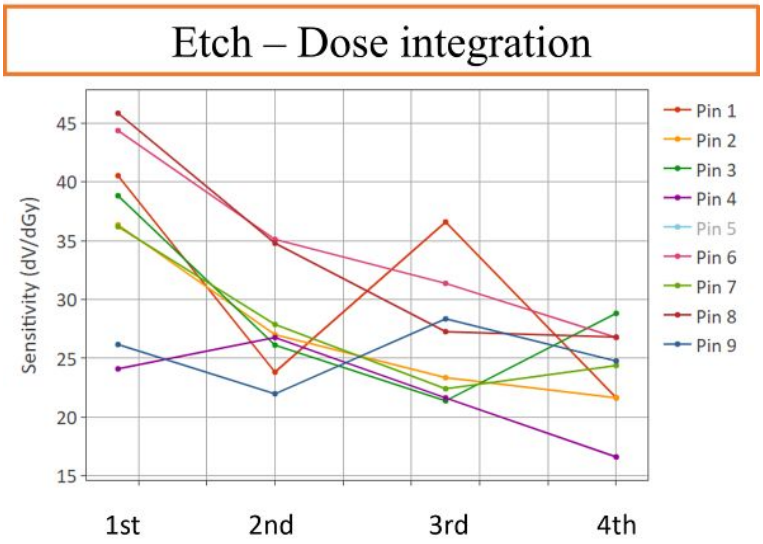

Figure 4.37: Sensitivity, associated to each irradiation, for all the working devices on the Etch sample. We performed irradiations providing a constant dose ($0.5\,mGy$ each) at constant X-rays energy ($60keV$).

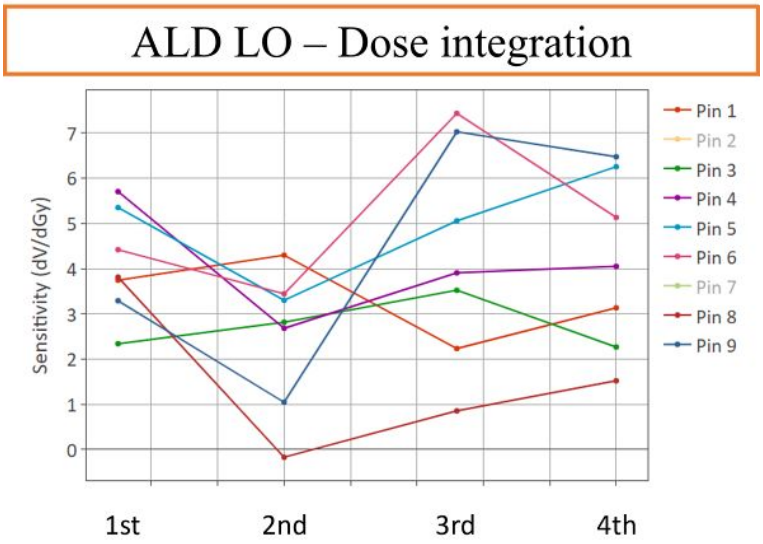

Figure 4.38: Sensitivity, associated to each irradiation, for all the working devices on the ALD LO sample. We performed irradiations providing a constant dose ($0.5\,mGy$ each) at constant X-rays energy ($60keV$).

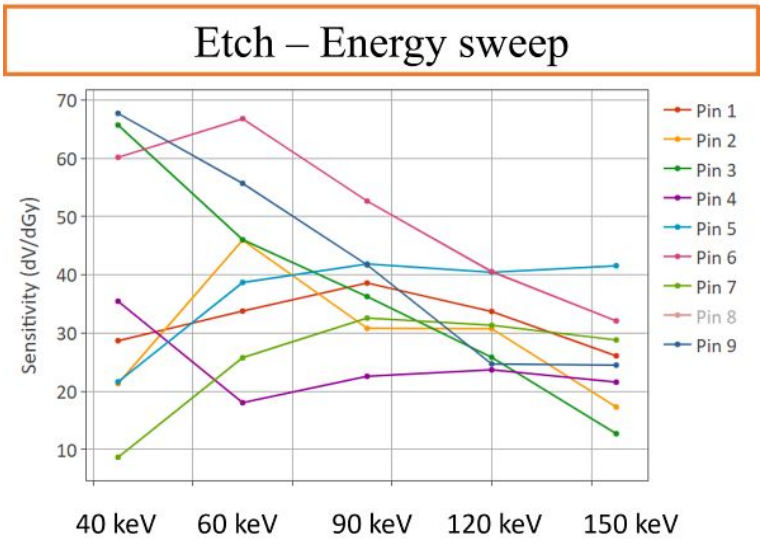

Figure 4.39: Sensitivity, associated to each irradiation, for all the working devices on the Etch sample. We performed irradiations providing a constant dose ($0.5\,mGy$ each) and increasing the X-rays energy.

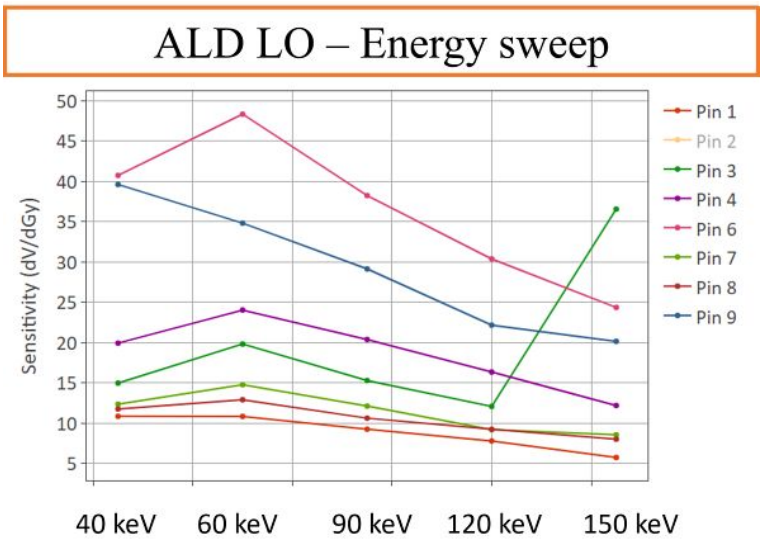

Figure 4.40: Sensitivity, associated to each irradiation, for all the working devices on the ALD LO sample. We performed irradiations providing a constant dose ($0.5\,mGy$ each) and increasing the X-rays energy.

Radiation sensitivity measurements on newly fabricated batch

We decided to perform radiation sensitivity measurements on those samples that had better electrical performances and more *working* devices available. Therefore, we selected the Ta20A, Ta40A, Ta60A and Ta80A samples, while we omitted the Ta100 samples due to their low statistical significance.

As an initial remark, we observed how visible light affects the behaviour of the TFT devices. To this end, we attached our samples as to perform a normal radiation sensitivity measurement, monitoring how the threshold voltage shifts over time. Then, instead of irradiating the samples with X-rays, we changed their illumination in a controlled way. The results of this tests, represented in Figure 4.41, proved that such ROXFET devices were strongly sensitive to visible light.

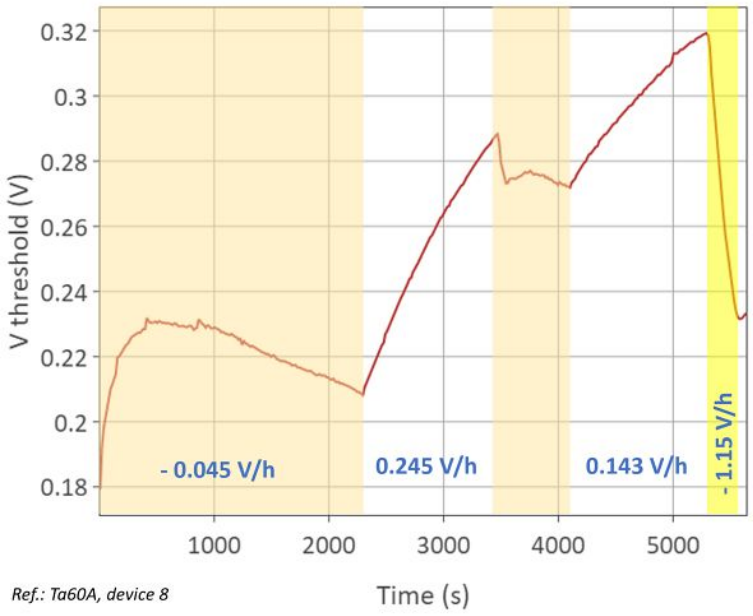

Figure 4.41: Effect, on threshold voltage of the TFTs, of the exposure to visible light. The different shades represent exposure to dim light - dark - dim light - dark - strong light.

Upon exposure to dim light (light source from another room) and to strong light (light source right above the sample), we observed a threshold voltage drift towards negative values. Instead, when in a dark environment (obtained by covering the sample with a cardboard box), the ROXFET devices experienced a positive V_{th} drift. This observation suggests that exposure to visible light might be able to induce electrons accumulation inside

the semiconductor (negative V_{th} drift), while such effect is rapidly recovered (positive V_{th} drift) when the exposure is interrupted.

As the extent of the threshold voltage drift was comparable (if not larger) than the shift that we later observed during irradiation, such drift could be confused (or could erase) the information related to the ionizing radiation detection. For this reason, we performed all the subsequent tests while keeping the samples in a dark environment (cardboard box enclosure).

Once again, we performed the radiation sensitivity tests as described in Section 3.3 and employing the usual measurement system (Figure 3.1). In order to assess the stability of the threshold voltage, before irradiating the samples we monitored the extent of the V_{th} drift over the first hour. Then, as a radiation source we employed the Hamamatsu micro focus X-ray source to provide a broad range of doses ($0.05\,mGy$ to $10\,mGy$) at different energies (40, 60 and $150kV$). During the experiments, we normally performed each irradiation as a series of identical doses (e.g. $1\,mGy$ as a series of ten $0.1\,mGy$ doses). In this way, the measured signal had a step-like trend that allowed us to better observe the response of the devices.

Figure 4.42 represents the radiation sensitivity results obtained for the best performing device on sample Ta20A. Over the first hour (excluding an initial $60\,s$ stabilization period), the threshold voltage has shifted by $0.03\,V$, the lowest amount observed across samples. Then, contrary to all other samples, after irradiation the threshold voltage started to drift towards negative values. We hypothesized that this behaviour, which may appear as a continued radiation detection, might be related to the structure of the device. Indeed, we can expect that most of the interaction of the dielectric with radiation occurs in the Ta_2O_5 layer, which has an atomic number much higher than that of Al_2O_3. Being the *sensitive* layer located *far* from the interface with the semiconductor ($80\,nm$ away), we may suppose that slow charge transport mechanisms induced a partial delay in the migration of the generated charges (reflected into a continued detection even long after the irradiation has concluded).

Figure 4.43 represents the radiation sensitivity results obtained for the best performing device on sample Ta40A. Over the first hour, the threshold voltage has shifted by $0.14\,V$. Then, the device was not able to detect the $0.05\,mGy$ and $0.1\,mGy$ irradiations provided, while it started to be sensitive to $1\,mGy$ doses. After exposure, V_{th} recovered as expected.

The radiation sensitivity results obtained for the best performing device on sample Ta60A are reported in Figure 4.44. Over the first hour, the threshold voltage has shifted by $0.2\,V$. The device was not able to detect the $0.05\,mGy$ and $0.1\,mGy$ irradiations provided, while it started to be sensitive to $0.5\,mGy$ doses. After exposure, V_{th} recovered as expected.

Finally, the radiation sensitivity results obtained for the best performing device on sample Ta80A are reported in Figure 4.45. Over the first hour, the threshold voltage has shifted by $0.58\,V$, the largest extent observed among the samples. A first $0.05\,mGy$ exposure, yet not detected by the device, induced a change in the V_{th} drift, which started to be nearly constant. Then, the device started to be sensitive to $1\,mGy$ doses and presented the slowest V_{th} recovery after irradiation.

Table 4.13 summarizes the main results previously discussed. We calculated each sensitivity value by considering the cumulative dose of one series of irradiation steps and the associated V_{th} shift.

Sample	V_{th} **stability** ($\Delta V_{th}/1\,h$)	**Minimum dose** (mGy)	**Min-Max sensitivities** (dV/dGy)
Ta20A	+0.03	0.05	32-37
Ta40A	+0.14	1	1.5-1.6
Ta60A	+0.20	0.5	3.0-6.5
Ta80A	+0.58	1	8.2-8.5

Table 4.13: Overview of the radiation sensitivity of the newly fabricated batch. Values reported are those for the best performing device in each sample. The minimum dose refers to the lowest among dose provided during the experiments.

In conclusion, the devices we tested from this newly fabricated batch have showed radiation sensitivities much higher than those reported in the literature ($3.4\,V/Gy$ [5]). All samples experienced a V_{th} reduction after irradiation and a positive V_{th} recovery (with the exception of the Ta20A sample). Unfortunately, due to the small number of *working* samples, it is difficult to draw any strong conclusion on the best performing configuration. Moreover, contrary to what expected, neither sensitivity nor minimum dose can be correlated with the Ta_2O_5 layer thickness inside the dielectric.

Lastly, we can notice how Ta40A and Ta80A samples featured a nearly dose-independent sensitivity, while the Ta20A and Ta60A showed a decreasing trend after repeated irradiations. Also, threshold voltages of the Ta20A and Ta40A samples were the most stable before the irradiation had occurred, while that of Ta80A was the most stable after irradiation.

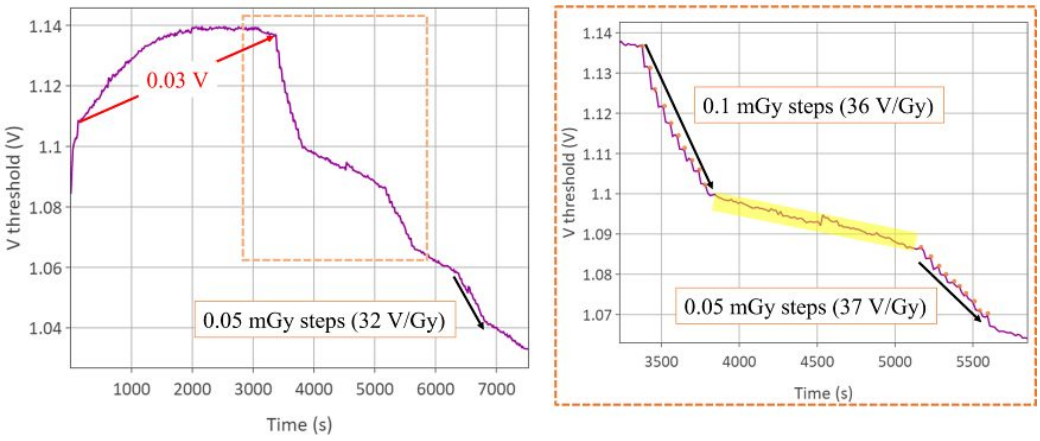

Figure 4.42: Results of the radiation sensitivity test, performed on Ta20A sample, for the best performing device. Each orange dot represents an irradiation. The yellow shaded area corresponds to a $20\,min$ recovery period in which the device experienced a $\Delta V_{th} = -10\,mV$ (equivalent to detecting $+0.4\,mGy$).

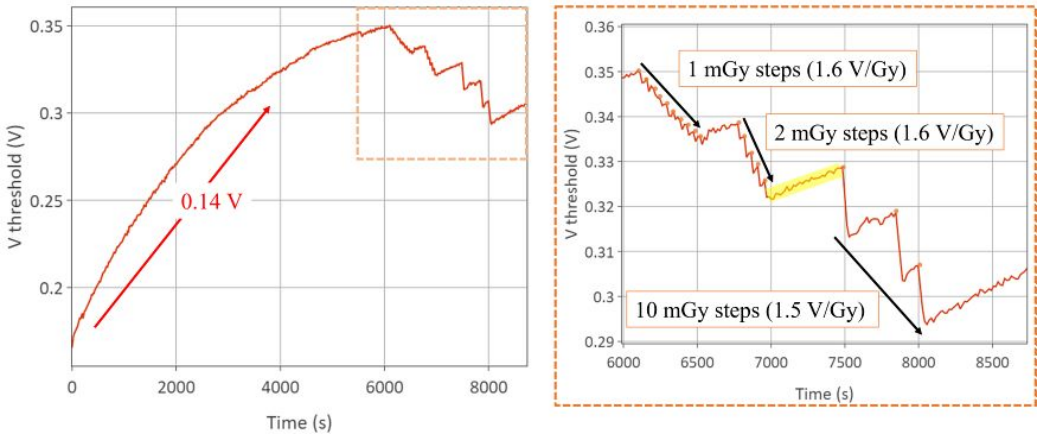

Figure 4.43: Results of the radiation sensitivity test, performed on Ta40A sample, for the best performing device. Each orange dot represents an irradiation. The yellow shaded area corresponds to a $5\,min$ recovery period in which the device experienced a $\Delta V_{th} = +5\,mV$ (equivalent to detecting $-3\,mGy$).

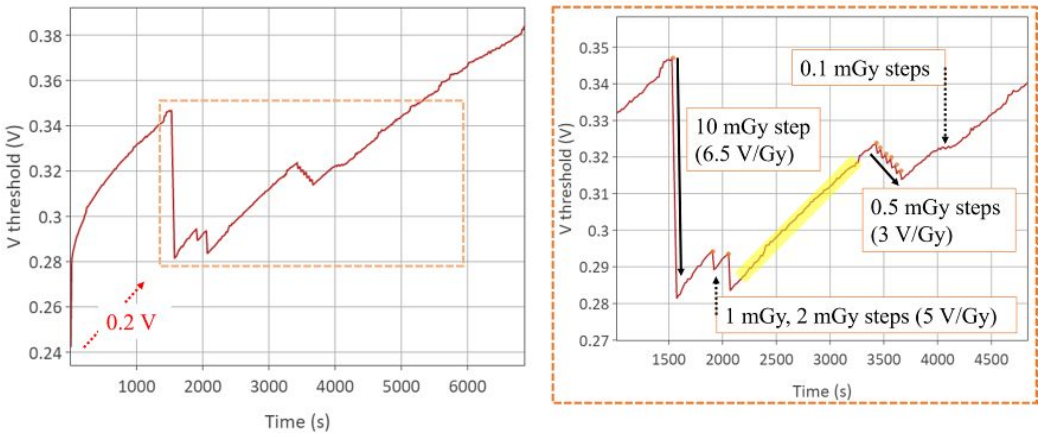

Figure 4.44: Results of the radiation sensitivity test, performed on Ta60A sample, for the best performing device. Each orange dot represents an irradiation. The yellow shaded area corresponds to a $20\,min$ recovery period in which the device experienced a $\Delta V_{th} = +35\,mV$ (equivalent to detecting $-7\,mGy$). The initial V_{th} stabilization values comes from a different dataset not presented here.

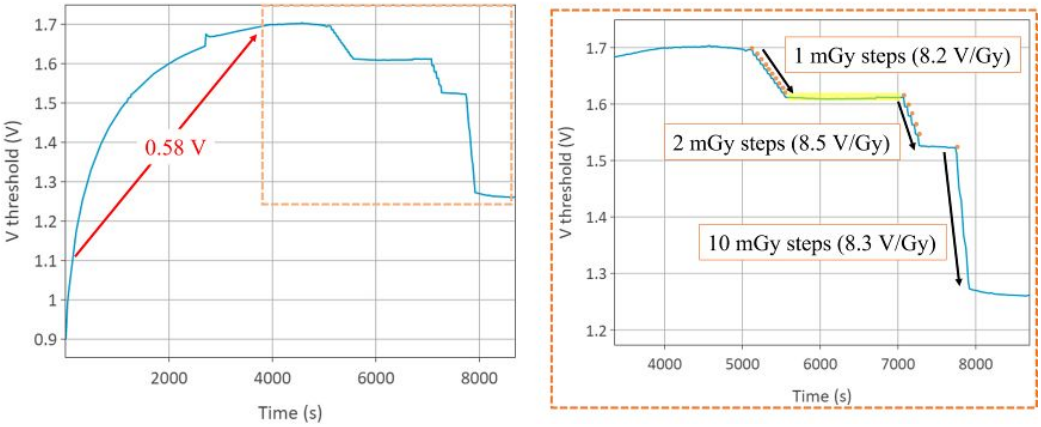

Figure 4.45: Results of the radiation sensitivity test, performed on Ta80A sample, for the best performing device. Each orange dot represents an irradiation. The yellow shaded area corresponds to a $20\,min$ recovery period in which the device experienced a $\Delta V_{th} = +2\,mV$ (equivalent to detecting $-0.3\,mGy$).

4.3.3 Final comparison and possible trends

From analyses performed on the previously fabricated batch we concluded that ALD LO sample has the ideal characteristics in terms of reproducibility, electrical performances and radiation sensitivity. The newly fabricated batch, which ideally reproduces the ALD LO standard, also featured improved radiation sensitivity respect to the literature reference.

It is interesting to notice that all the ALD fabricated samples always experiences normal V_{th} shifts, but only the Ta20 sample showed an anomalous *recovery* trend upon irradiation. This anomaly has also been confirmed from C-V measurements, possibly indicating a physical process that becomes negligible when the Ta_2O_5 amount inside the dielectric is increased.

From the newly fabricated batch it was not possible to correlated the Ta_2O_5 layer thickness neither with sensitivity nor with stability. Indeed, a positive correlation between tantalum oxide thickness and sensitivity can be found only if we neglect the Ta20 sample. Also, apparently no correlation is present with the V_{th} stability, as those devices that are more stable *before radiation* (i.e. show the lowest initial ΔV_{th}) tend to be less stable *after radiation* (i.e. present a faster V_{th} recovery), and vice versa. Indeed, more tests on identical samples are needed in order to draw any conclusion on both aspects.

From the PBGS measurements performed on reference devices, we hypothesised the existence of a ratio between the Ta_2O_5 and Al_2O_3 dielectric components at which the stability of V_{th} is highest. According to the two opposite behaviour observed between Ta20 (Figure 4.42) and Ta40 (Figure 4.43) samples, such *ideal* threshold may lie between the $20 - 40\,nm$ Ta_2O_5 thickness range. Indeed, further samples in this range are needed in order to confirm such hypothesis.

Chapter 5

Conclusions and future perspectives

Ionizing radiation detection has become pervasive in our everyday life, as it finds application in a wide range of scenarios: from radioactive waste management to radiotherapy, imaging, security or to industrial processes. Indeed, detectors need to continuously evolve in order to provide reliable and efficient solutions in all these cases.

Recent advances in the fields of materials Physics and microelectronics will soon enable the large scale production of low-cost radiation detectors and dosimeters that combine reliability with low-power (or even no power) operation, flexibility and adaptability to any surface and the possibility of real-time and remote read-out.

All these characterize the ROXFET which, as we saw, leverages the advantages offered by both amorphous oxide semiconductors (a-IGZO) and *high-k* dielectrics (Ta_2O_5). The aim of this thesis work was to contribute to the development of the ROXFET technology, either by assessing overall electrical and radiation sensitivity performances, by understanding the physical processes underlying its operation and by improving ROXFET architecture and fabrication processes.

By performing electrical characterization measurements on a previously fabricated batch, we observed that the thin film devices with the architecture presented in Section 4.3.1 featured good performances in terms of ON/OFF ratio, sub-threshold slope and mobility. In particular, those devices fabricated with a combination of Atomic layer deposition and Lift-off etching (sample ALD LO) featured the best reproducibility among samples, representing a possible standard approach for future fabrications. Then, by performing radiation detection measurements on the same batch, we confirmed that the ALD LO sample also provided excellent sensitivities, and

that ROXFET devices in general outperformed reference literature values.

Afterwards, we performed KPFM measurements on selected devices, scanning the semiconductor area while controlling the bias applied to the TFT's electrodes. From these results, we were able to map the channel's surface potential in the transistor under operation. Also, we applied a procedure for the determination of the density of states inside the semiconductor, to be then compared with what extracted from other techniques. Unfortunately, due to limitations imposed by the dimensions of the instrumentation, we have been able to test only few devices. Also, it would have been interesting to compare KPFM results extracted, in the same condition, before and after an irradiation. These measurements might provide an insightful description of the way in which charges accumulate upon exposure to ionizing radiation.

During this work we also fabricated a new batch of samples, trying to assess the reproducibility of the ALD LO reference while optimizing the dielectric structure and the overall fabrication process. Unfortunately, many of the fabricated devices were broken, due yet unclear fabrication issues that require further investigation. As a result, this batch did not constitute a solid evidence in favour of the ALD LO fabrication process. To this end, once inspected the samples and identified the cause of the damage, it would be meaningful to repeat the fabrication of this batch and perform new characterization measurements. Nevertheless, we were able to carry out the characterization of the *working* devices, observing interesting behaviours in terms of radiation sensitivity or threshold voltage stability. To be mentioned, the observation that samples are sensitive to visible light, as they experience a V_{th} shift analogous to the one induced by ionizing radiation. Moreover, we hypothesized that the use of a $20 - 40\,nm$ thick Ta_2O_5 layer in the dielectric may improve devices stability.

Finally, we performed C-V measurements on all available samples. Apart from the extraction of the gate-channel capacitance value, from multi-frequency analysis we were able to extract the band tail density of states (DOS) inside the semiconductor. By performing such measurements before and immediately after exposure to ionizing radiation, we were able to observe the induced shift in the shape of the DOS distribution.

During the period of this thesis work, we also conducted test that aimed at integrating the available experimental samples with a read-out electronics (Figure 5.1).

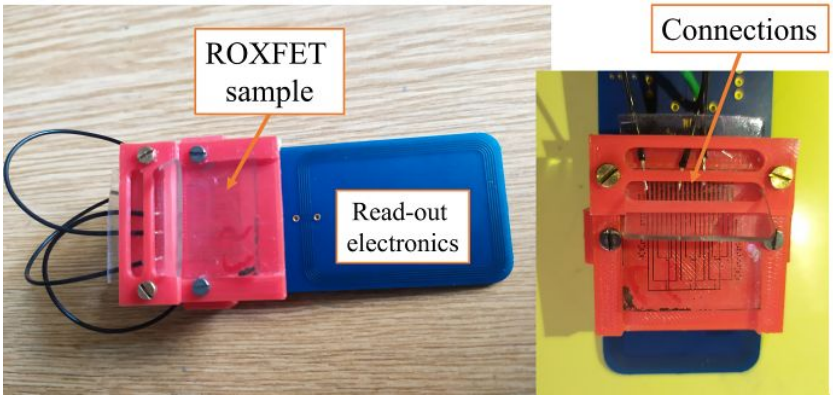

Figure 5.1: Pictures of a ROXFET sample attached to a RFID read-out electronics.

Although far from its final compact and flexible appearance, such prototype allowed us to demonstrate that a radiation induced variation of the channel impedance could be measured, passively and in real-time, with the simple use of a smartphone equipped with a NFC antenna. In conclusion, the ROXFET technology already appears promising given both its excellent electrical and radiation sensitivity results, and the relatively inexpensive and simple fabrication process. Its features allow ROXFET devices to be fabricated as flexible and light-weight devices, that can be operated at low power in real-time and remotely. In the near future, this technology finds potential applications in healthcare, individual radioprotection, industrial processes and security.

Appendix A

Determination of DOS from thin film transistor C-V data

The following derivation, obtained together with prof. Tobias Cramer, is based on the work by Lee et al. presented in [22].

As a first step we aim at a better understanding of the measured capacitance C. One contribution to C is due to the oxide dielectric. This geometric capacitor has a fixed capacitance C_{ox}, that depends only on the thickness of the dielectric, its permittivity and the area A of the channel. A second contribution to the total C comes from the fact that charges in the semiconducting layer accumulate only when this is energetically possible, as free states that can be occupied by charge carriers need to be available. In the simplest approximation, we can express the increment in charge Q for an increment in energy dE as:

$$dQ = q_0 \; dN = q_0 \; A \; t \; g\,(E) \;\; dE \tag{A.1}$$

Here q_0 is the elementary charge and t is the thickness of the semiconducting layer. To justify this expression, we use the definition of the density of states: $g\,(E) = \frac{1}{V}\frac{dN}{dE}$.

In capacitance measurements, the increment in energy is due to electrostatic potential (voltage) changes, thus: $dE = dU$. Here, we express energies in eV $(= J/q_0)$.

Accordingly, we can now define the quantum capacitance related to the DOS of the semiconductor:

$$C_D = \frac{dQ}{dU} = q_0 \frac{dQ}{dE} = \; q_0 A \; t \; g(E) \tag{A.2}$$

Equation A.2 provides a direct relation between the capacitance C_D and the density of states $g(E)$ at a given Fermi level. The experimentally measured capacitance C is the series combination of C_{ox} and C_D:

$$C = \frac{C_D C_{ox}}{C_D + C_{ox}} \tag{A.3}$$

Knowing C_{ox} we can calculate C_D from the experimental data using A.3. Equation A.2 is then used to calculate $g(U_G)$. In order to translate that into $g(E)$, a relation between E and U_G in a thin film transistor is needed. To this end, we can consider Figure A.1. In accumulation mode, we can express the gate voltage as:

$$U_G = U_{FB} + U_{ox} + \Phi = U_{FB} + \frac{Q_{ox}}{C_{ox}} + \Phi \tag{A.4}$$

Here, Φ is the surface potential at the dielectric interface, that quantifies the band bending in the IGZO semiconductor. From Equation A.4 we obtain the differential notation:

$$\frac{d\,\Phi}{dU_G} = 1 - \frac{d}{dU_G}\frac{Q_{ox}}{C_{ox}} = 1 - \frac{C}{C_{ox}} \tag{A.5}$$

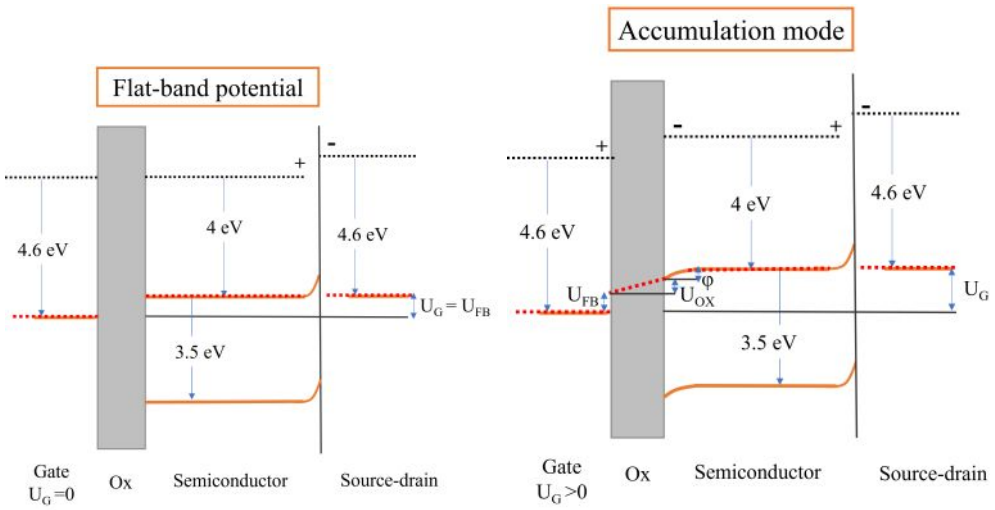

Figure A.1: Energy levels diagram of the TFT transistor.

Next, we assume of having an infinitely thin semiconducting layer, in which no band bending needs to be considered. In such a case, the change in Fermi level is equal to the change in surface potential $d\Phi = dE$. In addition,

we can introduce in Equation A.5 that the total capacitance C results form the series combination of C_{ox} and C_D:

$$\frac{dE}{dU_G} = 1 - \frac{C}{C_{ox}} = 1 - \frac{C_D}{C_D + C_{ox}} \tag{A.6}$$

This differential equation contains all the information needed to derive the function $E(U_G)$. By integration we obtain:

$$E = \int 1 - \frac{C}{C_{ox}}\, dU_G + const \tag{A.7}$$

By measuring $C(U_G)$ we can numerically solve the integral and obtain the relation needed to assign to U_G the related E value in the semiconductor and finally calculate $g(E)$. The value of *const* can be determined if U_{FB} is known (at $U_G = U_{FB}$ we have $E = 0$).

The procedure to follow is:

1. Calculate $C_D(U_G)$ from the data, using Equation A.3 :

$$C_D(U_G) = \frac{CC_{ox}}{C_{ox} - C} \tag{A.8}$$

2. Calculate $g(U_G)$ from the data

$$g\,(U_G) = \frac{C_D(U_G)}{q_0 A\ t} \tag{A.9}$$

3. Use Equation A.7 to calculate the relation that assigns at each U_G the related E_G, an unknown constant remains. To fix that, one needs to know $U_{G\,FB}$. However, if different devices are compared, we can associate changes in the DOS to changes in $V_{G\,FB}$.

Test of the procedure

For the test, we assume a density of states:

$$g\,(E) = g_0 \exp(\alpha E) \tag{A.10}$$

Then, from Equation A.2 we obtain:

$$C_D = \frac{dQ}{dU} = q_0\ A\ t\ g_0 \exp(\alpha E) \tag{A.11}$$

Through Equation A.7 we get:

$$\frac{dE}{dU_G} = 1 - \frac{C_D}{C_D + C_{ox}} \tag{A.12}$$

Combining A.12 with A.11, after integration we get:

$$-\frac{q_0\ A\ tg_0}{\alpha C_{ox}} \exp(\alpha E) + E = U_G + const \tag{A.13}$$

To determine the *const*, we use that fact that if $U_G = U_{FB}$ then $E = 0$:

$$\frac{q_0\ A\ tg_0}{\alpha C_{ox}} \exp(\alpha_0) + 0 = U_{FB} + const$$

$$const = \frac{q_0\ A\ tg_0}{\alpha C_{ox}} - U_{FB}$$

$$\frac{q_0\ A\ tg_0}{\alpha C_{ox}} \exp(\alpha E) + E = U_G + \frac{q_0\ A\ tg_0}{\alpha C_{ox}} - U_{FB} \tag{A.14}$$

Finally, we need to separate E inside Equation A.14, obtaining:

$$E = -\frac{1}{\alpha} W\left[\frac{q_0\ A\ tg_0}{C_{ox}} exp\left(\alpha U_G + \frac{q_0\ A\ tg_0}{C_{ox}} - \alpha U_{FB}\right)\right] + \left(U_G + \frac{q_0\ A\ tg_0}{\alpha C_{ox}} - U_{FB}\right) \tag{A.15}$$

$W[\,]$ indicates the *LambertW* function. Combined with Equations A.11 and A.3, this allows to calculate a $g(U_G)$ curve.

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