Alma Mater Studiorum · Università di Bologna

Scuola di Scienze
Dipartimento di Fisica e Astronomia
Corso di Laurea Magistrale in Fisica

FLEXIBLE OXIDE THIN FILM TRANSISTORS: DEVICE FABRICATION AND KELVIN PROBE FORCE MICROSCOPY ANALYSIS

Relatore:
Prof.ssa Beatrice Fraboni

Correlatore:
Dott. Tobias Cramer

Presentata da:
Ilaria Fratelli

Anno Accademico 2015/2016

Abstract

Amorphous oxide semiconductor thin film transistors (AOS TFTs) are promising candidates in the field of large area electronics. Unlike a-Si:H and poly-Si technologies, AOSs provides a high electrical mobility ($\mu > 10\ cm^2\ V^{-1}\ s^{-1}$) despite their amorphous structure. Moreover, the possibility to deposit oxide semiconductors at low temperature and on polymeric substrates, opens the perspective to achieve high-performance, large-area flexible electronics using this class of materials.

Towards the improvement of this technology several amorphous oxide TFTs have been fabricated during a four month stay at the clean-room facilities of the Nova University in Lisbon. All the transistors contain Gallium Indium Zinc Oxide (GIZO) amorphous semiconducting layer and two different dielectric materials have been implemented: an organic insulator formed by Parylene and a 7 multilayer dielectric realized with SiO_2 alternating SiO_2 + Ta_2O_5. All the devices have been realized on flexible substrates developing a new procedure for the lamination and delamination of the foils on a rigid carrier. The optimized fabrication method yields flexible thin-film transistors that maintain almost ideal characteristics known from rigid substrates (μ = (35.7 ± 0.9) $cm^2V^{-1}s^{-1}$; V_{ON} = (-0.10 ± 0.002) V; ON/OFF = (1.14 ± 0.01) $\cdot 10^6$; S = (0.084 ± 0.003)V dec^{-1}).

In order to provide a microscopic understanding of the different transistor performances in the fabricated devices, I applied Kelvin Probe Force Microscopy (KPFM) during my stay at the University of Bologna. The technique revealed the importance of contact resistance in less performing devices and pointed to the presence of charge trapping in parylene based dielectrics.

The excellent results obtained from the KPFM analysis suggest the further exploitation of this technique to reveal the impact of mechanical strains to the transistors performance. Understanding the mechanical failure due to the structural deformation at a microscopic level will be an essential step for the progress in the field of oxide flexible electronics.

Sommario

I transistor a film sottile basati su ossidi amorfi semiconduttori (AOSs TFTs) sono ottimi candidati nell'ambito dell'elettronica su larga scala. Al contrario delle tecnologie basate su a-Si:H a poly-Si, gli AOS presentano un'elevata mobilità elettrica ($\mu > 10\ cm^2\ V^{-1}\ s^{-1}$) nonostante la struttura amorfa. Inoltre, la possibilità di depositare AOS a basse temperature e su substrati polimerici, permette il loro impiego nel campo dell'elettronica flessibile.

Al fine di migliorare questa tecnologia, numerosi TFT basati su AOS sono stati fabbricati durante 4 mesi di attività all'Università Nova di Lisbona. Tutti i transistor presentano un canale formato da a-GIZO, mentre il dielettrico è stato realizzato con due materiali differenti: Parylene (organico) e 7 strati alternati di SiO_2 e $SiO_2 + Ta_2O_5$. I dispositivi sono stati realizzati su substrati flessibili sviluppando una nuova tecnica per la laminazione e la delaminazione di fogli di PEN su supporto rigido. L'ottimizzazione del processo di fabbricazione ha permesso la realizzazione di dispositivi che presentano caratteristiche paragonabili a quelle previste per TFT costruiti su substrati rigidi ($\mu = (35.7 \pm 0.9)\ \mathrm{cm^2V^{-1}s^{-1}}$; $V_{ON} = (-0.10 \pm 0.002)$ V; ON/OFF $= (1.14 \pm 0.01) \cdot 10^6$; S $= (0.084 \pm 0.003)\mathrm{V\ dec^{-1}}$).

Al Dipartimento di Fisica dell'UNIBO, l'utilizzo del KPFM ha permesso lo studio a livello microscopico delle prestazioni presentate dai dispositivi analizzati. Grazie a questa tecnica di indagine, è stato possibile analizzare l'impatto delle resistenze di contatto sui dispositivi meno performanti e identificare l'esistenza di cariche intrappolate nei TFT basati su Parylene.

Gli ottimi risultati ottenuti dall'analisi KPFM suggeriscono un futuro impiego di questa tecnica per lo studio del legame tra stress meccanico e degradazione elettrica dei dispositivi. Infatti, la comprensione dei fenomeni microscopici dovuti alla deformazione strutturale sarà un passaggio indispensabile per lo sviluppo dell'elettronica flessibile.

Contents

Introduction **11**

1 Oxide thin film transistors **13**

1.1 Thin film transistors 13

1.1.1 Brief history of TFTs 13

1.1.2 Device structure and operation 15

1.1.3 Present and future semiconductors for TFTs 21

1.2 Amorphous Oxide Semiconductors 22

1.3 Flexible oxide thin film transistors 25

1.3.1 a-IGZO as active layer 25

1.3.2 Dielectric layer 26

1.3.3 Flexibility 29

2 Thin film transistors fabrication process **33**

2.1 Optical Lithography 33

2.2 Etching 39

2.3 Sputtering deposition 41

2.4 Chemical vapor deposition 45

2.5 Post-deposition annealing 47

3 Scanning Probe Microscopy **49**

3.1 AFM in non-contact mode 49

3.2 Kelvin probe microscopy 54

3.3 Application of KPFM 58

4 Results and discussion **61**

4.1 Fabricated devices 62

4.1.1 Dielectric thickness 65

4.1.2 Dielectric roughness 66
4.2 Electrical characterization 68
4.2.1 Transport characterization 69
4.2.2 Capacitance characterization 71
4.2.3 Comparison 74
4.2.4 After detachment 76
4.3 KPFM analysis 77

5 Final conclusion and perspective **87**

Bibliography **91**

Introduction

Amorphous Oxide Thin Film Transistors, especially those based on a-GIZO semiconductor, have attracted tremendous attention in the last decades. These devices are excellent candidates for their implementation in the field of large area electronics. The low cost processability combined with the high electrical mobility presented by this class of material allows the integration of the oxide TFTs in circuit applications, in active matrix (AM)-LCDs or for driving organic light emitting diodes (OLEDs) displays, for realizing sensors and detectors etc. Moreover, oxide TFTs can be fabricated both on rigid and flexible substrates obtaining good electrical performance ($\mu > 10$ cm^2 V^{-1} s^{-1}) and giving the chance to realize and investigate flexible devices.

Even though many experiments have already demonstrated the great qualities of a-oxide TFTs, [1][2][9], more efforts must be involved to find the best structure and the most efficient combination of materials to achieve even better results and to lower the production costs.

A part from the huge development achieved in oxide semiconductors, the dielectric layer used in these devices has been mostly treated as secondary, despite being as important as the channel layer in a TFT as its properties determine the charge accumulation at the dielectric/semiconductor interface. An insulator which presents good properties as dielectric layer even if processed at low temperature is essential for the realization of performant flexible devices.

The objective of this thesis is the further improvement of amorphous oxide thin film transistors technology and the optimization of the fabrication process involving flexible polymeric substrates. To this end, several devices have been fabricated, implementing different insulators as dielectric layer, and electrically analyzed both in a macroscopic and microscopic way. The fabrication process has been accomplished during a four month stay at CENIMAT and CEMOP laboratories at the University Nova in Lisbon. In order to understand the microscopic origin

of the differences observed in the performance of the fabricated devices, scanning probe microscopies were employed at the Physics Department of the University of Bologna. In particular, Kelvin Probe Force Microscopy was exploited to investigate nano-scale transport phenomena and barriers in the channel of thin film transistors.

Chapter 1 introduces the generalities about thin film transistors (TFTs) based on amorphous oxide semiconductors (AOSs). After the description of TFTs structure and operation, a brief presentation of the main characteristics of AOSs is proposed focusing on the most promising material: Gallium/Indium/Zinc Oxide (GIZO). At the end of the chapter, the advantages shown by the implementation of this class of material in the TFT technology are listed and the importance of the dielectric layer is highlighted.

Chapter 2 describes the fabrication process followed for the realization the devices. Firstly, the basis of optical lithography are introduced and the etching procedure is explained. After, the two main techniques used for deposition of the dielectric layers are presented: RF-magnetron sputtering and Chemical Vapor Deposition (CVD).

Chapter 3 is focused on the Scanning Probe Microscopy (SPM) techniques used to characterize the devices from a microscopic point of view. At the beginning of the chapter, non-contact Atomic Force Microscopy (nc-AFM) is described. The second part of the chapter is dedicated to the main technique implemented during this work to study the microscopic electrical properties of the devices: Kelvin Probe Force Microscopy (KPFM).

Chapter 4 presents the results obtained during this work. First of all, the structure and the layout of the fabricated devices are described. Moreover, a novel technique to improve the fabrication onto flexible substrates is proposed. The second part of the chapter shows the macroscopic electrical behaviour of the analyzed samples focusing on the transport and capacitance characterization. A first comparison between several samples is pointed out through the calculated parameters. Furthermore, the electrical performance measured after the detachment of one of the sample from the rigid carrier is reported. The final section of this chapter is devoted to the results obtained by the KPFM microscopic analysis.

Chapter 5 addresses the achievements and the future perspectives of this thesis.

Chapter 1

Oxide thin film transistors

Amorphous oxide semiconductors, especially a-GIZO, are the most recent thin film transistor (TFT) materials implemented in large-area, flexible flat-panel displays and in other giant-microelectronics devices. In this chapter, a brief introduction about the devices and the materials studied in this thesis are presented. In the first section the operation and the structure of thin film transistors are shown. In the second section the physical properties of amorphous oxide semiconductors are illustrated and finally in the last section the implementation of this material as TFT active layer is discussed.

1.1 Thin film transistors

1.1.1 Brief history of TFTs

The *thin film transistor* (TFT) is a field effect transistor (FET). The invention of the TFT occurred in 1925 and was patented in 1930 by J.E. Lilienfeld and O. Heil, but at that time little was known about semiconductor materials and vacuum techniques to produce thin films. Therefore, these first reports are actually concept patents and no evidence exists about the production of devices. Still, in these patents, the idea of controlling the current flow in a material by the influence of a transversal electrical field was already present [1]. The first working TFT was fabricated by Weimer in 1962 at the RCA Laboratories. He used a vacuum technique to deposit gold electrodes, a polycrystalline cadmium sulfide (CdS) n-type semiconductor and a silicon monoxide (SiO) insulator, using shadow masks to define the patterns of these layers [3]. At first, these deposited transistors

didn't show very good performances. However, after placing an insulator between the gate and the semiconductor material, he obtained what he called 'beautiful characteristics'. His 1962 paper, 'The TFT– a new thin-film transistor', drew worldwide attention [5].

Other TFT semiconductor materials like CdSe, Te, InSb and Ge were investigated, but in the mid 1960s with the emergence of the MOSFET based on the crystalline silicon technology and the possibility to perform integrated circuits, led to a decline in TFT development activity by the end of the 1960s.

What dramatically changed the prospects for TFTs in the 1970s was the realization that MOSFETs represented a prohibitive cost when compared with TFTs whereas some applications required large arrays of low cost electronics, like for example displays. By this time many researchers and engineers were engaged in improving the characteristics of liquid crystal displays (LCDs), which had been recently discovered [6].

The largest innovation in the field of large area electronics was the introduction of hydrogenated amorphous silicon (a-Si:H) as active material of the TFTs (LeComber, Spear, and Ghaith, 1979). In spite of exhibiting considerably lower μ than polycrystalline materials such as CdSe (about 1 against 150–200 $cm^2V^{-1}s^{-1}$), a-Si:H was perfectly suitable for the application of TFTs as switching elements in LCDs, since it allowed for low cost, good reproducibility and uniformity in large areas and on/off exceeding 10^6. The major disadvantage of a-Si:H TFT is its low electron mobility that limits the ultimate speed of devices. However, an adequate device speed for the switching applications in the LCD has been achieved.

The main alternative for a-Si:H TFTs when high μ was needed was mostly achieved with the appearance of poly-Si as a semiconductor material in TFTs. A poly-Si-based TFT was initially reported by Depp et al. [7] in 1980 and over the next few years it became possible to achieve μ_{FE} ≈400 $\mathrm{cm^2\ V^{-1}\ s^{-1}}$ that allowed this TFTs to be used also as driver circuitry devices. However, poly-Si TFTs had a large cost, mostly because they required high temperature fabrication processes, which were only compatible with quartz substrates, not with normal glass. For this reason and because of the intrinsic limitation of the polycrystalline structure on large area processing, poly-Si based TFTs could not easily penetrate in the LCD market.

In 1990s' organic materials were introduced for the first time as semiconductors in TFTs. These devices reached performance comparable to a-Si:H ones. Organic

semiconductors have, however, a great advantage over a-Si:H, which is their extremely low processing temperature. This is the reason why organic semiconductor devices in general and organic TFTs in particular are pointed to as one of the most promising technologies for flexible electronics [3].

The new millennium opened the door to a new class of transparent semiconductor as active channel in TFTs: the oxide semiconductors. Even if the first attempts to use oxide semiconductors as active layer in TFT were in 1960s', the birth of transparent electronics is normally associated with reports on ZnO TFTs presented in 2001-2003. Only starting from this year in fact, oxide semiconductors showed such a good performance able to demonstrate that they could represent a viable technology.

While most of the researchers was working to binary oxides such as ZnO, In_2O_3 or SnO_2, in 2003 Nomura et al. suggested to use a complex $InGaO_3(ZnO)_5$ (or GIZO) single-crystalline semiconductor layer in a TFT [8]. This layer allowed to obtain a device that showed an impressive performance: effective mobility of 80 $cm^2\ V^{-1}\ s^{-1}$, turn-on voltage of -0.5 V and on/off ratio of 10^6. Even if such a good performance it was reached with a treatment at very high temperature (1400 °C), this paper showed that was possible to realize high-performance oxide semiconductor-based TFTs. In fact, in 2004 Nomura et al. realized a transparent TFT on a flexible substrate using near-room temperature processing evidencing the enormous potential of oxide semiconductors as active materials [9]. For this device, they used a PLD deposited amorphous GIZO layer as the semiconductor. In this case the performance was far from the ones showed by single-crystalline previously reported mostly because the low sensitivity of these multicomponent oxides to structural disorder: a saturation mobility of 9 $cm^2\ V^{-1}\ s^{-1}$, threshold voltage of 1–2 V and on/off ratio of 10^3. Since this year an enormous number of publications appeared and they continuous nowadays.

1.1.2 Device structure and operation

TFTs are three terminal field-effect devices, whose working principle relies on the modulation of the current flowing in a semiconductor placed between two electrodes (source and drain). A dielectric layer is inserted between the semiconductor and a transversal electrode (gate), being the current modulation achieved by the capacitive injection of carriers close to the dielectric/semiconductor interface. This

effect is turned possible due to the parallel plate capacitor structure formed by the gate electrode, dielectric and semiconductor and it is known as *field effect* [1].

According to the Weimer's classification of 1962, Figure **??** shows the most common TFT structure. These structures are denominated by staggered or coplanar, depending if the source-drain and the gate electrodes are on the same side or in the opposite sides of the semiconductor. In these structures, two configurations are possible: top-gate (or normal) and bottom-gate (or inverted) depending on the whether the gate electrode is on top or bottom of the structure [10].

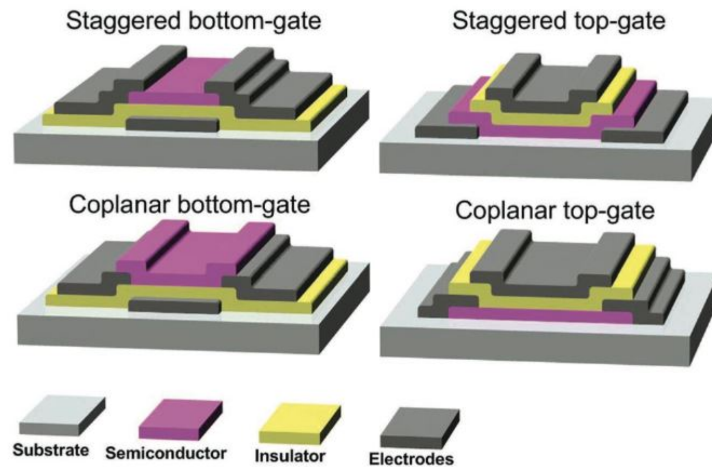


Figure 1.1: Most common TFT structures. [1]

Each of these structures present advantages and disadvantages and each of them are dedicated for different kind of TFTs depending on the material used. For example, staggered bottom-gate configuration is largely used for a-Si:H TFTs in LCDs because, due to the light-sensitive of this material, arranging the metal gate electrode on the bottom of the structure helps to shield the semiconductor from the back-light and enhances the electrical properties. On the other hand, a coplanar top-gate structure is normally preferred for poly-Si TFTs because of the high temperature required to obtain a polycrystalline semiconductor. This process at high temperature in fact could damage all the layers previously deposited and their interfaces. In the top-gate configuration the metal electrode may act as a passivation, which protects the channel layer from external damage. On the other hand, in both the bottom-gate structures the semiconductor surface is exposed to air and this fact can cause undesirable instability effects. For this reason, an extra layer is often added in the bottom-gate structures: a passivation layer

that insulates the active layer from the atmosphere and protects chemically and mechanically the semiconductor.

TFTs are quite similar to other field-effect devices in terms of operation and composing layers, however some important differences exist (see Figure 1.2):

- While in TFTs the substrate is an insulator (typically glass), in MOSFETs the silicon wafer plays the role of semiconductor and mechanical substrate at the same time.
- Different temperature regime during the fabrication: for MOSFET a temperature of 1000°C is commonly reached but on the contrary TFTs technology imposes a lower limit because of the softening point of the substrate.
- MOSFETs have a p-n junction at the source and drain regions, which are absent in the TFTs.
- Even if both the transistors' operation is based on field effect, MOSFETs work in inversion regime while TFTs work in the accumulation one.

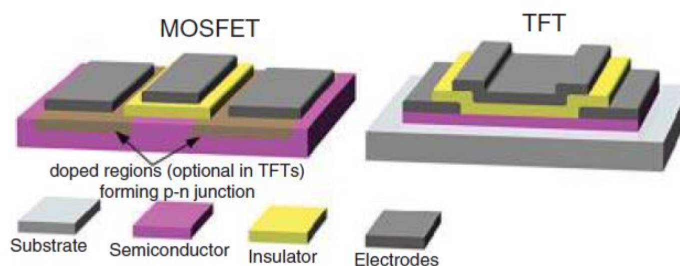


Figure 1.2: Comparison between TFT and MOSFET [1].

The ideal operation of an n-type TFT depends on the existence of an electron accumulation layer at the dielectric/semiconductor interface. This ideal operation can be described by analyzing the energy band diagram of the capacitor comprised by the gate electrode, dielectric and semiconductor. In Figure 1.3 the ideal operation of a n-type TFT is shown: applying a V_G <0 V causes a depletion region at the dielectric interface, while V_G >0 V makes a downward band-bending and the appearance of an accumulation region. In a real device, the two possible regimes of operation are separated by a voltage value which corresponds to downward band-bending of the semiconductor close to its interface with the dielectric: the

threshold voltage (V$_{th}$). In a real device, V$_{th}$ deviates from 0 V, being a function of the gate electrode-semiconductor work function difference, the background carrier concentration of the semiconductor (N), the charge density residing within the dielectric and the trap density at the interface and within the semiconductor. Depending on the sign of V$_{th}$ two different mode of operation for TFT can be distinguished: enhancement and depletion for positive or negative threshold voltage respectively (for n-type TFT).

Once defined the threshold voltage, the role of TFTs as a switch is evident. For V$_G$ >V$_{th}$, provided that a positive drain voltage (V$_D$) is applied, current flows between the drain and source electrodes (I$_D$), corresponding to the on-state of the TFT. For V$_G$ <V$_{th}$, regardless of the value of V$_D$ the upward band-bending of the semiconductor close to the interface with the dielectric is verified, resulting in a low I$_D$ that corresponds to the TFT off-state [3].

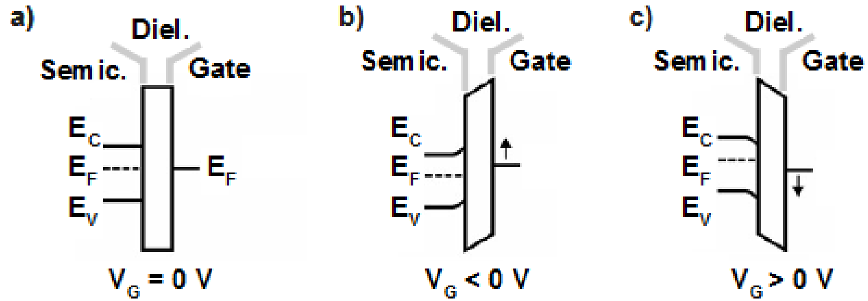


Figure 1.3: Energy band diagram of an ideal gate electrode/dielectric/n-type semiconductor capacitor for different bias conditions: **a)** equilibrium (V$_G$ = 0 V); **b)** depletion (V$_G$ <0 V); **c)** accumulation (V$_G$ >0 V)) [10].

Considering now the *on-state* of the TFT, depending on the intensity of V$_D$ two different regimes can be distinguished:

- **Pre-pinch off regime** $V_D < (V_G - V_{th})$

  In this regime the drain current (I$_D$) can be expressed using the Eq. 1.1

$$I_D = C_i \mu_{FE} \frac{W}{L} \Big[(V_G - V_{th}) V_D - \frac{1}{2} V_D^2 \Big], \tag{1.1}$$

  where C$_i$ indicates the capacitance of the dielectric per unit area, μ_{FE} is the field effect mobility and W,L are the geometrical dimensions of the channel. In this regime a uniform distribution of charge throughout the entire channel

is supposed. When a very little voltage is applied through the drain electrode, the second order term in Eq.1.1 can be ignored and the relation between current and voltage drain becomes linear.

- **Post-pinch off or saturation regime** $V_D > (V_G - V_{th})$

  When the drain voltage overcomes $(V_G - V_{th})$, the accumulation layer close to the drain region becomes depleted, leading to the saturation of I_D.

  In the saturation regime the drain current (I_D) can be expressed using the Eq. 1.2

$$I_D = C_i \mu_{sat} \frac{W}{2L} \left(V_G - V_{th} \right)^2, \tag{1.2}$$

  where μ_{sat} is the saturation mobility.

The eq. 1.1 and eq. 1.2 are based on some assumptions. One of these was proposed by Shockley and is known as "gradual channel approximation": the gradient of the lateral field within the channel is negligible compared with the variation of the vertical field. This assumption is not valid near the drain electrode or for short-channel devices in the saturation regime. Another important assumption not always valid with oxide TFTs is the independence of μ_{FE} and μ_{sat} from V_G.

The electrical performances of TFTs are described by several parameters evaluable from the electrical characterization of the devices. In Figure 1.4 the transfer and output characteristic are shown. From these plot one can extract several parameters like:

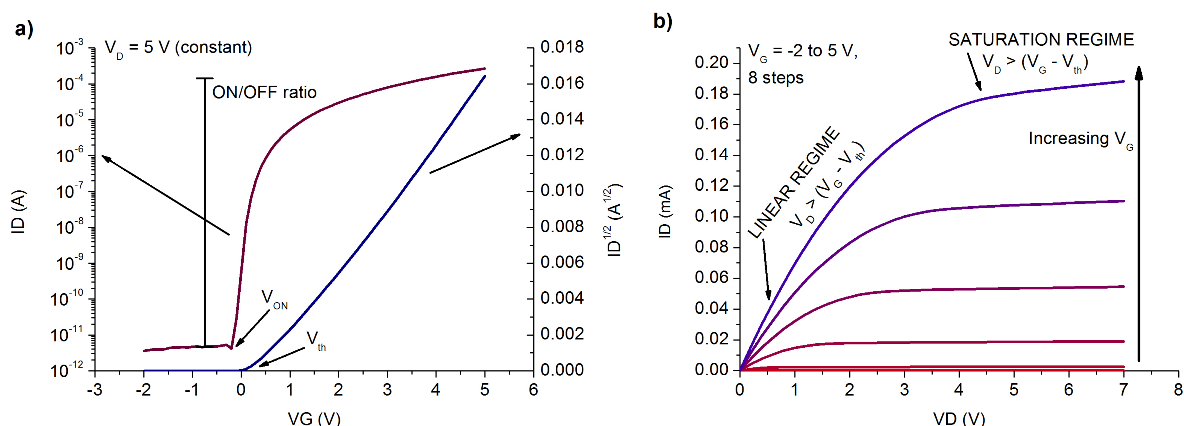


Figure 1.4: a) Transfer and **b)** Output Characteristics of a n-type TFT.

On/off ratio This parameter defines the ratio between the maximum and the minimum value of the drain current. A large value is desirable to obtain a good device for successful usage as electronic switch.

V_{th}/V_{ON} V_{th} indicates the value to overcome from the gate electrode to achieve an accumulation region in the interface between semiconductor and dielectric layer. This value can be evaluated by a linear extrapolation in the I_D-V_G plot (for low V_D) or in the $I_D^{1/2}$-V_G one (for high V_D).

V_{ON} indicates the gate voltage value for which the drain current starts to grow, as it is shown in the transfer characteristic reported in Figure 1.4.

Subthreshold swing (S) S is defined as the inverse of the maximum slope of the transfer characteristic. It represents the necessary V_G to increase I_D by one decade.

$$S = \left(\frac{\partial log(I_D)}{\partial V_G} \bigg|_{max} \right)^{-1}. \tag{1.3}$$

Mobility (μ) Mobility is related to the efficiency of carriers transport in a material and is directly connected to the maximum I_D and switching speed of the devices. For instance, it has a direct impact on the maximum operating frequency or cutoff frequency (f_{co}), which can be defined as:

$$f_{co} = \frac{\mu V_D}{2\pi L^2}. \tag{1.4}$$

The mobility is directly affected by the scattering mechanisms present in the material, for examples by lattice vibrations, ionized impurities, grain boundaries and other structural defects. In the case of TFTs, where the charges have to flow in a narrow region near the dielectric interface, we have to consider other mechanisms of scattering such as Coulomb scattering from dielectric charges and from interface states or surface roughness scattering.

As it has already been said, the mobility is modulated by V_G and for this reason, depending on the regime, several type of mobility can be calculated [1]:

- *Effective mobility* (μ_{eff}) Obtained by the conductance ($g_d = \frac{L \cdot I_D}{W \cdot V_G}$), with low V_D:

$$\mu_{eff} = \frac{g_D}{2\pi L^2}. \tag{1.5}$$

This value is difficult to obtain because it requires the knowledge of V_{th}. Besides this is very sensitive to contact resistance because of the low V_D.

- *Field Effect mobility* (μ_{FE}) Obtained by the transconductance ($g_m = \frac{\partial I_D}{\partial V_G}$), with low V_D:

$$\mu_{FE} = \frac{g_m}{C_i \frac{W}{L} V_D}. \tag{1.6}$$

This value is easier to obtain because the transconductance is extractable from the transfer characteristic and it doesn't require the knowledge of V_{th}. On the opposite side, this mobility is affected by the contact resistance too.

- *Saturation mobility* (μ_{sat}) Obtained with high V_D:

$$\mu_{sat} = \frac{\left(\frac{\partial \sqrt{I_D}}{\partial V_G}\right)^2}{\frac{1}{2} C_i \frac{W}{L} V_D}. \tag{1.7}$$

This mobility doesn't require V_{th} and it is less sensitive to the contact resistance but it describes a situation where the channel is pinched-off and its effective length is smaller than L.

1.1.3 Present and future semiconductors for TFTs

In this section an overview and a comparison between the most important TFT technologies is reported. The most common class of semiconductors used as active layer in TFTs are a-Si:H, polycrystalline Si, organic and oxide semiconductors.

The maturity of a-Si:H TFTs technology is unquestionably greater than any of the other technologies. But, during the last decades a great industrial and research implementation has been done to introduce alternative technologies. Besides, the increasing interest in flexible and transparency electronic devices has conduced to the emergence of oxide and organic semiconductor technologies.

Poly-Si offers the advantage to present the greatest electrical mobility (it can exceed 100 cm^2 V^{-1} s^{-1}) and a great stability. On the other hand this technology shows a great disadvantage regarding large area deposition: short-range non

uniformity due to the grain boundaries. The electrical properties of this polycrystalline semiconductor are strongly dependent from the grain size and orientation. On the opposite side a-Si:H, organic and oxide semiconductors can all exhibit amorphous structure that is the most adapt to the large area deposition.

Both a-Si:H and poly-Si technologies require high temperature (over 300 °C) during the fabrication process to exhibit the best performances. On the contrary, devices based on organic or oxide semiconductor can be processed at room temperature and this fact keeps the cost of production lower and makes it possible to use cheap substrate like glass or even plastic.

Finally, even if the higher electrical mobility is attributed to the poly-Si technology, oxide semiconductors exhibit a mobility one order of magnitude higher than the one presented by a-Si:H or organic devices ($<$1 cm^2 V^{-1} s^{-1}).

Oxide semiconductors are quite sensitive to electrical stress. On the other hand they exhibit a great stability if compared with organic or a-Si:H to the exposure to the visible light due to their huge energy gap ($E_G > 3$ eV).

Since the first report about amorphous oxide semiconductors (Nomura et al., 2004 [9]), this new class of materials caught significant attention worldwide because of their potential in achieving high mobility, excellent spatial uniformity of the devices parameters, and good scalability to large substrate sizes.

1.2 Amorphous Oxide Semiconductors

During the last decades amorphous oxide semiconductors (AOSs) are widely involved as new channel materials in thin-film transistors (TFTs) for large-area, flexible flat-panel displays and other giant-microelectronics devices.

Two of the most studied binary oxides are ZnO and In_2O_3. These oxides have been investigated intensively because their structure is expected to exhibit better performance than a-Si:H and organic TFTs owing to their large Hall mobility (200 cm^2 V^{-1} s^{-1}). However, both these binary compounds present a great limitation for the large-area production: they form polycrystalline structures even if deposited at room temperature. This feature is undesirable because of the consequent short-range non uniformity due to the grain boundary.

Because of the inhibition of the transport caused by grain boundary, amorphous materials started to be investigated. These kind of structure in fact eliminates the effects of the boundaries and demonstrates to be the most adapt especially

for devices covering large areas. Amorphous Si (a-Si:H) with its use in active-matrix flat-panel displays was the first amorphous semiconductor used for the implementation of electronic devices.

Initially it is believed that the properties of amorphous semiconductors are considerably degraded compared with their corresponding crystalline phases. For instance this is the case of silicon where the mobility of c-Si reaches 1500 cm^2 V^{-1} s^{-1} while a-Si:H presents a mobility less than 2 cm^2 V^{-1} s^{-1}. This misunderstanding was corrected by the finding of large-mobility highly doped AOS in 1996 [13]. In fact, amorphous multicomponent oxide semiconductors present the particularity of exhibiting large electron mobilities greater than 10 cm^2 V^{-1} s^{-1} even in amorphous phase.

The reason for the unusual behaviour of AOS can be understood looking at the electronic structure and chemical bonding of these ionic compounds (Figure 1.5 **(a,b,c)**).

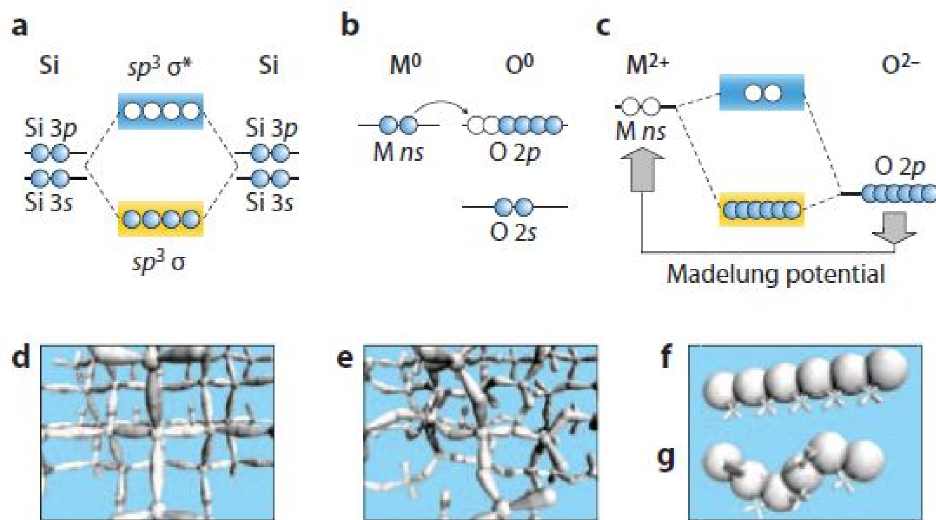


Figure 1.5: Schematic electronic structures of silicon and ionic oxide semiconductors. Bandgap formtion in **(a)** colvalent and **(b,c)** ionic semiconductors. Carrier transport paths in **(d)** c-Si, **(e)** a-Si, **(f)** crystalline oxide and **(g)** amorphous oxide [12].

In silicon, the conduction band minimum (CBM) and valence band maximum (VBM) are made of anti-bonding (sp^3 σ^*) and bonding (sp^3 σ) states of Si sp^3 hybridized orbitals, and its bang gap is formed by the energy splitting of the σ^*-σ levels (Figure 1.5**(a)**). By contrast, oxides have strong ionicity and charge transfer occurs from metal to oxygen atoms (Figure 1.5**(b)**), and the electronic structure is stabilized by the Madelung potential formed by these ions, raising the electronic

levels in cations and lowering the levels in anions. Consequently, the CBM is primarily formed by the unoccupied *s* orbitals and the VBM of cations by fully occupied O *2p* orbitals (Figure 1.5**(c)**). The separation between the two band edges results ≥3 eV and such a wide band gap assures the optical transparency of this materials.

The CBM of the AOSs are mainly formed by the empty *s* orbitals of the heavy metal cations. This post-transition metals present this electronic configuration: $(n-1)d^{10}ns^0$. For the elements with $n>4$, the size of the spherical *s* orbital exceeds the inter-cation distance and forms a largely hybridized CBM with broad band dispersion, which is the reason for the small electron effective mass. Besides, the overlapping of the spherical *s* orbitals are not altered appreciably by the disordered amorphous structure. As we can see in Figure 1.5 **(d,g)** in the AOSs the electronic levels of CBM are insensitive to the local structural randomness, and electron transport is not affected significantly [12].

The AOS material can be doped, but, due to the flexibility of the ionic bond, this is not achieved by introducing different valence atoms, but most commonly occurs via the oxygen vacancy. The vacancy results in a non-bonded metal cation producing a shallow donor level. As we can see in Figure 1.6 a-IZO has higher electron mobilities than a-IGZO, but is much more difficult to control at the low electron concentrations required for TFTs to ensure a low off-current (*e.g* far below 10^{17} cm^{-3}).

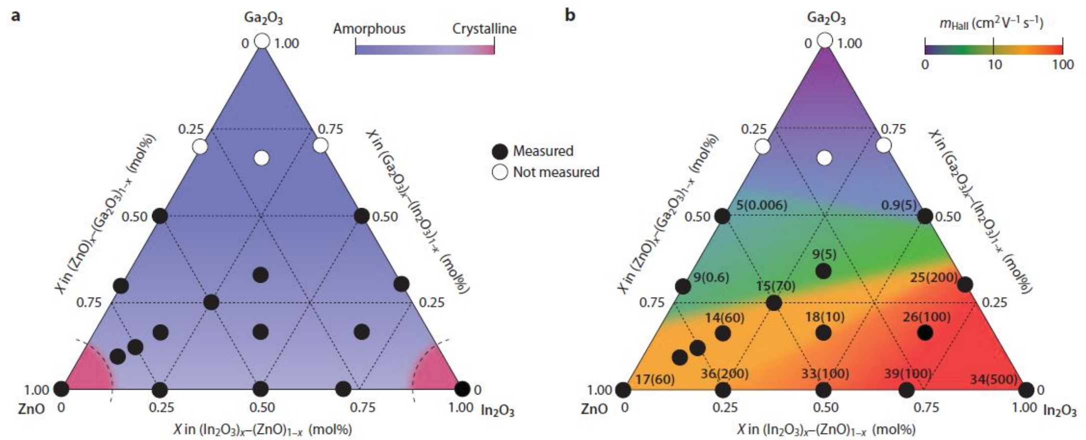


Figure 1.6: **(a)** Amorphous formation and **(b)** electron transport properies of In_2O_3-Ga_2O_3-ZnO thin films. The values in **(b)** denote the electron Hall mobility (cm^2/V s) with density (10^{18} cm^{-3}) in parenthesis. [12].

Gallium plays an important role in this respect: Ga-O bonds are much stronger than In-O and Zn-O bonds, meaning that the incorporation of Ga suppressed the formation of oxygen deficiencies and the consequent generation of mobile electrons. In addition, the free carrier concentration can be further reduced by increasing the oxygen partial pressure during sputtering deposition of the semiconductor. For this reason, $InGaZnO_4$ (IGZO) results the preferred composition for TFTs, even though it is not the highest mobility material. [16]

1.3 Flexible oxide thin film transistors

1.3.1 a-IGZO as active layer

As it has been discussed in the previous sections, amorphous oxide semiconductors are expected for channel materials of large-area and low temperature thin-film transistors because they exhibit good performances such as a field-effect mobility of 10 cm^2/Vs even if fabricated at room temperature. A number of AOS TFTs, which include amorphous In–Ga–Zn–O (a-IGZO), In–Zn–O, In–Ga–O, and Sn–Ga–Zn–O, have been reported since the first report in 2004 [9].

Amorphous-IGZO is now considered the most favorable material for practical TFTs because a-IGZO TFTs satisfy all the requirements for practical applications such as liquid crystal displays (LCDs) and organic light-emitting diode (OLED) displays. Therefore, several prototype displays including active matrix (AM) color electronic papers and AMOLED displays have been demonstrated. The a-IGZO TFT technology is rapidly expanding to more practical prototypes such as AMOLED and AMLCD high-resolution displays. [17]

The main advantages presented by the AOSs are reported as follows [12] [11]:

Low processing temperature Oxide TFTs exhibits great performance even if fabricated at room temperature. This temperature makes them compatible with inexpensive substrates as glass or even plastic, turning possible the concept of flexible electronics.

Large electron mobility They exhibit intermediate mobility between a-Si:H, organic and poly-Si: 10 $cm^2\ V^{-1}\ s^{-1}$. This mobilities are compatible with OLEDs, large LCDs and high-frame-rate 3D displays.

Low operation voltage The low defect density due to their electronic structures allows small S values and low operation voltage.

Large allowance in the choice of gate insulator In general, the choice of a gate insulator is critical for field-effect transistors including TFTs. However, as it will be shown in the next section, a variety of gate insulator have been examined for oxide TFTs, and good operation characteristics have been demonstrated in each case.

Excellent uniformity and surface flatness They have excellent uniformity and surface flatness owing to their amorphous structure.

Transparency This characteristic due to the large energy gap of these semiconductors can be useful in some applications like in fully transparent electronic circuits but also in the display products and in solar cells.

Ease of fabrication The conventional direct-current (DC) sputtering methods widely used for the deposition of ITO in solar cells and flat-panel displays may also be used for AOS TFTs.

1.3.2 Dielectric layer

While many research efforts on oxide TFTs focus on semiconductor layer to optimize field effect mobility and stability, the development of a high performance gate dielectric has been treated as secondary. However the dielectric layer is as important as the channel layer in a TFT because its properties determine the charge accumulation at the dielectric/semiconductor interface.

An optimal gate dielectric would be amorphous and atomically smooth, while exhibiting a large breakdown field, a low leakage current density, a large relative dielectric constant, and a low interface state density in conjunction with the channel layer. [14]

The most important gate dielectric in modern day electronics is SiO_2, thermally grown at high temperature (1000 °C) on Si. However this is not a practical option for large area electronics or electronics on plastic. In fact, a higher processing temperature is generally needed to produce gate dielectrics with low leakage current and high breakdown voltage because this temperature regime promotes a denser film growth with incorporation of fewer defects [6].

Another issue regarding SiO_2 is the dielectric thickness imposed by the continuous down-scale of the technology expected by Gordon Moore in 1965. Today's demand for miniaturization requires that in the new generation of transistors with channel dimensions below 45 nm the thickness of the SiO_2 layer must be lower than 1 nm, which represents a critical issue even for such an excellent insulator as thermal SiO_2, because gate leakage current dramatically increases due to quantum tunneling effects. [3]

Because of the incompatibility of the fabrication process and the technological limitation imposed by the geometrical dimensions, other dielectric are investigating for their implementation in the oxide TFTs.

One of the best possibility for overcoming these limitations involves the usage of materials with a higher dielectric constant than SiO_2, the so-called high-k dielectrics. As it has been discussed in the first section, the capacitance of the gate-dielectric has a great impact on transistor electrical performance. If we consider the structure gate electrode/dielectric/semiconductor as a capacitor, the capacitance of the dielectric can be expressed as follow:

$$C = \frac{A}{d} \cdot k \cdot k_0, \qquad (1.8)$$

where A rapresents the product of the length (L) and the width (W) of the channel, d is the thickness of the dielectric layer, k_0 and k are the permittivity of the vacuum and of the material, respectively. From Equations 1.1 and 1.2 it is possible to see that gate dielectric layer has an impact on the operating voltage of the TFT; an higher dielectric capacitance result in a smaller operating voltage, for the same semiconductor material and the same transistor dimensions. There are two different ways to reach an high value of capacitance: decreasing the thickness of the dielectric layer or looking for dielectric materials with high-k.

Besides the general effect on operating voltage and charge-carrier mobility in TFTs, the gate-dielectric layers have to withstand the applied electric field to prevent gate leackage. The gate current should be as smaller as possible. Considering the leackage current, the decreasing of the dielectric thickness could be a risk: in fact, since every layers have to be processed at low temperature because of the low-cost substrate, the insulating characteristics obtained are not so good.

Taking into account these observations, the best materials that permit to use a minimal gate operating voltage to induce carriers into the accumulation layer channel are the high-k dielectrics.

However, materials with very high-k present some drawbacks, such as increased parasitic capacitances and lower E_G, since for most metal oxide dielectrics E_G is inversely proportional to k (Figure 1.7 **(a)**). Even if the high-k materials allow the realization of thicker dielectric layer preserving the capacitance, if the E_G is too low, undesirable leackage current can still remain an issue. Besides, even if the E_G of the dielectric is much larger than the one of the semiconductor, it is very important that the offsets of the dielectric's VBM (for a p-type transistor) and CBM (for a n-type transistor) relatively to the ones of the semiconductor are at least 1 eV (Figure 1.7 **(b)**).

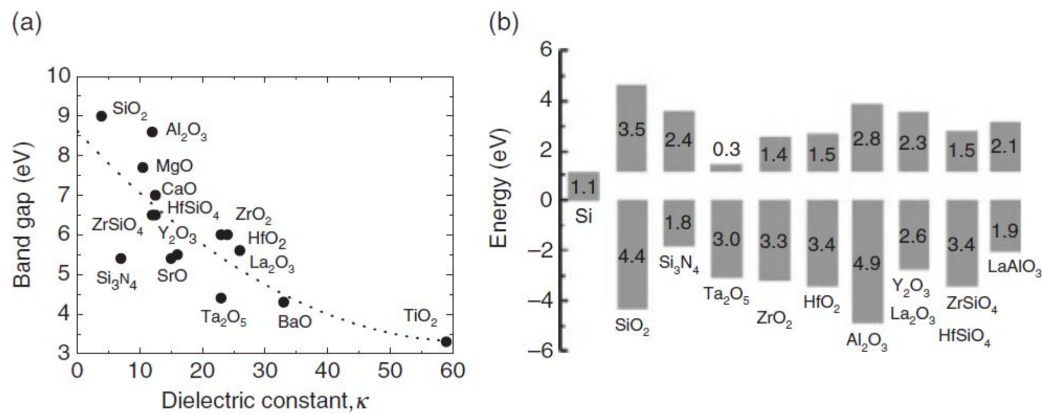


Figure 1.7: **(a)** Relation between the energy gap E_G and dielectric constant (k) of some dielectrics; **(b)** Calculated band offsets of some dielectrics on crystalline silicon [3].

Another important aspect to be considered is the structure of the dielectric material: while most of the high-k dielectrics are polycrystalline even at low temperatures, amorphous structures are preferred because grain boundaries act as preferential paths for impurity diffusion and leackage current. Besides that, amorphous materials present smoother surfaces, resulting in improved interface properties. The use of a multi-component dielectric can be a solution for this issue. By mixing a high-k/low-E_G oxide (e.g. Ta_2O_5 or HfO_2) with a low-k/high-E_G oxide (e.g. SiO_2 or Al_2O_3) it is possible to achieve a gate dielectric which allow low operation voltage, low leackage current and assures an amorphous structure.

In this work, a multilayer dielectric has been achieved using a co-sputtering technique with SiO_2 and Ta_2O_5. Ta_2O_5 is a high-k material with high sputtering rate even with low RF power, which results in low damages to the growing film and its interfaces.

Because of the oxide TFTs emerging in the field of flexible large-area electronics

and considering the implementation of this technology for the realization of inexpensive applications, alternative gate dielectrics and low-cost fabrication methods are of interest. Solution-processable polymer are started to be used as gate-dielectric layer in oxide TFTs. These materials can be deposited using low-cost fabrication methods. The most common technique is the deposition of a polymer solution (polymer dissolved in a suitable solvent) by spin-coating, spray-coating or printing and subsequent drying of the film by evaporating the solvent. Another method of forming polymeric insulating films on a substrate is the "growth" of polymers from monomers directly on the gate electrode surface. An example of this approach is poly-para-xylylene (Parylene), in which the pyrolysis of a para-xylylene dimer generates radicals that polymerize on a substrate held at room temperature forming an insulating film [18].

1.3.3 Flexibility

Flexible electronics is rapidly emerging. It is characterized by electronic circuits fabricated on organic (soft) plastic substrates instead of inorganic (hard) glasses. This area was born to meet a strong demand for large-area displays because glass substrates, which are heavy and fragile, are obviously inconvenient. Amorphous semiconductors are much preferable than crystalline semiconductors for flexible electronics. So far, organic molecule semiconductors have been almost exclusively examined but in the last years huge efforts to implement the AOSs TFTs in the field of flexible electronics started.

In terms of flexibility and material costs, plastic substrates look very attractive, and they have been the subject of considerable research, which has identified and addressed many of the problems involved in shifting from glass to plastic substrates.

Different strategies have been developed in order to fabricate TFTs on plastic substrates: direct fabrication on the plastic substrates at reduced temperatures, carrier plate and transfer plate processing. For carrier plate processing, the plastic substrates are temporarily bonded to glass carrier plates during processing, and, at its completion, the plastic substrate, plus its TFT layers, are detached from the glass. For the transfer process, the TFT layers themselves are detached from the glass, and bonded to a separate plastic substrate.

The main issues about the flexible electronic are related to the differences in

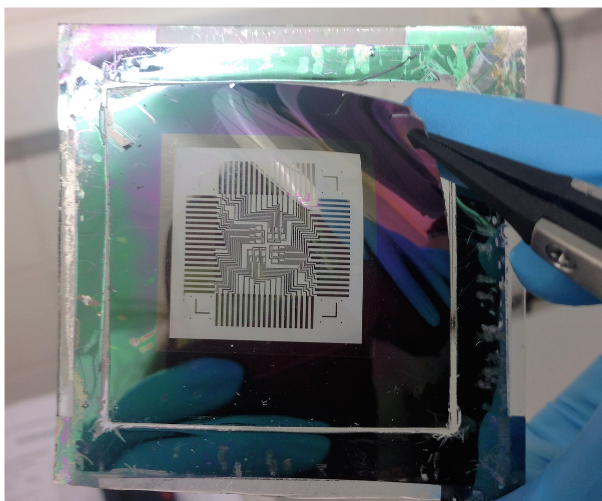


Figure 1.8: Carrier plate processing: the plastic substrate is detached from the rigid carrier at the end of the fabrication process.

thermal and mechanical properties between TFT materials and the "soft" substrate. To achieve the best electrical performance, the plastic substrates must present several properties [19]:

Optical properties - Transmissive or bottom-emitting displays need optically clear substrates.

Surface roughness - The thinner the device films, the more sensitive their electrical function is to surface roughness. Asperities and roughness over short distance must be avoided, but roughness over long distance is acceptable.

Thermal and Thermomechanical properties - The working temperature of the substrate, for example the glass transition temperature (T_g) of a polymer, must be compatible with the maximum fabrication process temperature (T_{max}). Thermal mismatch between device films and substrate may cause films to break during the thermal cycling associated with fabrication. A rule of thumb for tolerable mismatch is that the strain should be kept below 0.3%. The strain is defined as:

$$\epsilon = (\alpha_f - \alpha_s) \cdot \Delta T, \qquad (1.9)$$

where α_f and α_s are the coefficients of thermal expansion (CTE) of the device film and substrate respectively, and ΔT is the temperature excursion during processing. This rule limits further the processing temperature achievable

for the flexible devices production. Dimensional stability during processing is a concern with plastic substrates.

Chemical properties - The substrate should not release contaminants and should be inert against process chemicals. Of advantage are substrates that are good barriers against permeation by atmospheric gases. In fact, water absorption, as well as oxygen absorption, lead for a swelling of the plastic, which compromise its dimensional stability.

Mechanical properties - A high elastic modulus makes the substrate stiff, and a hard surface supports the device layers under impact.

Besides, for photolithography, good dimensional stability is essential for the correct registration of successive mask patterns. On the opposite side, plastic films show tendency to shrink at typical processing temperatures. To maintain dimensional stability throughout the TFT fabrication process, they need to be preshrunk, prior to device processing, by annealing them at the intended processing temperature.

The polymers investigated and used so far for flexible substrates include: the thermoplastic semicrystalline polymers: polyethylene terephthalate (PET) and polyethylene naphthalate (PEN), the thermoplastic noncrystalline polymers: polycarbonate (PC) and polyethersulphone (PES), and high-T_g materials: polyarylates (PAR), polycyclic olefin (PCO), and polyimide (PI). Much research has been conducted with PET, PEN, and PI (Kapton), with their relatively small CTEs of 15, 13, and 16 ppm/$°C$, respectively, relatively high elastic moduli, and acceptable resistance to process chemicals. Both PET and PEN are optically clear with transmittance of >85% in the visible. They absorb relatively little water ($\sim$0.14%), but their process temperatures are only $\sim$150 and $\sim$200/$°C$, even after prestabilization by annealing. In contrast, PI has a high glass transition temperature of $\sim$350/$°C$, but it is yellow because it absorbs in the blue. [14]

Chapter 2

Thin film transistors fabrication process

During this work several thin film transistors have been fabricated (*Chapter 4*). The fabrication process is described by the scheme in Figure 2.1. In this chapter we will focus on the techniques used to realize these devices, describing their main characteristics and phisical properties and indicating the facilities used.

Firstly, I will introduce the photo-lithogrphy and etching process used to transfer the desired pattern from the photomasks to the samples with a micro-scale resolution.

In the second part of this chapter, I will discuss the two main deposition techniques used during this work: sputtering and chemical vapor deposition (CVD).

Finally, I will present a brief discussion about the post-annealing treatment.

2.1 Optical Lithography

Optical lithography is a technique which allows to transfer a desired pattern from a photomask to the surface of a sample. The substrate is covered with a photosensitive solution (called photoresist, PR) and a UV lamp is used for the exposure. The exposure occurred only in selected regions of the sample uncovered by the photomasks and only in the illuminated area the chemical properties of the photoresist change.

There are three elements in the photolithography process:

- *Optics:* radiation generation, propagation, focusing, diffraction, interface;

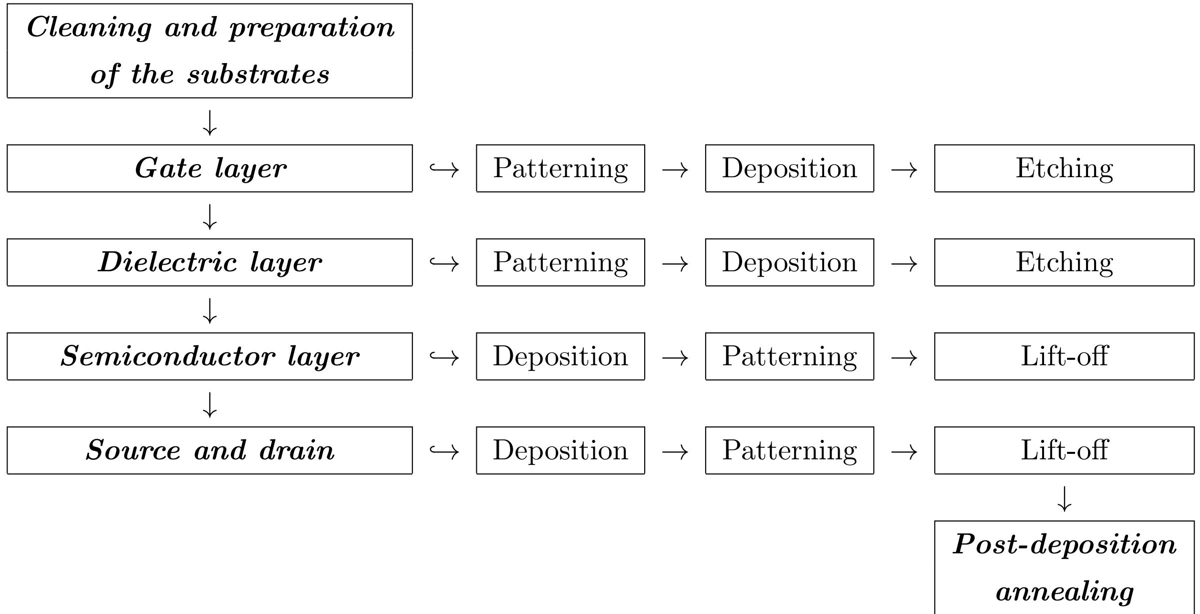


Table 2.1: TFTs fabrication process.

- *Chemistry:* phtochemical reactions in the resist, development;
- *Mechanics:* mask to substrate alignment.

Following, I will describe the several steps of the photolithography process.

Spin coating

Spin coating is the standard resist application method. It is a non-vacuum deposition technique which offers some advantages such as the fast processing time and a low equipment cost. Typically this process involves the application of a thin film onto the surface of a substrate by coating a solution of the desired material in a solvent while it is rotating. The substrate is held in vacuum to a chuck which rotates at high speed. The thickness of the obtained photoresist layer depends on the deposition conditions such as the rotating velocity and acceleration, but also on the intrinsic properties of the deposited material (i.e. viscosity, drying rate, surface tension).

Resistants have three main components [20]:

Base resin which determines the mechanical and thermal properties;

Photoactive compound which determines sensitivity to radiation;

Solvent which controls viscosity.

In this work, the photoresist *AZ6632* has been deposited by *Headway Research, Inc, model PWM32* spin coater. To reach a uniform layer 1.2 μm thick, a two steps process has been used: **step 1** 10 s , 3000 rpm for covering the entire substrate; **step 2** 20 s, 4000 rpm to reach the desired thickness.

Soft Baking or Prebaking

A drying step called *soft baking*, or *prebaking*, is typically used to improve adhesion and to remove solvent from the photoresist. The prebake step involves the physical removal of the casting solvent without the degradation of the resist components. By removing the casting solvent from the film, a solid state is formed which prevents mixing of the exposure products with the unexposed zone. Since the prebake process can have an effect on subsequent processes such as exposure and development of the image, the prebake process should be precise, uniform across the wafer, and reproducible. [22]

To this end, after the deposition of PR, the samples were placing on an hot plate at 118 °C for 1'15" to induce the evaporation of the solvent and to improve the adhesion of the resist with the substrate.

Mask Alignment

The complex pattern from a photomask, a square glass plate with a patterned metal film on one side, must be transferred to the surface of the substrate.

In proximity lithography a small gap, e.g. 3 to 50 μm, is left between the mask and the substrate. During the exposure, the UV beam hits the mask and passes through it only in the region specified by the pattern. The obtained image is the same size as the original. To evaluate the resolution of the lithographty process, Fresnel diffraction formulae have to be used:

$$R = 3 \cdot \sqrt{\frac{\lambda}{n} \times \left(g + \frac{d}{2}\right)}, \tag{2.1}$$

where R indicates the minimum resolvable period, λ is the wavelength of exposing radiation, g is the gap between the mask and PR, d represents the resist thickness and n is the resist refractive index.

During the phase of alignment, both the mask and the sample are inserted into a mask aligner. The substrate is held on a vacuum chuck and carefully moved into position below the mask using an adjustable x-y stage. In fact, each mask following the first must be carefully aligned to the previous pattern on the sample. A good alignment is essential to realize working devices and alignment marks (i.e. crosses or lines) are used for this purpose.

During this work a *Karl-Suss MA6* has been used as mask aligner (see Figure 2.1).

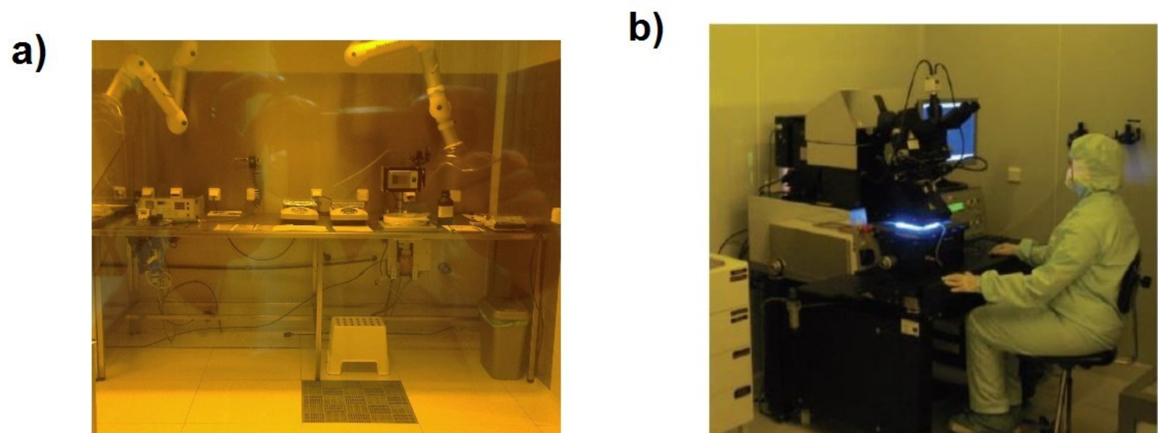


Figure 2.1: a) Picture of the Yellow zone existing at CEMOP laboratories; spin coaters and hot plates. **b)** Mask aligner used during this work [4].

Exposure

The exposure step can be executed in proximity or in contact mode. Despite the contact lithography presents the best resolution in term of dimensions (see Eq. 3.2), the risk to damage the mask makes contact printing not very production worthy. Proximity lithography is a modification of the latter and it has been used during this work.

A mercury lamp is used to produce UV radiation that uniformly goes through the photomask. This light source has an emission spectrum which matches the photoresist absorption one. When the PR is exposed to the UV light, its chemical properties change and this feature is the key point of the developing step and it makes possible the patterning of the layers.

The photoresists are sensitive to the UV rays and to the blue part of the visible spectrum. For this reason, in the room where the photolithography takes place a yellow light is present (see Figure 2.1 **a**).

Development

In this paragraph I will present fistly the conventional development process which involves a *positive photoresist* and the subsequent etching of the sample. At the end of the section I will discuss some variations to this standard process.

The developer is able to remove the PR wherever the previously deposited material has to be eliminated by etching. Depending on the photoresist used, different developer are available.

During this work, a positive PR has been used. This means that, when the UV rays hit the PR uncovered by the mask, the photoresist exposed releases carboxylic acid and becomes soluble in an alkaline developer. Hence, washing the substrate with the developer, permits to obtain only the desired pattern covered by the PR (see Figure 2.2**a**). This layer of photoresist will protect the deposited material during the etching phase.

After the etching of the uncovered thin film, all the PR has to be stripped from the sample. To this end, the dipping of the sample into a liquid that dissolves the PR is necessary. In this work the samples have been washed into acetone and after they have been rinsed by ultra pure water.

The same result can be achieved using a different type of PR: *negative photoresist*. In this case, the solubility of the PR decreases in the region exposed to the UV because of a polymerization reaction. Therefore, since only the exposed PR remains to protect the underlayer deposited material, a "negative" mask has to be used to obtain the desired pattern onto the substrate.

Lift-off An important deviation from the conventional development process just described is represented by a different technique called *lift-off* (see Figure 2.2**b**). Herein a positive PR and a "negative" mask are used.

In this case the optical lithography precedes the deposition of the material that has to be patterned. After the deposition, the sample is directly stripped and both the PR and the material deposited on the top are removed. During this work, the lift-off has been accomplished using acetone (twice), IPA to avoid striations on the

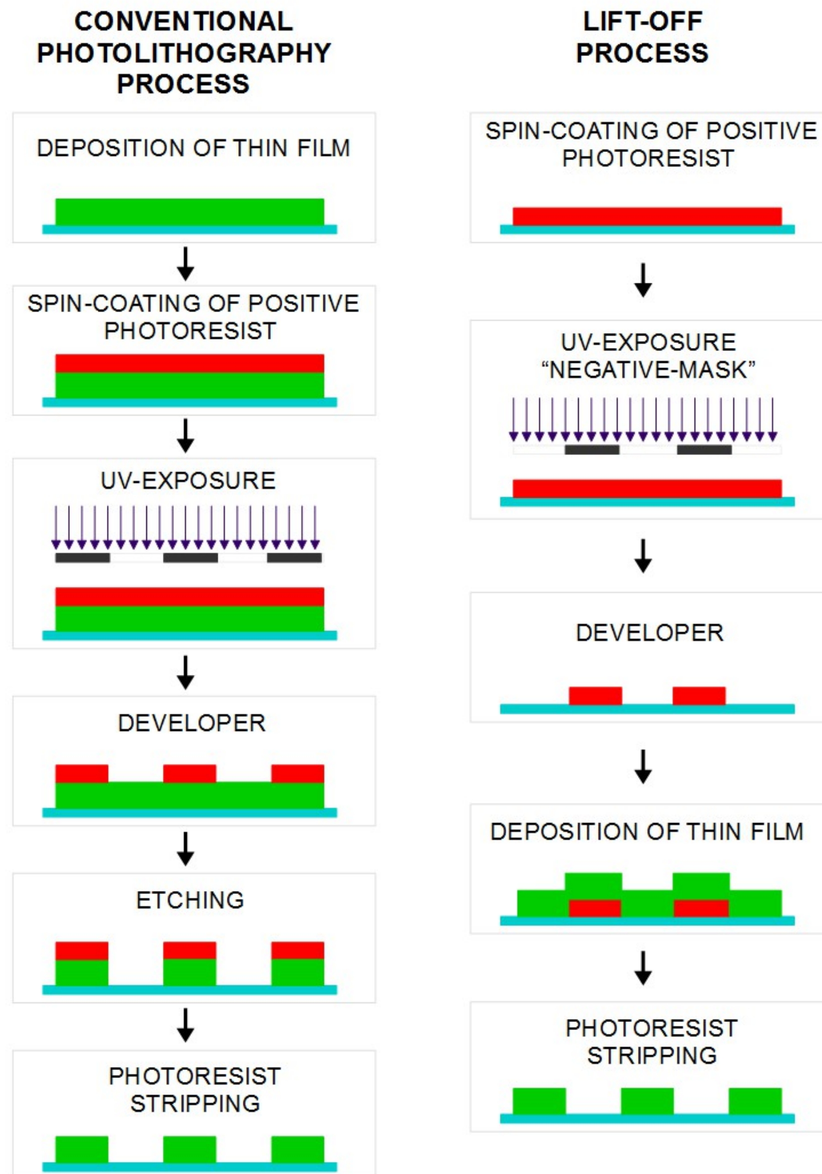


Figure 2.2: Several steps regarding **a)** conventional lithography process; **b)** lif-off process.

substrate and ultra-pure water.

The lift-off results preferable compared to the etching for preventing damages to the underlayer materials. On the opposite side, this technique leads to less defined structures and it can be used only to pattern thin layers.

During this work, the lift-off has been used for the semiconductor layer and to pattern the source and drain electrodes.

Finally, during this work, a positive photoresist (*AZ6632*) and a metal ion free

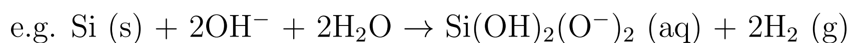
developer, *AZ 726 MIF*, primarily composed by tetrametil ammonium hydroxide have been used.

2.2 Etching

After the lithographic resist patterning, the etching of the underlying material occurs. A high degree of selectivity is required so that the etchant removes the unprotected layer much more rapidly than it attacks the photoresist layer [21].

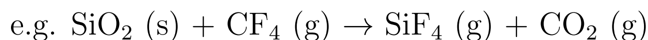
Etching is often divided into two classes: *wet etching* and *plasma etching*. These two types of etching are mainly distinguishable for the basic reactions involved [20]:

Wet etching solid + liquid etchant → soluble products



e.g. $Si\ (s) + 2OH^- + 2H_2O \rightarrow Si(OH)_2(O^-)_2\ (aq) + 2H_2\ (g)$

Plasma etching solid + gaseous etchant → volatile products



e.g. $SiO_2\ (s) + CF_4\ (g) \rightarrow SiF_4\ (g) + CO_2\ (g)$

Moreover, while wet etching is accomplished into a heated quarz bath, the plasma etch equipment consists in a vacuum chamber with a RF-generator and a gas system.

For both these two classes, there are three steps that must take place for etching to proceed:

- transport of etchants to surface;
- surface reaction;
- removal of product species.

In the next paragraphs I will briefly discuss the two procedures.

Wet Etching

Wet etching is a material removal process that uses liquid chemicals or etchants to remove the uncovered materials from a substrate. This process involves multiple chemical reactions that consume the original reactants producing new ones. After the diffusion of the liquid etchant to the structure that has to be removed, the

chemical reaction occurs (typically a reduction-oxidation reaction). Finally the diffusion of the byproducts from the reacted surface completes the process. [23]

Wet chemical etching tends to be an isotropic process, etching equally in all the directions. This means that the etching process attacks the material under the resist by a distance equal to the thickness of the film (see Figure 2.3). This *undercutting* becomes a serious problem in processes requiring line widths really small ($< 1\mu$m).

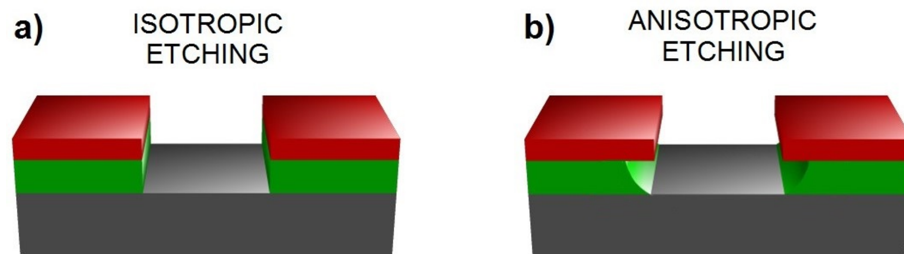


Figure 2.3: **a)** Anisotropic and **b)** isotropic etching.

Several problems can affect this kind of procedure: the reaction products may hinder the etching reaction, etching reaction can produce substances that catalyse the reaction, etching reaction can be exothermic and temperature rises during etching.

However, wet etching presents an high level of selectivity and an etch rate of 10-100 nm/min. Moreover, the equipment for this procedure is very cheap if compared to plasma etching

Dry Etching

Dry etching, as opposed to wet etching, is often used as a synonym for plasma etching even if there are dry methods that do not involve plasma. In dry etching, plasmas or etchant gasses remove the substrate material. The reaction that takes place can be done involving high kinetic energy of particle beams, chemical reaction or a combination of both.

Plasma etching has been an indispensable tool since the early 1980s, and it has always offered the possibility to etch, with high precision, those structures that lithography has been able to print. As a matter of fact, this procedure is an highly anisotropic type of etching that avoids the undercutting problem (see Figure 2.3) characteristic of wet processes. Besides, dry etching requires only small amount of

reactant gasses, whereas wet etching requires disposal of relatively large amounts of liquid chemical wastes.

Plasma systems use RF excitation to ionize a variety of source gases in a vacuum system. These ionic gases are accelerated by the RF field and impart energy directionally to the surface. The mode of operation depends upon the operating pressure, temperature, power, gas flows and on the reaction causes the removal of the material. Three different kind of dry etching can be distinguished.

Physical dry etching Etching occurs by physically knocking atoms off the surface of the substrate. Highly anisotropic etching can be obtained, but selectivity is often poor.

Chemical dry etching This process involves a chemical reaction between etchant gases to attack the surface of the sample. This kind of procedure is usually isotropic and exhibits high selectivity.

Reactive Ion Etching (RIE) This mode of operation combines physical and chemical mechanisms to achieve high levels of resolution. In RIE, plasma systems are used to ionize reactive gases, and the ions are accelerated to bombard the surface. Etching occurs through a combination of the chemical reaction and momentum transfer from the etching species. This technique combines an high level of anisotropy and a good selectivity.

During this work dry etching has been used and it has been realized by *TRION PHANTOM III RIE*. The molibdenum gate layers have been etched using a SF6 flow. Then, for the dielectric layers two different gasses have been used: for the Parylene dielectric O_2 was the reactive gas while, for the multilayer SF6 has been used. Since this latter is able to react with the underlayer Mo, a test to check the time necessary to etch only the dielectric and avoid the removal of the gate layer had been necessary. RT and 50 mTorr were the temperature and pressure conditions for all the etching processes.

2.3 Sputtering deposition

Physical vapor deposition (*PVD*) and chemical vapor deposition (*CVD*) are the two typical deposition methods.

The general idea of PVD is particles ejection from a solid target material and transport in vacuum to the substrate surface. PVD is divided into two categories depending on the technique used to evaporate the solid source materials into the vapor phase: thermal evaporation and sputtering. Herein I will focus on the sputtering technique.

Compared to other thin-film deposition methods, sputtering presents several advantages: low substrate temperatures (down to RT and fundamental for polymeric substrates implemented in the flexible electronics), good adhesion of films on substrates, high deposition rate, uniformity of the thickness and high density of the films, relatively cheap deposition method, possibility to deposit a broad range of materials (either by using different target compositions, a reactive gas or simultaneous sputtering from two or more target sources) and good scalability to large areas [24].

By first creating a gaseous plasma and then accelerating the ions from this plasma into a target composed by the material that one wants to deposit, the source material is eroded by the arriving ions via energy transfer and it is ejected in the form of neutral particles. Gaseous plasma is a dynamic condition where neutral gas atoms, ions, electrons and photons exist in a near balanced state simultaneously. An energy source is required to maintain this state. The neutral particles ejected by the target would travel in a straight line, but because of the entity of sputtering pressure (from 1 to 10 mTorr) they will experience many collisions before reaching the substrate. This phenomena is called *thermalization* and it leads to positive and negative consequences: on one side the sputtered particles cool down reducing their energy before reaching the substrate and this avoids the damage of the sample and decreases the re-sputtering rate; on the other side, these collisions decrease the number of particles reaching the substrate and the sputtering rate results lower.

As Figure 2.4 shows, this technique occurs in a vacuum chamber containing two electrodes: the cathode including the target and the anode covered by the substrate generally grounded. Then an inert gas is introduced into the chamber, typically argon due to its low cost and high cross section, and an electric field is created between the two electrodes. Due to this field, ever present electrons are accelerated towards the anode and are able to ionize or excite the neutral gas atoms encountered in their path.

When the excited argon atoms come back to the original electronic configuration, the emission of photons occurs creating the so-called glow discharge. On

the other side, Ar^+ are accelerated toward the cathode electrode sputtering the surface and creating new free electrons which feed the formation of ions and the continuation of the plasma. An important issue related to these secondary electrons is the fact tht they could reach the substrate causing damages to the layer and re-sputtering of the growing film.

The most important processes of the glow discharge occur close to the target surface. In this region a high positive charge is accumulated because electrons are quickly accelerated away from the cathode because of their small mass compared to the ions' one. This strong field generated in front of the target provides the ion acceleration necessary to sputter the atoms from the target.

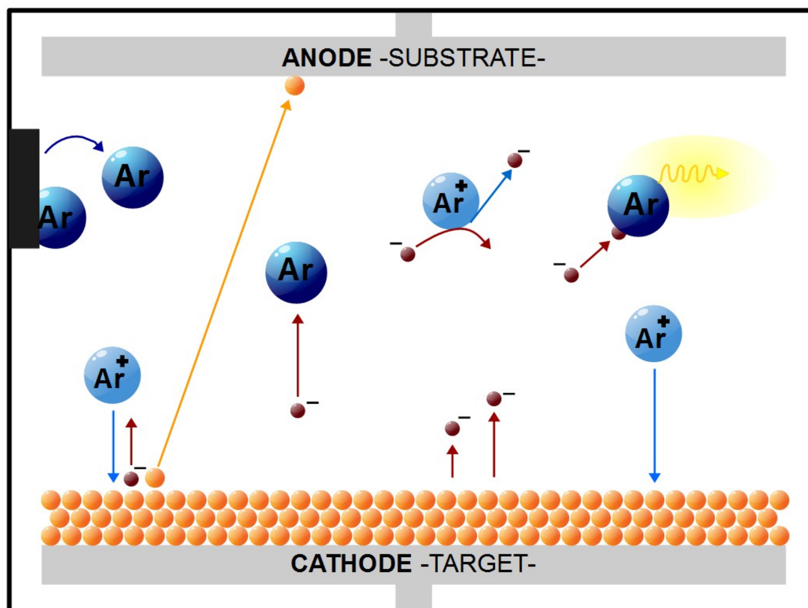


Figure 2.4: Scheme rapresenting a typical sputtering process.

In order to obtain the sputtering process, the incident ions have to possess a kinetic energy larger than a threshold value to achieve a *sputter yield* (Y) higher than the unity. Y is a measure of the number of atoms ejected from the target for each bombardment ion. The yield depends on the ion incident angle, the energy of the ions, the masses of the ions and target atoms, the surface binding energy of atoms in the target, and the crystalline orientation of the target when crystals are used as the source material.

Sputtering can also be accomplished by using a reactive gas inside the system such as oxygen or nitrogen (*reactive sputtering*). However, the high electronegativity related to some of this element (e.g. oxygen) can cause some troubles during

the deposition. In fact a high concentration of these reactive gases can induce re-sputtering in the substrate due to the incidence of the negative ions.

Now the main three types of sputtering are presented: DC, RF and magnetron. The first two types are known as *diode sputtering*.

DC sputtering involves a DC bias between the cathode and the anode. Even if this is the simplest configuration, it inhibits the usage of insulator materials as targets. In fact insulators are not able to supply the target surface with sufficient secondary electrons to maintain the glow discharge.

On contrary, **RF sputtering** can operate both with conductive and insulator target materials. In fact, since high frequency voltage is supplied to the target, even if the target does not supply enough secondary electrons during the negative portion of RF signal, electrons are attracted towards the target during the positive portion of the RF signal. Since the target area is much smaller than the grounded anode and given the lower mass of electrons relatively to ions, a self-biased d.c. voltage emerges in the target, creating the conditions for sputtering to occur.

These two techniques present two main problems: they show low deposition rate and the electron bombardment of the substrate is extensive and can cause overheating and serious structural damage. **Magnetron sputtering** (see Figure 2.5) offers good solutions to overcome both of these issues.

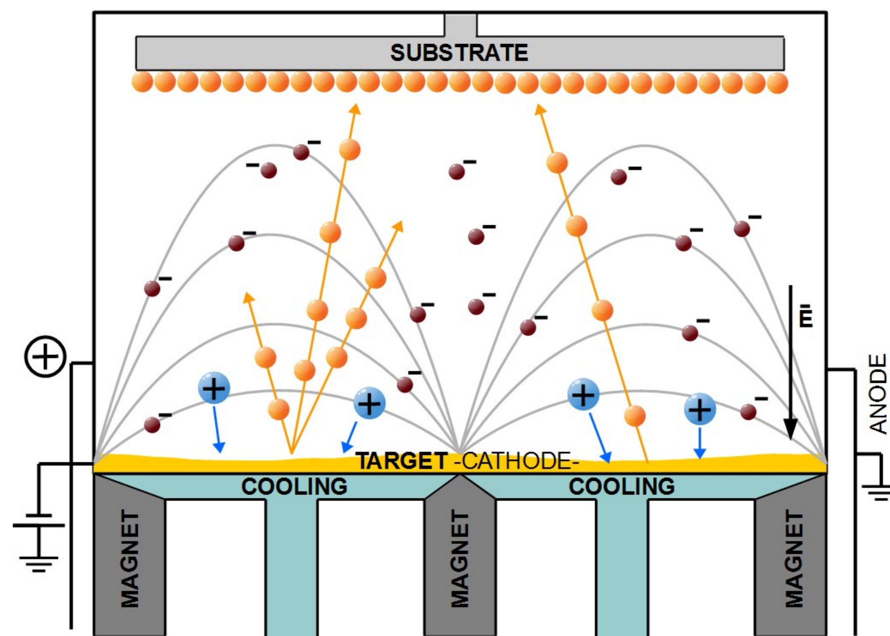


Figure 2.5: Magnetron sputtering.

This technique implements magnets behind the cathode to trap the free electrons in a magnetic field directly above the target surface. Therefore, these electrons are not free to bombard the substrate and at the same time, they enhance their probability of hitting and ionizing a neutral gas molecule. This increase of ionized gas improve the sputtering rate. Because of higher ionization rates, plasma can be sustained at a lower pressure. A disadvantage presented by magnetron sputtering is the poor target utilization, since the material is preferentially eroded in the areas defined by the magnetic field.

During this work, Electrodes layers, a-GIZO semiconductor and the multilayer dielectric were deposited by *rf* magnetron sputtering without intentional substrate heating during the process. *AJA ATC-1300F* and *AJA ATC 1800-S* existent at CEMOP have been used for this purpose (see Figure 2.6). The a-GIZO deposition has been accomplished from a multicomponent ceramic target with 1:2:2 (atomic Ga:In:Zn ratio) composition, with the addiction of oxygen to the Ar flow.

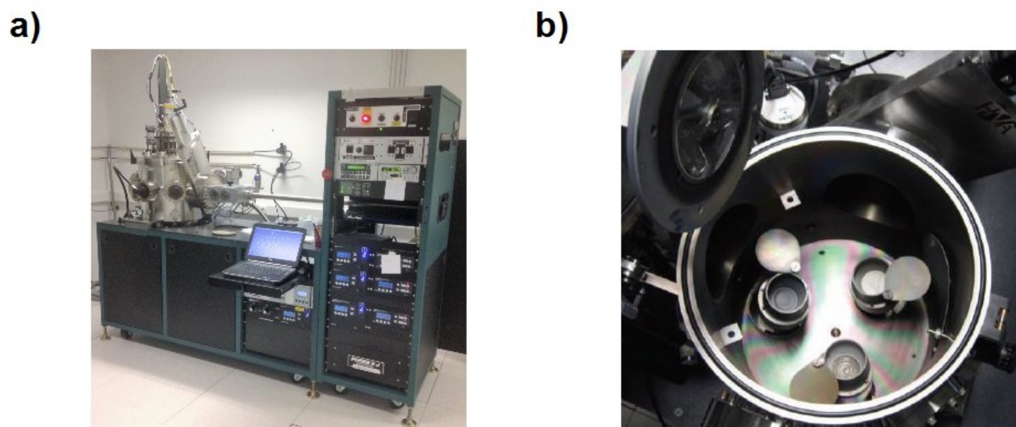


Figure 2.6: a) *AJA ATC 1800-S*. **b)** Main chamber of *AJA ATC-1300F*; three targets are shown.

2.4 Chemical vapor deposition

Chemical vapor deposition (*CVD*) forms thin films on the surface of a substrate by thermal decomposition or reaction of gaseous compounds. The desired material is deposited directly from the gas phase onto the surface of the substrate.

This technique has been used to deposit the Parylene dielectric layers.

Parylene is a unique polymer consisting of a linear chain of Benzene rings with two Methylene groups replacing 2 Hydrogen atoms on opposite sides of the Benzene ring serving as coupling links for the polymer. This material offers some good properties such as the imperviousness to water transmission. This quality makes Parylene one of the most popular material to encapsulate circuits and devices. Besides, because of its good insulation properties, recently it starts to be studied as dielectric layer in the field of organic electronic and it has been experimented as insulator layer in oxide-based devices. Moreover, the optical transparency and the ability to execute the deposition process at room temperature make this polymer very desirable for transparent flexible electronics. [29]

Figure 2.7 **a)** shows the steps composing the Parylene deposition process.

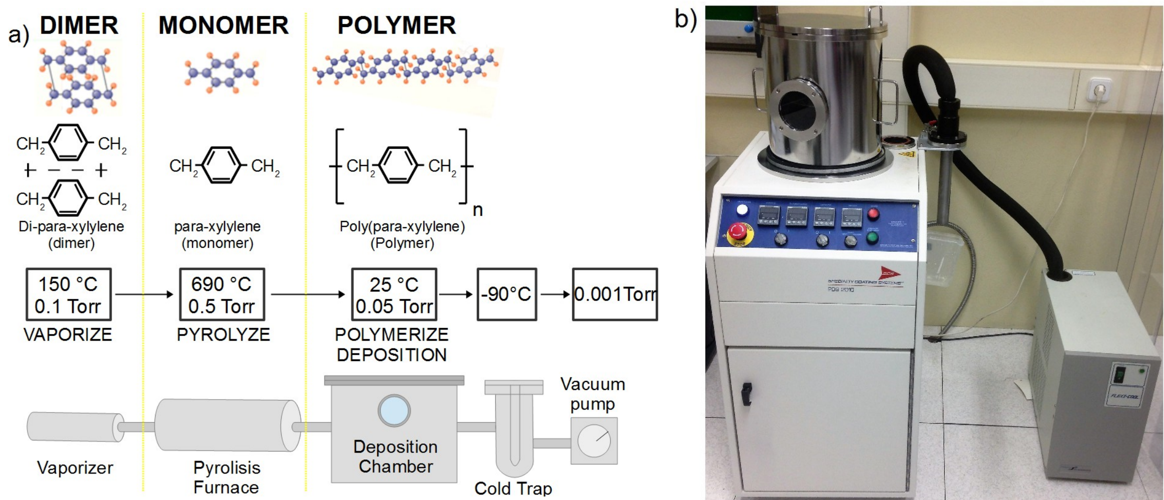


Figure 2.7: a) Parylene deposition process. **b)** SCS Labcoter® Parylene Deposition System (CVD-PDS-2010).

The source material for the deposited film is a dimer form of the parylene molecule in which two monomers are coupled in parallel by the Methylene ends. The dimer is sublimated in a Vaporizer chamber, broken into monomer molecules in the Pyrolizer furnace and then deposited as long chain polymers on substrates in the deposition chamber. The exhaust is pumped into a liquid-Nitroger trap by a mechanical oil trap. The cold trap serves to prevent vapors being evacuated from the process from entering the vacuum pump where they would condense and contaminate all the system.

Parylene C has been implemented as dielectric layer in some of the fabricated samples using *CVD-PDS-2010* (see Figure 2.7**b**). This kind of polymer differs

from the standard one because of the substitution of a Cl atom instead of one of the aromatic H. An adhesion promoter consisting of Sylane A-147 was used during the deposition in order to improve the adhesion between parylene-C and the underlayers [30].

2.5 Post-deposition annealing

Properties of thin films can be modified by several post-deposition process. For instance post-deposition annealing leads to a marked improvement of the TFTs electrical performance. Especially in oxide TFTs, where the oxygen concentration is one of the key parameter influencing electrical behaviour, the annealing implies large consequences. Many experiments showed [31] that thermal treatments reduce the density of electron traps enhancing TFTs performance and stability.

Increasing temperature can also have a great impact on other properties of thin films and devices by promoting the crystallization of initially amorphous structures and/or by modifying interfaces, due to annihilation of surface states or interdiffusion of different elements [4].

Finally, as far as the flexibility is concerned, post-deposition annealing plays an important role. In fact, thermal treatment serves to reduce the mechanical stress accumulated by the devices during the entire fabrication process. However, the polymeric entity of the substrates limits the annealing temperature at a maximum of 150-180 °C.

During this work, post-deposition anealing has been performed at $T_A = 150$ °C in air using an hot plate (*Torrey Pines ECHOTerm*). The heating ramp was 7.5 °C/min and the sample have been left of the hot plate for one hour at the desired temperature.

Chapter 3

Scanning Probe Microscopy

During this work I characterized the fabricated devices using several techniques of investigation.

Firstly I analyzed the TFTs electrical behaviour focusing on the macroscopic properties shown by the devices. The typical parameters listed in *Chapter 1* have been extracted from standard electrical measurements. The process used for this purpose will be described in the next chapter.

In this chapter, I rather focus on the investigation technique used to study the devices in a microscopic way. To this end a Kelvin Probe Force Microscopy (KPFM) analysis has been accomplished.

Since the KPFM experimental is an Atomic Force Microscopy (AFM) based apparatus, herein I first discuss the basic operational principles and the instrumentation of AFM.

In the second part of the chapter, I present the basic principle and the operation tool of KPFM.

Finally I compare KPFM with other investigation techniques and I briefly discuss the advantages and disadvantages shown by this technology.

3.1 AFM in non-contact mode

Surface science was revolutionized in 1982 by the invention of the scanning tunneling microscope (STM) by Binnig and Rohrer [32][33]. This technique allowed for the first time to image sample surfaces with atomic resolution. Unfortunately, this technique can be used only to study conductive samples. But, in 1986 the invention of Atomic Force Microscopy (AFM) widened the range of samples from conductive

to non conductive ones [34]. Further development led to the non-contact mode of the AFM, where a *cantilever* supporting a sharp tip at its end is vibrated close to its resonance frequency and changes in the vibration due to tip-sample interaction are employed to maintain a constant distance to the sample surface while scanning across the sample [35]. Combining this technique with other measurement methods leads to the study of a huge number of sample properties maintaining the atomic resolution. Before focusing on one of the operation mode which allows to study the electrical properties of the sample (KPFM), I briefly describe the basic operational principles and instrumentation of AFM.

Basic principles

As I said, AFM exploits the interaction between the atoms of a very sharp tip and the sample surface. The interaction between two atoms separated by a distance r can be expressed by the Lennard-Jones potential

$$U(r) = U_0 \left\{ -2\left(\frac{r_0}{r}\right)^6 + \left(\frac{r_0}{r}\right)^{12} \right\}, \tag{3.1}$$

where the first term indicates the attractive force at large distance mainly produced by dipole-dipole interaction (codified by van der Waals force), the second term represents the short-range repulsion due to the Pauli exclusion principle and r_0 indicates the interatomic distance in the equilibrium condition.

Figure 3.1 represents the L. J. potential. Depending on the distance compared to r_0 one can distinguish two different forces: for $r < r_0$ the force results repulsive while $r > r_0$ leads to an attractive interaction.

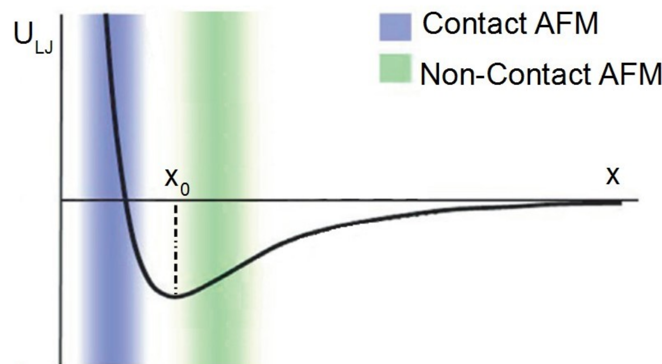


Figure 3.1: Lennard-Jones potential. Repulsive and attractive interactions are rapresented for $r < r_0$ and $r > r_0$ respectively. Adapted from [36].

These two regimes are used to implements two different AFM operation modes:

Contact mode The AFM tip touches the sample surface, and the tip-sample repulsive force deflects the tip-cantilever. Here the cantilever deflection is monitored and used as a feedback signal.

Non-contact mode The cantilever is externally oscillated at its resonance frequency. The tip-sample attractive interaction is altered as the tip-sample distance changes, leading to a change in oscillation amplitude and resonance frequency. These deviations from the reference amplitude and frequency are used as feedback signals to obtain the topography of the sample surface.

Even if, as we can see from the graph in Figure 3.1, the curve which defines the repulsive interaction presents a huge slope resulting in a greater resolution of the contact-mode compared to the non-contact one, bringing the tip into contact with the sample can caused several damage both for the tip and for the sample surface. For this reason non-contact mode is often used despite it presents a lower resolution.

In non-contact mode, the tip and the sample are separate and the weak interaction between these two cannot be measured directly by the deflection of the cantilever. So, non-contact AFM detects the changes in the phase or in the vibration amplitude of the cantilever that are induced by the attractive force between the probe tip and the sample while the cantilever is mechanically oscillated near its resonant frequency.

The oscillation of the cantilever can be described by its equation of motion, considering the tip as a point-mass spring:

$$m\ddot{z} + \frac{m\omega_0}{Q}\dot{z} + kz = F_{ts} + F_0 cos(\omega_d t), \tag{3.2}$$

where k represents the elastic (or spring) constant, Q the quality factor, F_{ts} the tip-sample interaction, F_0 and ω_d the amplitude and angular frequency of the driving force respectively.

The free resonance frequency ($F_{ts} = 0$) can be expressed by the equation

$$\omega_0 = 2\pi f_0 = \sqrt{\frac{k}{m^*}}, \tag{3.3}$$

where m^* denotes the effective mass which takes into account also the geometry of the cantilever.

When approaching the tip to the sample, the interaction forces will cause a shift of the resonance curve of the cantilever. For small oscillation amplitudes the system can be treated as a weakly perturbed harmonic oscillator. In this case the shift of the resonance curve can be approximated by introducing an effective spring constant k_{eff}:

$$k_{eff} = k - \frac{\partial F_{ts}}{\partial z}. \tag{3.4}$$

In the non-contact AFM, $\frac{\partial F_{ts}}{\partial z} > 0$ and the effective spring constant is lowered by the force gradient. Therefore, in case of attractive forces, for small force gradient a shift of the resonance curve to lower frequencies is obtained. The frequency shift can be approximated by

$$\Delta f_0 = -\frac{f_0}{2k}\frac{\partial F_{ts}}{\partial z}. \tag{3.5}$$

As one can see, this operation mode makes more sensitive responds to the force gradient as opposed to the force itself.

The quality factor Q determines the AFM resolution. In fact it is defined as

$$Q = \frac{f_0}{\Delta f_0}, \tag{3.6}$$

which represents a measure of the energy loss of the oscillation due to the interaction between the tip and the sample surface.

Hence, to obtain the topography of the sample surface, one has to record the force gradient scanning the x-y area (i.e. varying the distance tip-surface). To measure this quantity the knowledge of the frequency shift due to the tip-sample interaction is essential. Figure 3.2 shows this procedure. If one vibrates the cantilever (Figure 3.2 **b**) at a frequency f_1 (a little larger than f_0) where a steep slope is observed in the graph 3.2**a**, the amplitude change (ΔA) at f_1 becomes very large even with a small change of intrinsic frequency caused by atomic attractions. Therefore, the amplitude change measured in f_1 reflects the distance change (Δd) between the probe tip and the surface atoms (Figure 3.2**c**). If the change in the intrinsic frequency resulting from the interaction between the surface atoms and the probe or the amplitude change (ΔA) at a given frequency (f_1) can be measured, the non-contact mode feedback loop will then compensate for the distance change between the tip and the sample surface. By maintaining constant cantilever's amplitude (A_0) and distance (d_0), non-contact mode can measure the topography

of the sample surface by using the feedback mechanism to control the Z scanner movement following the measurement of the force gradient represented in Equation 3.4 [37].

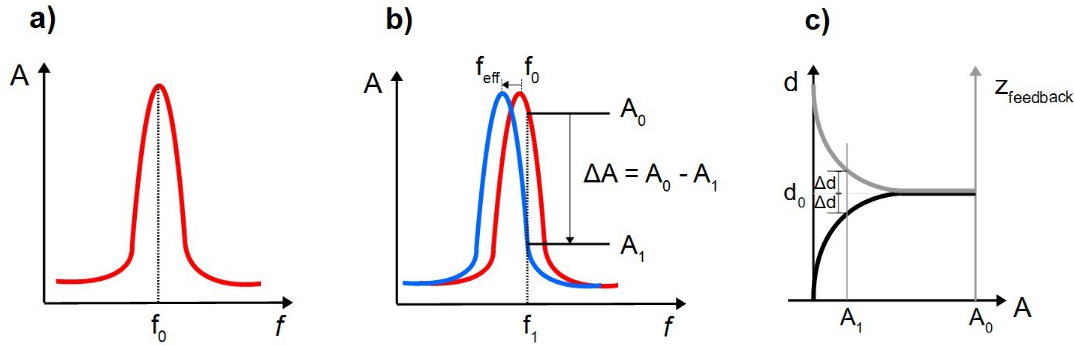


Figure 3.2: **a)** Free resonance frequency, **b)** frequency shift, **c)** distance of the tip from the sample surface (d) and z-feedback as a function of amplitude modulation. Adapted from [37]

AFM system

Herein the AFM system is described in more detail.

Figure 3.3 represents the scheme of the nc-AFM system. The sample is located on a piezo tube scanner, which can move the sample in the x-y dierections and in the z direction.

A bimorph is used to mechanically vibrate the cantilever at the desired frequency, typically near to the free resonance frequency which is usually between 100 and 400 kHz. The AC signal applied to the bimorph presents an amplitude decided by the operator through the *Amplitude drive*. This parameter, in fact, controls the strength of the drive amplitude used for the cantilever vibration.

The deflection of the cantilever, depending on the topography of the sample surface, is measured with a Position Sensitive Photo Detector (PSPD) which is a four-section split photodiode. It receives information about the cantilaver movement changes exploiting the variation on the reflected laser beam intensity. Then, it can establish a feedback loop which controls and coordinates the piezo tube z-scanner comparing the signal received from the PSPD with the parameters set by the operator. In particular, the *Amplitude setpoint* represents the reference amplitude of the cantilever's vibration and *Z servo gain* controls how much the

error signal in the feedback loop is amplified before used to generate a feedback voltage to the z-scanner.

The voltage signal used by the z feedback-loop to compensate the deviation of the cantilever oscillation amplitude from the one set by the operator provides the necessary information to obtain the topograaphy of the sample.

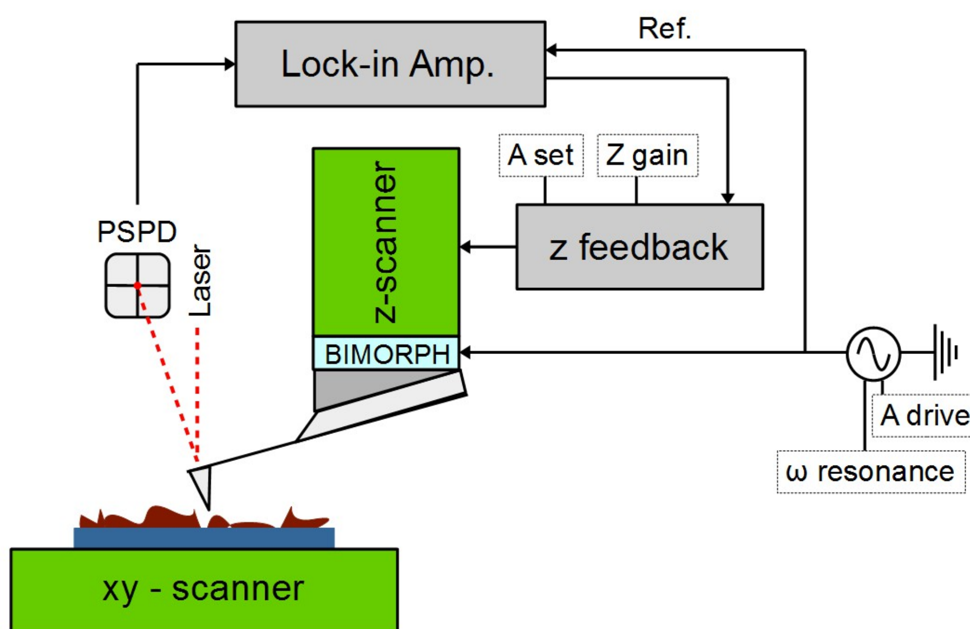


Figure 3.3: nc-AFM system.

3.2 Kelvin probe microscopy

Kelvin probe force microscope (KPFM) was first developed by Nonnenmacher et al. and it allows to image surface electronic properties, namely the contact potential difference (CPD). The name *Kelvin probe force microscope* originates from the macroscopic method developed by Lord Kelvin in 1898 using a vibrating parallel plate capacitor arrangement, where a voltage applied to one vibrating plate is controlled such that no current is induced by the vibration. The reduction of this exact principle to the microscopic scale however results in a poor sensitivity, since the size of the plates is too small to generate a sufficient current. Therefore, in KPFM the electrostatic force is used [35].

Basic principles

The KPFM measures CPD between a conducting AFM tip and a sample. The contact potential difference (V_{CPD}) between the tip and sample is defined as:

$$V_{CPD} = \frac{\phi_{tip} - \phi_{sample}}{-e}, \tag{3.7}$$

where Φ_{tip} and Φ_{sample} are the work functions of the sample and tip respectively and e is the electron charge.

Bringing the conductive AFM tip close to the sample surface generates an electric force due to the difference of the Fermi level of the tip and the sample. To reach a steady state (i.e. Fermi levels aligned) an electrical current starts to flow and charges accumulate on both the tip and the sample surface (Figure 3.4 **b**). Therefore an apparent V_{CDP} forms between the tip and the sample. An electrical force acts on the contact area due to this voltage. Figure 3.4 **c** shows that an external voltage bias (V_{DC}) with the same magnitude of V_{CDP} but with opposite polarity can be applied to nullified this electrical force. This external bias results exactly equal to the work function difference between the tip and the sample. Hence, measuring $V_{DC}(x, y)$ scanning the surface provides information about the local work function of the sample, just with a constant offset which represent the work function of the tip.

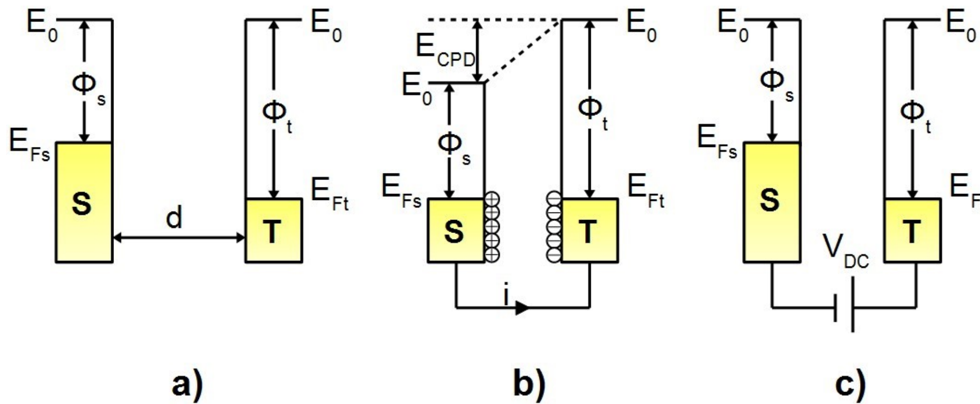


Figure 3.4: Electronic energy levels of the sample and AFM tip. **a)** No electrical contact; **b)** tip and sample in electrical contact; **c)** external bias (V_{DC}) is applied between tip and sample to nullify the CPD and, therefore, the tip-sample electrical force [38].

In addition to the electrostatic force, the van der Waals forces between the tip and the sample surface are always present and they change according to the tip-

sample distance. Hence, an ac-voltage $V_{AC} sin(\omega_{AC} t)$ is added to the compensating dc-voltage V_{DC} for separating the electrostatic from other forces. Accordingly, V_{AC} generates oscillating electrical forces between the tip and the sample surface, and V_{DC} nullifies the oscillating electrical forces which are originated from CPD.

If one considers the tip-sample system as a capacitor ($U = 1/2CV^2$), the electrostatic force depending only from the distance between tip and sample surface in the z direction, can be expressed by:

$$F_{es}(z) = -\frac{1}{2}\Delta V^2 \frac{\partial C}{\partial z}, \tag{3.8}$$

where ΔV is the potential difference between V_{CDP} and the voltage applied to the AFM tip and $\partial C/\partial z$ is the gradient of the capacitance between the tip and the sample surface. Supposing to apply the external bias V_{DC} to the tip, the ΔV results:

$$\Delta V = V_{tip} – V_{CPD} = (V_{DC} - V_{CDP}) + V_{AC} sin(\omega_{AC} t). \tag{3.9}$$

Hence the electrostatic force applied to the tip results:

$$F_{es}(z,t) = -\frac{1}{2}\frac{\partial C}{\partial z}[(V_{DC} - V_{CDP}) + V_{AC} sin(\omega_{AC} t)]^2. \tag{3.10}$$

This equation can be divided into three parts:

$$F_{DC} = -\frac{\partial C}{\partial z}\Big[\frac{1}{2}(V_{DC} - V_{CDP})^2\Big], \tag{3.11}$$

$$F_{\omega} = -\frac{\partial C}{\partial z}[(V_{DC} - V_{CDP}) V_{AC} sin(\omega_{AC} t)], \tag{3.12}$$

$$F_{2\omega} = \frac{\partial C}{\partial z}\frac{1}{4}V_{AC}^2[cos(2\omega t) - 1]. \tag{3.13}$$

Here, F_{DC} induces a static bending of the cantilever, F_{ω} is used to measure the CPD and $F_{2\omega}$ can be used for capacitance microscopy. When electrostatic forces are applied to the tip by V_{AC} with V_{DC} additional oscillating components due to the electrical force are superimposed to the mechanical oscillation of the AFM tip (the one imposed by the z controller). To separate the electrostatical contribute identified by the ω_{AC} frequency, another lock-in amplifier is involved. This component is able to isolate the signal component at the right frequency using a filter and this signal is directly proportional to the difference between

V_{CPD} and V_{DC}. The V_{CPD} value can be measured by applying V_{DC} to the AFM tip, such that the output signal of the lock-in amplifier is nullified and F_ω equals zero. Subsequently, acquiring the value of V_{DC} for each point (x, y) makes possible to draw a map of the surface potential of the entire sample surface. [38]

KPFM system

Figure 3.5 depicts the typical KPFM system used to map the contact difference potentials between the tip ad the surface sample.

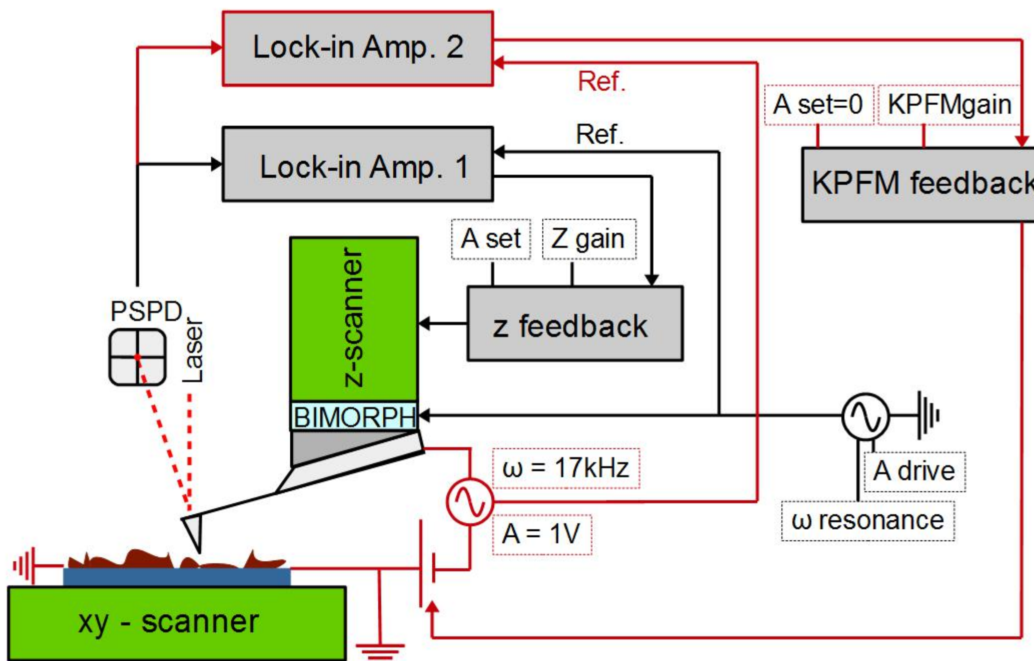


Figure 3.5: KPFM system.

As we said in the previous section, KPFM is based on the non-contact AFM system. In fact, this technique allows to obtain the electrical and morphological information at the same time. The key point of this operation mode is the implementation of a further feedback loop which control the electrical information relative to the sample surface. This lock-in (*Lock-in 2* in Figure 3.5) is able to separate the information about the surface potential from the ones relative to the topography because of a filter in frequency. In fact, to probe the electrostatic forces, an AC bias of 1 V amplitude at a frequency 17 kHz is applied to the tip.

This frequency is lower than the resonance frequency of the cantilever so that the two different impulses imposed to the cantilever can not interfere and the signal which transports CDP information can be filtered by the second lock-in amplifier. The resulting tip oscillation is fed after lock-in amplification into a second feed-back loop engaged to null the electrostatic interaction by adjusting the DC voltage applied to the tip. This V_{DC} has the same magnitude of V_{CDP} and it is recorded to map the surface potential of the sample.

3.3 Application of KPFM

Kelvin probe force microscopy offers the opportunity to study the electrical characteristics of metal and semiconductor surfaces and devices from a microscopic point o view. Other techniques able to measure the surface potential of a sample exist: Kelvin Probe (KP), Photoelectron Spectroscopy (PE), Scanning Electron Microscopy (SEM) with electron beam induced current (EBIC) analysis.

KP presents the same working principle of KPFM. This technique provides the measure of CPD as well but it avoids a local analysis of the surface.

PES measures the energy of photo-stimulated electrons emitted from a sample surface and it is usually involved to obtain the electronic band structure of the sample.

SEM permits to measure the electronic structure of a semiconductor sample, acquiring the electron beam induced current generated into the material by energetic electrons bombardment.

The best quality of KPFM compared to these techniques is the combination of a high energy resolution with huge spatial sensitiveness (see Table 3.1).

Method	Energy resolution	Spatial resolution
KPFM	5-20 meV	Better than 10 nm
KP	1 meV	Averaging a whole sample surface
PES	20 meV	Better than 100 nm
SEM	Not a quantitative method	Better than 70 nm

Table 3.1: Comparison between KPFM and other techniques able to measure the surface potential of a sample [38].

Despite the high energy and spatial resolutions, KPFM presents some disad-

vantages.

First, the measurements are always affected by the offset relative to the work function of the tip. To obtain an absolute measurement about the sample surface potential one has to calibrate the KPFM probe and this procedure decreases the accuracy of the measurement.

Second, an abrupt topographic height change can affect the surface potential measurement because of the contribution of capacitance gradient to the surface potential (Eq. 3.8).

Finally, the simultaneous operation of the two lock-in controlling both the height and the surface potential causes a relative long time to acquire an image. During all the acquisition, the sample is subjected to electrical signals which can stress the device.

Despite these features, KPFM is widely used to characterize the electrical properties of metallic nanostructures and semiconductor surfaces and devices such as quantum dots, electrical junctions, transistors and solar cells [38].

During this work, KPFM has been used to analyze the electrical properties of flexible oxide TFTs offering the opportunity to understand the microscopic features which can cause a decrease of device performance (*Chapter 4*).

Chapter 4

Results and discussion

In this chapter I present the results obtained during this work.

In the first section I describe the fabricated and analyzed devices focusing on the structure, the materials used and introducing a new technique to laminate and delaminate flexible substrate on a rigid carrier.

In the second section I discuss the electrical characterization of the devices before and after the detachment from the rigid support. I analyze the properties of transport and the capacitance of each samples. Besides, I compare the performances of different TFTs in a macroscopic way.

In the last section I investigate the microscopic origin for the differences observed by the electrical analysis using a Kelvin Probe Force Microscopy.

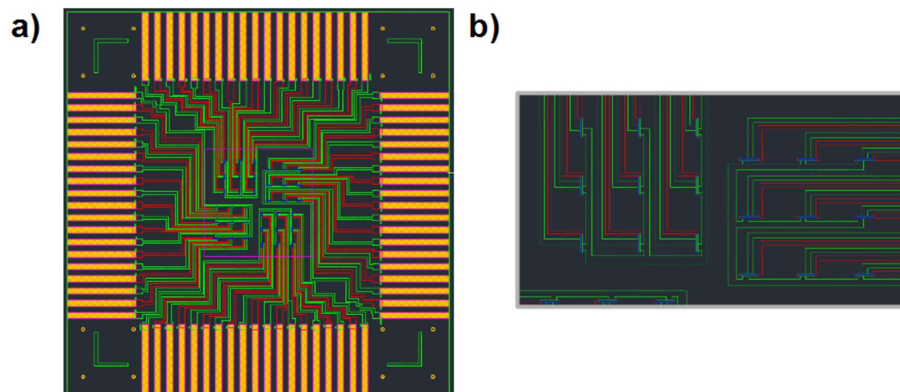


Figure 4.1: a) Schematic of the masks used to fabricate the TFTs. **b)** A detail of two units of 3x3 TFTs.

4.1 Fabricated devices

N-channel thin film transistors were fabricated at the University FCT in Lisbon, in particular in CEMOP and CENIMAT laboratories. The devices were fabricated following the procedures described in *Chapter 2* and using the masks shown in Figure (4.1). The facilities used for the fabrication are listed in *Chapter 2*.

As shown in the optical image reported in Figure 4.2, each sample contains 36 TFTs divided in four blocks with 3x3 matrix each. In each block the channels are oriented in the same direction and two by two are perpendicular each other.

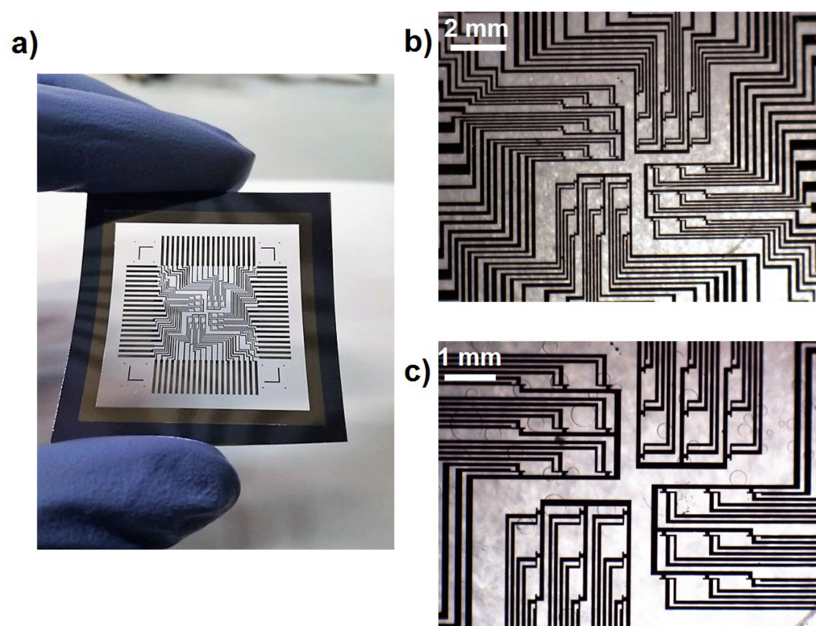


Figure 4.2: **a)** Immage of one of the fabricated device. **b-c)**Optical immages of the 36 TFTs matrix.

All the devices have a staggered structure with a bottom-gate and top contacts. In Figure 4.3 we can observe the structure of the TFTs and an optical image of the device. Besides, analyzing the device by an Atomic Force Microscope (AFM) makes it possible to extract the profile of the TFT and to observe the overlap of the several layers.

All of the fabricated devices were realized on flexible substrates. As it has been discussed in Section 1.3.3, using flexible substrates presents some drawbacks regarding the process of fabrication. The main problem is related to the fact that during the lithography process the substrate have to be perfectly flat allowing a correct alignment of the masks. Besides, mechanical stress during the fabrication

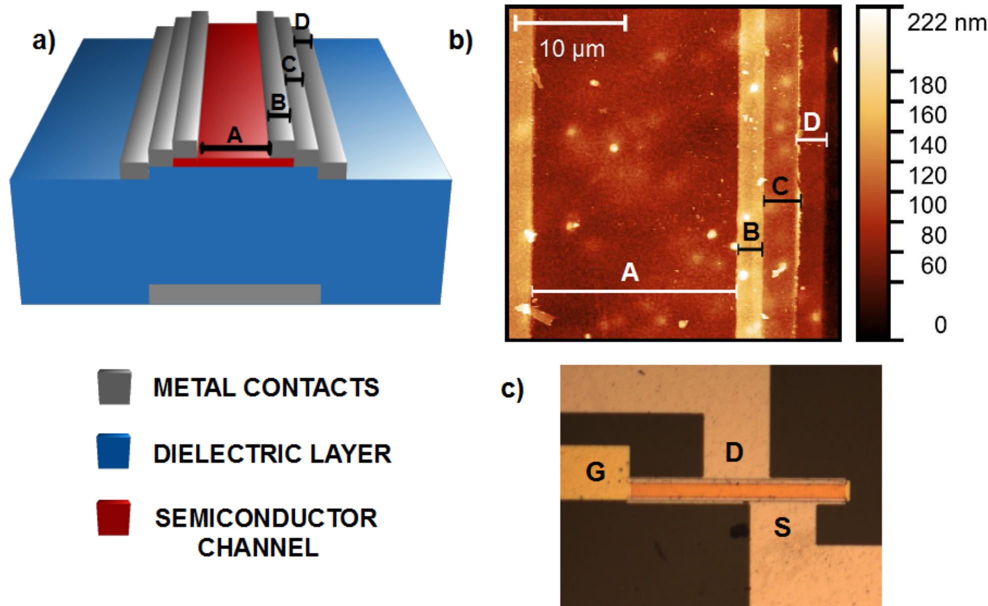


Figure 4.3: a) Cross section, **b)** nc-AFM immage and **c)** optical immage of the devices fabricated (Channel dimensions WxL, W = 320 μm, L = 20 μm).

due to the bending of the substrate could cause bad consequences on the stability and on the quality of the final device.

To address the difficulties related to handling the flexible substrates during the fabrication, a new process based on temporary bonding of flexible substrates onto a solid carrier was developed. The adhesive used to fix the flexible onto the rigid carrier has to present some properties such as the insensitiveness to the UV, acetone/IPA/acids resistant, heating-resistant up to 150 °C. In this work the Polydimethylsiloxane (PDMS) has been used as adhesive layer, treated with a curing agent. After cleaning both the glass and the flexible substrates, the PDMS was spin-coated onto the rigid carrier at 2000 rpm for 90 seconds achieving an uniform layer ∼2 μm thick. Then the PEN foils were placed onto the PDMS layer moving a little the substrate in the two directions to obtain little overlaps of the adhesive on the borders of the foil. These little "hills" prevented the insertion of external agents between the foil and the rigid carrier during all the process. The substrates were subsequently cured at 85 °C for one hour to ensure complete hardening of the adhesive. At the end of the process, the flexible substrate could easily be detached from the rigid carrier cutting the PDMS at the borders.

A great number of devices were fabricated during this work (Figure 4.4, Table 4.1). The differences between the samples are the flexible substrate and the

dielectric layer used.

Figure 4.4: TFTs fabricated. The different coulors are related to the different thickness and materials used as dielectric layer and to different substrates.

Three different flexible substrates were used to fabricate the devices: polyimide (kapton), PEN Q51 and PEN Q65. The difference between the two PEN is that the latter is composed by two sides, one planarized and the other not. For this reason it presents a smaller roughness compared to the PEN Q51. All the devices present a bottom-gate electrode deposited with a 60 nm thick Mo. This layer was previously patterned by photo-lithography, followed by dry etching. The dielectric layer was subsequently deposited by a different technique depending on the type of insulator: multilayer dielectrics composed by Ta_2O_5 and SiO_2 were deposited by RF magnetron sputtering, while Parylene dielectric layer was grown by CVD. A 30 nm thick a-GIZO 1:2:2 active layer was deposited forming channels which present the following dimensions: W = 320 μm, L = 20 μm. At the end, source and drain electrodes were deposited with 60 nm thick Mo. The electrodes and the semiconductor layers were all deposited by RF sputtering. All the layers were patterned using the photolithography technique described in *Chapter 2*. After the last layer, a post-deposition annealing at 150°C for one hour on the hot plate occurred. Even if a layer of passivation typically improve the performance and the stability of the TFTs ([27], [28]), these sample were not passivated because it would imply a loss of resolution for the SPM analysis shown in the next section.

After observing the performance of each device I decided to deeply analyze only four of the fabricated samples (the ones written in red in the Table 4.1). In

SAMPLE	SUBSTRATE	CONTACTS	CHANNEL	DIELECTRIC LAYER
1	PEN Q51	Mo	GIZO	Parylene (***)
2	PEN Q65			
3	KAPTON			
4	PEN Q51			Parylene (**)
5				Parylene (*)
6				14 multilayer Ta_2O_5+SiO_2 // SiO_2
7	KAPTON			
8	PEN Q51			7 multilayer Ta_2O_5+SiO_2 // SiO_2

Table 4.1: Fabricated devices. The stars (*) indicate different thickness of Parylene layer decreasing starting from 300 nm.

fact, as far as **S2** and **S3** concerned, they both present a minor rate of working devices compared to **S1**. Furthermore, the implementation of the 14 multilayer dielectric failed probably because of an excessive thermal stress of the substrate due to the long sputtering deposition.

In the next sections I present an electrical and a morphological analysis of the selected four samples. A microscopic analysis by KPFM allows to understand the structural differences between TFTs of the same sample working different. Besides, an analysis about the impact of the different dielectric layer will be proposed.

4.1.1 Dielectric thickness

As it has been said in the last section, all the fabricated devices present a bottom gate structure. In this kind of TFTs, an etching of the dielectric layer is essential to be able to extract and apply a signal from the gate contact. In the samples, the dry etching following the dielectric deposition opens little “windows” in the dielectric to contact the gate pad (Figure 4.5).

The analysis of the profile of these squares allows to measure the thickness of the deposited dielectric layer.

In Figure 4.6 I report the height curve obtained by a nc-AFM analysis.

In Table 4.2 the dielectric thicknesses of the four samples are shown. As far as the Parylene dielectric is concerned, the estimation of the thickness can be

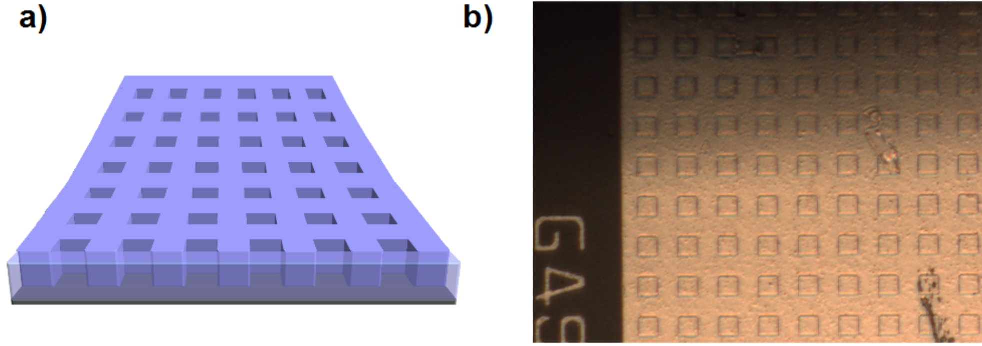


Figure 4.5: **a)** Schematic of a etched gate pad. **b)** Optical immage of a gate pad. The little squares are the holes obtained by etching the dielectric layer and through which the connection of the gate electrode is possible.

considered quite accurate. On the opposite side, for the multilayer dielectric this technique presents a limitation. While Parylene was etched using O_2 which is not able to attack the Mo gate layer, on the contrary the multilayer was etched by SF6 that could remove part of the underlayer made by Mo. For this reason the measured thickness of the 7-multilayer could be overestimated.

SAMPLE	DIELECTRIC THICKNESS (nm)
1 → P300	(300 ± 15)
4 → P250	(250 ± 1)
5 → P170	(170 ± 4)
8 → M207	(207 ± 8)

Table 4.2: Dielectric thicknesses. In the first column the acronyms of the samples are indicated.

4.1.2 Dielectric roughness

After the nc-AFM analysis the surface roughnesses of the samples were calculated. The values of the roughness are reported in Table 4.3.

Since the only difference between the samples is in the dielectric layer, we have to analyze these data paying attention to the insulator thickness and the technique

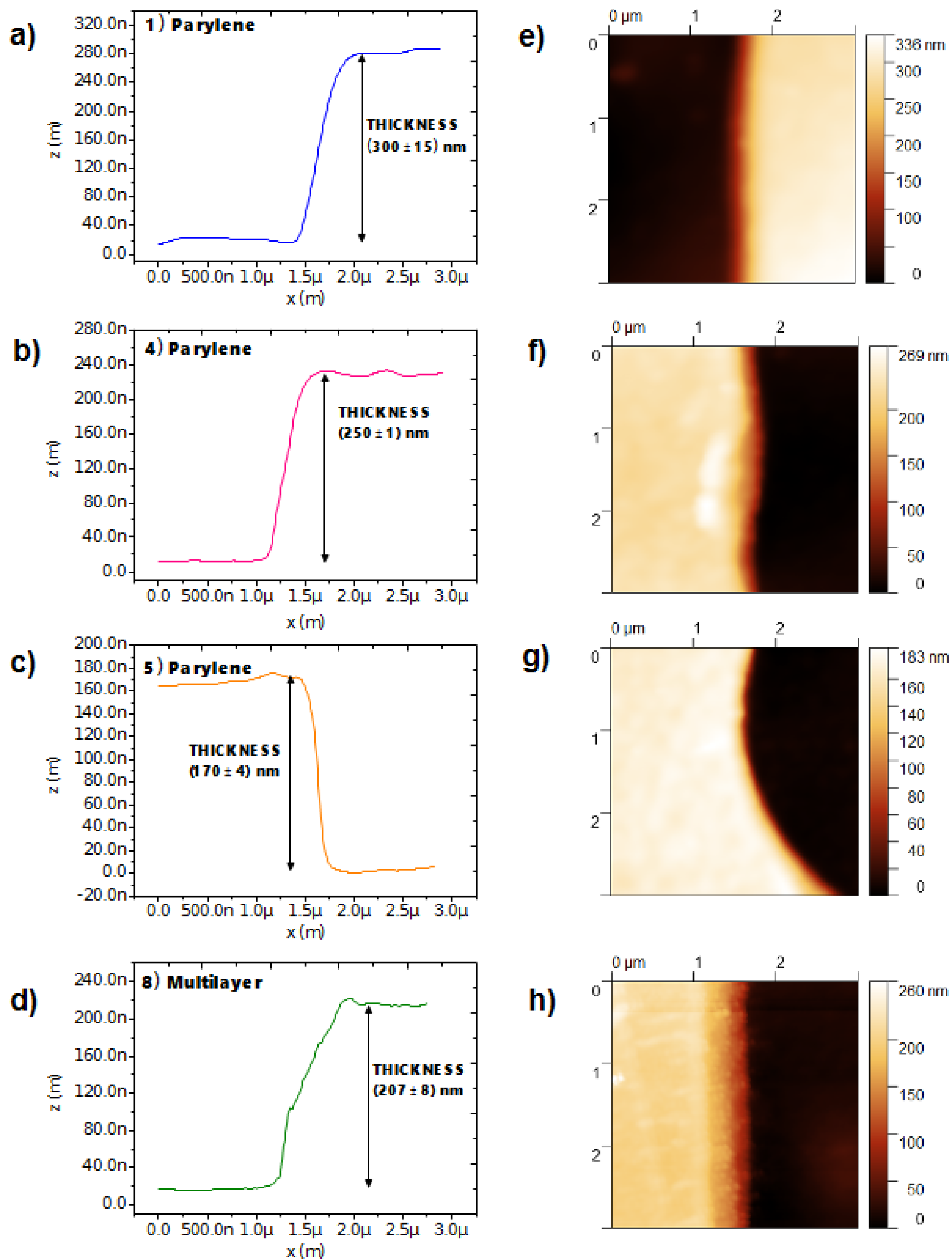


Figure 4.6: Dielectric thickness. **a-d)** profile measured by nc-AFM. **e-h)** nc-AFM immages.

SAMPLE	DIELECTRIC	ROUGHNESS (nm)
P300	Parylene (300 ± 15) nm	(9 ± 3)
P170	Parylene (170 ± 4) nm	(6 ± 1)
M207	multilayer (207 ± 8) nm	(11 ± 5)

Table 4.3: Surface roughness.

of deposition used. From the obtained results I could conclude that increasing the thickness of the Parylene dielectric layer leads to a rise of the surface roughness. Besides, the multilayer sample is rougher than the Parylene ones. This could be due to the different deposition technique used (RF sputtering instead of CVD) or to the fact that in this case the insulator layer is composed by 7 separate layers.

4.2 Electrical characterization

Device electrical characterizations were performed in air at room temperature using a probe station with micromanipulators with tungsten tips to contact the TFT electrodes and a *Keithley 2614B* SMU. In this section I will first present the transport characterization of the devices. Then, a study of the capacitance will be shown. After these two paragraphs, I will list the TFT parameters obtained by a statistical analysis and I will compare the different macroscopic behaviours between each samples. At the end I will discuss the performance of the multilayer sample after the detachment from the rigid carrier.

4.2.1 Transport characterization

For each sample I analyzed several independent TFTs (N > 10) to verify the uniformity of the devices and to be able to obtain a significant statistical analysis.

The characteristic curves of the best TFTs for each sample are shown in Figure 4.7.

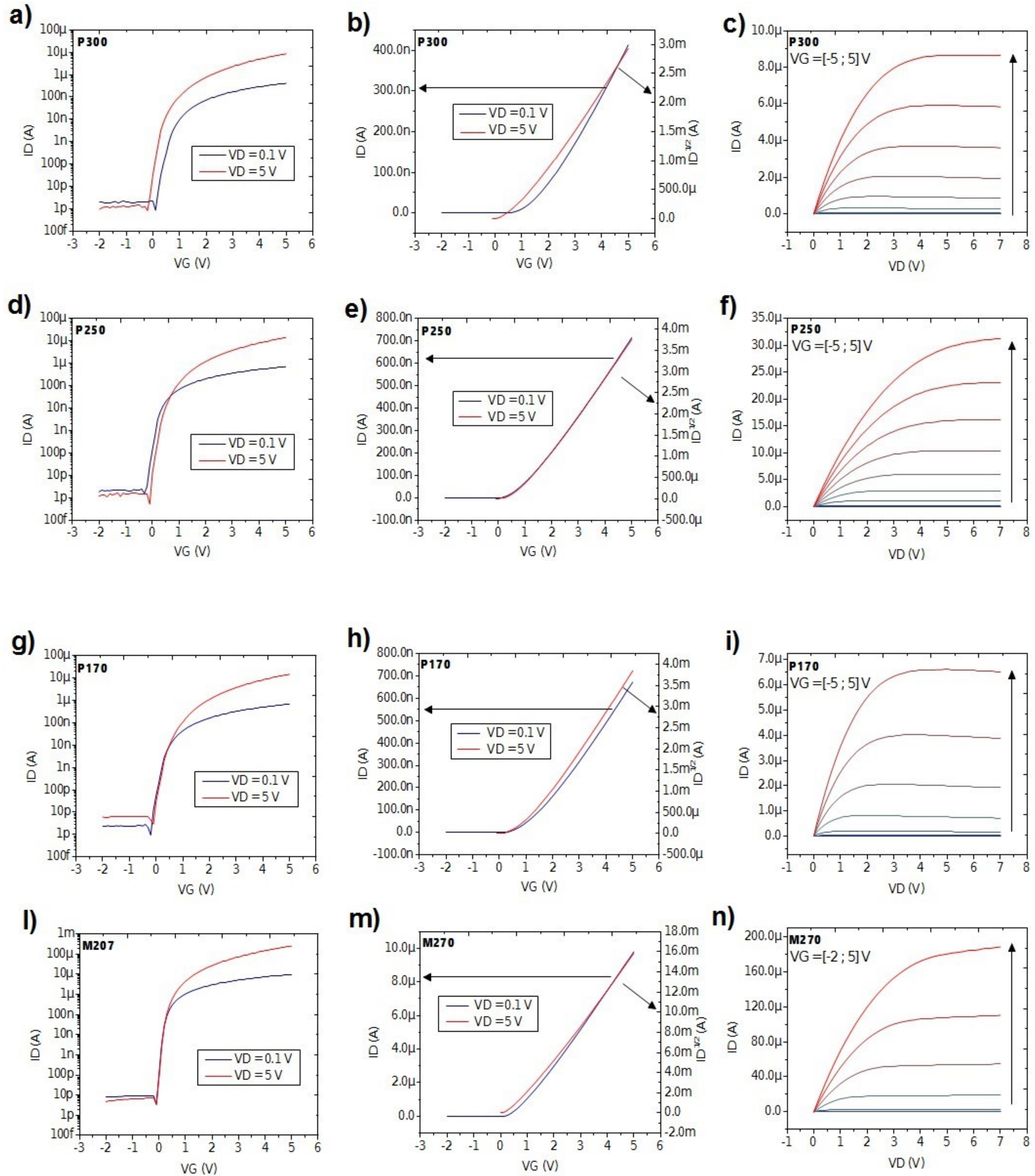


Figure 4.7: TFTs characteristic curves. **a-c)** P300, **d-f)** P250, **g-i)** P170, **l-n)** M207.

From the graphs reported in Figure 4.7, we can conclude that the analyzed devices show good performances: the slope of the transfer characteristics shows that they are strongly affected by the field effect; they all turn on around 0 V as an ideal n-channel TFT; in linear and in saturation regimes they present a linear and quadratic trend respectively according to the drain current Equations 1.1 and 1.2. Besides, we can qualitatively observe that the multilayer sample shows a better performance compared to the Parylene ones. In the next section I will investigate this difference by microscopy.

In the graphs of Figure 4.8 the saturation transfer characteristic of several TFTs laying on the same sample are reported. These curves demonstrate that the fabricated devices present a good level of uniformity.

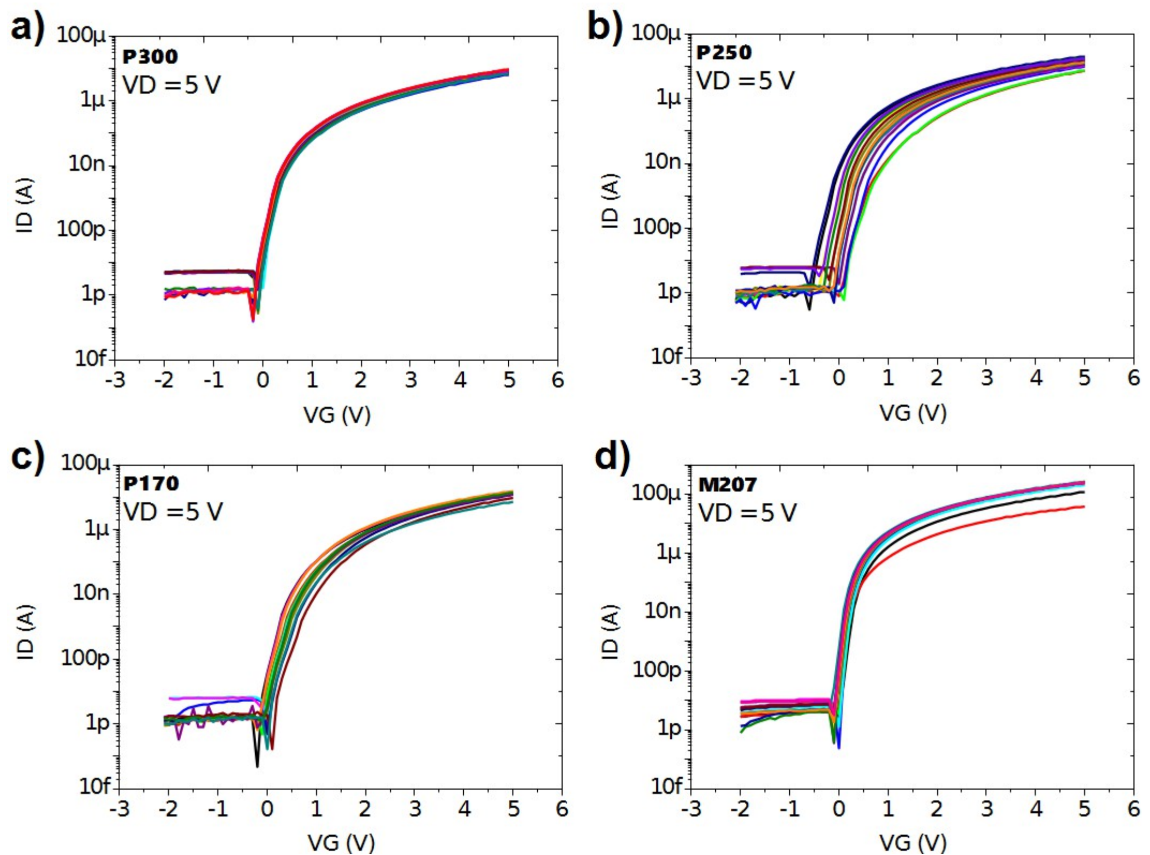


Figure 4.8: TFTs transfer saturation characteristics (VD = 5 V). **a)** P300, **b)** P250, **c)** P170, **d)** M207.

4.2.2 Capacitance characterization

As we have discussed in the *Chapter 1*, the capacitance of the dielectric layer has a huge impact on the TFT performance. In particular, a dielectric with a great capacitance and an high breakdown field leads a device which presents low operation voltage and low leackage current. For this reason the subthreshold swing (S) and the ON/OFF ratio are strongly determined by the choice of the insulator material implemented as dielectric layer (i.e. permittivity k) and its thickness (d).

The capacitance of the several dielectric layers have been measured using the *AUTOLAB PGSTAT204* potentiostat. In these measurements I extracted the values of impedance (Z) for different DC voltage maintaining the frequency (f) of the signal at 10 kHz. The graphs showing Z vs V_{DC} are reported in Figure 4.9.

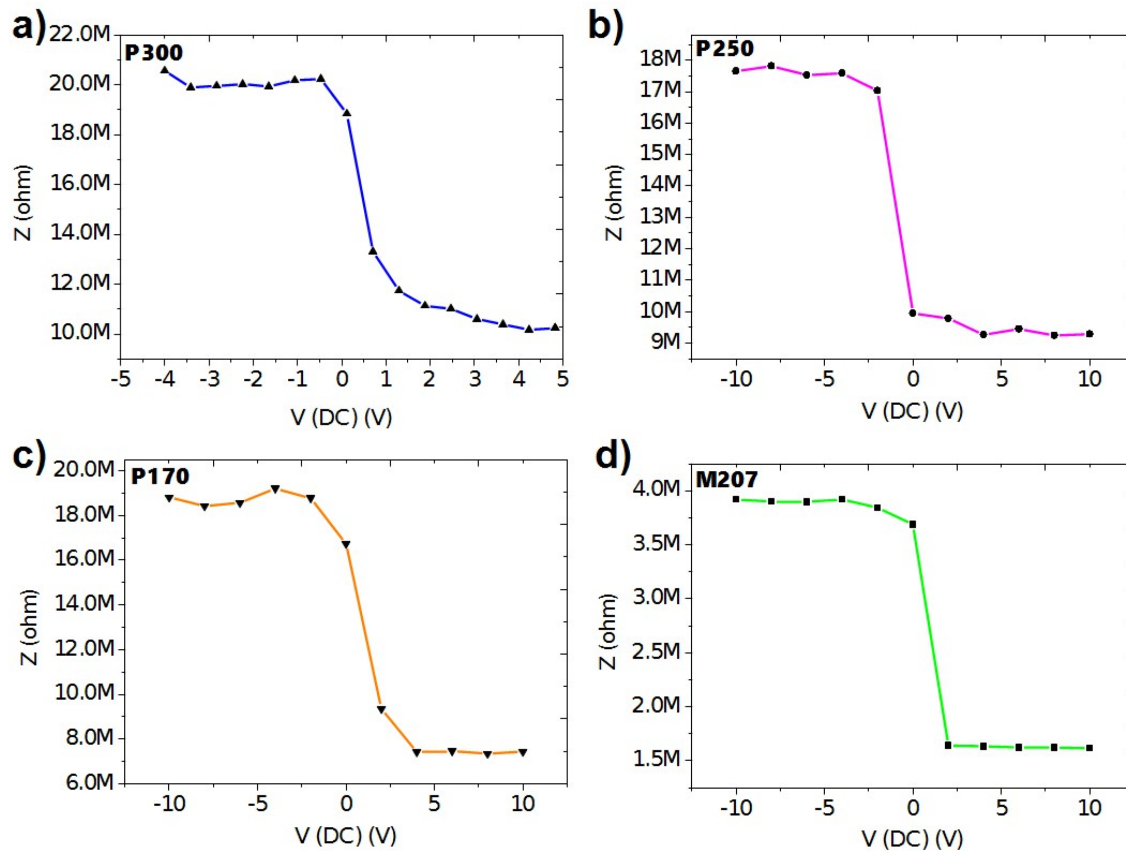


Figure 4.9: Impedence vs DC voltage. The frequency of the signal is 10 kHz. **a)** P300, **b)** P250, **c)** P170, **d)** M207.

Looking at these graphs one can notice that the impedance falls down when the applied voltage go from negative to positive values. In fact, while the higher values of Z are referred to the TFT off-state including only the capacitance ef-

fect due to the electrodes overlaps, the lower values are obtained for the TFT on-state in which the channel contribution has to be added. Indeed, when V_G becomes positive, the active layer starts to be conductive and the channel surface contributes to the entire capacitance reducing the impedance of the device. To take into account only the effect caused by the accumulation layer forming in the semiconductor, I calculated the difference between the OFF and the ON state impedances respectively ($\Delta Z = Z_{OFF} - Z_{ON}$).

Using the Equations

$$\omega = 2\pi f, \tag{4.1}$$

$$C = \frac{1}{\omega \Delta Z}, \tag{4.2}$$

$$C_i = \frac{C}{WL}, \tag{4.3}$$

I calculated the capacitance per unit area of each sample.

To consider the border effect of the capacitor composed by gate electrode / insulator / channel, the following argument has been developed. From the literature we know that the dielectric permittivity of Parylene C is around 3 [1]. The capacitances obtained using Eq. 1.8 result different from the values found with the potentiostat analysis. The difference between the two values can be attributed to the existence of a fringe field at the borders of the non-ideal capacitances. I decided to include this border effect introducing a new parameter (*form factor*). f could be calculated for each Parylene sample:

$$f = \frac{C}{C_i}, \tag{4.4}$$

where $C = \frac{1}{\omega \Delta Z}$ and $C_i = \frac{k k_0}{d}$.

The form factors relative to each Parylene samples are reported in Table 4.4.

The terms f/ W · L indicate the ratio between the form factor and the nominal area of the channel. In every Paryene TFT this ratio results >1 which indicates that to include the fringe field we have to consider an effective area greater than the nominal one. Since f represents a deviation from the ideal behaviour of a capacitor, as we can see in Table 4.4, thinner is the dielectric, smaller is the border correction. In particular, Figure 4.10 shows the linear relation obtained between

SAMPLE	C (pF)	C_i F m^{-2}	f m^2	f / W · L
P300	(1.72 ± 0.04)	$(8.9 \pm 0.4) \cdot 10^{-5}$	$(1.9 \pm 0.1) \cdot 10^{-8}$	(3.0 ± 0.2)
P250	(1.73 ± 0.06)	$(10.62 \pm 0.04) \cdot 10^{-5}$	$(1.63 \pm 0.06) \cdot 10^{-8}$	(2.5 ± 0.1)
P170	(2.14 ± 0.03)	$(15.62 \pm 0.04) \cdot 10^{-5}$	$(1.37 \pm 0.05) \cdot 10^{-8}$	(2.14 ± 0.08)

Table 4.4: Form factors.

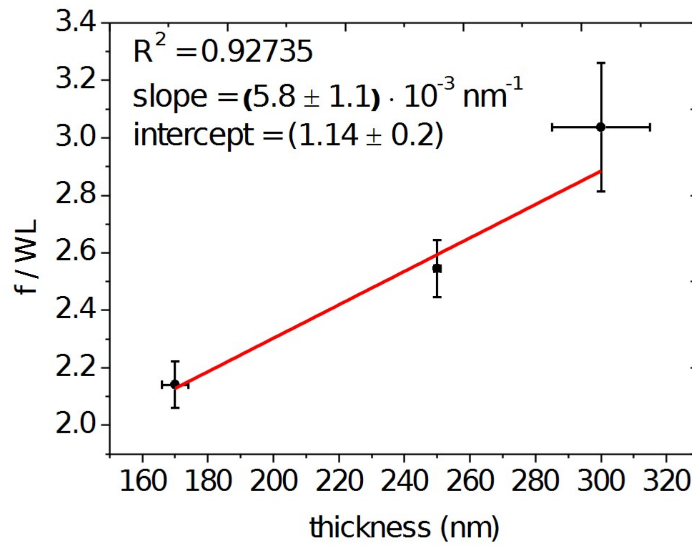


Figure 4.10: Linear dependence of form factor normalized for the nominal area from dielectric thickness.

f/ W · L and the dielectric thickness.

Knowing the thickness of the multilayer dielectric, we can extrapolate from the graph in Figure 4.10 the form factor of **M207**. Therefore, the permittivity of this dielectric layer has been calculated from Eq. 1.8: $k = (11.2 \pm 1.6)$.

Finally, I calculated the effective capacitance per unit area of each dielectric layer including the border effects (Table 4.5) using:

$$C_i = \frac{C_{potentiostat}}{f} \tag{4.5}$$

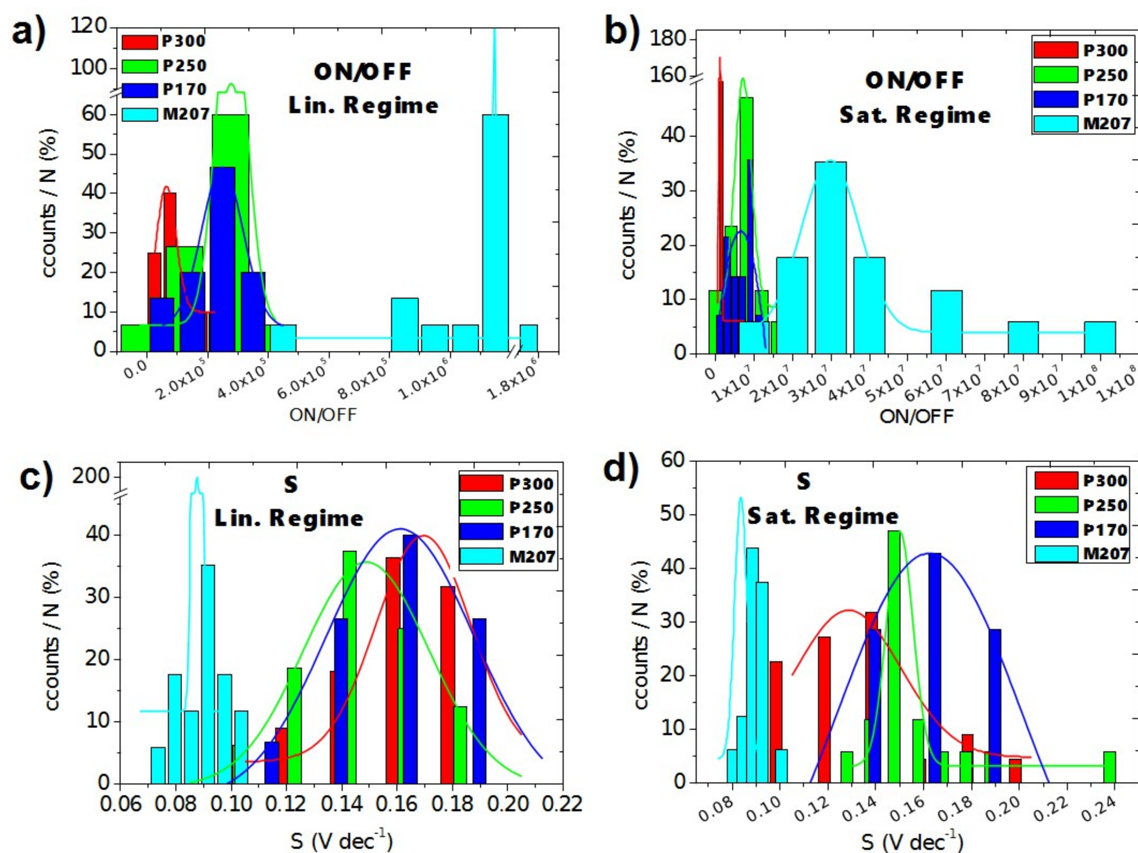
[1]Data compiled and published by VP Scientific, Inc., 9823 Pacific Heights Boulevard, Suite T San Diego, CA 92121, $http://www.vp-scientific.com/parylene_properties.htm$

SAMPLE	C_{pot} (pF)	f (m^2)	C_i ($F\ m^{-2}$)
P300	(1.72 ± 0.04)	$(1.9 \pm 0.1) \cdot 10^{-8}$	$(8.9 \pm 0.7) \cdot 10^{-5}$
P250	(1.73 ± 0.06)	$(1.63 \pm 0.06) \cdot 10^{-8}$	$(10.6 \pm 0.5) \cdot 10^{-5}$
P170	(2.14 ± 0.03)	$(1.37 \pm 0.05) \cdot 10^{-8}$	$(15.6 \pm 0.6) \cdot 10^{-5}$
M207	(7.16 ± 0.03)	$(1.5 \pm 0.2) \cdot 10^{-8}$	$(47.8 \pm 0.7) \cdot 10^{-5}$

Table 4.5: Capacitance per unit area.

4.2.3 Comparison

A quantitative analysis of the devices is presented in this section. The mobility, the turn-on voltage, the subthreshold swing and the ON/OFF ratio have been calculated for several TFTs on each sample. The values obtained from a statistical analysis (see Figure 4.11) are listed in Table 4.6.



Firs of all, the superior performance showed by the multilayer sample compared to the ones of Parylene is pointed out by the values reported. The huge mobility

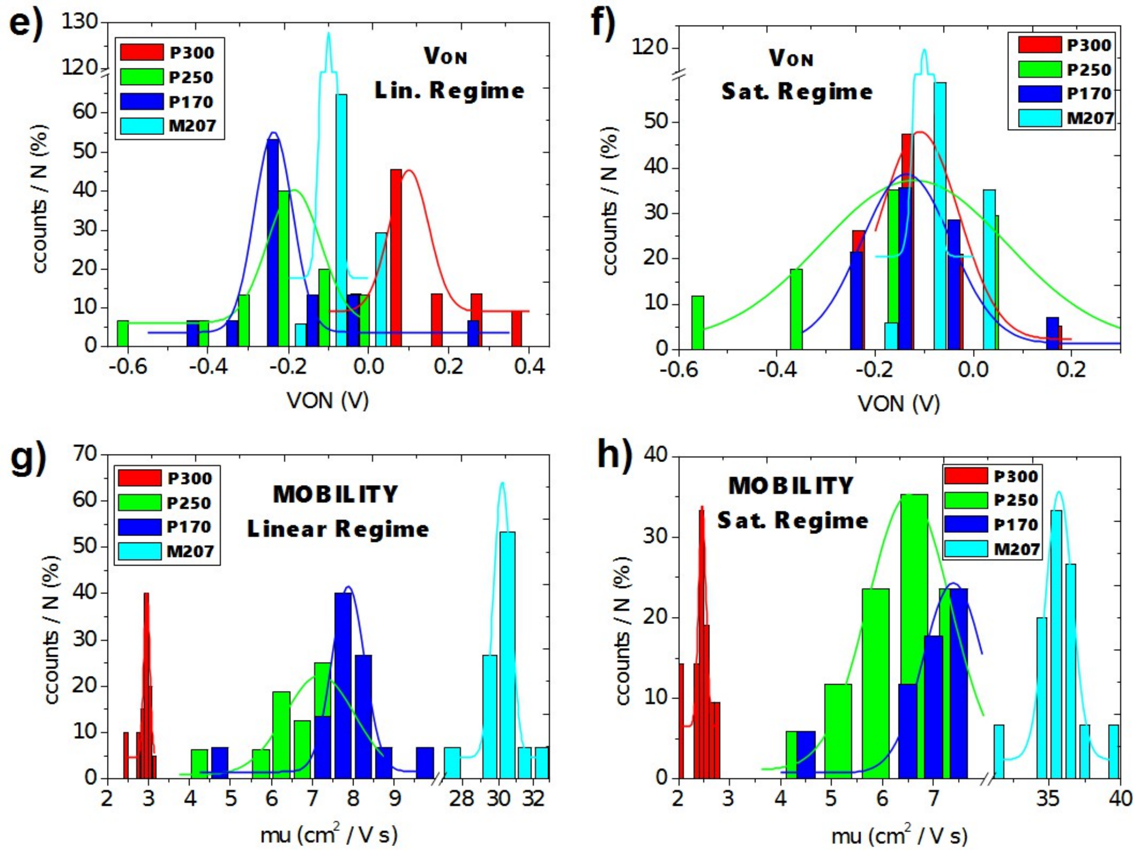


Figure 4.11: TFTs statistical analysis. **a-b)** ON/OFF ratio, **c-d)** Subthreshold swing, **e-f)** Turn-on voltage, **g-h)** Electrical mobility.

(μ_{FE} = (30.2 ± 0.5) $cm^2V^{-1}s^{-1}$ and μ_{sat} = (35.7 ± 0.9) $cm^2V^{-1}s^{-1}$) and the small subthreshold swing (S_{lin} = (0.088 ± 0.001) V dec^{-1} and S_{sat} = (0.084 ± 0.003)V dec^{-1}) confirm that the multilayer sample is a very promising oxide TFT.

The histograms reported in Figure 4.11 show that all the samples present a good level of spatial uniformity.

All the devices present a good ON/OFF ratio (between 10^4 and 10^6 for the linear regime and between 10^6 and 10^7 in the condition of saturation) and the turn on voltage is around 0 V for all the samples confirming the ideal behaviour of an N-channel TFT. The difference between the turn on voltage in the linear and in the saturation regimes indicate only an electrical stress of the devices due to the two characterizations one after the other.

Looking at the Parylene TFTs, an observation on the differences caused by the dielectric thickness merits comment. The subthreshold swing is smaller for the thiner dielectric layer. This represents what I pointed out in the *Chapter 1*: when

P300	**P250**	**P170**	**M207**
ON/OFF			
$(6 \pm 3) \cdot 10^4$ $(1.3 \pm 0.3) \cdot 10^6$	$(2.8 \pm 0.5) \cdot 10^5$ $(7 \pm 2) \cdot 10^6$	$(2.5 \pm 0.7) \cdot 10^5$ $(6.5 \pm 0.3) \cdot 10^6$	$(1.14 \pm 0.01) \cdot 10^6$ $(3.0 \pm 0.7) \cdot 10^7$
S ($V\ dec^{-1}$)			
(0.17 ± 0.02) (0.13 ± 0.02)	(0.15 ± 0.02) (0.150 ± 0.005)	(0.16 ± 0.03) (0.16 ± 0.04)	(0.088 ± 0.001) (0.084 ± 0.003)
VON (V)			
(0.10 ± 0.05) (-0.10 ± 0.08)	(-0.19 ± 0.07) (-0.12 ± 0.18)	(-0.23 ± 0.05) $(-0.14 \pm 0.09$	(-0.10 ± 0.02) (-0.10 ± 0.002)
MOBILITY ($cm^2\ V^{-1}\ s^{-1}$)			
(2.96 ± 0.07) (2.46 ± 0.07)	(7.2 ± 0.9) (6.5 ± 0.8)	(7.9 ± 0.4) (7.4 ± 0.6)	(30.2 ± 0.5) (35.7 ± 0.9)

Table 4.6: TFTs parameters obtained from the statistical analysis. For each parameter, the first row indicates the values relative to the Linear Regime, while the second one is referred to the Saturation Regime.

a high capacitance density gate dielectric is used (i.e. thinner dielectric) S can be quite small, allowing the devices to abruptly and strongly turn on for $V_G > V_{on}$.

Finally, the growing of mobility with the falling down of the Parylene dielectric thickness could be explained by a non-ideal behaviour of the devices. In fact, as we saw in the *Chapter 1*, the electrical mobility depends on the gate voltage and the effective voltage perceived by the channel is linked to the capacitance of the dielectric layer.

In the next sections we will try to understand in a microscopic way the reasons for the different performances showed by each sample and by the TFTs with the same material and structural characteristics.

4.2.4 After detachment

As I pointed out at the beginning of this chapter, during this work I've improved the fabrication process on flexible substrates developing a procedure to fix them

temporarily onto a rigid carrier (glass).

After the characterization of the samples in the "flat-mode" I tried to detach the **M207** from the support and the new electrical characterization of the devices (see Figure 4.12) show that this procedure didn't damage the TFTs.

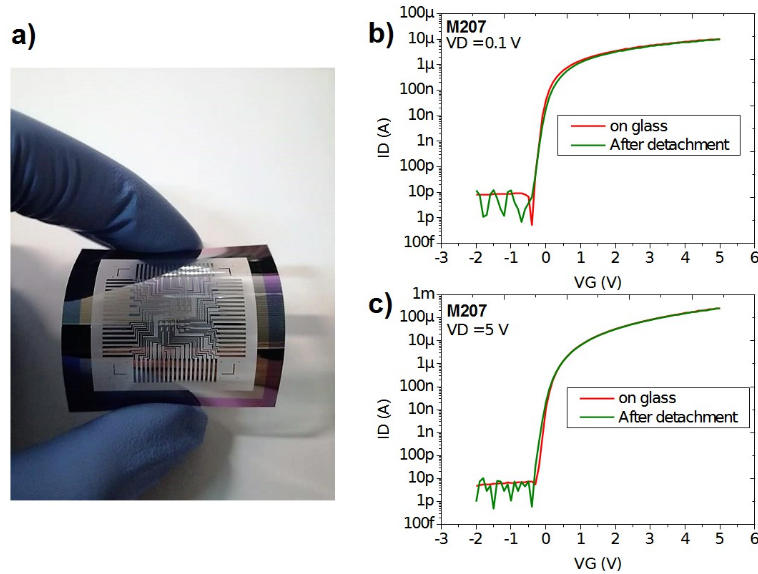


Figure 4.12: a) Picture of one of the analyzed sample detached from the rigid carrier. Transfer **b)** Linear and **c)** Saturation characteristics of the multilayer device before and after the detachment.

From the data acquired we can conclude that the procedure developed represents a successful way to improve the fabrication of electronic devices on flexible substrates.

4.3 KPFM analysis

In this section I will discuss a microscopic analysis of the samples introduced before. A scanning probe microscope (*Park, NX10*) has been used for this purpose. In particular I used two different techniques: non-contact AFM (nc-AFM) and KPFM.

This instrument and these operation modes have been described in *Chapter 3*.

These microscopic considerations could give an explanation for the different behaviour presented by TFTs of the same sample and could explain some of the differences reported by the two classes on devices analyzed in this work: oxide-based TFTs (multilayer) and hybrid TFTs (inorganic/organic Parylene dielectric).

M207 and **P170** have been analyzed using KPFM. The multilayer sample has been studied deeply compared to the Parylene one because of its great electrical performance and because it is less sensitive to electrical stress cause by this investigation technique.

During this work I developed a dedicated probe station to contact the samples during the KPFM analysis. The electrical interconnections were realized using the probe station shown in Figure 4.13 and a *Keisight, b2900A*.

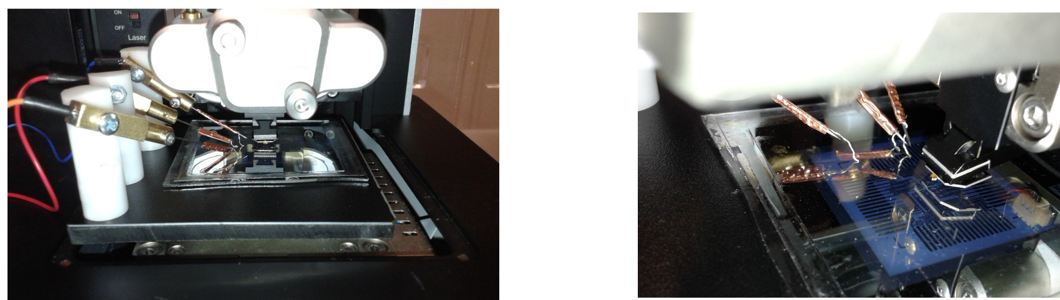


Figure 4.13: Pictures of the probe station dedicated for the KPFM analysis.

Applying 0 V both to the gate and to the drain electrodes, the difference of the surface potentials between Mo electrodes and GIZO channel has been measured (Figure 4.14). This value ΔVsp = (186 ± 9) mV) constitutes an offset in all the measurements that I will present in this section.

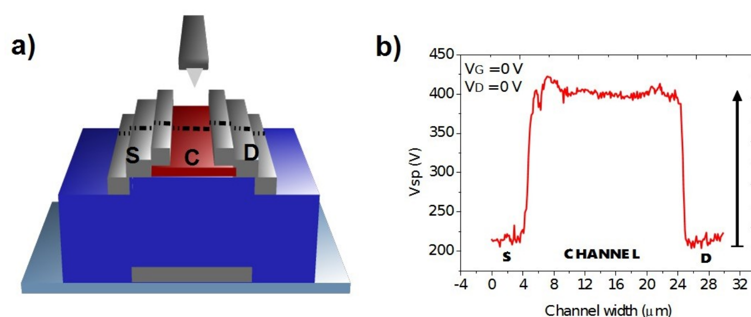


Figure 4.14: a) Schematic figure of the probe scan during the KPFM analysis; **b)** Potential profile of the channel when 0 V is applied to each electrode. The arrow indicates the difference of the surface extraction potentials between GIZO and Molibdenum (ΔVsp = (186 ± 9) mV).

In Figure 4.15 we can see the images of the surface potential when one of the multilayer TFTs is in Linear and Saturation regime respectively.

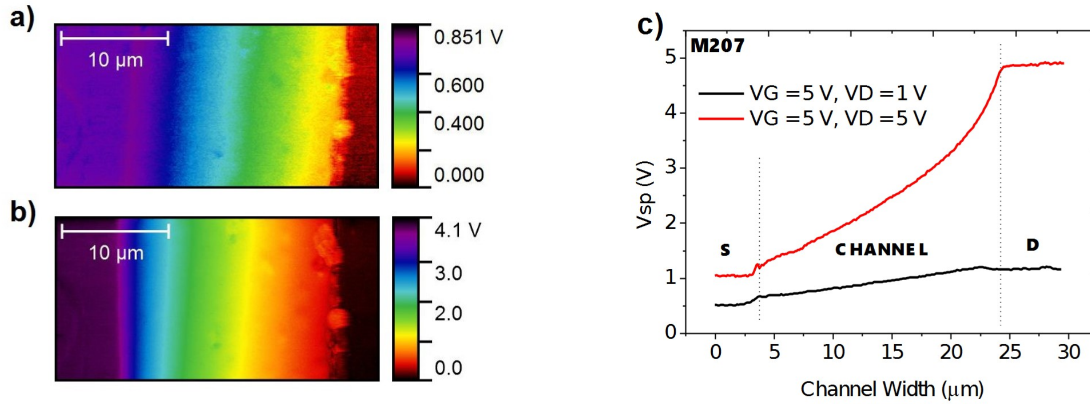


Figure 4.15: Surface potential of TFT 4.4 of the sample **M207** maintained in the **a)** linear (VG = 5 V, VD = 1 V) and in **b)** saturation regime (VG = 5 V, VD = 5 V). **c)** Profile of these images.

Here a constant voltage is applied both in gate and drain electrodes: VG = 5 V in both cases and VD = 1 V for the Linear regime and 5 V for the Saturation one. From the profile reported in Figure 4.15 **c** we can see the typical trend of a TFT in the two regimes: while the linear line points out a uniform distribution of the charges inside the channel, in the saturation regime we can observe the so called *pinch off* and the depleted region next to the drain electrode.

As far as the multilayer sample is concerned, I analyzed two different TFTs. The parameters of these two devices are reported in Table 4.7. TFT 4.4 is a very performant device, on the opposite side TFT 1.7 shows worse parameters especially in terms of electrical mobility.

	TFT 1.7		**TFT 4.4**	
	LIN	*SAT*	*LIN*	*SAT*
ON/OFF	$4.99 \cdot 10^5$	$1.66 \cdot 10^7$	$1.77 \cdot 10^6$	$1.35 \cdot 10^8$
S V dec^{-1}	0.11	0.09	0.09	0.08
Von V	-0.6	-0.2	-0.4	-0.3
Mobility $cm^2\ V^{-1}\ s^{-1}$	7.13	5.17	29.89	34.77

Table 4.7: Parameters of the two multilayer TFTs analyzed by KPFM analysis.

Figure 4.16 **a, b)** report the surface voltages of the two TFTs in the saturation condition (VG = 5 V, VD = 5 V). Extracting the profiles of these two images (Figure 4.16 **c)**), we can observe a microscopic difference between the two devices that could explain the electrical lack of uniformity on the same sample.

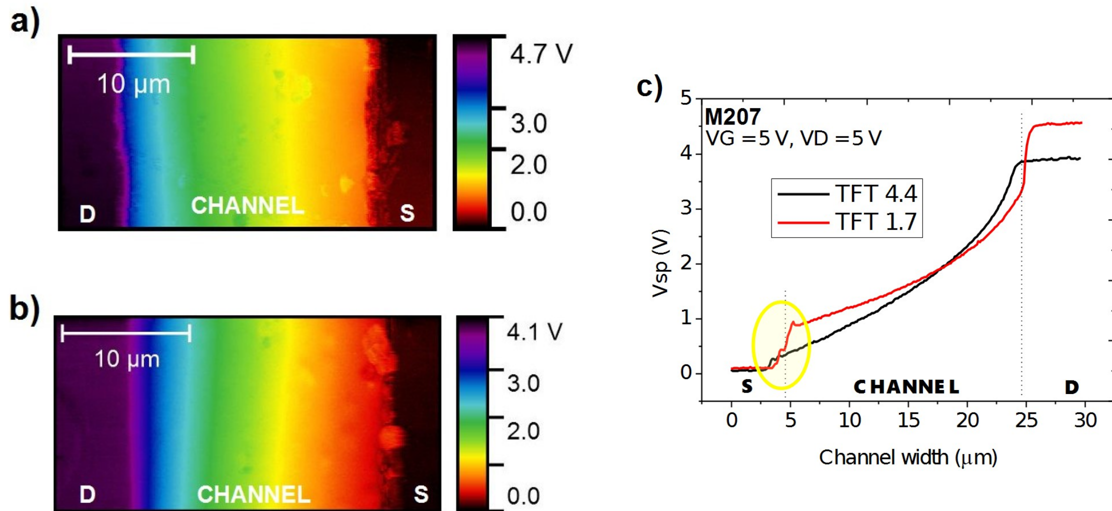


Figure 4.16: KPFM images of **a)** multilayer TFT 1.7 and **b)** TFT 4.4 maintained in the saturation condition. **c)**Profile of the surface potentials measured on the two TFTs. The yellow circle highlights the source contact resistances.

As we said before, the KPFM analysis allows a microscopical study of the devices. Hence the impact of the electrode contact resistances have been studied pointing out that it could be the reason for the different electrical behaviour showed by TFTs fabricated on the same sample.

For instance, calculating the source contact resistances of TFT 1.7 and 4.4 I discovered that in the first case we have a $Rc_S = (6300 \pm 500)\Omega$ while the second TFT presents $Rc_S = (55 \pm 16)\Omega$. The huge difference between these two values could explain the different electrical behaviour of the two TFTs. Since the materials composing the devices are the same, the only difference could be attributed to the alignment phase during the fabrication process. In fact, if the overlap between the semiconductor and the really thin source and drain electrodes changes, the injection properties of the contacts result different and consequently the contact resistances vary.

From the images reported in Figure 4.16 we can consider another important aspect. At the beginning of this chapter we saw the layout of these samples. The long connection lines could have a great impact on the operation of the devices.

Indeed, observing the Figure 4.16, I realized that a resistive parasitic effect is present and it obviously depends on the flowing drain current. Looking at the drain surface voltage, this is confirmed by the fact that the more performant TFT 4.4 is more penalized by this effect than the other one.

Now we can focus on the comparison between the multilayer devices and the Parylene ones. As we saw in the previous sections the choice of the dielectric layer causes a big difference in term of electrical performances. By the KPFM analysis I tried to give a microscopical reason to understand this issue.

The TFTs showed in Table 4.8 were compared for this purpose.

	M207 TFT 4.6		**P170 TFT 3.7**	
	LIN	*SAT*	*LIN*	*SAT*
ON/OFF	$1.87 \cdot 10^6$	$6.58 \cdot 10^7$	$4.80 \cdot 10^5$	$1.85 \cdot 10^7$
S V dec^{-1}	0.09	0.08	0.16	0.18
Von V	-0.4	-0.3	-1.5	-0.8
Mobility cm^2 V^{-1} s^{-1}	29.98	35.36	8.49	8.25

Table 4.8: Parameters of the two multilayer TFTs analyzed by KPFM analysis.

The two samples present very different electrical performance: the multilayer mobility is around four times higher than the Parylene one, the turn on voltage is more negative for the Parylene sample compared to the multilayer one and finally S and ON/OFF ratio confirm a better behaviour for the **M207-TFT 4.6** than **P170-TFT 3.7**.

By the KPFM, I measured the profiles of the TFTs' surface potential in the ON-state (V_G = 5 V constant) varying the drain voltage V_D from 1 V to 10 V (Figure 4.17).

From the images acquired and shown in Figure 4.17 I calculated the contact resistances for each V_D both for the source and the drain electrodes. While the drain contact resistance results negligible in most of the cases for both the samples, the source contact resistance results constant for different V_D (Figure 4.17 **b,d)**). **M207** and **P170** show a source contact resistance of (342 ± 12) Ω and (10.8 ± 0.5) kΩ respectively. As in the previous case, the huge difference between these

two values could be one of the reason for the different electrical behaviour of the two samples.

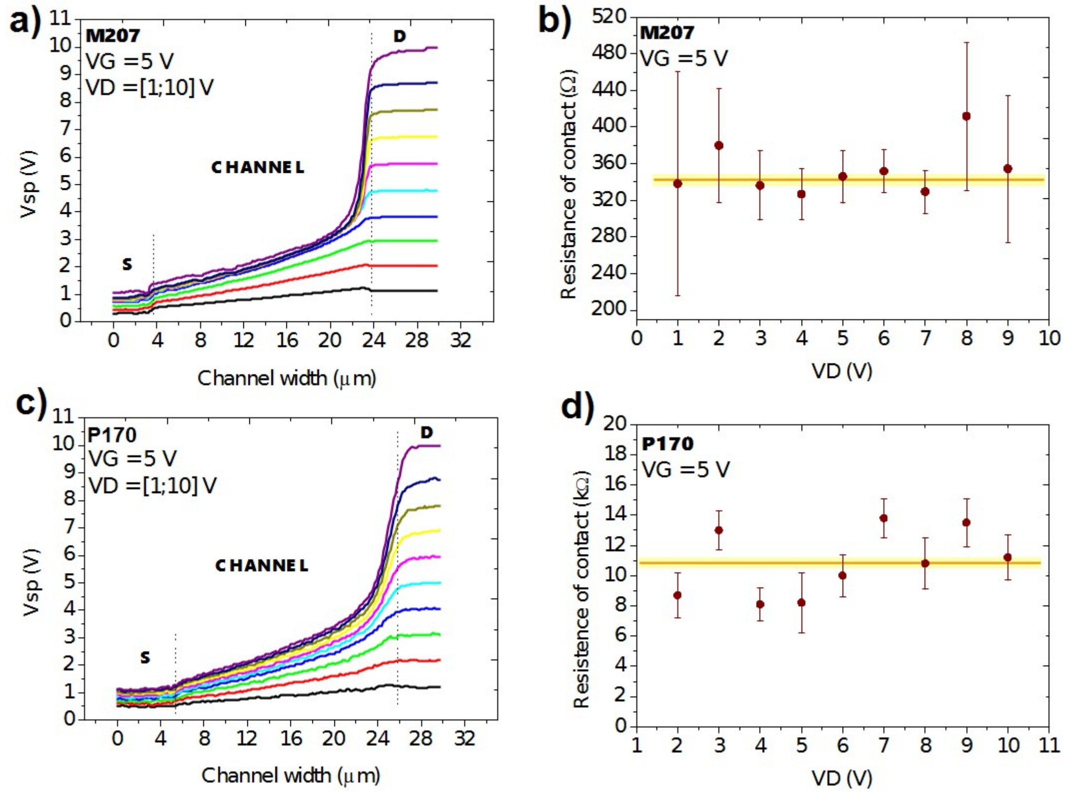


Figure 4.17: Surface potentials of **a)** TFT 4.6-M207 **b)** TFT 3.7-P170; VG= 5 V, VD = [1;10] V. Source contact resistences of **c)** TFT 4.6-M207 **d)** TFT 3.7-P170 for several values of drain voltage.

Before focusing on the other reasons which could explain the difference between the two samples, we can see that for the multilayer transistor, 10 V on the drain electrode caused the delamination of the device (see Figure 4.18).

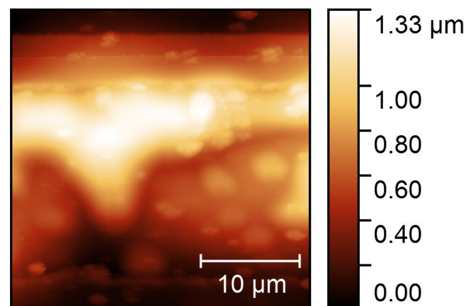


Figure 4.18: nc-AFM immage of delaminated TFT 4.6-M207 after the applying of V_D = 10 V.

Observing the nc-AFM image it is possible to explain why the delamination occurred: probably the device suffered a huge thermal stress caused by the high current flowing and this hypothesis could be confirmed by the fact that the TFT results particularly damaged next to the drain contact.

As I said, other issues that could justify the difference between **M207** and **P170** have been investigated.

Just observing the Figure 4.19 I realized that Parylene could present some drawbacks as far as its transport properties are concerned.

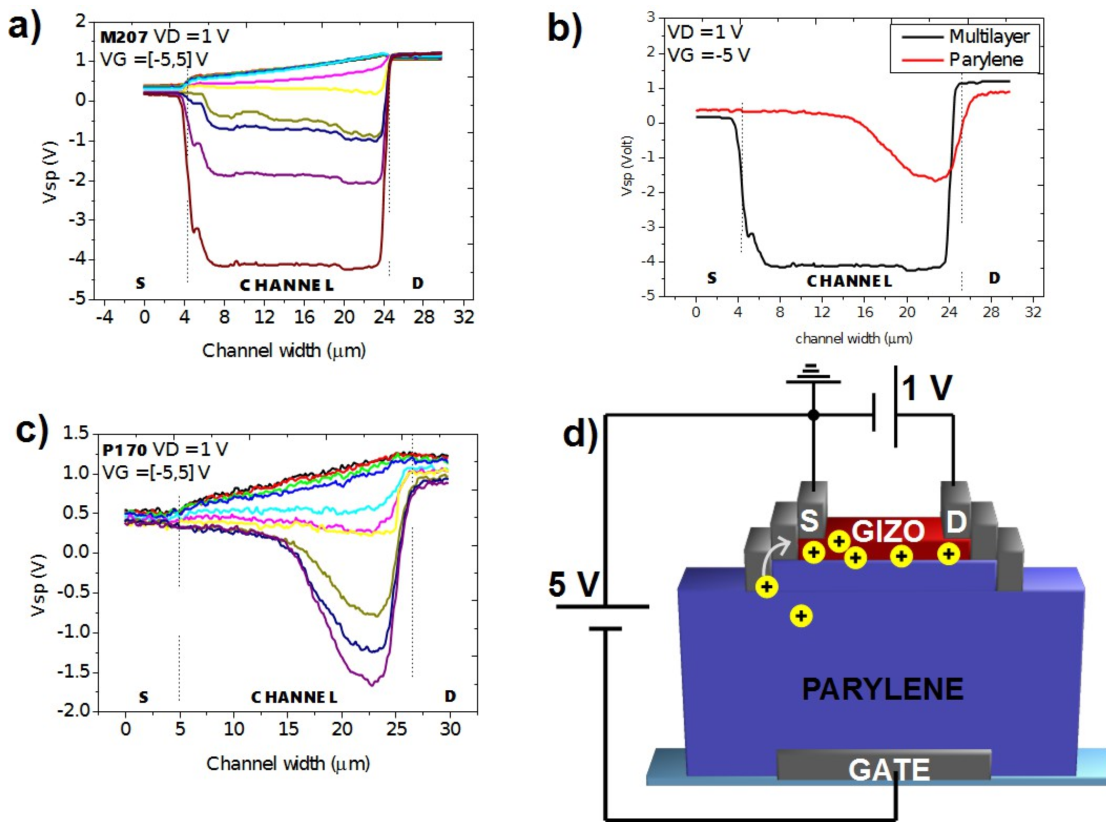


Figure 4.19: Surface voltage of **a)** multilayer and **b)** Parylene TFTs obteined applying VD = 1V constant and VG from 5 V (on-state) to -5 V (off-state). **c)** Comparison between the two samples. **d)** reports a schematic of the Parylene sample in the off-state. The yellow circles rapresent positive trapped charges inside the dielectric layer.

Figure 4.19 **a)** displays the **M207** behaviour. As we can see, applying a negative voltage to the gate electrode leads to a totally depletion of the channel and a negative surface voltage is measured along the whole width of the active layer. This represents the ideal off-state of an n-channel TFT confirming the great performance of the analyzed device.

On the opposite side, Figure 4.19 **b)** shows an anomalous behavior presented by the Parylene sample. In this case, the negative gate voltage doesn't cause a complete depletion of the channel. Figure 4.19 **c)** shows the difference between the two samples in the same condition. I supposed that, when a negative gate voltage is applied to the device, positive trapped charges migrate on a slow time scale from the Parylene to the semiconductor layer causing an increase of the voltage measured on the semiconductor. These positive charges enter the channel from the source electrode and this could explain the lack of symmetry in the potential profile reported (Figure 4.19 **d)**).

This hypothesis can be confirmed by another measurement (see Figure 4.20).

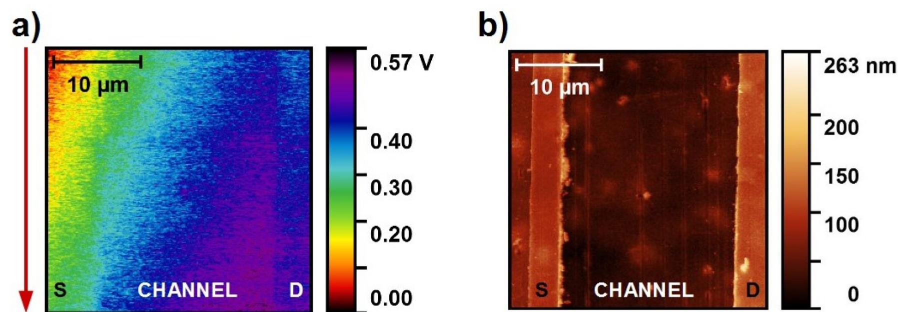


Figure 4.20: a) Surface potential and **b)** height profile of TFT 3.7-S5 manteining 0V at all the elctrodes. The red arrow indicates the scanning direction.

Figure 4.20 shows the surface potential of the channel when 0 V is applied to all the electrodes. In this image it is possible to observe the same dynamic migration of charges. In fact, looking at the figure along the scan direction (red arrow) a gradual increase of the potential points out the movement of positive charges going out from the channel.

Hence, we can conclude that there are several reasons that confirm and explain the different macroscopic behaviours of Parylene and multilayer TFTs. As we said, the different contact resistances is one of these causes. However, I suppose that the latter aspect presented is the one which has the main impact on the Parylene TFTs performance.

As we know, in the TFTs the conductive channel is created in a very thin region localized next to the interface between dielectric and semiconductor. For this reason, a part from the bulk properties of the dielectric material such as the permittivity, a good interface with the active layer is essential to achieve a performant device.

The presence of trapped charges indicates a bad interface between GIZO and Parylene layers. In fact, as we have seen in this last section, the extra charges can screen the gate voltage involving a degradation of the field effect. As a matter of fact, higher subthreshold swing are measured for all the Parylene devices compared with the multilayer one. Moreover, the low mobility can be connected to this issue too if we assume (*Chapter 1*) that in the TFT $\mu = \mu(V_G)$. Finally, the presence of these positive charges at the interface between Parylene and semiconductor could be the reason for the more negative turn-on voltage observed in these devices. As we saw the trapped charges flowing into the channel leads to an effective more positive voltage than the one applied trough the gate electrode. Thus, the device could be turned on for more negative voltage than the ideal 0 V.

Chapter 5

Final conclusion and perspective

Transparent amorphous oxide semiconductors are widely involved in the field of large area electronics. In fact, the possibility to achieve extraordinary electrical performance despite the low cost physical deposition process used to produce these kind of devices, made the amorphous oxides promising candidate for large scale applications and for the substitution of a-Si:H in the field of displays. The fabrication process implemented for this class of materials allowed to lowering the production costs and to improve the performance of large area devices such as (AM)-OLEDs displays and big-area sensors achieving an unusual spatial uniformity. Furthermore the possibility to execute the deposition process at RT maintaining an high electrical mobility, allowed to realize electrical devices on flexible polymeric substrates opening the door to the field of flexible electronics.

Even though in the past, oxide-based devices have already demonstrated good electrical performance and several improvements have been achieved regarding the fabrication process on flexible substrates[1][11], researchers are still engaged in this field to get better results in terms of electrical mobility, strain resistance under mechanical stress and production costs. To this end, different combinations of materials are still tested and many efforts are fulfilled to find improved materials, deposition conditions and device architectures. Moreover, other researches are getting unexpected results as far as the flexibility is concerned, demonstrating that the production of large area flexible devices can become a reality.

Towards the improvement of this technology, amorphous oxide thin film transistors fabricated on flexible substrates and containing different types of dielectric have been fabricated and analyzed during this work. Several devices were fabricated during four months spent at CENIMAT and CEMOP laboratories at

University Nova of Lisbon. Devices were then investigated by scanning probe microscopies during a two month period at the Physics Department, University of Bologna.

The first achievement of this thesis is the development of a new procedure for the lamination and delamination of the flexible substrates onto a rigid carrier. Using the PDMS as a temporary adhesive has permitted to improve the entire fabrication process. In fact, fixing the PEN foils on glass supports allowed to obtain a better alignment during the photolithography phase and to simplify the handling of the substrates during the fabrication steps. The detachment of the samples from the carrier and the subsequent characterization of the devices (Figure 5.1) confirmed the success of this procedure. This achievement could be exploited for a more intensive production and study of flexible devices analyzing the electrical performance of the TFTs after several cycles of mechanical stress.

The improvement of TFTs fabrication due to this novel technique is demonstrated by the achievement of a sample, **M207**, which exhibits extraordinary electrical performance. Indeed, the parameters calculated for the multilayer sample show the impressive capability of this device: mobility $\mu = (35.7 \pm 0.9)$ cm^{2}V^{-1}s^{-1}, subthreshold swing S $= (0.084 \pm 0.003)$V dec^{-1}, ON/OFF ratio of $(1.14 \pm 0.01) \cdot 10^6$ and turn on voltage V_{ON} = (-0.10 $\pm$ 0.002) V. Such a good electrical behaviour makes this kind of device a promising technology to be implemented in integrated circuits.

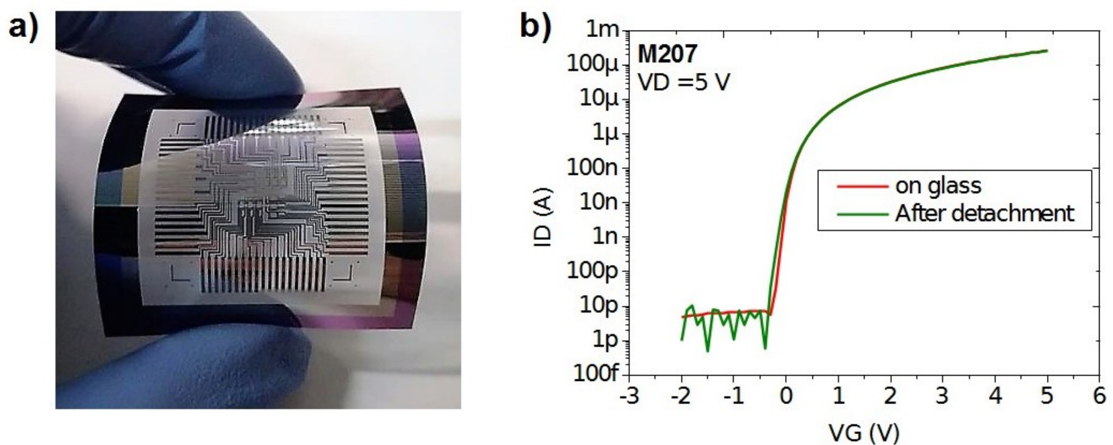


Figure 5.1: **a)** Picture of the detached sample from the rigid carrier. **b)** Transfer saturation characteristic of the device before and after the detachment.

As a second achievement, two different types of dielectric layer have been com-

pared during this work: an organic one composed by Parylene and deposited by CVD and a 7 multilayer dielectric achieved by sputtering and constituted by SiO_2 alternating with SiO_2+Ta_2O_5. All devices exhibit good electrical performances and a great level of spatial uniformity. This aspect results important because looking at the layout of these samples, one can see that this matrix composed by 36 TFTs could be used as a sensor able to detect some physical quantity in different position (x,y) at the same time.

The macroscopic investigation of the devices and the measurements of their electrical behaviours show differences between the analyzed TFTs. As a matter of fact, all the parameters calculated for the several samples (Table 4.6) highlight the superior performance of the multilayer devices compared to the Paryelen ones: the electrical mobility and the ON/OFF ratio is higher for **M207** indicating a better conduction and the lower S registered in this case confirms a stronger field effect compared to the one originates in the Parylene samples.

As a third achievement, scanning probe microscopies, in particular Kelvin Probe Force Microscopy (KPFM) was demonstrated to yield microscopic details about transport phenomena occurring in the channel of the thin film transistors. Combination of these microscopic findings with the macroscopic transistor characteristics provided explanations for the different observed transistor performances.

Firstly, this analysis points out the features that causing the exceptional electrical performance of the multilayer devices. In fact, the high mobility registered for these TFTs is confirmed by the KPFM measurements which show a very low contact resistance ($Rc_S = (55 \pm 16)\ \Omega$). Moreover, from the images acquired, one can see that **M207** presents the ideal n-type TFT behaviour: a perfect homogeneous electric field is recorded in the channel for the linear regime while the pinch off is visible when the V_D goes to higher values. Furthermore, a completely depletion of the channel is measured for negative V_G.

Besides, other measurements demonstrated that contact resistance can affect the electrical performance of the devices and that it can be the main reason for the lack of spatial uniformity. As far as the difference between Parylene and multilayer devices are concerned a more complicate phenomena has to be taken into account. In fact, the KPFM analysis showed that the Parylene/GIZO interface presents some drawbacks. Indeed, the presence of trapped charges into the dielectric layer can be supposed and it could explain the worse performance shown by the Parylene devices compared with the multilayer ones. In fact, the gate voltage causes the

movement of these charges into the channel from the source electrode resulting in a partial screening of the field effect. This phenomena could be the microscopic reason for the low mobility obtained for these sample. As a matter of fact, ideally μ depends only on the semiconductor material but in TFT technology it is also a function of V_G. Accordingly, if the screening effect exists in the Parylene devices this dependence can be pointed out. In the future, more analysis dedicated on the study of the density of trap states could confirmed this hypothesis.

Finally, this thesis lays the foundations to start with more detailed analysis of how tensile or compressive strain impacts of transistor performances. Implementing bending tests which can apply mechanical stress cycles to the TFTs, one can study the degradation of the macroscopic device electrical performance. Moreover, as this work demonstrated, the KPFM analysis can be used to study the devices and their flexible properties in a microscopic way. Measuring the surface potential of the TFTs, in fact, one can easily identify the microscopic origins of device failure due to the mechanical stress. This technique has already been implemented to study Organic TFTs based on TIPS-pentacene ([40]) and it could be very interesting to extend the same analysis to oxide devices testing different materials combination. In fact, the study of the structural and morphological limitation due to the mechanical bending of these devices is an essential step for the technological and scientific progress in the field of flexible electronics.

Bibliography

[1] E. Fortunato, P Barquinha, R. Martins, *Adv. Mater.*, 2012, 24, 2945-2986.

[2] P. Barquinha, L. Pereira, G. Gonçalves, R. Martins, and E. Fortunato, *Electrochemical and Solid-State Letters*, 2008, 11, H248.

[3] P. Barquinha, R. Martins, L. Pereira and E. Fortunato, *Transparent Oxide Electronics. From materials to devices*, Wiley, 2012.

[4] P. M. C. Barquinha, *Transparent Oxide Thin-Film Transistors: production, characterization and integration*, PhD dissertation in Nanotechnologies and Nanosciences, Universidade Nova de Lisboa, 2010.

[5] P. K. Weimer, *TFT-new thin-film transistor*, Proceedings of the Institute of Radio Engineers, vol. 50, 1462-1469, 1962.

[6] A. Facchetti, T. J. Marks, *Transparent Electronics. From synthesis to applications*, Wiley, 2010.

[7] C. R. Kagan, P. Andry, *Thin-Film Transistors*, Marcel Dekker, 2003.

[8] K. Nomura, H. Ohta, K. Ueda, T. Kamiya, M. Hirano, H. Hosono, *Science*, 2003, 300, 1269-1272.

[9] K. Nomura, H. Ohta, A. Takagi, T. Kamiya, M. Hirano, H. Hosono, *Nature*, 2004, 432, 488-492.

[10] S. Pearton, *GaN and ZnO-based Materials and devices*, Springer, 2011.

[11] K. Nomura, H. Ohta, A. Takagi, T. Kamiya, M. Hirano, H. Hosono, *Sci. Technol. Adv. Mater.*, 2010, volume 11, number 4.

[12] T. Kamiya, H. Hosono, *NPG Asia Mater.*, 2010, 2, 15-22.

[13] T. Kamiya, K. Nomura, H. Hosono, *Journal of display technology*, 2009, vol. 5, no. 12, 468-483.

[14] J. F. Wager, D. A. Keszler, R. E. Presley *Transparent Electronics*, Springer, 2008.

[15] D. S. Ginley, associated editors H. Hosono and D. C. Paine, *Handbook of transparent conductors*, Springer, 2010.

[16] S.D. Brotherton, *Introduction to Thin Film Transistors. Physics and Technology of TFTs*, Springer, 2013.

[17] K. Nomura, T. Kamiya, H. Ohta, M. Hirano, H. Hosono, *Applied physics letters*, 2008, 93, 192107(1-3).

[18] H. Klauk, *Organic Electronics. Materials, Manufacturing and Applications*, Wiley-VCH, 2006.

[19] W. S. Wong, A. Salleo, *Flexible Electronics. Materials and Applications*, Springer, 2009.

[20] S. Franssila, *Introduction to Microfabrication*, Wiley, 2004.

[21] R. C Jaeger, *Volume V, Introduction to Microelectronic Fabrication*, Prentice Hall, 2002.

[22] W. M. Moreau, *Semiconductor Lithography. Principles, Practices, and Materials*, Plenum Press, 1988.

[23] B. Bhushan, *Encyclopedia of Nanotechnology*, Springer, 2012.

[24] K. Ellmer, *Appl. Phys.*, 2000, 33, R17-R32.

[25] *www.ajaint.com.*

[26] K. Wasa, S. Hayakawa, *Handbook of sputter deposition technology. Principles, Technology and Applications*, Noyes Publications, 1992.

[27] S. Yang, C. S. Hwang, J. I. Lee, S. M. Yoon, M. K. Ryu, K. I. Cho, S. H. K. Park, S. H. Kim, C. E. Park, and J. Jang, *Appl. Phys. Lett.*, 2011, 98, 103515.

[28] J. F. Wager, K. Hoshino, E. S. Sundholm, R. E. Presley, R. Ravichandran, C. C. Knutson, D. A. Keszler, R. L. Hoffman, D. A. Mourey, and J. Robertson, *J. Soc. Inf. Disp.*, 2012, 20, 589.

[29] A. Kiazadeh, H. L. Gomes, P. Barquinha, J. Martins, A. Rovisco, J. V. Pinto, R. Martins, and E. Fortunato, *Appl. Phys. Lett.*, 2016, 109, 051606.

[30] J. Gao, T. Chen, C. Dong, Y. Jia, P. Mak, and M. Vai, *RSC Adv.*, 2015, 5, 48626.

[31] K. Nomura, T. Kamiya, H. Ohta, M. Hirano and H. Hosono *Appl. Phys. Lett.*, 2008, 93, 192107.

[32] G. Binnig, H. Rohrer, C. Gerber, E. Weibel, *Phys. Rev. Lett.*, 1982, 49(1), 57.

[33] G. Binnig, H. Rohrer, C. Gerber, E. Weibel, *Phys. Rev. Lett.*, 1982, 40(2), 178.

[34] G. Binnig, C.F. Quate, C. Gerber, *Phys. Rev. Lett.*, 1986, 56, 930.

[35] S. Sadewasser, T. Glatzel, *Kelvin Probe Force Microscopy. Measuring and Compensating Electrostatic Forces*, Springer, 2012.

[36] *www.parfafm.com.*

[37] P. S. Corporation, *NX10 user's manual*, 2013.

[38] W. Melitz, J. Shen, A. C. Kummel, S. Lee, *Surface Science Reports*, 2011, 66, 1-27.

[39] D. A. Bonnell, S. V. Kalinin, *Scanning Probe Microscopy for Energy Research*, World Scientific, 2013.

[40] T. Cramer, L. Travaglini, S. Lai, L. Patruno, S. de Miranda, A. Bonfiglio, P. Cosseddu and B. Fraboni, *Scientific Reports*, World Scientific, 6, 38203.